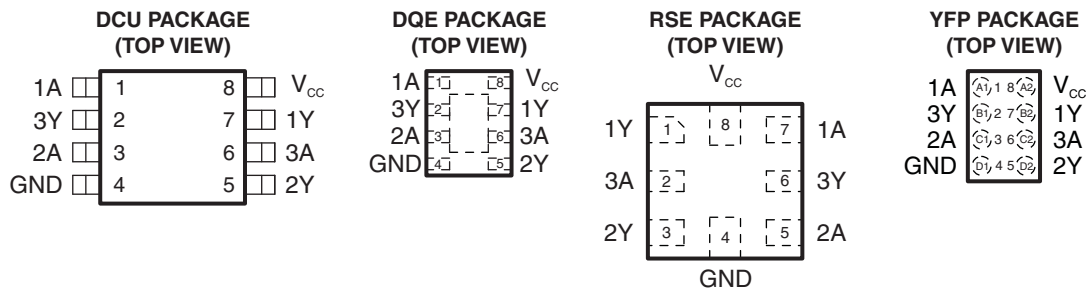# LOW-POWER TRIPLE BUFFER GATE

Check for Samples: SN74AUP3G34

FEATURES

- **Available in the Texas Instruments NanoStar™ Package**
- **Low Static-Power Consumption (I_{CC} = 0.9 μA Maximum)**
- **Low Dynamic-Power Consumption (C_{pd} = 4.3 pF Typ at 3.3 V)**
- **Low Input Capacitance (C_i = 1.5 pF Typical)**
- **Low Noise – Overshoot and Undershoot <10% of V_{CC}**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Wide Operating V_{CC} Range of 0.8 V to 3.6 V**

- **Optimized for 3.3-V Operation**
- **3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **t_{pd} = 4.3 ns Maximum at 3.3 V**
- **Suitable for Point-to-Point Applications**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

DCU PACKAGE
(TOP VIEW)

1A	1	8	V_{CC}
3Y	2	7	1Y
2A	3	6	3A
GND	4	5	2Y

DQE PACKAGE
(TOP VIEW)

1A	1	8	V_{CC}
3Y	2	7	1Y
2A	3	6	3A
GND	4	5	2Y

RSE PACKAGE
(TOP VIEW)

V_{CC}

1Y	1	8	7	1A
3A	2		6	3Y
2Y	3	4	5	2A

GND

YFP PACKAGE
(TOP VIEW)

1A	(A1) 1 8 (A2)		V_{CC}
3Y	(B1) 2 7 (B2)		1Y
2A	(C1) 3 6 (C2)		3A
GND	(D1) 4 5 (D2)		2Y

See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see Figure 1). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in Figure 2).
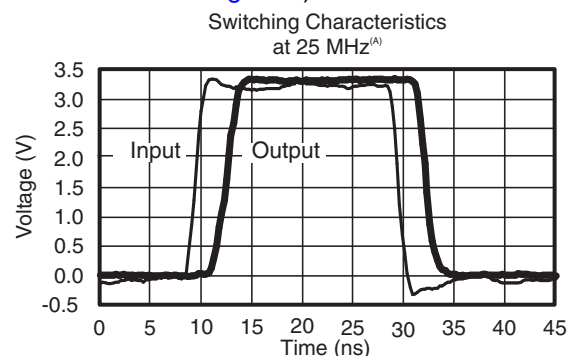
Static-Power Consumption (μA)

3.3-V Logic[A]

AUP

Dynamic-Power Consumption (pF)

3.3-V Logic[A]

AUP

[A] Single, dual, and triple gates

Switching Characteristics at 25 MHz[A]

Input   Output

[A] SN74AUP3Gxx data at C_L = 15 pF.

Figure 1. AUP – The Lowest-Power Family

Figure 2. Excellent Signal Integrity

The SN74AUP3G34 performs the Boolean function Y = A in positive logic.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar is a trademark of Texas Instruments.

SN74AUP3G34

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION[1]

T_A	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[3]
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP3G34YFPR	_ _ H 9 _
	uQFN – DQE	Reel of 5000	SN74AUP3G34DQER	TZ
	QFN – RSE	Reel of 5000	SN74AUP3G34RSER	TZ
	SSOP – DCU	Reel of 3000	SN74AUP3G34DCUR	H34_
			SN74AUP3G34DCURG4	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DCU: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YFP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

LOGIC DIAGRAM (POSITIVE LOGIC)
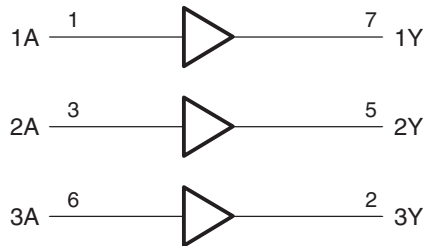
Pin numbers shown are for the DCU and DQE packages.

Product Folder Link(s): *SN74AUP3G34*

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range[2]		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	4.6	V
V_O	Output voltage range in the high or low state[2]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance[3]	DCU package		220	°C/W
		DQE package		261	
		RSE package		253	
		YFP package		132	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.6		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.9	
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 0.8 V		–20	µA
		V_{CC} = 1.1 V		–1.1	mA
		V_{CC} = 1.4 V		–1.7	
		V_{CC} = 1.65		–1.9	
		V_{CC} = 2.3 V		–3.1	
		V_{CC} = 3 V		–4	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	µA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Product Folder Link(s): *SN74AUP3G34*

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25°C$			$T_A = -40°C$ to $85°C$		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OH}		$I_{OH} = -20$ µA	0.8 V to 3.6 V	$V_{CC} - 0.1$			$V_{CC} - 0.1$		V
		$I_{OH} = -1.1$ mA	1.1 V	$0.75 \times V_{CC}$			$0.7 \times V_{CC}$		
		$I_{OH} = -1.7$ mA	1.4 V	1.11			1.03		
		$I_{OH} = -1.9$ mA	1.65 V	1.32			1.3		
		$I_{OH} = -2.3$ mA	2.3 V	2.05			1.97		
		$I_{OH} = -3.1$ mA		1.9			1.85		
		$I_{OH} = -2.7$ mA	3 V	2.72			2.67		
		$I_{OH} = -4$ mA		2.6			2.55		
V_{OL}		$I_{OL} = 20$ µA	0.8 V to 3.6 V			0.1		0.1	V
		$I_{OL} = 1.1$ mA	1.1 V			$0.3 \times V_{CC}$		$0.3 \times V_{CC}$	
		$I_{OL} = 1.7$ mA	1.4 V			0.31		0.37	
		$I_{OL} = 1.9$ mA	1.65 V			0.31		0.35	
		$I_{OL} = 2.3$ mA	2.3 V			0.31		0.33	
		$I_{OL} = 3.1$ mA				0.44		0.45	
		$I_{OL} = 2.7$ mA	3 V			0.31		0.33	
		$I_{OL} = 4$ mA				0.44		0.45	
I_I	A or B input	$V_I = $ GND to 3.6 V	0 V to 3.6 V			0.1		0.5	µA
I_{off}		V_I or $V_O = 0$ V to 3.6 V	0 V			0.2		0.6	µA
ΔI_{off}		V_I or $V_O = 0$ V to 3.6 V	0 V to 0.2 V			0.2		0.6	µA
I_{CC}		$V_I = $ GND or (V_{CC} to 3.6 V), $I_O = 0$	0.8 V to 3.6 V			0.5		0.9	µA
ΔI_{CC}		$V_I = V_{CC} - 0.6$ V[1], $I_O = 0$	3.3 V			40		50	µA
C_i		$V_I = V_{CC}$ or GND	0 V		1.5				pF
			3.6 V		1.5				
C_o		$V_O = $ GND	0 V		3				pF

(1)   One input at $V_{CC} - 0.6$ V, other input at V_{CC} or GND

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 5$ pF (unless otherwise noted) (see Figure 3 and Figure 4)

| PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			$T_A = -40°C$ to $85°C$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		18				ns
			1.2 V ± 0.1 V	2.6	7.3	12.8	2.1	15.6	
			1.5 V ± 0.1 V	1.4	5.2	8.7	0.9	10.3	
			1.8 V ± 0.15 V	1	4.2	6.6	0.5	8.2	
			2.5 V ± 0.2 V	1	3	4.4	0.5	5.5	
			3.3 V ± 0.3 V	1	2.4	3.5	0.5	4.3	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V$_{CC}$	T$_A$ = 25°C			T$_A$ = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t$_{pd}$	A or B	Y	0.8 V		21				ns
			1.2 V ± 0.1 V	1.5	8.5	14.7	1	17.2	
			1.5 V ± 0.1 V	1	6.2	10	0.5	11.3	
			1.8 V ± 0.15 V	1	5	7.7	0.5	9	
			2.5 V ± 0.2 V	1	3.6	5.2	0.5	6.1	
			3.3 V ± 0.3 V	1	2.9	4.2	0.5	4.7	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V$_{CC}$	T$_A$ = 25°C			T$_A$ = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t$_{pd}$	A or B	Y	0.8 V		24				ns
			1.2 V ± 0.1 V	3.6	9.9	16.3	3.1	19.9	
			1.5 V ± 0.1 V	2.3	7.2	11.1	1.8	13.2	
			1.8 V ± 0.15 V	1.6	5.8	8.7	1.1	10.6	
			2.5 V ± 0.2 V	1	4.3	5.9	0.5	7.3	
			3.3 V ± 0.3 V	1	3.4	4.8	0.5	5.9	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V$_{CC}$	T$_A$ = 25°C			T$_A$ = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t$_{pd}$	A or B	Y	0.8 V		32.8				ns
			1.2 V ± 0.1 V	4.9	13.1	20.9	4.4	25.5	
			1.5 V ± 0.1 V	3.4	9.5	14.2	2.9	16.9	
			1.8 V ± 0.15 V	2.5	7.7	11	2	13.5	
			2.5 V ± 0.2 V	1.8	5.7	7.6	1.3	9.4	
			3.3 V ± 0.3 V	1.5	4.7	6.2	1	7.5	

OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER		TEST CONDITIONS	V$_{CC}$	TYP	UNIT
C$_{pd}$	Power dissipation capacitance	f = 10 MHz	0.8 V	4	pF
			1.2 V ± 0.1 V	4	
			1.5 V ± 0.1 V	4	
			1.8 V ± 0.15 V	4	
			2.5 V ± 0.2 V	4.1	
			3.3 V ± 0.3 V	4.3	

Product Folder Link(s): *SN74AUP3G34*

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)

From Output Under Test

C_L (see Note A)   1 MΩ
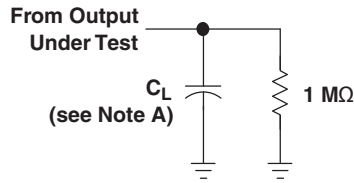
LOAD CIRCUIT

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, for propagation delays t_r/t_f = 3 ns, for setup and hold times and pulse width t_r/t_f = 1.2 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{pd}.

F. All parameters and waveforms are not applicable to all devices.
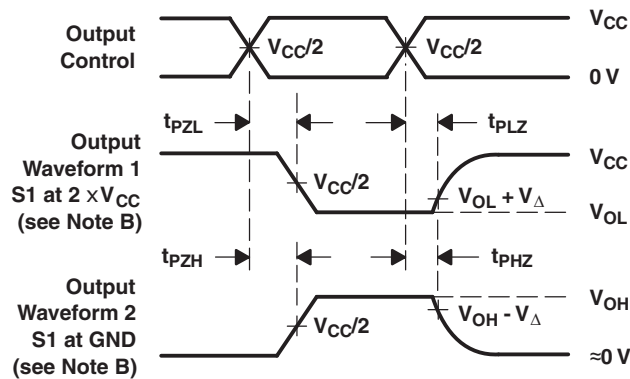
Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)
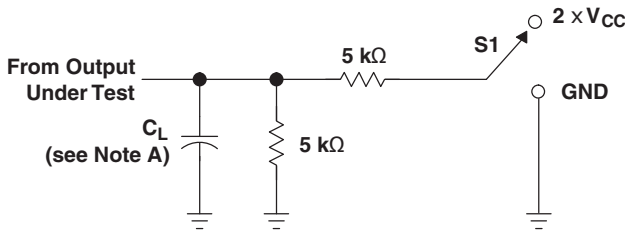
LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V $\pm$ 0.1 V	V_{CC} = 1.5 V $\pm$ 0.1 V	V_{CC} = 1.8 V $\pm$ 0.15 V	V_{CC} = 2.5 V $\pm$ 0.2 V	V_{CC} = 3.3 V $\pm$ 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PLH} and t_{PHL} are the same as t_{pd}.

G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision B (March 2010) to Revision C   **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP3G34DCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H34R	Samples
SN74AUP3G34DCURG4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H34R	Samples
SN74AUP3G34DQER	ACTIVE	X2SON	DQE	8	5000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TZ	Samples
SN74AUP3G34RSER	ACTIVE	UQFN	RSE	8	5000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TZ	Samples
SN74AUP3G34YFPR	ACTIVE	DSBGA	YFP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	H9N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

17-Aug-2015

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP3G34DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP3G34DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP3G34DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
SN74AUP3G34RSER	UQFN	RSE	8	5000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
SN74AUP3G34YFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP3G34DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP3G34DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP3G34DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
SN74AUP3G34RSER	UQFN	RSE	8	5000	202.0	201.0	28.0
SN74AUP3G34YFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0

DCU (R−PDSO−G8)   PLASTIC SMALL−OUTLINE PACKAGE (DIE DOWN)
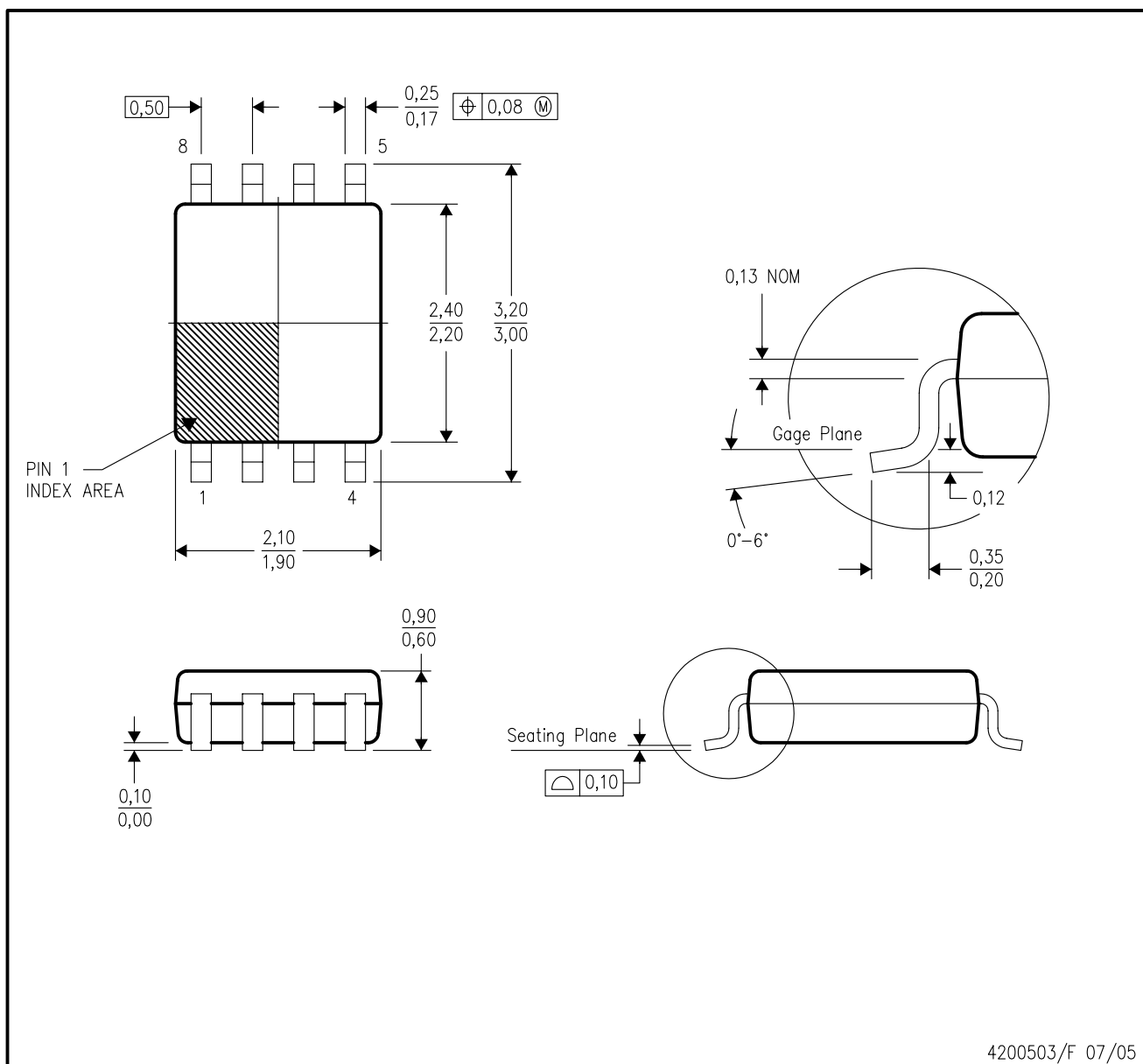
4200503/F 07/05

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
        D. Falls within JEDEC MO−187 variation CA.

TEXAS
INSTRUMENTS
www.ti.com

DCU (S−PDSO−G8)   PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)

Example Board Layout
(Note C,E)

6x 0,5

3,1

Example Stencil Design
(Note D)

8x 0,25   6x 0,5

8x 0,75

3,1

0,3

Example
Solder Mask Opening

0,8

Pad Geometry

0,05

All Around

4210064/C 04/12

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC−7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PIN 1 INDEX AREA

B

1.55
1.45

A

1.55
1.45

0.6 MAX

C

SEATING PLANE

0.05
0.00

0.05 C

2X 0.35
0.25

6X 0.4
0.3

0.1 Ⓜ C AⓈ BⓈ
0.05 Ⓜ C

2X 0.45
0.35

4

3

5

2X
1

SYMM
℄

2X 0.25
0.15

1

0.1 Ⓜ C AⓈ BⓈ
0.05 Ⓜ C

7

4X 0.5

8

4X 0.3
0.2

SYMM
℄

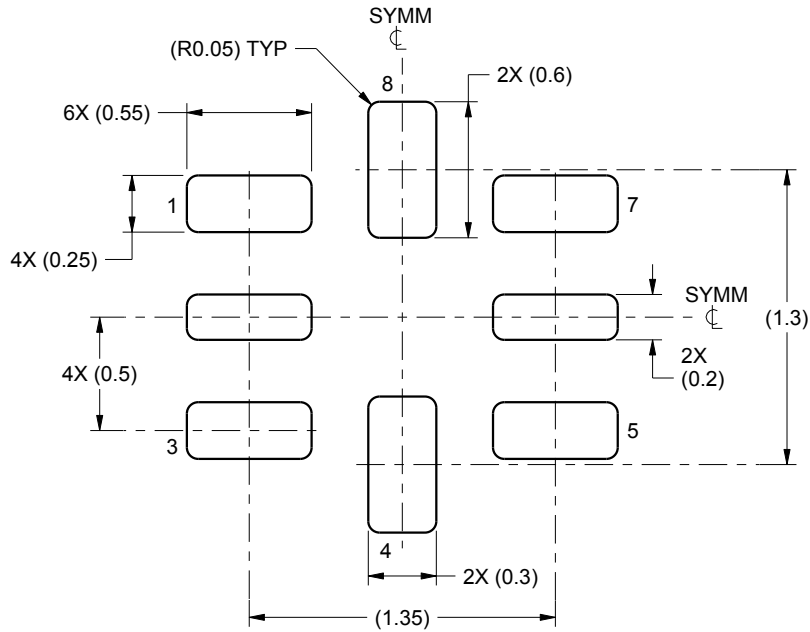0.1 Ⓜ C AⓈ BⓈ
0.05 Ⓜ C

PIN 1 ID
(45° X 0.1

(0.12)
TYP
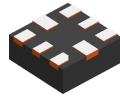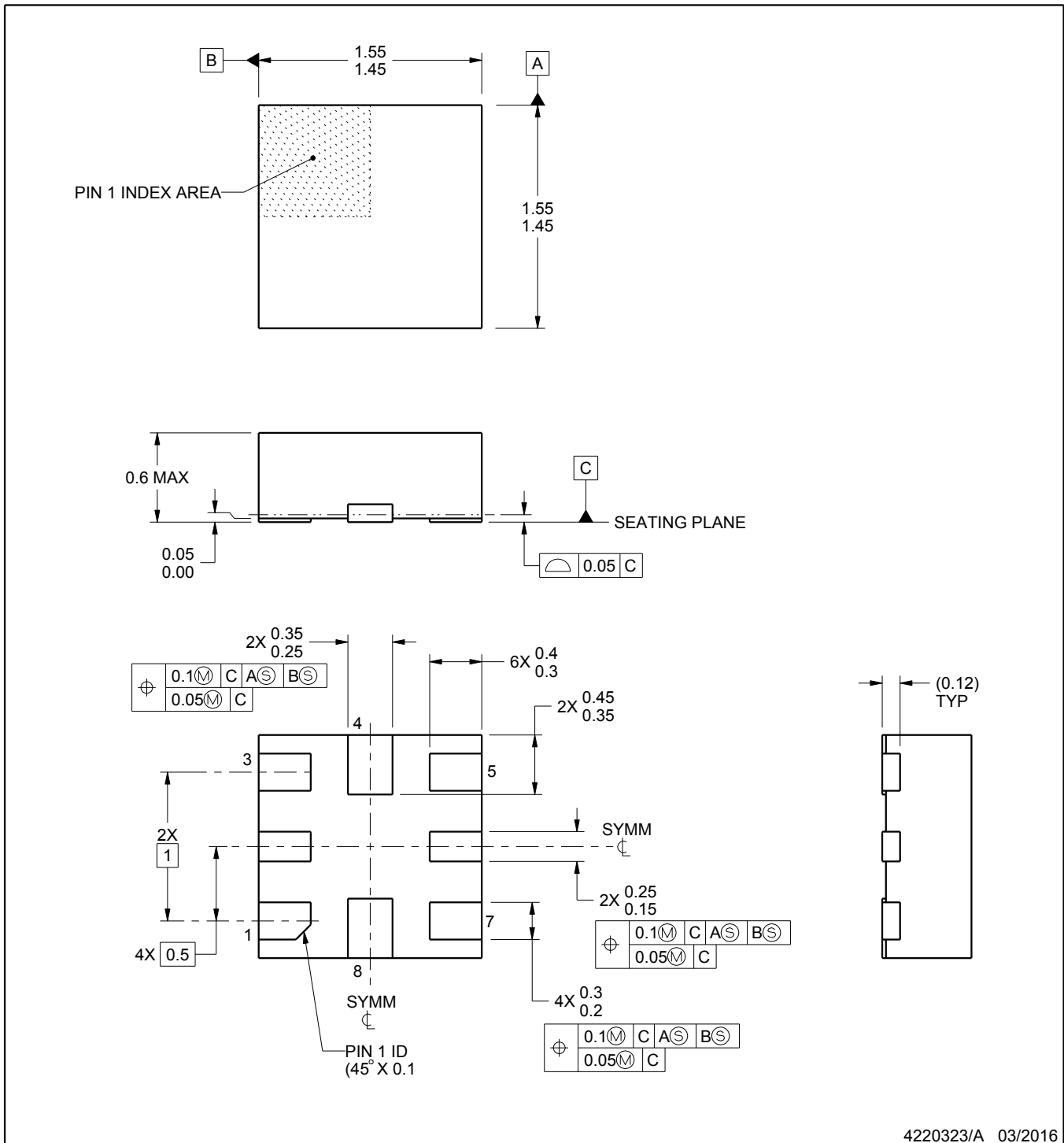
4220323/A   03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
    per ASME Y14.5M.
2. This drawing is subject to change without notice.

TEXAS
INSTRUMENTS
www.ti.com

SYMM

(R0.05) TYP

8

2X (0.6)

6X (0.55)

1

4X (0.25)

SYMM

(1.3)

4X (0.5)

2X (0.2)

3

5

4

2X (0.3)

(1.35)

LAND PATTERN EXAMPLE
SCALE:30X

0.07 MAX
ALL AROUND

METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL
UNDER
SOLDER MASK

SOLDER MASK
DEFINED
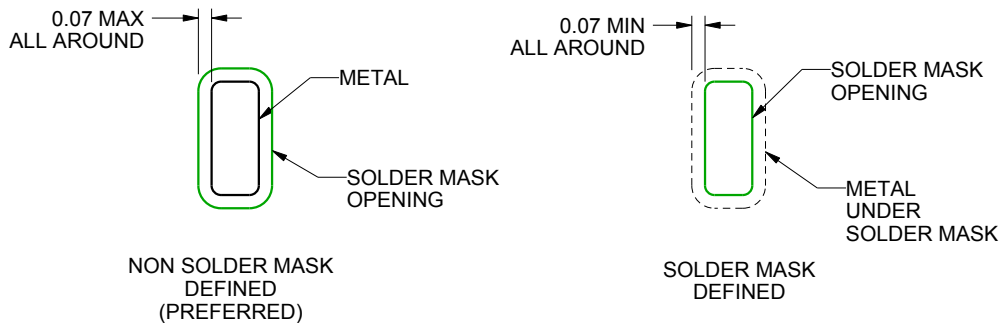
SOLDER MASK DETAILS
NOT TO SCALE

4220323/A   03/2016

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

TEXAS
INSTRUMENTS
www.ti.com
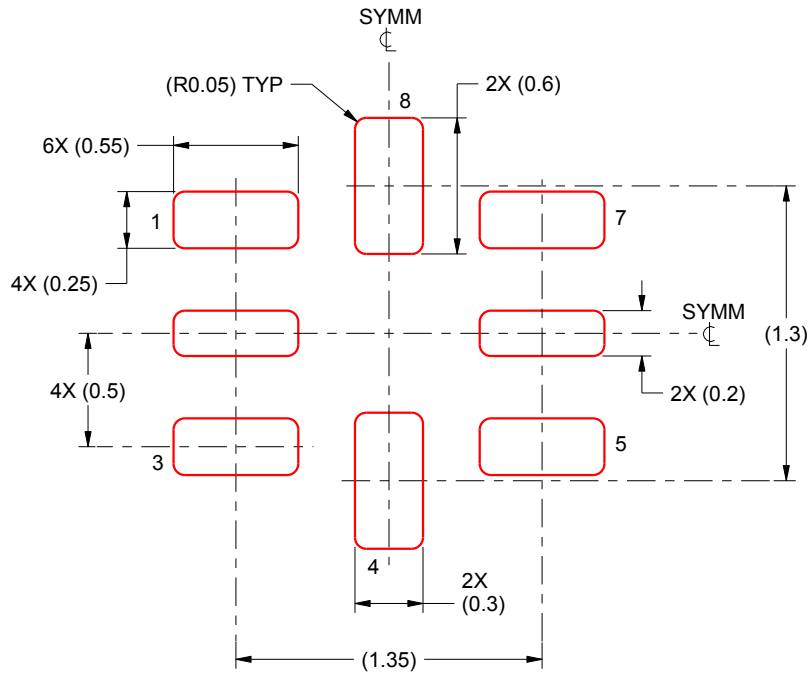
SOLDER PASTE EXAMPLE
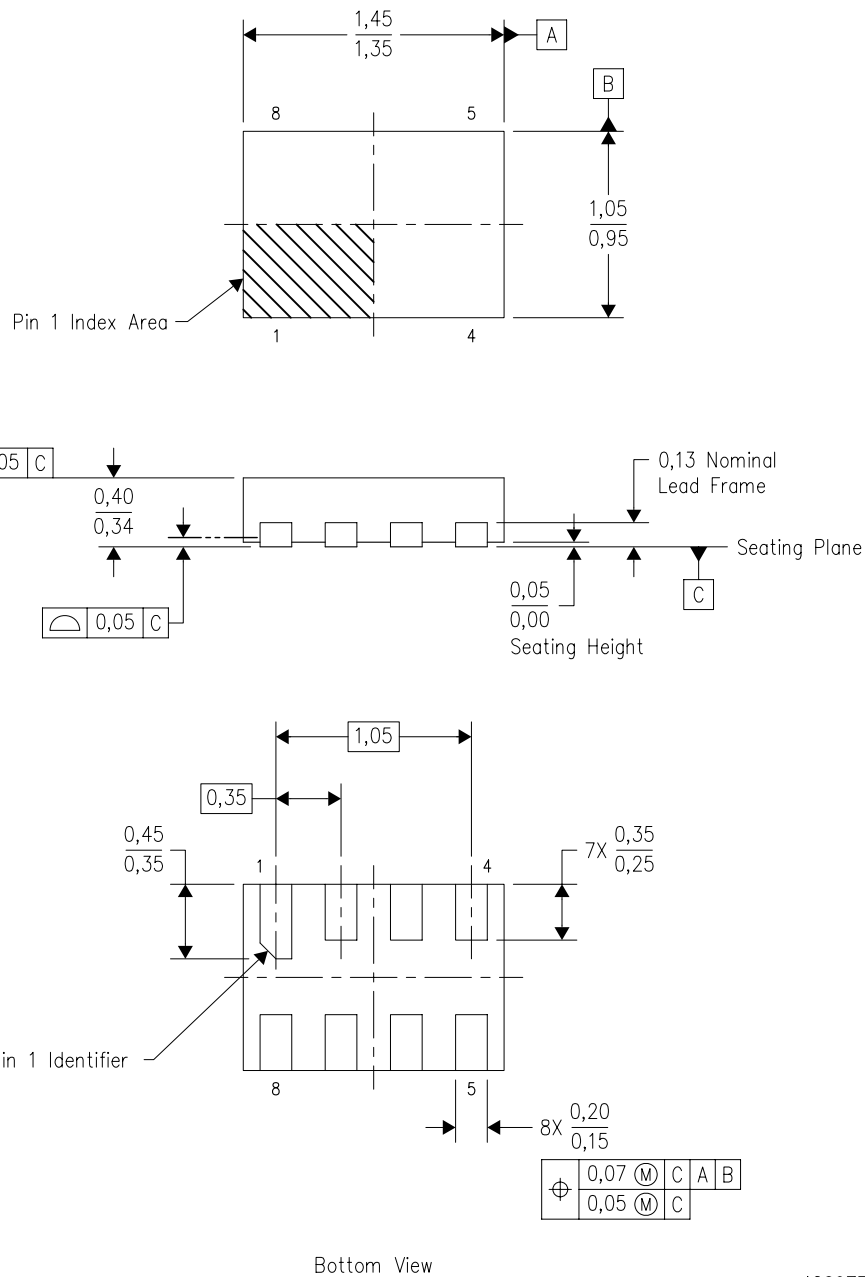BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220323/A   03/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

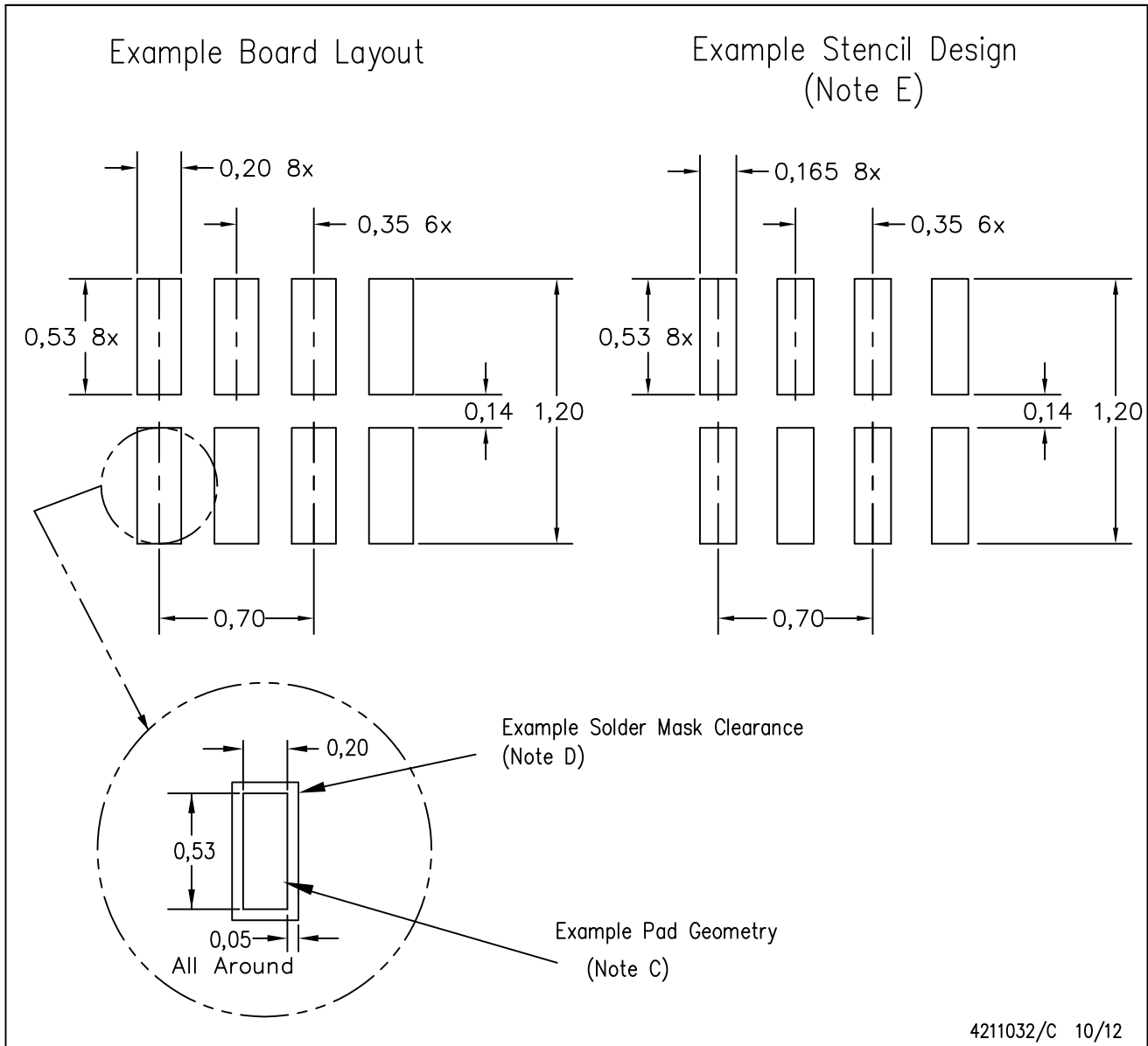DQE (R−PX2SON−N8)   PLASTIC SMALL OUTLINE NO−LEAD

Pin 1 Index Area

// 0,05 C

0,40
0,34

⌒ 0,05 C

0,13 Nominal
Lead Frame

Seating Plane

0,05
0,00
Seating Height

1,45
1,35   A

B

1,05
0,95

1,05

0,35

0,45
0,35

7X 0,35
0,25

Pin 1 Identifier

8X 0,20
0,15

⊕ 0,07 Ⓜ C A B
   0,05 Ⓜ C

Bottom View

4209779/B 10/2008

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   SON (Small Outline No−Lead) package configuration.
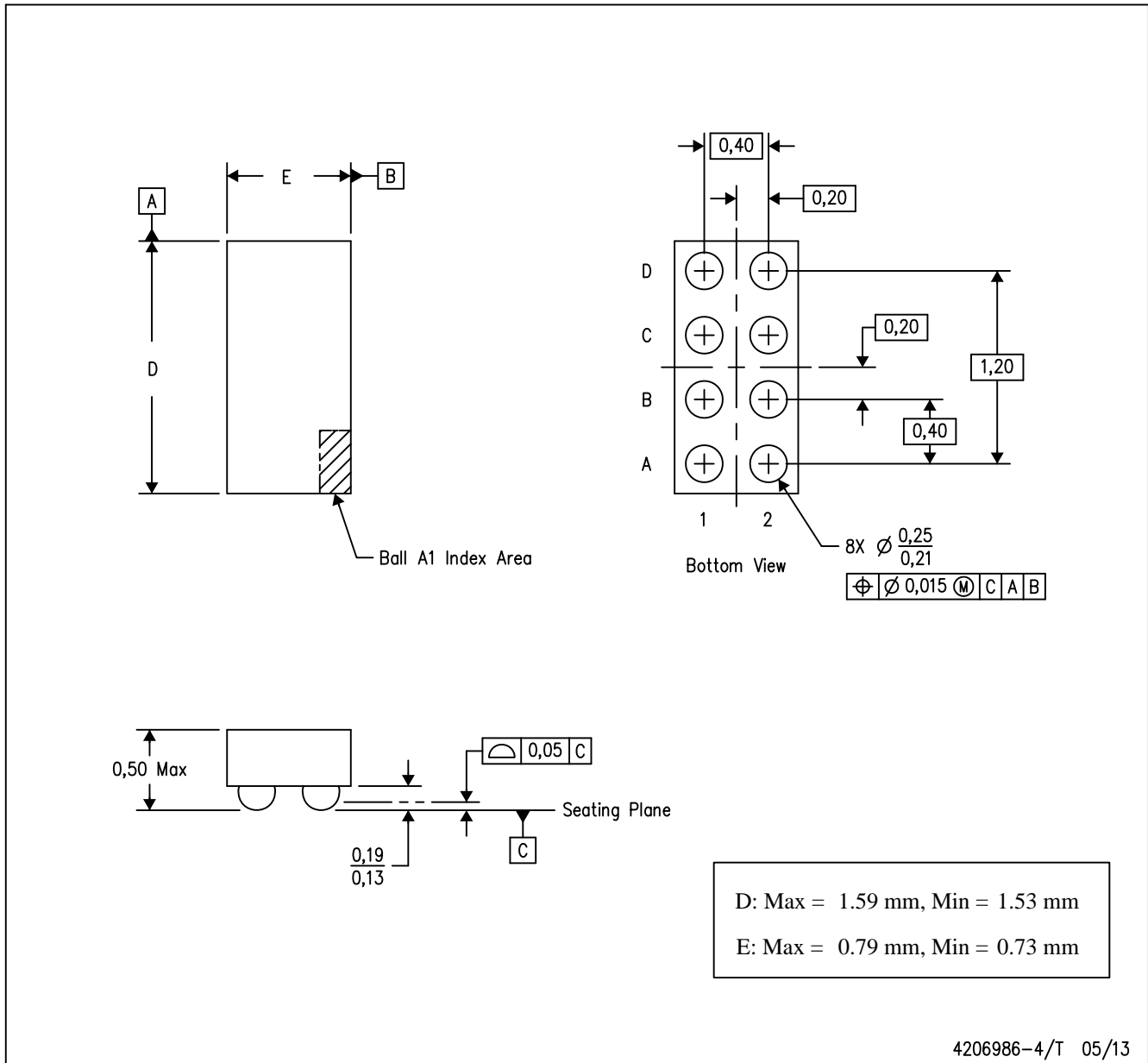   D.   This package complies to JEDEC MO−287 variation X2EAF.

DQE (R−PX2SON−N8)   PLASTIC SMALL OUTLINE NO−LEAD

Example Board Layout

Example Stencil Design
(Note E)

0,20 8x

0,35 6x

0,53 8x

0,14 1,20

0,70

0,165 8x

0,35 6x

0,53 8x

0,14 1,20

0,70

Example Solder Mask Clearance
(Note D)

0,20

0,53

0,05
All Around

Example Pad Geometry
(Note C)

4211032/C 10/12

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
            If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
        E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
        F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        G. Over−printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further
            reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
        H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
        I. Component placement force should be minimized to prevent excessive paste block deformation.

TEXAS
INSTRUMENTS
www.ti.com

YFP (R−XBGA−N8)   DIE−SIZE BALL GRID ARRAY

Ball A1 Index Area

Bottom View

8X ∅ $\frac{0,25}{0,21}$

$\oplus$ | ∅ 0,015 Ⓜ | C | A | B

0,50 Max

$\frac{0,19}{0,13}$

0,05 | C

Seating Plane

C

D: Max = 1.59 mm, Min = 1.53 mm

E: Max = 0.79 mm, Min = 0.73 mm

4206986−4/T 05/13

NOTES: A. All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		