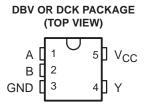
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- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- ESD Protection Exceeds 1500 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Operating Range of 2 V to 5.5 V
- † Contact factory for details. Q100 qualification data available on request.

- Max t_{pd} of 6.5 ns at 5 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±8-mA Output Drive at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17



description/ordering information

The SN74AHC1G32 is a single 2-input positive-OR gate. The device performs the Boolean function Y = A + B or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

ORDERING INFORMATION

TA	PACKAGE	‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING§
4000 1- 40500	SOT (SOT-23) – DBV	Reel of 3000	SN74AHC1G32TDBVRQ1	A32_
-40°C to 105°C	SOT (SC-70) - DCK	Reel of 3000	SN74AHC1G32TDCKRQ1	AG_

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

	INPUT	S	OUTPUT
	4	В	Υ
H	+	Χ	Н
>	X	Н	Н
l	L	L	L

logic diagram (positive logic)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



[§] The actual top-side marking has one additional character that designates the assembly/test site.

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Output voltage range, VO (see Note 1)	
Input clamp current, $I_{ K }(V_{ C } < 0)$	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2	5.5	V
		V _{CC} = 2 V	1.5		
V_{IH}	High-level input voltage	V _{CC} = 3 V	2.1		V
		V _{CC} = 5.5 V	3.85		1
		V _{CC} = 2 V		0.5	
V_{IL}	Low-level input voltage	V _{CC} = 3 V		0.9	0.9 V
		V _{CC} = 5.5 V	1.65 0 5.5 0 V _{CC}		
VI	Input voltage		0	5.5	V
VO	Output voltage		0	VCC	V
		V _{CC} = 2 V		-50	μΑ
loh	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	
	Low-level input voltage Input voltage Output voltage High-level output current Low-level output current Input transition rise or fall rate	$V_{CC} = 5 V \pm 0.5 V$		-8	mA
		V _{CC} = 2 V		50	μΑ
loL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	
		$V_{CC} = 5 V \pm 0.5 V$	0.9 1.65 0 5.5 0 V _{CC} -50 -4 -8 50	mA	
A 1 / A	hand to self as visc on fall and	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100	
Δt/Δv	input transition rise or fall rate	$V_{CC} = 5 V \pm 0.5 V$		1.65 5.5 VCC -50 -4 -8 50 4 8 100 20	ns/V
T _A	Operating free-air temperature		-40	105	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

B4 B 444 E E B	DADAMETED TECT COMPITIONS V		T,	Δ = 25°C	;				
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	UNIT	
		2 V	1.9	2		1.9			
	$I_{OH} = -50 \mu\text{A}$	3 V	2.9	3		2.9			
VOH		4.5 V	4.4	4.5		4.4		V	
	I _{OH} = -4 mA	3 V	2.58			2.48			
	I _{OH} = -8 mA	4.5 V	3.94			3.8			
		2 V			0.1		0.1		
	I _{OL} = 50 μA	3 V			0.1		0.1		
VOL		4.5 V			0.1		0.1	V	
	I _{OL} = 4 mA	3 V			0.36		0.44	0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.44		
lį	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μΑ	
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ	
Ci	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

24244555	FROM	то	LOAD	T,	4 = 25°C	;			
PARAMETER	(INPUT)	(OUTPUT) CAPACITANC	CAPACITANCE	MIN	TYP	MAX	MIN M	MAX	UNIT
^t PLH	A D		C _L = 50 pF		8	11.4	1	13	
t _{PHL}	A or B	Y			8	11.4	1	13	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

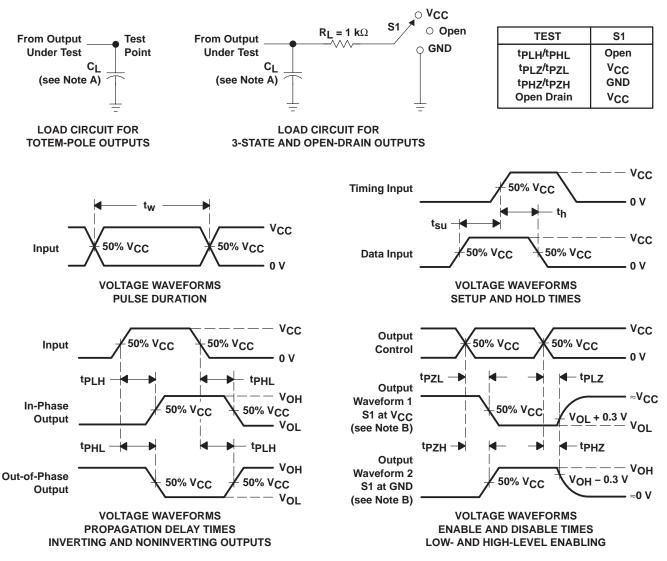
DADAMETER	FROM	то	LOAD	T,	4 = 25°C	;	BAINI	BAAV	
PARAMETER	(INPUT)	PUT) (OUTPUT) CAPACITANCE	CAPACITANCE	MIN	TYP	MAX	MIN MAX	MAX	UNIT
t _{PLH}	A D	V	0 50 - 5		5.3	7.5	1	8.5	
^t PHL	A or B	Y	C _L = 50 pF		5.3	7.5	1	8.5	ns

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST C	ONDITIONS	TYP	UNIT
C _{pd} Power dis	sipation capacitance	No load,	f = 1 MHz	14	pF



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

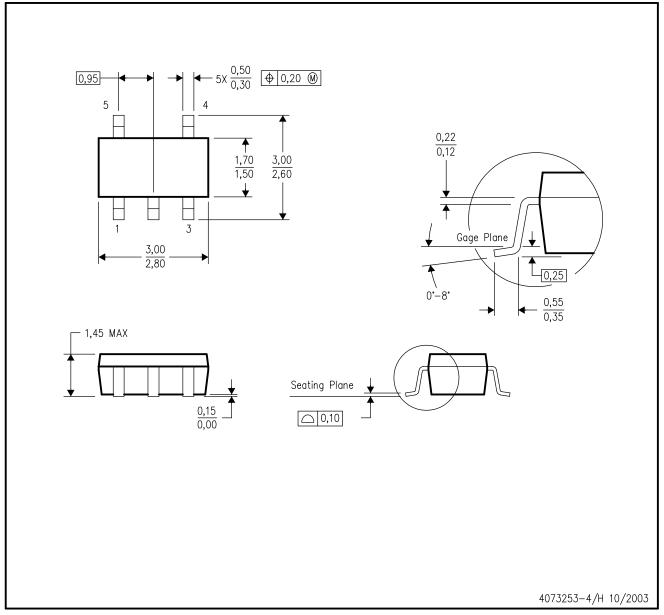
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns. $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



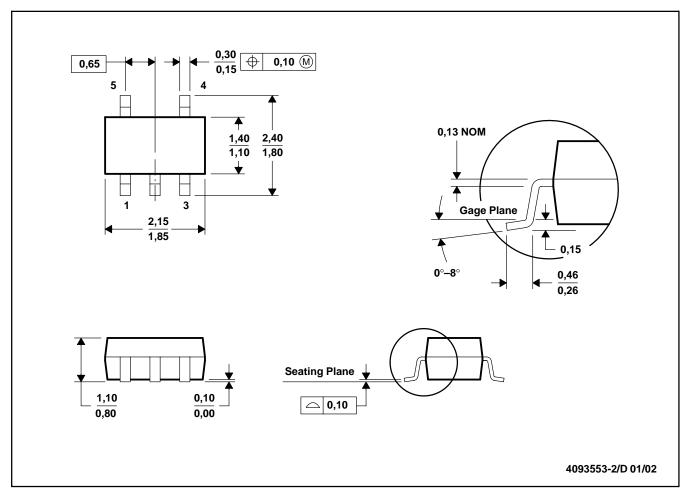
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- C. Body dimensions do not include mold fla D. Falls within JEDEC MO—178 Variation AA. Body dimensions do not include mold flash or protrusion.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion.

D. Falls within JEDEC MO-203

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