DATA SHEET

PEMD6; PUMD6

NPN/PNP resistor-equipped transistors;
R1 = 4.7 kΩ, R2 = open

Product data sheet
Supersedes data of 2003 Nov 04

2004 Apr 07

NPN/PNP resistor-equipped transistors; R1 = 4.7 kΩ, R2 = open

PEMD6; PUMD6

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- Low current peripheral driver
- Replacement of general purpose transistors in digital applications
- Control of IC inputs.

DESCRIPTION

NPN/PNP resistor-equipped transistors (see "_Data_Sheet_Remark Supersedes data of 2003 Nov 04" for package details).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{CEO}	collector-emitter voltage	–	50	V
I_O	output current (DC)	–	100	mA
TR1	NPN	–	–	–
TR2	PNP	–	–	–
R1	bias resistor	4.7	–	kΩ
R2	open	–	–	–

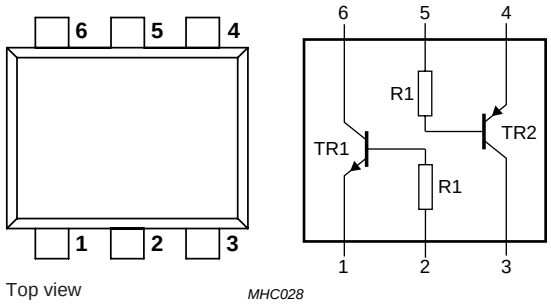
PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	NPN/NPN COMPLEMENT	PNP/PNP COMPLEMENT
	PHILIPS	EIAJ			
PEMD6	SOT666	–	D6	PEMH7	PEMB3
PUMD6	SOT363	SC-88	D*6[1]	PUMH7	PUMB3

Note

1. * = p: Made in Hong Kong.
   * = t: Made in Malaysia.

SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PEMD6; PUMD6	 Top view	1	emitter TR1
		2	base TR1
		3	collector TR2
		4	emitter TR2
		5	base TR2
		6	collector TR1

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PEMD6	–	plastic surface mounted package; 6 leads	SOT666
PUMD6	–	plastic surface mounted package; 6 leads	SOT363

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity					
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	50	V
V_{EBO}	emitter-base voltage	open collector	–	5	V
I_O	output current (DC)		–	100	mA
I_{CM}	peak collector current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1			
	SOT363	note 1	–	200	mW
	SOT666	notes 1 and 2	–	200	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		−65	+150	°C
Per device					
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1			
	SOT363	note 1	–	300	mW
	SOT666	notes 1 and 2	–	300	mW

Notes

1. Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
2. Reflow soldering is the only recommended soldering method.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per transistor				
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1		
	SOT363		625	K/W
	SOT666		625	K/W
Per device				
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1		
	SOT363		416	K/W
	SOT666		416	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.

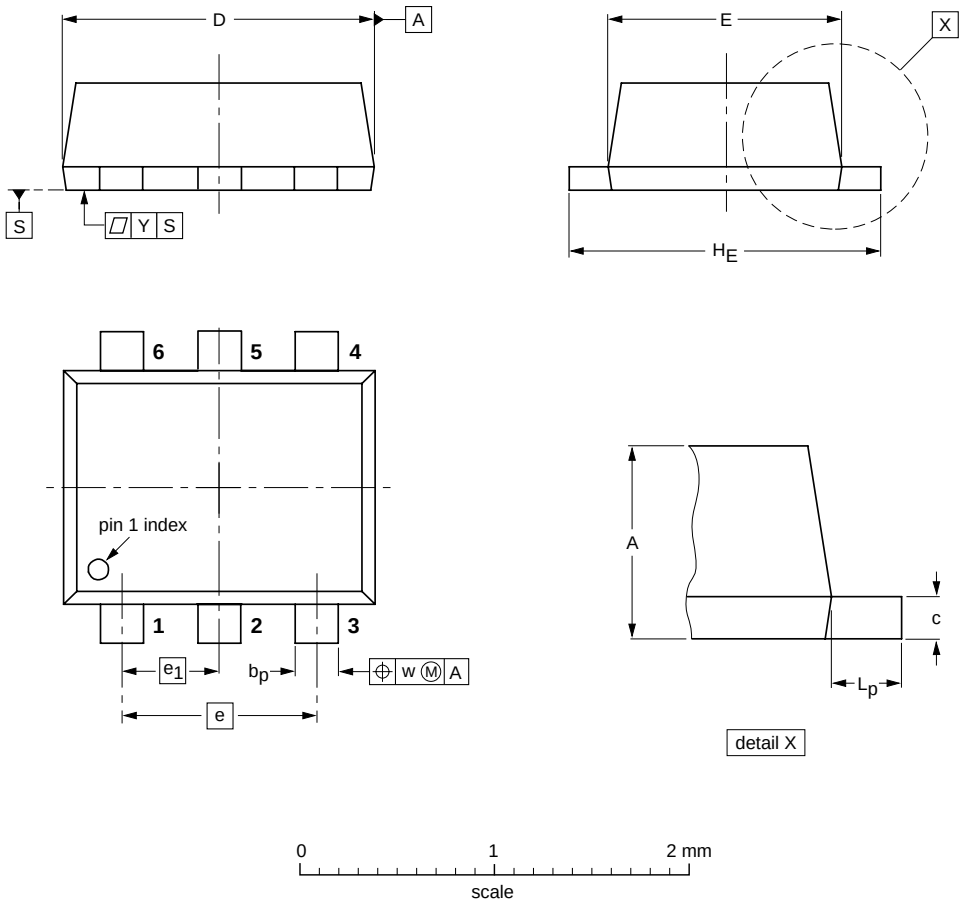
CHARACTERISTICS

T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0	–	–	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0	–	–	1	μA
		V_{CE} = 30 V; I_B = 0; T_j = 150 °C	–	–	50	μA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0	–	–	100	nA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 1 mA	200	–	–	
V_{CEsat}	collector-emitter saturation voltage	I_C = 5 mA; I_B = 0.25 mA	–	–	100	mV
R1	input resistor		3.3	4.7	6.1	kΩ
C_c	collector capacitance	$I_E = I_e$ = 0; V_{CB} = 10 V; f = 1 MHz				
	TR1 (NPN)		–	–	2.5	pF
	TR2 (PNP)		–	–	3	pF

PACKAGE OUTLINES

Plastic surface-mounted package; 6 leads **SOT666**

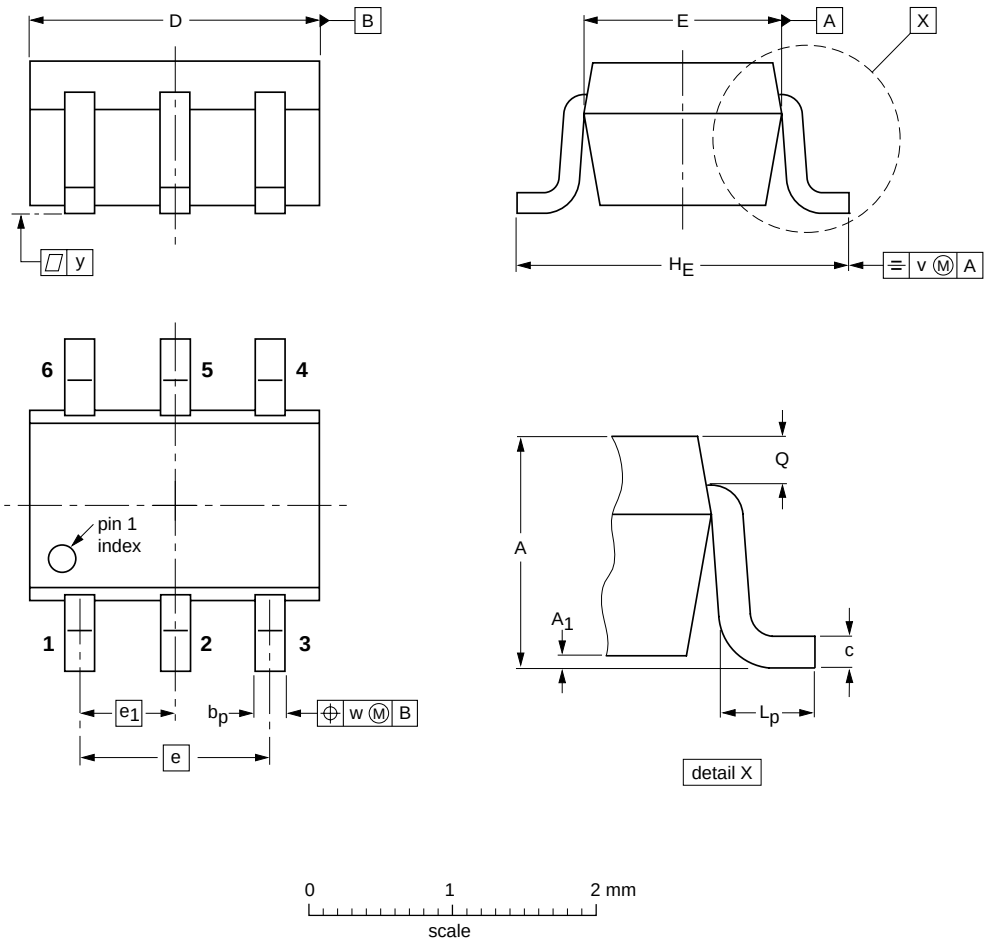


DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT666						~~04-11-08~~ 06-03-16

Plastic surface-mounted package; 6 leads **SOT363**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT363			SC-88			~~04-11-08~~ 06-03-16

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
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NXP Semiconductors

Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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