

PSMN8R3-40YS

N-channel LPAK 40 V 8.6 mΩ standard level MOSFET

Rev. 01 — 25 June 2009

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in LPAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Advanced TrenchMOS provides low $R_{DS(on)}$ and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LPAK provides maximum power density in a Power SO8 package

1.3 Applications

- DC-to-DC convertors
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference

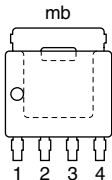
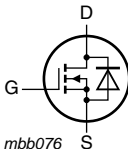
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	-	70	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	74	W
T_j	junction temperature		-55	-	175	°C
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $I_D = 62\text{ A}$; $V_{sup} \leq 40\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$	-	-	33	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; see Figure 14 ;	-	4.5	-	nC
$Q_{G(tot)}$	total gate charge	see Figure 15	-	20	-	nC

Table 1. Quick reference ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 100\text{ }^{\circ}\text{C}$; see Figure 12	-	-	11.6	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 12 ; see Figure 13	-	6.6	8.6	mΩ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>SOT669 (LPAK)</p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN8R3-40YS	LPAK	plastic single-ended surface-mounted package (LPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	40	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	50	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	-	70	A
I_{DM}	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$; see Figure 3	-	274	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	74	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{slid(M)}$	peak soldering temperature		-	260	°C

Source-drain diode

I_S	source current	$T_{mb} = 25\text{ °C}$	-	70	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	274	A

Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 62\text{ A}$; $V_{sup} \leq 40\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$	-	33	mJ
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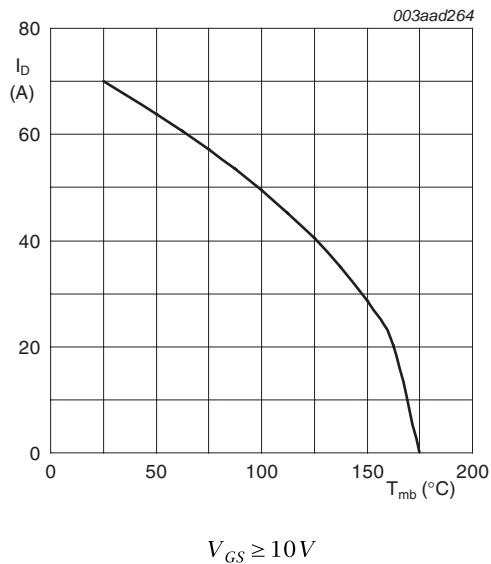


Fig 1. Continuous drain current as a function of mounting base temperature

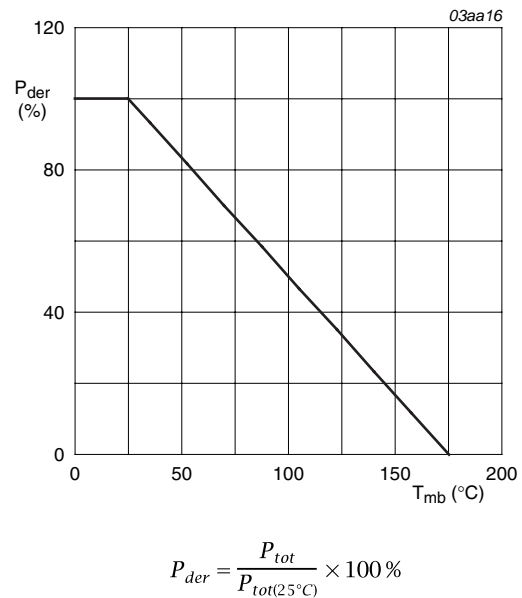
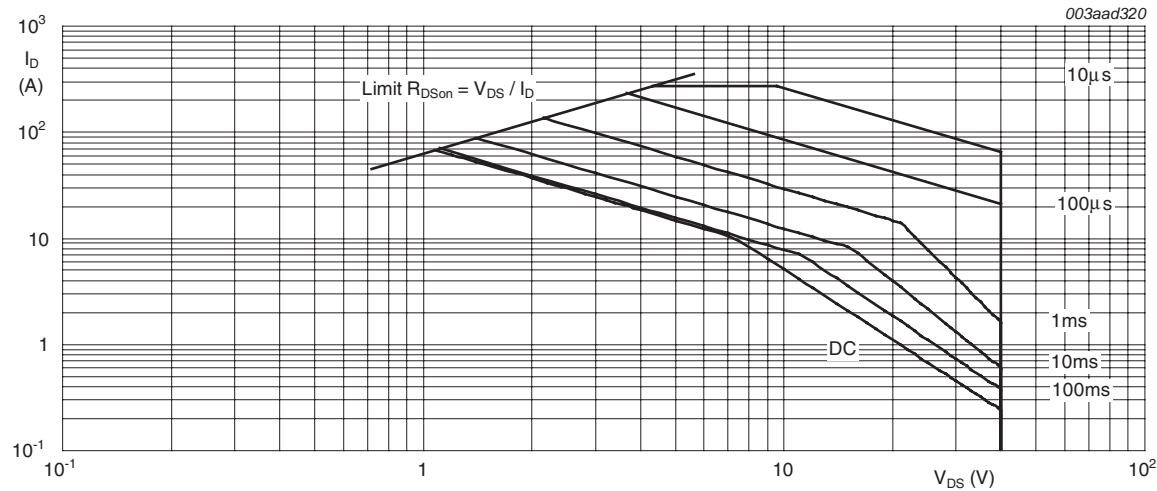


Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25\text{ }^{\circ}\text{C}; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	1.39	2	K/W

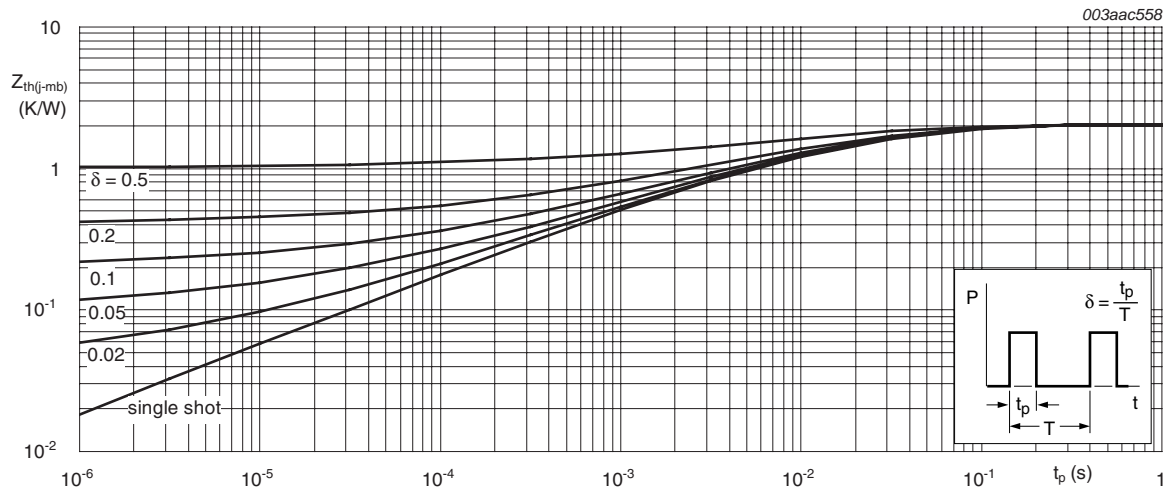


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = -55 ^\circ C$	36	-	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = -55 ^\circ C$; see Figure 10 ; see Figure 11	-	-	4.6	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = 175 ^\circ C$; see Figure 10 ; see Figure 11	1	-	-	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = 25 ^\circ C$; see Figure 10 ; see Figure 11	2	3	4	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-	-	1.5	μA
		$V_{DS} = 40 V$; $V_{GS} = 0 V$; $T_j = 125 ^\circ C$	-	-	10	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	-	100	nA
		$V_{GS} = -20 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 15 A$; $T_j = 100 ^\circ C$; see Figure 12	-	-	11.6	mΩ
		$V_{GS} = 10 V$; $I_D = 15 A$; $T_j = 175 ^\circ C$; see Figure 12	-	-	16	mΩ
		$V_{GS} = 10 V$; $I_D = 15 A$; $T_j = 25 ^\circ C$; see Figure 12 ; see Figure 13	-	6.6	8.6	mΩ
R_G	internal gate resistance (AC)	$f = 1 MHz$	-	0.63	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A$; $V_{DS} = 20 V$; $V_{GS} = 10 V$; see Figure 14 ; see Figure 15	-	20	-	nC
		$I_D = 0 A$; $V_{DS} = 0 V$; $V_{GS} = 10 V$	-	17	-	nC
Q_{GS}	gate-source charge	$I_D = 25 A$; $V_{DS} = 20 V$; $V_{GS} = 10 V$; see Figure 14 ; see Figure 15	-	8	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	4	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	4	-	nC
Q_{GD}	gate-drain charge		-	4.5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A$; $V_{DS} = 20 V$; see Figure 14 ; see Figure 15	-	5.5	-	V
C_{iss}	input capacitance	$V_{DS} = 20 V$; $V_{GS} = 0 V$; $f = 1 MHz$; $T_j = 25 ^\circ C$; see Figure 16	-	1215	-	pF
C_{oss}	output capacitance		-	270	-	pF
C_{rss}	reverse transfer capacitance		-	146	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 V$; $R_L = 1.5 \Omega$; $V_{GS} = 10 V$; $R_{G(ext)} = 4.7 \Omega$	-	13	-	ns
t_r	rise time		-	11	-	ns
$t_{d(off)}$	turn-off delay time		-	21	-	ns
t_f	fall time		-	6	-	ns

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17	-	0.84	1.2	V
t_{rr}	reverse recovery time	$I_S = 50\text{ A}$; $di_S/dt = -100\text{ A/}\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	29	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}$	-	26	-	nC

[1] Tested to JEDEC standards where applicable.

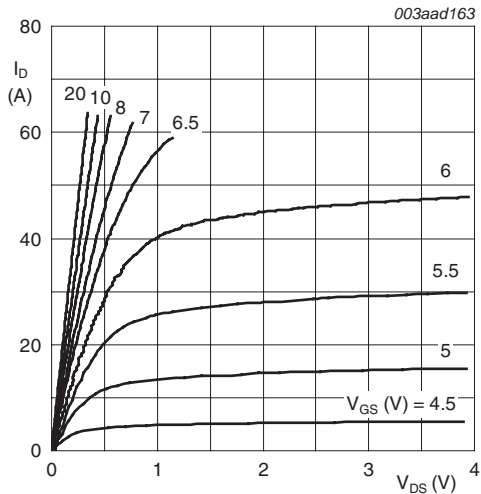


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

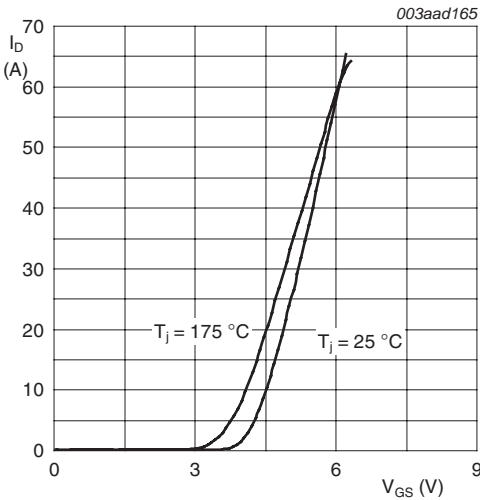


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

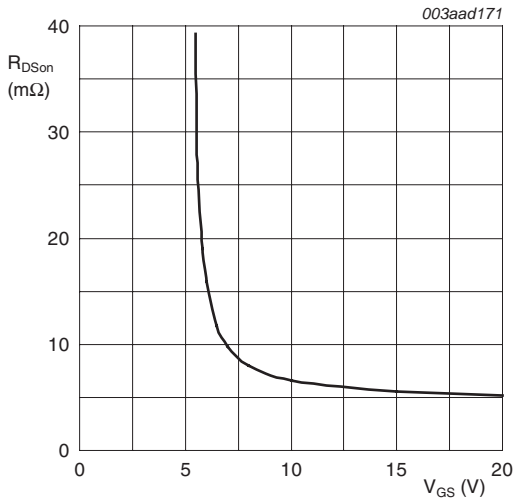


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

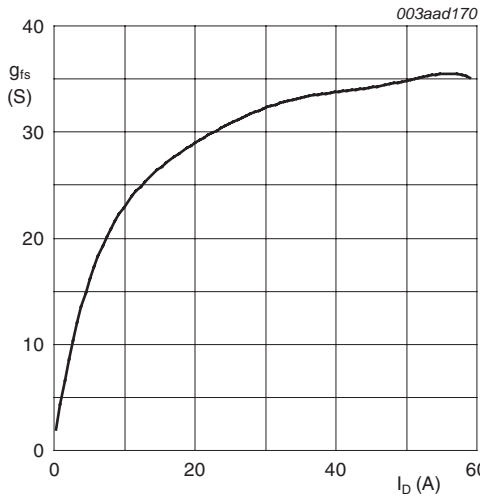
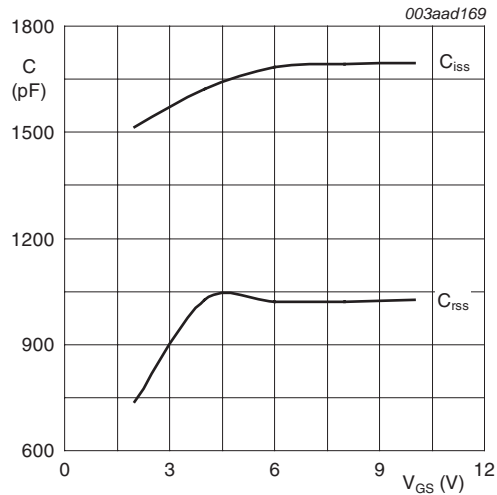
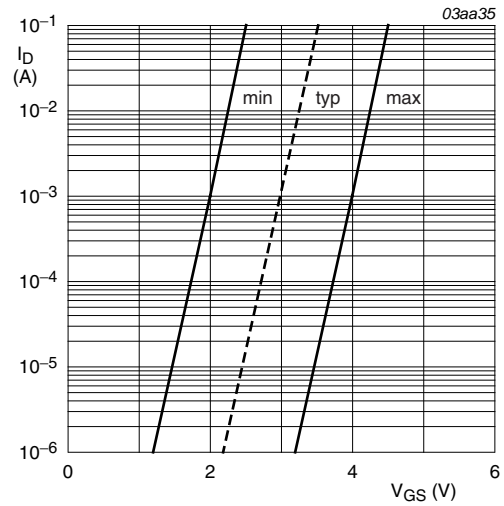


Fig 8. Forward transconductance as a function of drain current; typical values



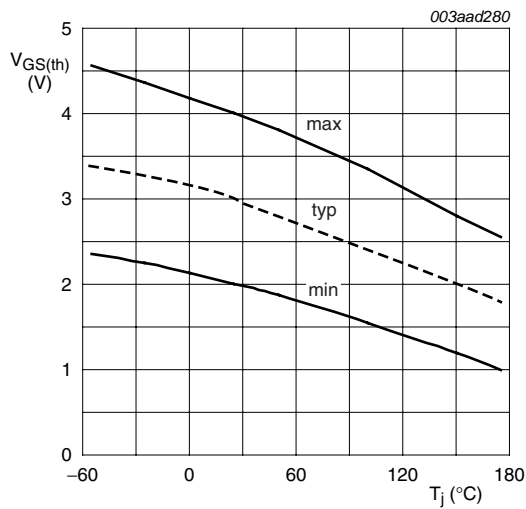
$$V_{DS} = 0V; f = 1MHz$$

Fig 9. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



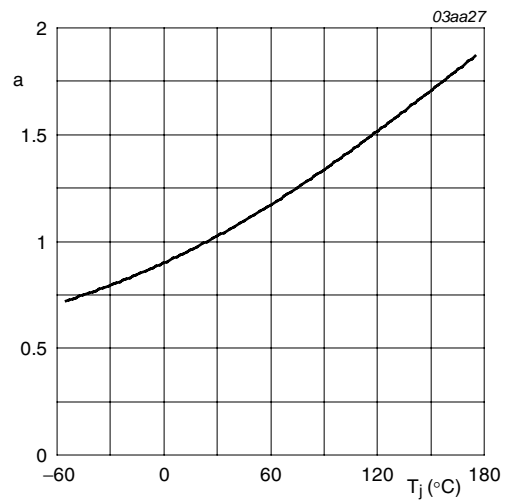
$$T_j = 25^{\circ}C; V_{DS} = 5V$$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



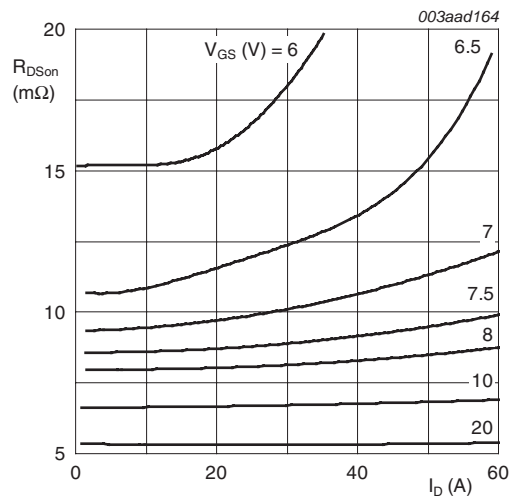
$$I_D = 1mA; V_{DS} = V_{GS}$$

Fig 11. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ C; t_p = 300 \mu s$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

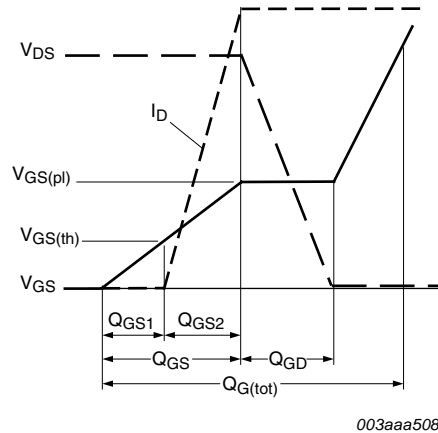
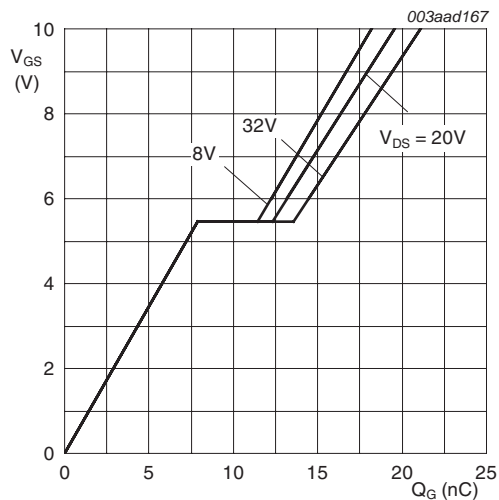
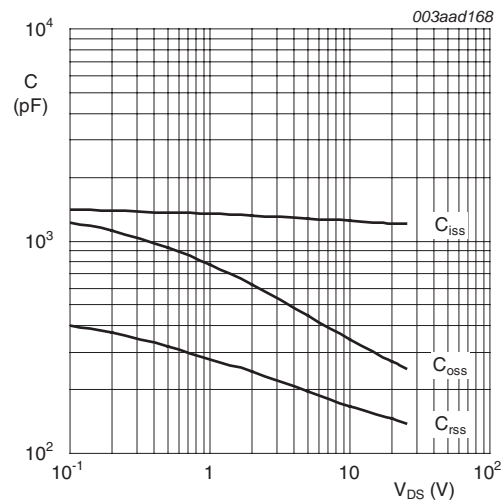


Fig 14. Gate charge waveform definitions



$T_j = 25^\circ C; I_D = 25 A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0 V; f = 1 MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

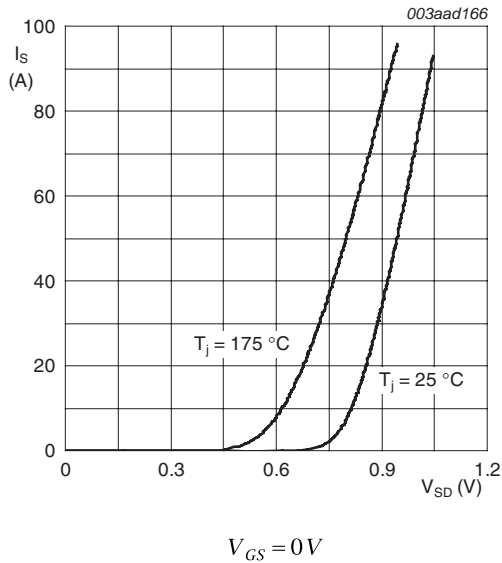


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

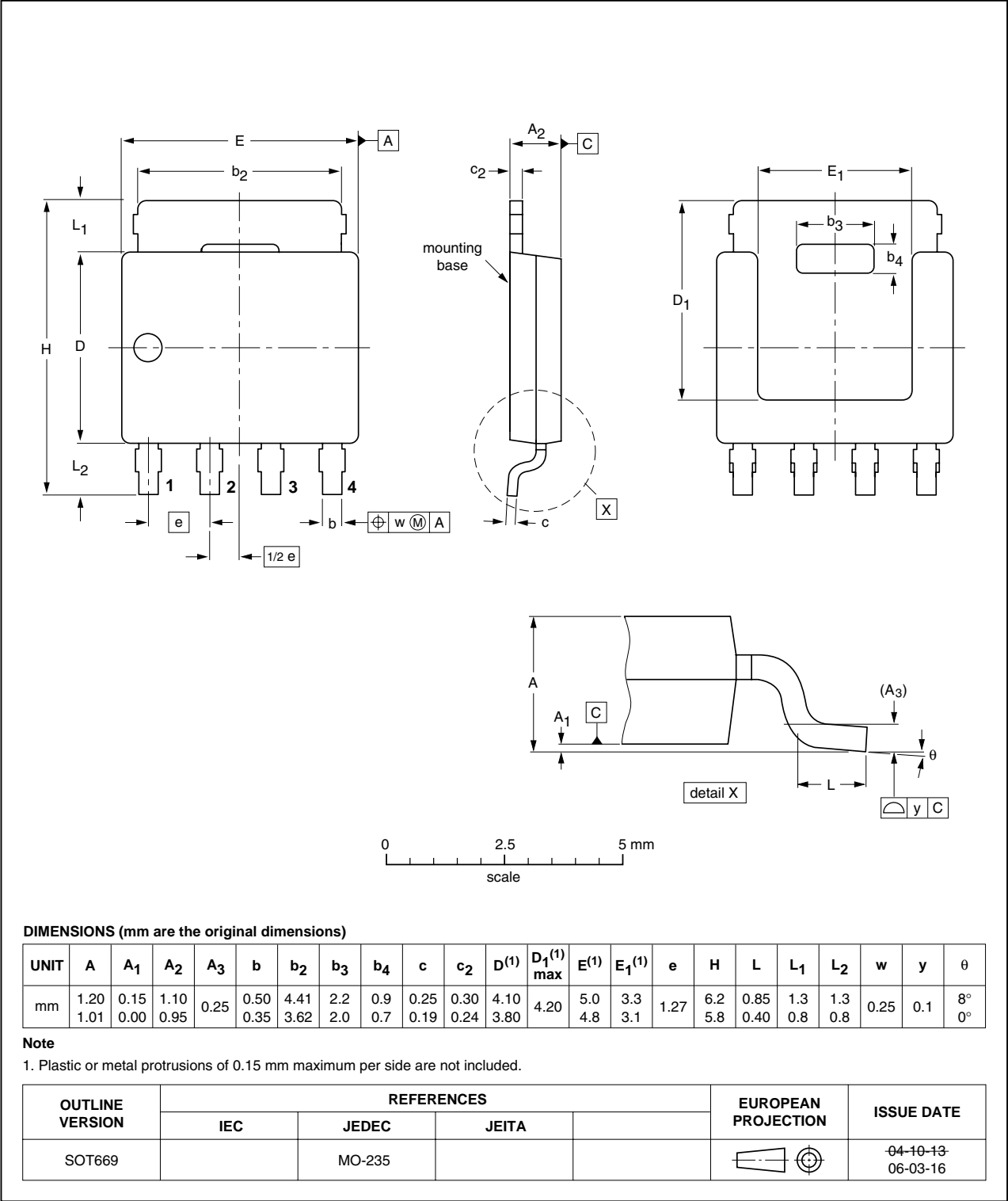


Fig 18. Package outline SOT669 (LPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN8R3-40YS_1	20090625	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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