



PMXB120EPE

30 V, P-channel Trench MOSFET

24 September 2013

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Leadless ultra small and ultra thin SMD plastic package: $1.1 \times 1.0 \times 0.37$ mm
- Exposed drain pad for excellent thermal conduction
- ElectroStatic Discharge (ESD) protection 1 kV HBM
- Drain-source on-state resistance $R_{DSon} = 100$ m Ω

3. Applications

- High-side load switch and charging switch for portable devices
- Power management in battery driven portables
- LED driver
- DC-to-DC converter

4. Quick reference data

Table 1. Quick reference data

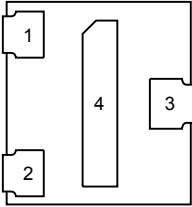
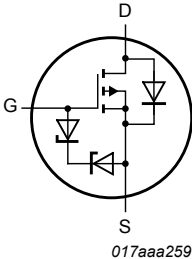
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25$ °C		-	-	-30	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$V_{GS} = -10$ V; $T_{amb} = 25$ °C	[1]	-	-	-2.4	A
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10$ V; $I_D = -2.4$ A; $T_j = 25$ °C		-	100	120	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view DFN1010D-3 (SOT1215)	 017aaa259
2	S	source		
3	D	drain		
4	D	drain		

6. Ordering information

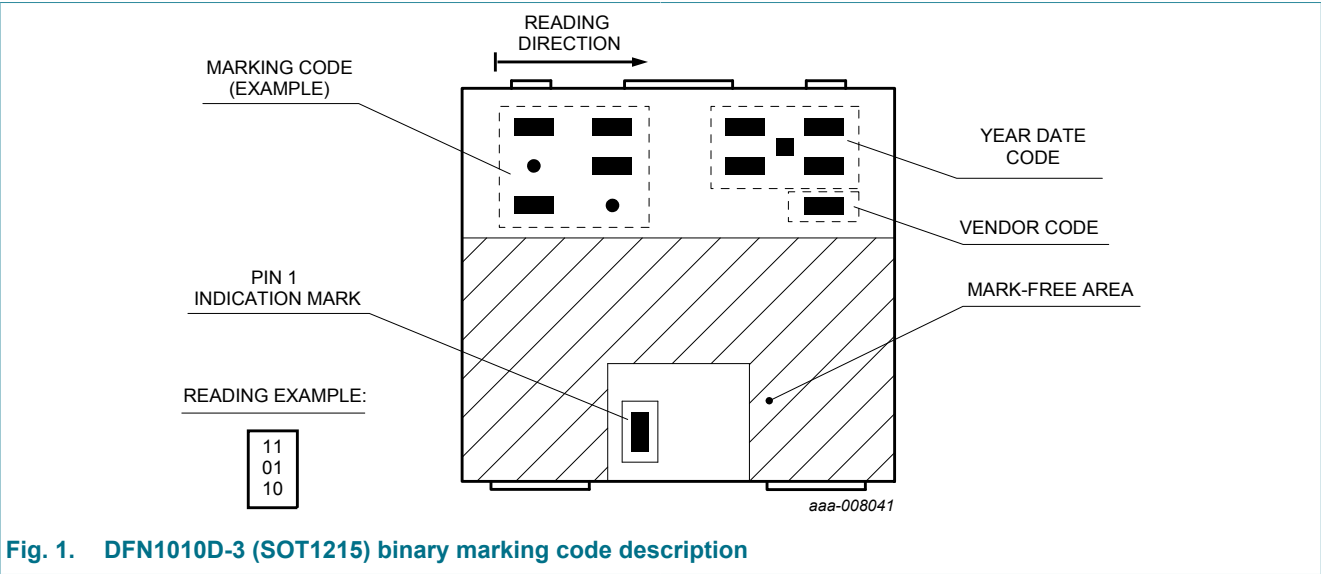
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMXB120EPE	DFN1010D-3	plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body 1.1 x 1.0 x 0.37 mm	SOT1215

7. Marking

Table 4. Marking codes

Type number	Marking code
PMXB120EPE	10 01 00



8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-30	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = -10 V; T _{amb} = 25 °C	[1]	-	-2.4	A
		V _{GS} = -10 V; T _{amb} = 100 °C	[1]	-	-1.5	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-10	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	0.4	W
			[1]	-	1.07	W
		T _{sp} = 25 °C		-	8.33	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-0.9	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

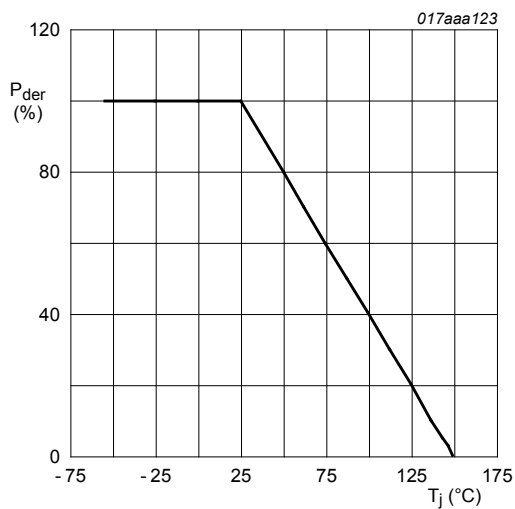


Fig. 2. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$

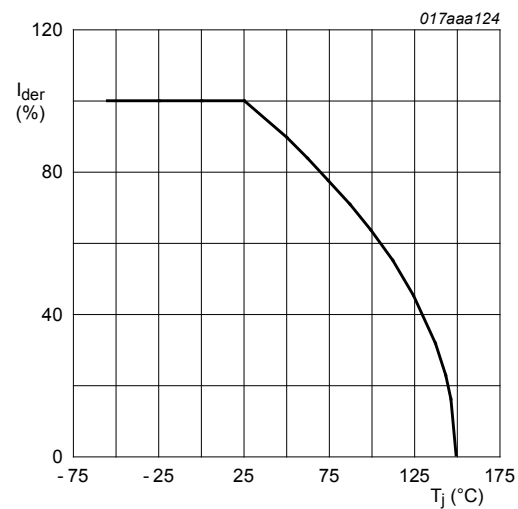
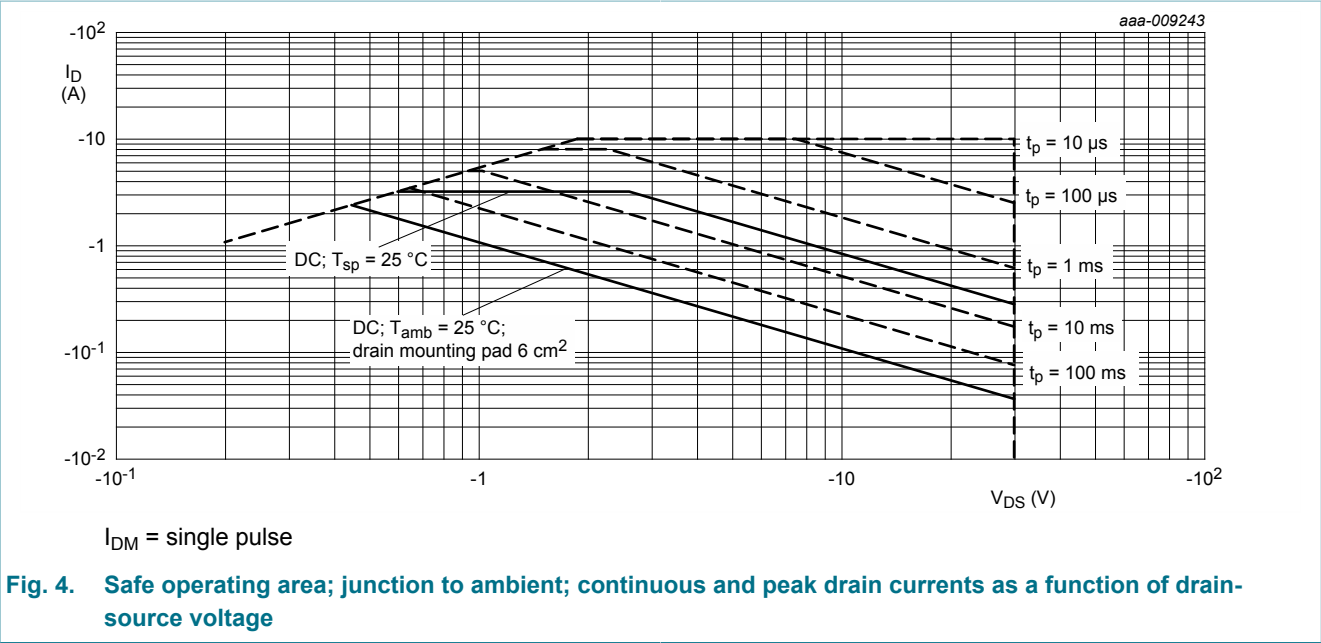


Fig. 3. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	271	312	K/W
			[2]	-	102	117	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	10	15	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain $6 cm^2$.

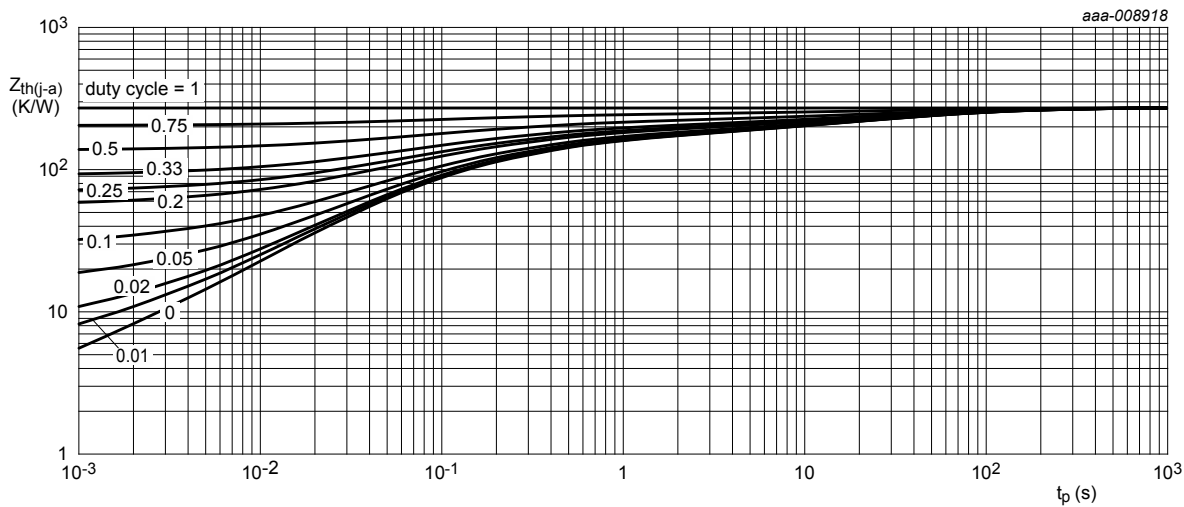


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

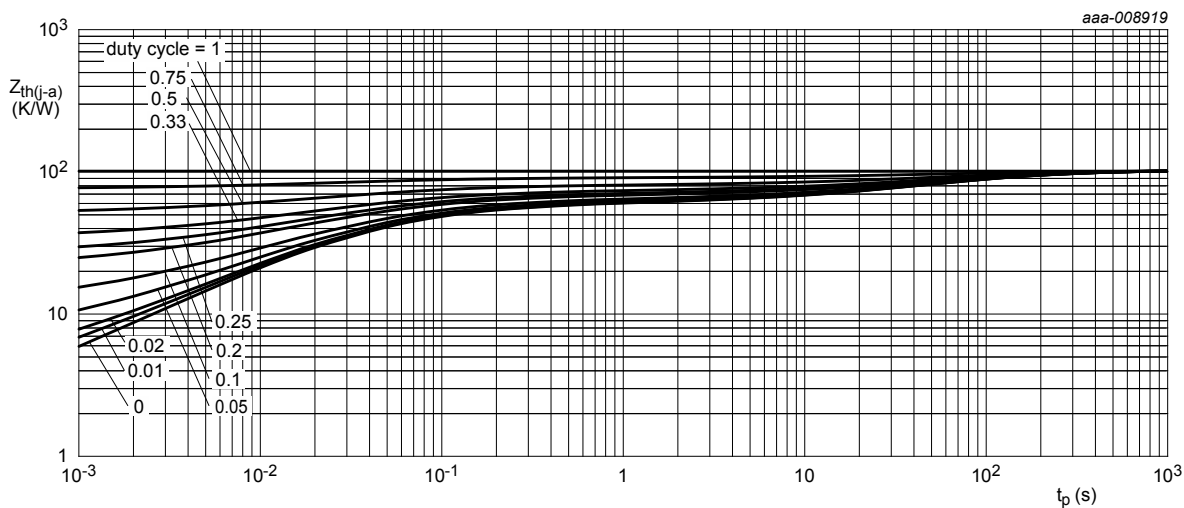


Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-30	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		-1	-1.5	-2.5	V
I _{DSS}	drain leakage current	V _{DS} = -30 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
I _{GSS}	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -16 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-10	μA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-1	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = -10 V; I _D = -2.4 A; T _j = 25 °C		-	100	120	mΩ
		V _{GS} = -10 V; I _D = -2.4 A; T _j = 150 °C		-	156	187	mΩ
		V _{GS} = -4.5 V; I _D = -2 A; T _j = 25 °C		-	125	170	mΩ
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -2.4 A; T _j = 25 °C		-	5	-	S
R _G	gate resistance	f = 1 MHz		-	14.5	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -15 V; I _D = -2.4 A; V _{GS} = -10 V; T _j = 25 °C		-	6.2	11	nC
Q _{GS}	gate-source charge			-	0.9	-	nC
Q _{GD}	gate-drain charge			-	1.1	-	nC
C _{iss}	input capacitance	V _{DS} = -15 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	309	-	pF
C _{oss}	output capacitance			-	41	-	pF
C _{rss}	reverse transfer capacitance			-	32	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -15 V; I _D = -2.4 A; V _{GS} = -10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	4	-	ns
t _r	rise time			-	11	-	ns
t _{d(off)}	turn-off delay time			-	16	-	ns
t _f	fall time			-	7	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -0.9 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.8	-1.2	V

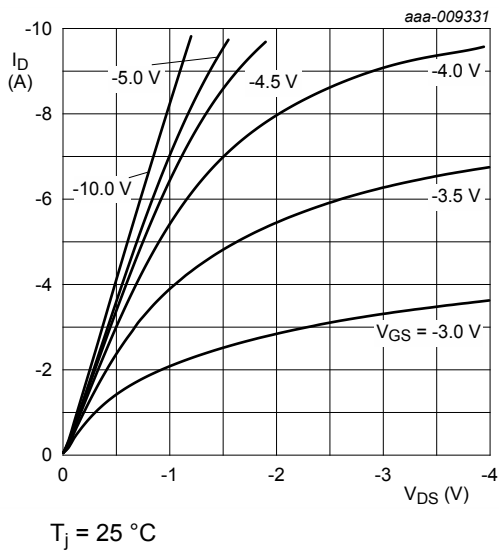


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

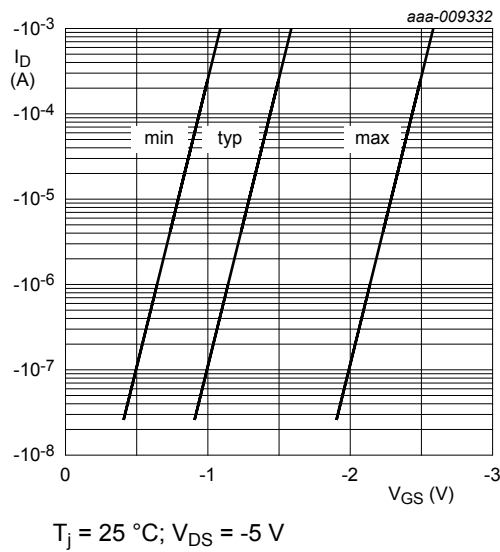


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

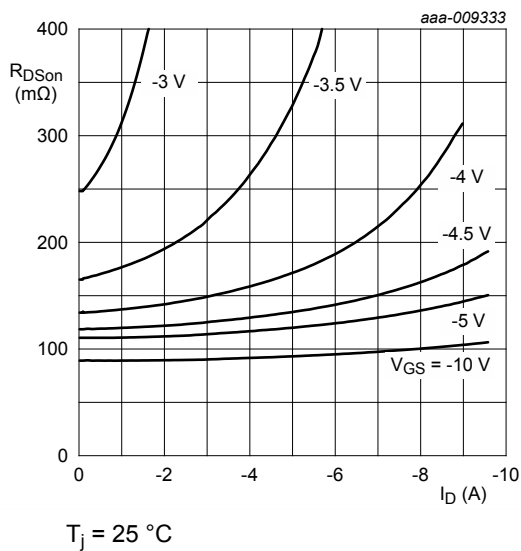


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

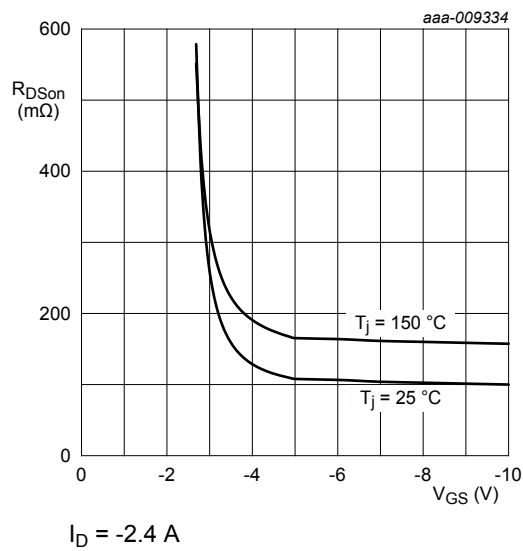


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

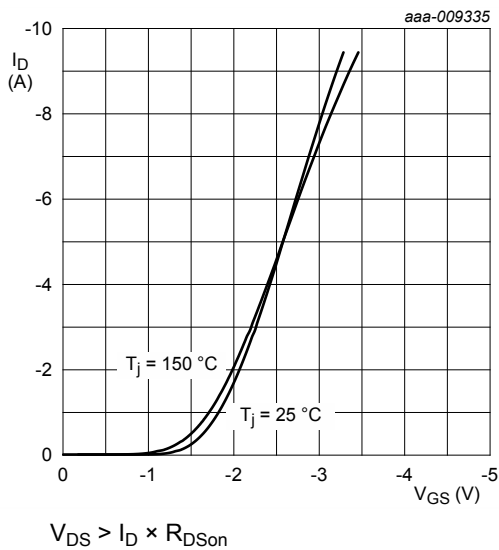


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

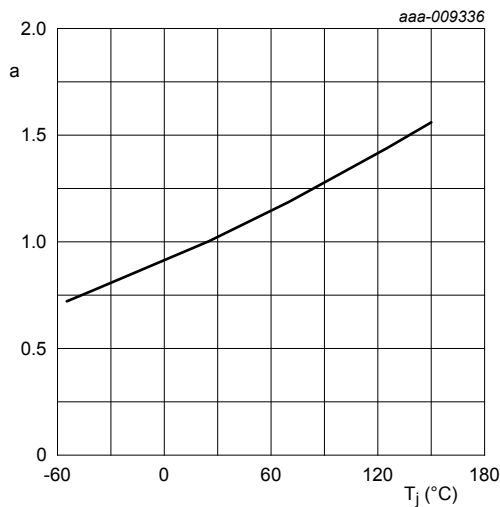


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$$

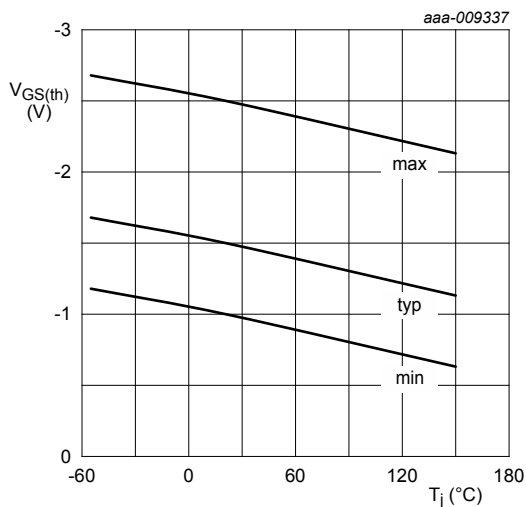


Fig. 13. Gate-source threshold voltage as a function of junction temperature

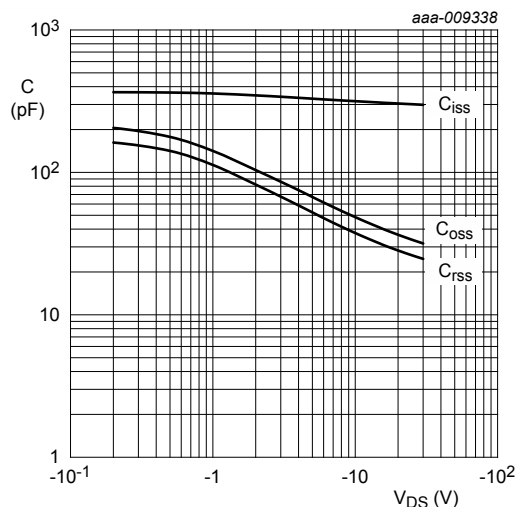


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

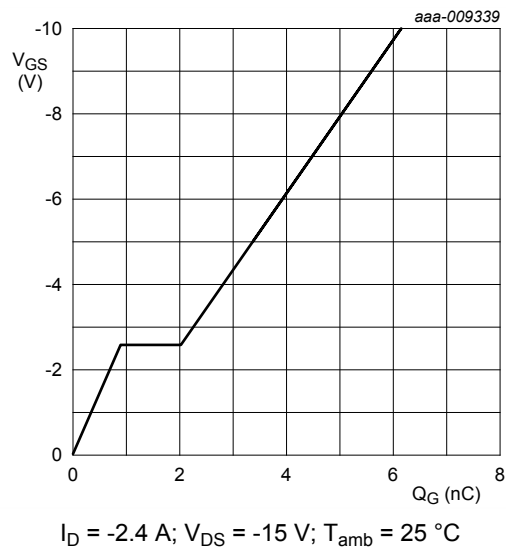


Fig. 15. Gate-source voltage as a function of gate charge; typical values

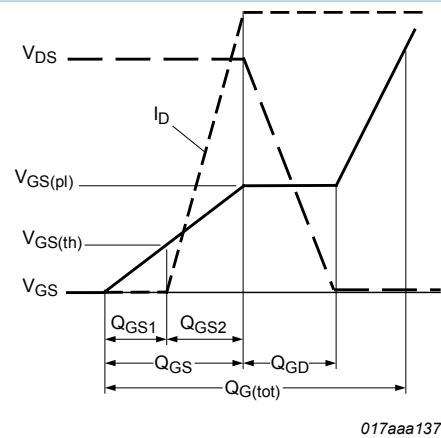


Fig. 16. MOSFET transistor: Gate charge waveform definitions

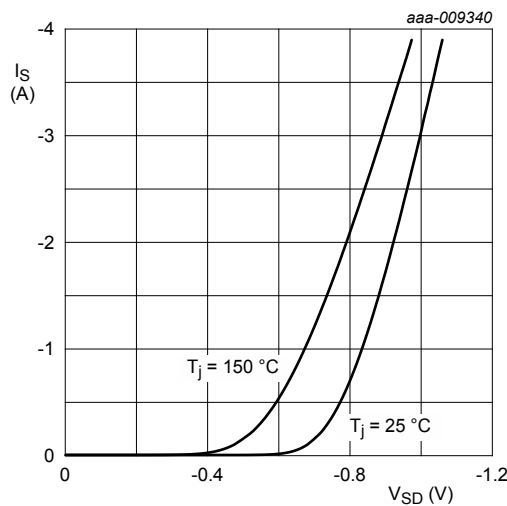


Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

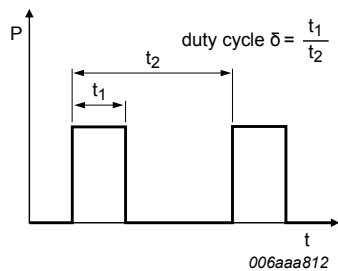


Fig. 18. Duty cycle definition

12. Package outline

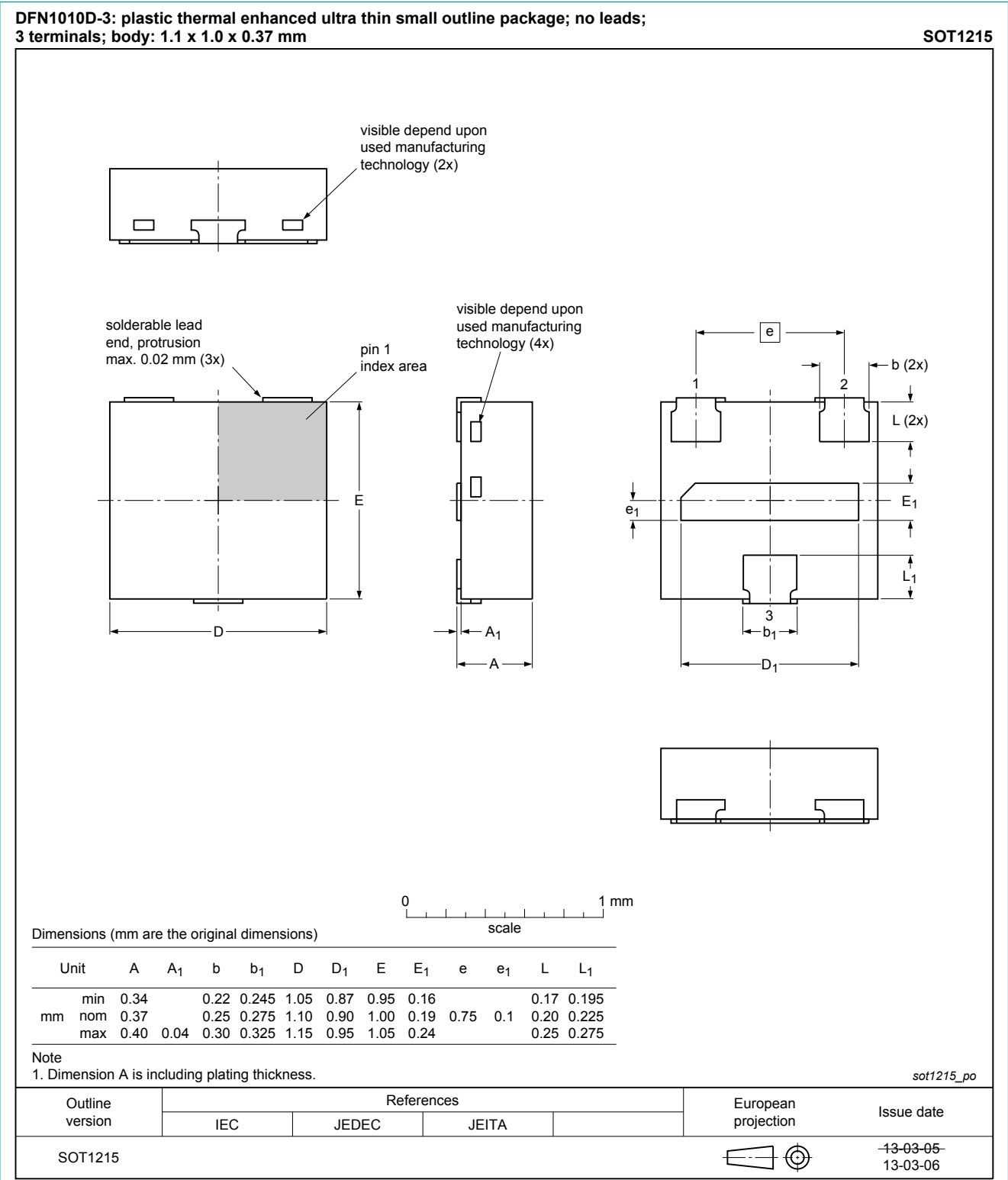


Fig. 19. Package outline DFN1010D-3 (SOT1215)

13. Soldering

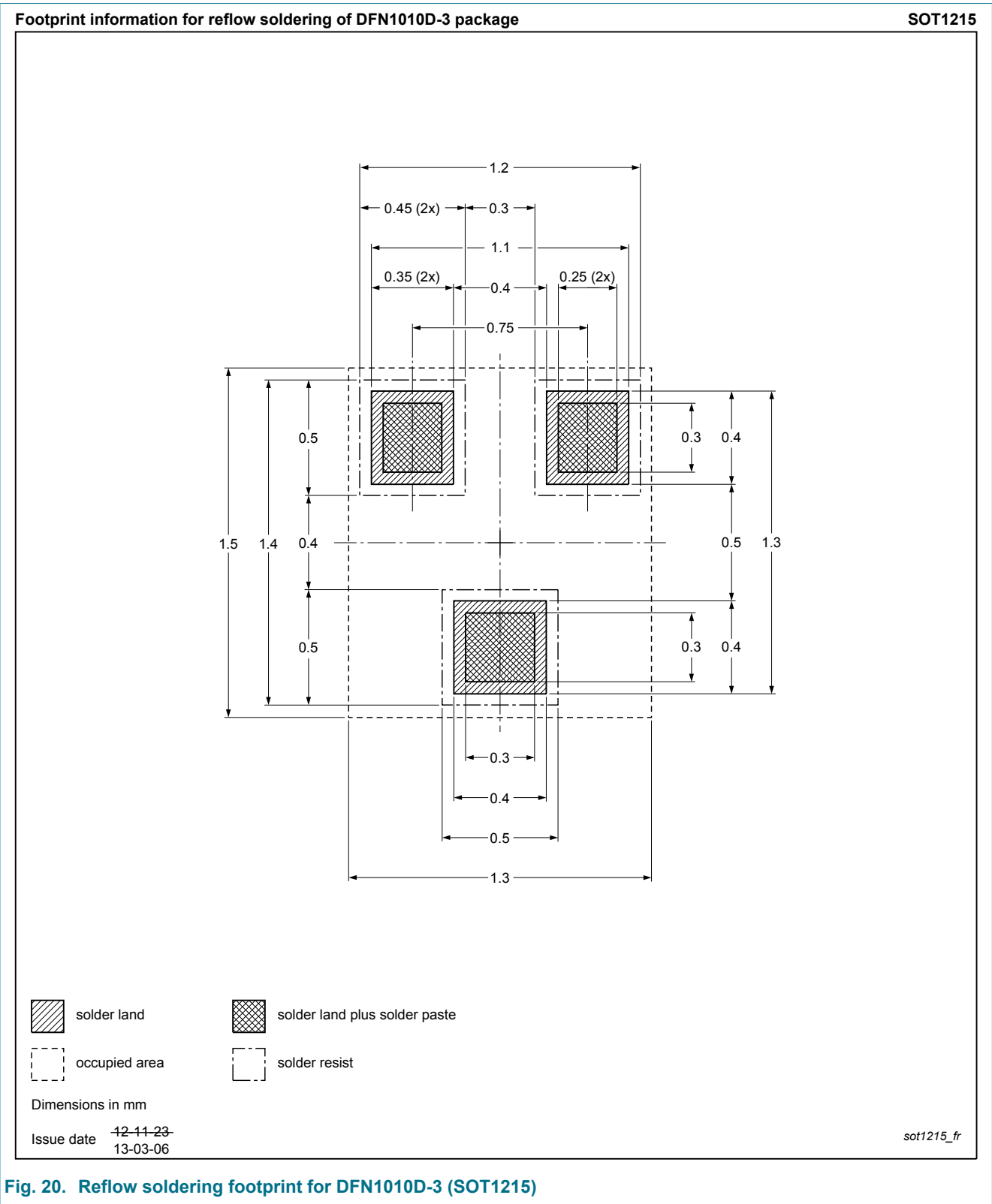


Fig. 20. Reflow soldering footprint for DFN1010D-3 (SOT1215)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMXB120EPE v.1	20130924	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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