



1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- TrenchMOS™ technology
- Low threshold voltage
- Very fast switching
- Subminiature surface mount package.

1.3 Applications

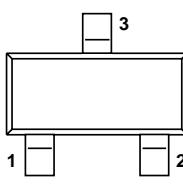
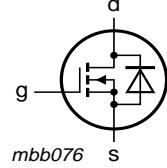
- Battery management
- High-speed switch
- Low power DC-to-DC converter.

1.4 Quick reference data

- $V_{DS} \leq 20\text{ V}$
- $I_D \leq 3.76\text{ A}$
- $P_{tot} \leq 1.92\text{ W}$
- $R_{DSon} \leq 85\text{ m}\Omega$

2. Pinning information

Table 1: Pinning - SOT23, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	source (s)		
3	drain (d)	 Top view MSB003	 mbb076



3. Ordering information

Table 2: Ordering information

Type number	Package			Version
	Name	Description		
PMV56XN	SOT23	Plastic surface mounted package; 3 leads		SOT23

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C}$	-	20	V
V_{GS}	gate-source voltage (DC)		-	± 8	V
I_D	drain current (DC)	$T_{sp} = 25 \text{ }^\circ\text{C}; V_{GS} = 4.5 \text{ V}$; Figure 2 and 3	-	3.76	A
		$T_{sp} = 70 \text{ }^\circ\text{C}; V_{GS} = 4.5 \text{ V}$; Figure 2	-	3	A
I_{DM}	peak drain current	$T_{sp} = 25 \text{ }^\circ\text{C}$; pulsed; $t_p \leq 10 \mu\text{s}$; Figure 3	-	15	A
P_{tot}	total power dissipation	$T_{sp} = 25 \text{ }^\circ\text{C}$; Figure 1	-	1.92	W
T_{stg}	storage temperature		-65	+150	$^\circ\text{C}$
T_j	junction temperature		-65	+150	$^\circ\text{C}$
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25 \text{ }^\circ\text{C}$	-	1.6	A

5. Characteristics

Table 4: Characteristics

$T_j = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(\text{BR})\text{DSS}}$	drain-source breakdown voltage	$I_D = 10 \mu\text{A}; V_{GS} = 0 \text{ V}$	20	-	-	V
$V_{GS(\text{th})}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$; Figure 9	0.65	-	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}$				
		$T_j = 25^\circ\text{C}$	-	0.01	1.0	μA
		$T_j = 55^\circ\text{C}$	-	-	10	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 8 \text{ V}; V_{DS} = 0 \text{ V}$	-	10	100	nA
$R_{DS\text{on}}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 3.6 \text{ A}$; Figure 7 and 8	-	56	85	$\text{m}\Omega$
		$V_{GS} = 2.5 \text{ V}; I_D = 3.1 \text{ A}$; Figure 7 and 8	-	77	115	$\text{m}\Omega$
Dynamic characteristics						
$Q_{g(\text{tot})}$	total gate charge	$V_{DD} = 10 \text{ V}; V_{GS} = 4.5 \text{ V}; I_D = 3.6 \text{ A}$; Figure 13	-	5.4	-	nC
Q_{gs}	gate-source charge		-	0.65	-	nC
Q_{gd}	gate-drain (Miller) charge		-	1.6	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 10 \text{ V}; f = 1 \text{ MHz}$; Figure 11	-	230	-	pF
C_{oss}	output capacitance		-	125	-	pF
C_{rss}	reverse transfer capacitance		-	80	-	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DD} = 10 \text{ V}; R_L = 5.5 \Omega; V_{GS} = 4.5 \text{ V}; R_G = 6 \Omega$	-	12	-	ns
t_r	rise time		-	23	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	50	-	ns
t_f	fall time		-	34	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 1.6 \text{ A}; V_{GS} = 0 \text{ V}$; Figure 12	-	0.8	1.2	V