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Kind regards,

Team Nexperia

PHKD3NQ10T

Dual N-channel TrenchMOS standard level FET

Rev. 02 — 16 December 2010

Product data sheet

1. Product profile

1.1 General description

Dual standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for use in compact designs due to low profile
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- DC-to-DC converters
- Motor and relay drivers

1.4 Quick reference data

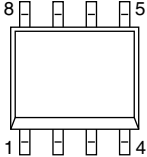
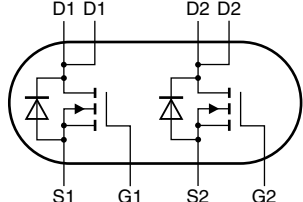
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	100	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; One MOSFET conducting	-	-	3	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$	-	-	2	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 1.5\text{ A}$; $T_j = 25\text{ °C}$	-	70	90	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 3\text{ A}$; $V_{DS} = 80\text{ V}$; $T_j = 25\text{ °C}$	-	8	-	nC



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 SOT96-1 (SO8)	 mbk725
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D	drain2		
6	D	drain2		
7	D	drain1		
8	D	drain1		

3. Ordering information

Table 3. Ordering information

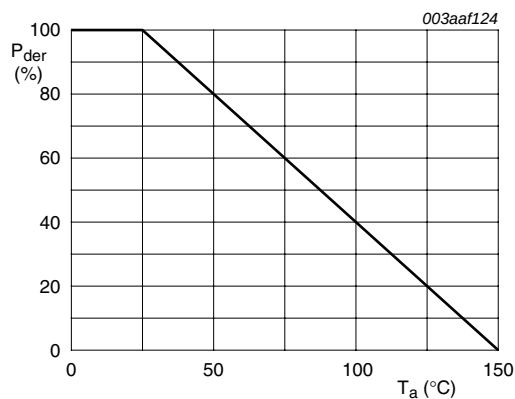
Type number	Package		Version
	Name	Description	
PHKD3NQ10T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

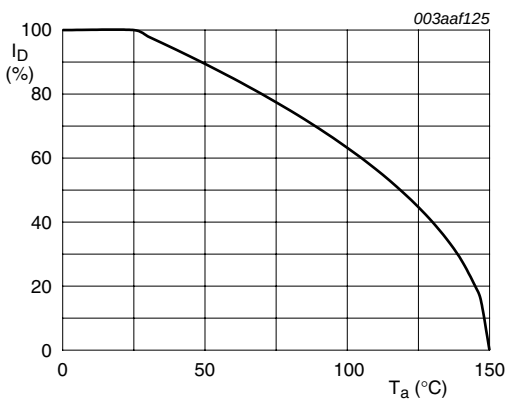
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$T_j \leq 150\text{ °C}$; $T_j \geq 25\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; both MOSFETs conducting	-	2.2	A
		$T_{sp} = 70\text{ °C}$; one MOSFET conducting	-	2.4	A
		$T_{sp} = 70\text{ °C}$; both MOSFETs conducting	-	1.7	A
		$T_{sp} = 25\text{ °C}$; One MOSFET conducting	-	3	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; One MOSFET conducting	-	12	A
P_{tot}	total power dissipation	$T_{sp} = 70\text{ °C}$	-	1.3	W
		$T_{sp} = 25\text{ °C}$	-	2	W
T_{stg}	storage temperature		-65	150	°C
T_j	junction temperature		-65	150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ °C}$	-	2	A
I_{SM}	peak source current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$	-	12	A



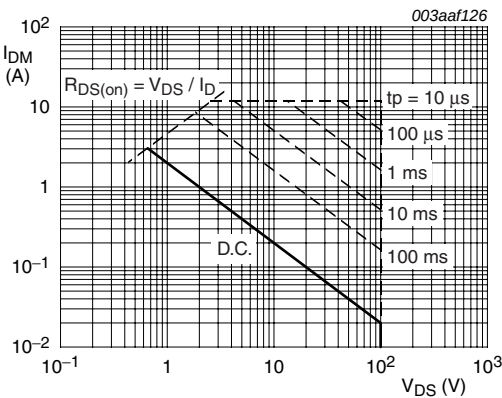
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Surface mounted on FR4 board ; either or both MOSFETs conducting ; $t \leq 10$ sec	-	-	62.5	K/W
		Surface mounted on FR4 board ; either or both MOSFETs conducting	-	150	-	K/W

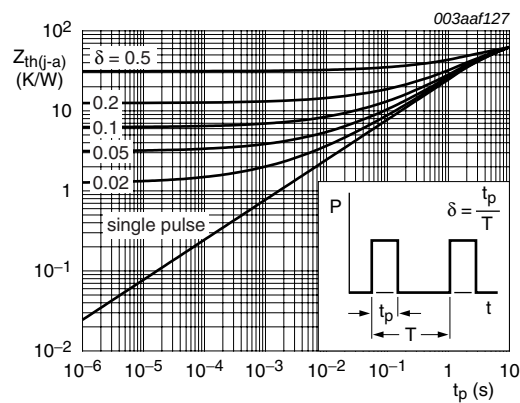


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	89	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	100	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C	-	-	6	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 150 °C	1.1	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C	2	3	4	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	10	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 150 °C	-	-	100	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 1.5 A; T _j = 150 °C	-	-	216	mΩ
		V _{GS} = 10 V; I _D = 1.5 A; T _j = 25 °C	-	70	90	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 3 A; V _{DS} = 80 V; V _{GS} = 10 V; T _j = 25 °C	-	21	-	nC
Q _{GS}	gate-source charge		-	2.5	-	nC
Q _{GD}	gate-drain charge		-	8	-	nC
C _{iss}	input capacitance	V _{DS} = 20 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C	-	633	-	pF
C _{oss}	output capacitance		-	103	-	pF
C _{rss}	reverse transfer capacitance		-	61	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 15 Ω; V _{GS} = 10 V; R _{G(ext)} = 5.6 Ω; T _j = 25 °C	-	6	-	ns
t _r	rise time		-	12	-	ns
t _{d(off)}	turn-off delay time		-	20	-	ns
t _f	fall time		-	10	-	ns
L _D	internal drain inductance	measured from drain lead to centre of die ; T _j = 25 °C	-	2.5	-	nH
L _S	internal source inductance	measured from source lead to source bond pad ; T _j = 25 °C	-	5	-	nH
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 2 A; V _{GS} = 0 V; T _j = 25 °C	-	0.8	1.2	V
t _{rr}	reverse recovery time	I _S = 2 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 25 V; T _j = 25 °C	-	55	-	ns
Q _r	recovered charge	V _{DS} = 25 V; T _j = 25 °C	-	135	-	nC

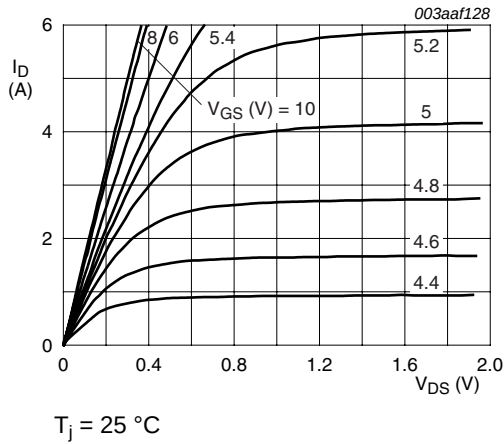


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

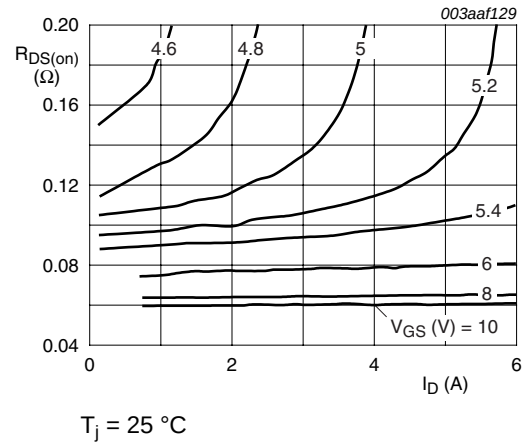


Fig 6. Drain-source on-state resistance as a function of drain current; typical values

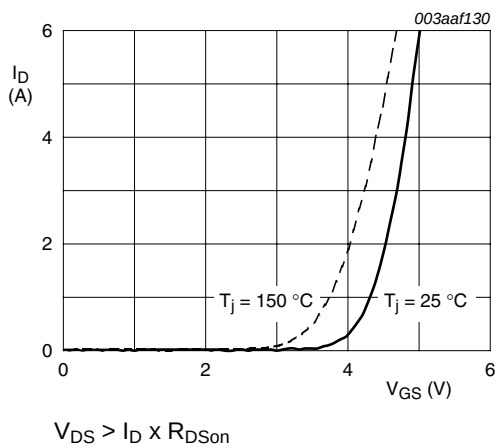


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

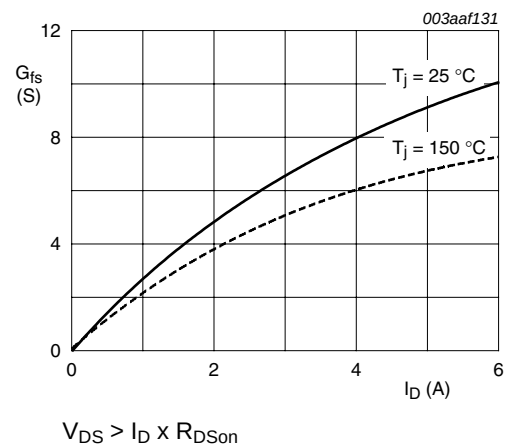


Fig 8. Forward transconductance as a function of drain current; typical values

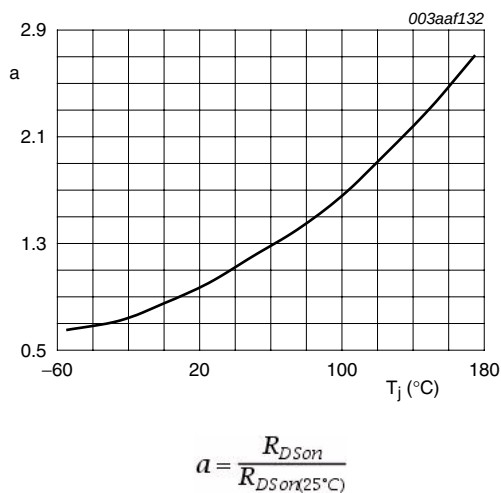


Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature

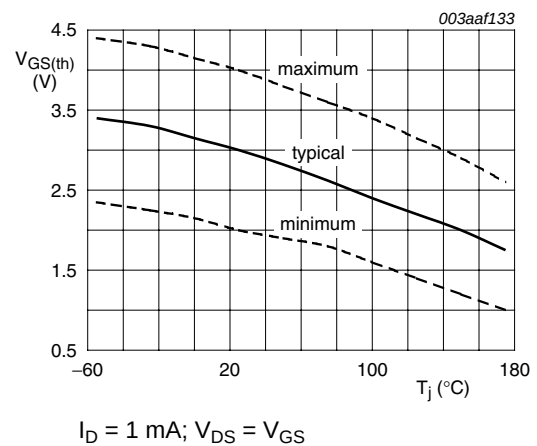


Fig 10. Gate-source threshold voltage as a function of junction temperature

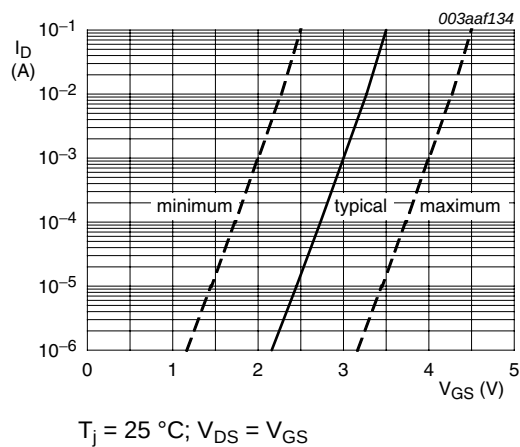


Fig 11. Sub-threshold drain current as a function of gate-source voltage

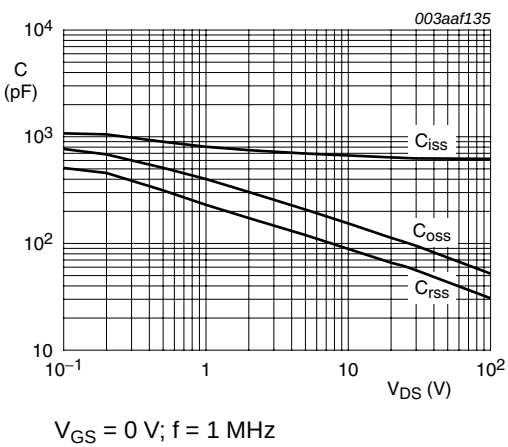


Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

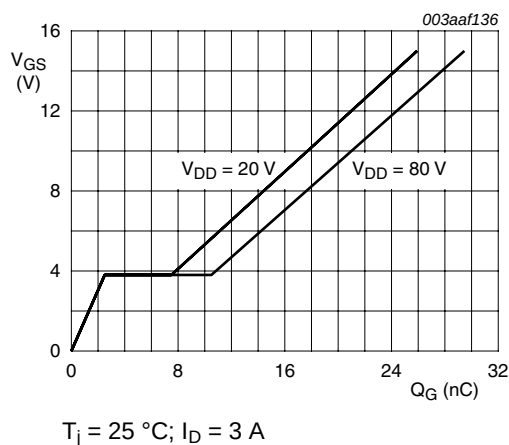


Fig 13. Gate-source voltage as a function of gate charge; typical values

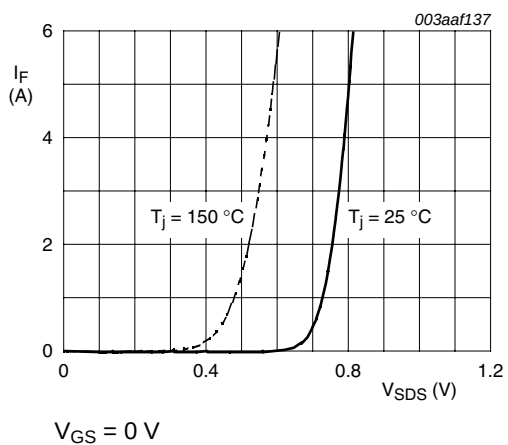


Fig 14. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

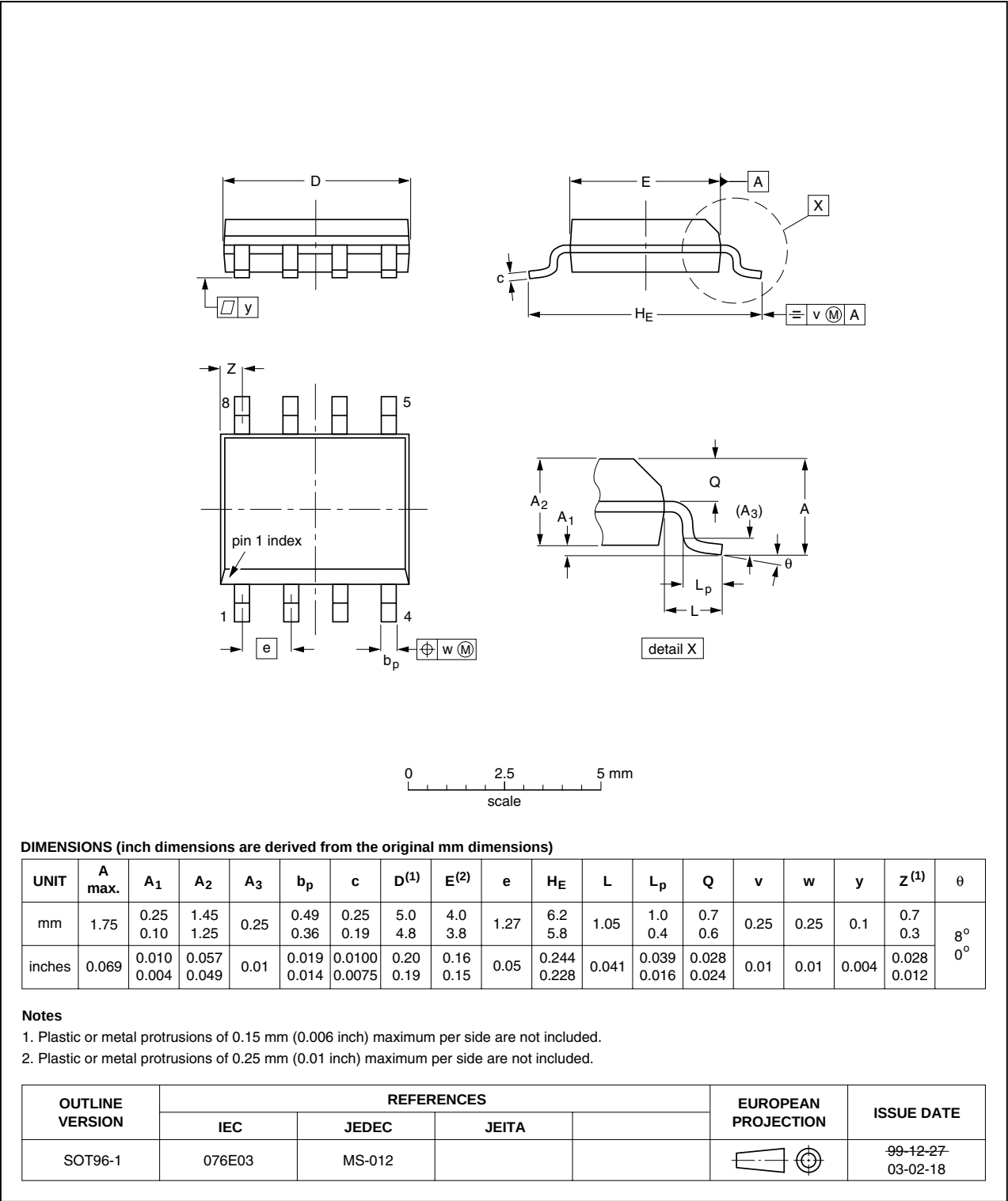


Fig 15. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHKD3NQ10T v.2	20101216	Product data sheet	-	PHKD3NQ10T v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
PHKD3NQ10T v.1	19990801	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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