PGA900 Programmable Resistive Sensing Conditioner With Digital and Analog Outputs

1 Features

- High Accuracy, Low Noise, Low Power, Small Size Resistive Sensing Signal Conditioner
- User-Programmable Temperature and Nonlinearity Compensation
- On-Chip ARM® Cortex® M0 Microprocessor Allows Users to Develop and Implement Calibration Software
- One-Wire Interface Enables the Communication through Power Supply Pin Without Using Additional Lines
- On-Chip Power Management Accepts Wide Power Supply Voltage From 3.3 V to 30 V
- Operating Temperature Range: –40°C to +150°C
- Memory
  - 8 kB Software Memory
  - 128 Bytes EEPROM
  - 1 kB Data SRAM
- Accommodates Sensor Sensitivities From 1 mV/V to 135 mV/ V
- Two Individual Analog-Front End (AFE) Chains, Each Including:
  - Low Noise Programmable Gain Amplifier
  - 24-Bit Sigma-Delta Analog-to-Digital Converter
- Built-In Internal Temperature Sensor With Option to Use External Temperature Sensor
- 14-Bit DAC With Programmable Gain Amplifier
- Output Options:
  - Ratiometric and Absolute Voltage Output
  - 4- to 20-mA Current Loop Interface
  - One-Wire Interface (OWI) Over Power Line
  - PWM Output
  - Serial Peripheral Interface (SPI)
  - Inter-Integrated Circuit (I^2C)
- Depletion MOSFET Gate Driver
- Diagnostic Functions

2 Applications

- Pressure Sensor Transmitters and Transducers
- Liquid Level Meters and Flow Meters
- Weight Scales, Load Meters, and Strain Gauges
- Thermocouples, Thermistors, and 2-Wire Resistance Thermometers (RTD)
- Resistive Field Transmitters

3 Description

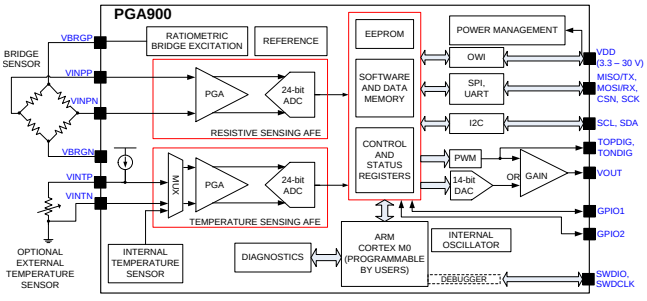
The PGA900 is a signal conditioner for resistive sensing applications. It can accommodate various sensing element types. The PGA900 conditions its input signals by amplification and digitization through two analog front end channels. With the user programmed software in the on-chip ARM Cortex M0 processor, the PGA900 can perform linearization, temperature compensation, and other user defined compensation algorithms. The conditioned signal can be output as ratiometric voltage, absolute voltage, 4- to 20-mA current loop or PWM. The data and configuration registers can also be accessed through SPI, I^2C, UART, and two GPIO ports. In addition, the unique OWI allows communication and configuration through the power supply pin without using additional lines. The PGA900 operating voltage is from 3.3 V to 30 V and it can operate in temperatures from –40°C to +150°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PGA900	VQFN (36)	6.00 mm × 6.00 mm
	DSBGA (36)	3.66 mm × 3.66 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

PGA900 Simplified Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2015) to Revision B — **Page**

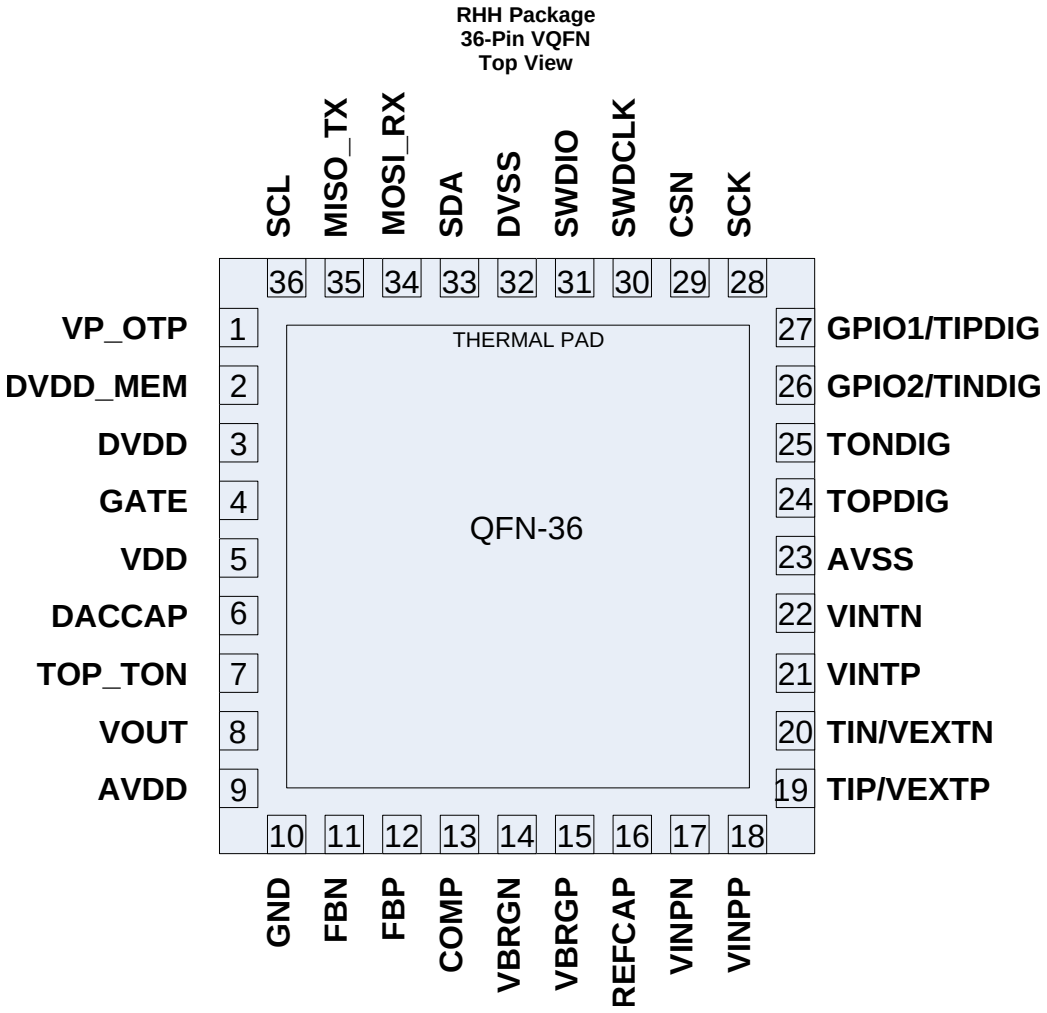
- Added a new package to the *Device Information* table ... 1
- Added new YZS package drawing ... 3
- Changed minimum and nominal OTP programming voltages from 7.0 and 7.4 to 7.2 and 7.6 ... 6
- Added DSBGA thermal info ... 7
- Added statement related to waiting time before reading trace FIFO ... 61
- Replaced "Data" with "Development" ... 69
- Fixed broken figure crossreference ... 71
- Replaced "PADC" with "TADC" ... 86
- Replaced "PADC" with "TADC" ... 86
- Fixed description for "0" state ... 109

Changes from Original (January 2015) to Revision A — **Page**

- Updated device to production data ... 1

5 Pin Configuration and Functions

YZS Package
36-Pin DSBGA
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DSBGA	VQFN		
AVDD	E6	9	O	Analog voltage
AVSS	B1	23	—	Analog ground
COMP	E5	13	I	Output compensation
CSN	A2	29	I	SPI chip select
DACCAP	D4	6	O	DAC capacitor
DVDD	B6	3	O	DVDD regulator output
DVDD_MEM	A6	2	I	Power supply for EEPROM and OTP
DVSS	A3	32	—	Digital ground
FBN	F6	11	I	Feedback N
FBP	F5	12	I	Feedback P
GATE	C5	4	O	N-channel depletion MOSFET drive
GND	E4	10	—	Ground
GPIO_1/TIPDIG	B2	27	I/O	General-purpose I/O 1 or digital test in P
GPIO_2/TINDIG	C2	26	I/O	General-purpose I/O 2 or digital test in N
MISO/TX	A5	35	O	SPI slave data out or UART Tx
MOSI/RX	A4	34	I	SPI slave data in or UART Rx
REFCAP	F2	16	O	ADC reference capacitor
SCK	A1	28	I	SPI clock
SCL	B4	36	I	I^2C clock
SDA	C4	33	I/O	I^2C data
SWDCLK	C3	30	I	Serial wire debug clock
SWDIO	B3	31	I/O	Serial wire debug I/O
VBRGN	F4	14	O	Bridge drive N
VBRGP	F3	15	O	Bridge drive P
VDD	C6	5	I	Input power supply
VINTN	C1	22	I	External temperature sensor N input
VINTP	D1	21	I	External temperature sensor P input
VINPN	E1	17	I	Resistive sensor N input
VINPP	F1	18	I	Resistive sensor P input
VOUT	D6	8	O	DAC gain output
VP_OTP	B5	1	I	OTP programming voltage
TONDIG	D3	25	O	Digital test output N
TIN/VEXTN	E3	20	I	Analog test N in or V external N for T signal path
TIP/VEXTP	E2	19	I	Analog test P in or V external P for T signal path
TOP_TON	D5	7	O	Analog testout P or analog testout N
TOPDIG	D2	24	O	Digital test output P

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Voltage	VDD	–28	33	V
	GATE	–0.3	33	
	At VP_OTP	–0.3	8	
	At sensor input and drive pins	–0.3	2	
	At any I/O pin	–0.3	3.6	
	At FBP pin	–2	V_{DD} + 0.3	
I_{DD}	Short on VOUT supply current		25	mA
T_{Jmax}	Maximum junction temperature		155	°C
T_{lead}	Lead temperature (soldering, 10 s)		260	°C
T_{stg}	Storage temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) – EIA/JESD22-A114	±2000	V
		Field induced charge device model (CDM) – JESD22-C101	±500	

6.3 Recommended Operating Conditions

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Power supply voltage		3.3		30	V
	Slew rate	V_{DD} = 0 to 30 V			0.5	V/µs
I_{DD}	Power supply current – normal operation	No load on VBRG, no load on DAC, *f* = 1 MHz			2.6	mA
I_{DD}	Power supply current – EEPROM programming	While EEPROM is being programmed, no load on VBRG, no load on DAC			9 (1)	mA
VP_OTP	OTP programming voltage		7.2	7.6	7.8	V
	OTP programming voltage slew rate				1	V/µs
I_VP_OTP	OTP programming current	During OTP programming			5	mA
tprog_OTP	OTP programming timing per byte		120		200	µs
T_A	Operating ambient temperature		–40		150	°C
	Programming temperature	OTP or EEPROM	–40		140	°C
	Start-up time (including analog and digital)	VDD ramp rate 0.5 V/µs			1	ms
	Capacitor on VDD pin		10			nF

(1) Programming EEPROM results in additional 6 mA of current on VDD pin.

6.4 Thermal Information

THERMAL METRIC(1)		PGA900		UNIT
		RHH (VQFN)	YZS (DSBGA)	
		36 PINS	36 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.6	49.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.4	0.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	10	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.4	10.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

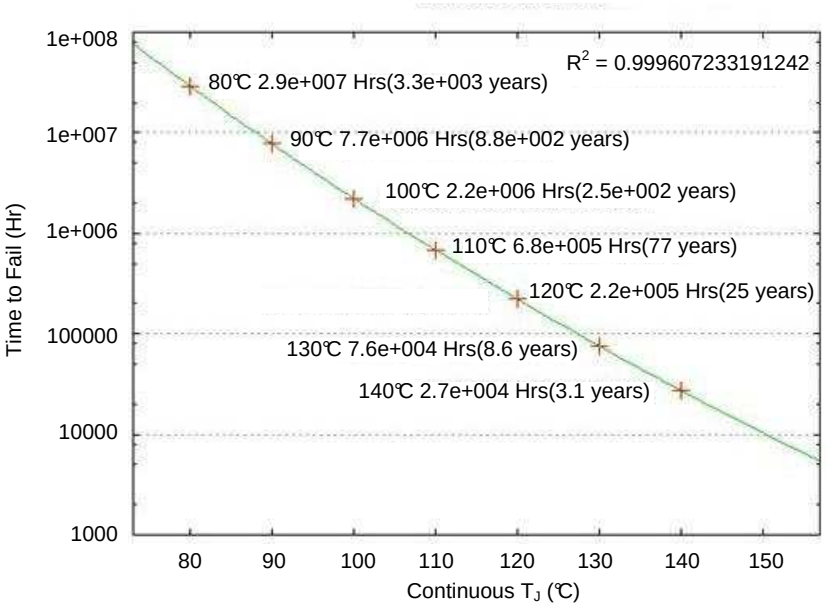


Figure 1. Estimated QFN Wirebond Life is 10392 hours (1.2 years)

6.5 Electrical Characteristics—Gate Drive

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD voltage when using GATE control(1)(2)	V_{DD} = 5 V		3.5		V
PSRR while in regulation			87		dB

(1) When Gate Drive is not being used, the GATE pin must be connected to GND and gate control must be disabled by setting GATE_CTRL_SD bit in ALPWR register to 1.
(2) When Gate Drive is used, a capacitor of up to 1 nF is recommended to be connected to the GATE pin. The gate threshold voltage for the external depletion NMOS must be less than –1.5 V.

6.6 Reverse Voltage Protection

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reverse voltage		–28			V
Voltage drop across reverse voltage protection element			20		mV
RDS_{on} of reverse voltage protection element(1)	VDD = 5 V	1.67		6.66	Ω

(1) Specified by design

6.7 Regulators

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AVDD}	AVDD voltage	C_{AVDD} = 100 nF		3		V
V_{AVDD_POR}	AVDD voltage – digital POR			2.7		V
	AVDD voltage – digital POR Hysteresis			0.1		V
I_{AVDD}	External load on AVDD pin				4	mA
V_{DVDD}	DVDD voltage – operating	C_{DVDD} = 100 nF		1.8		V
V_{DVDD_POR}	DVDD voltage – digital POR			1.5		V
	DVDD voltage – digital POR hysteresis			0.1		V

6.8 Internal Reference

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
Inaccurate reference voltage		1.2		V
Accurate reference voltage		2.5		V
Accurate reference initial error	–0.1%		0.1%	
Accurate reference voltage TC(1)	–10	±4.5	10	ppm/°C
Capacitor value on REFCAP pin	10		1000	nF

(1) $$\text{TEMP DRIFT} = \frac{\text{Value at TEMP} - \text{Value at 25°C}}{\text{Value at 25°C} \times \Delta\text{TEMP}} \times 10^6$$

6.9 Internal Oscillator

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal oscillator frequency	T_A = 25°C		4		MHz
Internal oscillator frequency variation	Across operating temperature		±1%		

6.10 Bridge Sensor Supply

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBRG SUPPLY FOR RESISTIVE BRIDGE SENSORS						
V_{BRGP}-V_{BRGN}	Bridge supply voltage	Bridge supply control bit = 0b00, no load		2.5		V
		Bridge supply control bit = 0b01, no load		2		
		Bridge supply control bit = 0b10, no load		1.25		
	Bridge supply voltage temperature variation (1)	Across temperature for 2.5 V bridge output at no load		6.5	20	ppm/°C
		Across temperature for 2 V bridge output at no load		7.5		
		Across temperature for 1.25 V bridge output at no load		15.5		
I_{BRG}	Current supply to the bridge				1.5	mA
C_{BRG}	Capacitive load	R_{BRG} = 20 kΩ			2	nF

(1) $$\text{TEMP DRIFT} = \frac{\text{Value at TEMP} - \text{Value at 25°C}}{\text{Value at 25°C} \times \Delta\text{TEMP}} \times 10^6$$

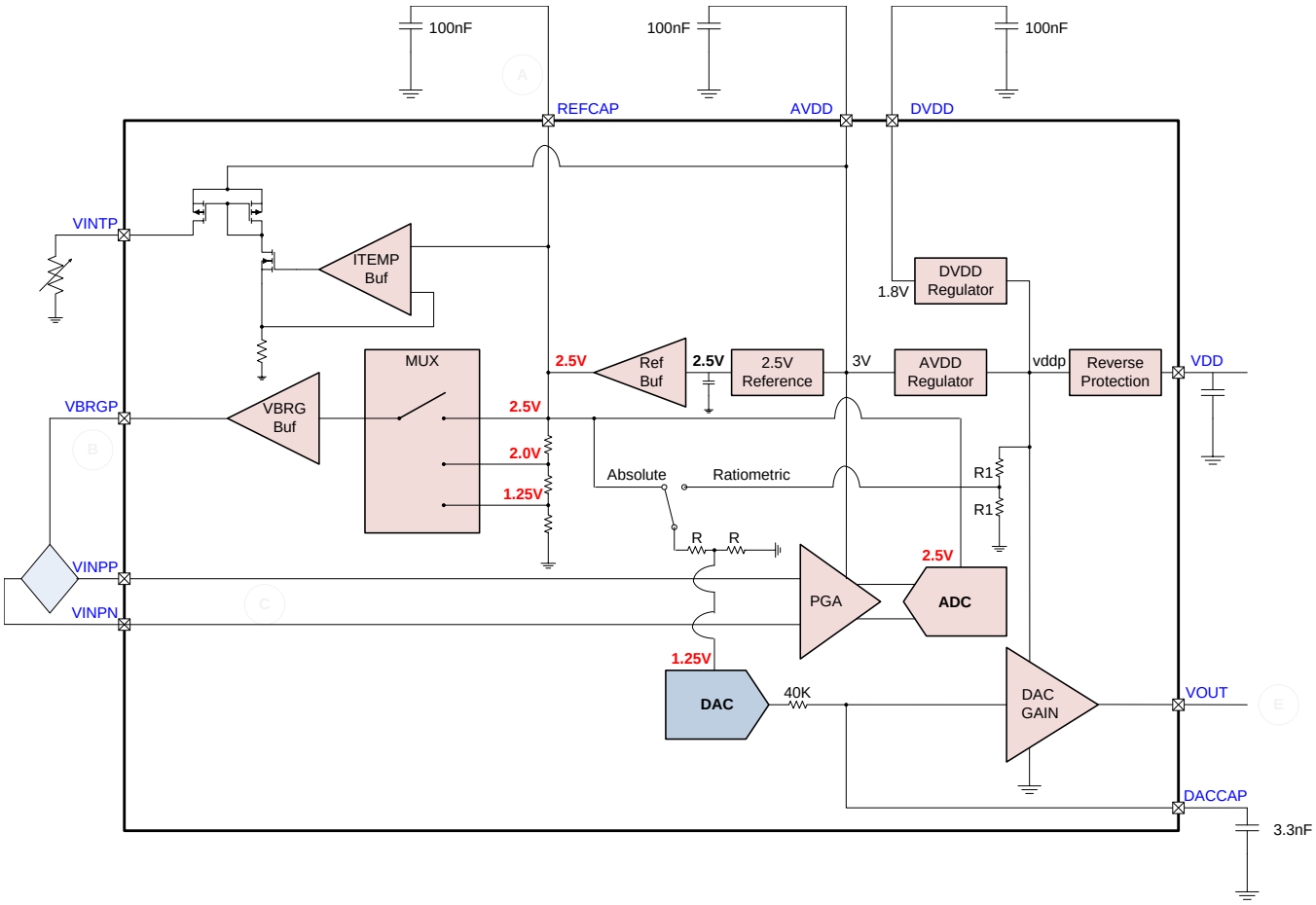


Figure 2. Bridge Supply and P ADC Reference are Ratiometric

6.11 Temperature Sensor Supply

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ITEMP SUPPLY FOR TEMPERATURE SENSOR						
I_{TEMP}	Current supply to temperature sensor	Control bit = 0b000		25		µA
		Control bit = 0b001		50		
		Control bit = 0b010		100		
		Control bit = 0b011		500		
		Control bit = 0b1xx		off		
I_{TEMP}	Current drift over temperature (1)	Control bit = 0b000		37		ppm/°C
		Control bit = 0b001		35		
		Control bit = 0b010		42		
		Control bit = 0b011		35		
C_{TEMP}	Capacitive load				100	nF
	Output impedance			15		MΩ

(1) $$\text{TEMP DRIFT} = \frac{\text{Value at TEMP} - \text{Value at 25°C}}{\text{Value at 25°C} \times \Delta\text{TEMP}} \times 10^6$$

6.12 Internal Temperature Sensor

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted) (1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature range		–40		150	°C
Gain	24-bit ADC		6632.1		LSB/°C
Offset			1710281.3		LSB
Total error without trim	Using gain and offset values mentioned in this table		±6		°C

(1) For higher accuracy, each device must be calibrated using a two point method at 25°C and 125°C. Temperature can be calculated using the following formula, Output code = Offset + Gain × Temperature

6.13 P Gain (Chopper Stabilized)

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain steps (5 bits)	00000, at DC		5		V/V
	00001		5.48		
	00010		5.97		
	00011		6.56		
	00100		7.02		
	00101		8.00		
	00110		9.09		
	00111		10.00		
	01000		10.53		
	01001		11.11		
	01010		12.50		
	01011		13.33		
	01100		14.29		
	01101		16.00		
	01110		17.39		
	01111		18.18		
	10000		19.05		
	10001		20.00		
	10010		22.22		
	10011		25		
	10100		30.77		
	10101		36.36		
	10110		40.00		
	10111		44.44		
	11000		50		
	11001		57.14		
	11010		66.67		
	11011		80		
	11100		100		
	11101		133.33		
	11110		200		
	11111		400		
Gain bandwidth product(1)			10		MHz
Input-referred noise density	f = 0.1 Hz to 2 kHz Total input-referred noise including gain noise, ADC reference noise, ADC thermal noise, and ADC quantization noise at gain = 400 V/V, sampling rate = 128 µs, across temperature		15		nV/√Hz
Input offset voltage			10		µV
Input offset voltage temperature drift			0.06		µV/°C
Gain temperature drift(1)	Gain = 400 V/V		–0.24		ppm/°C
Gain nonlinearity(1)	Gain = 400 V/V		0.16		m%FSO
Total unadjusted error	Includes offset error, gain error and INL across temperature		0.04	0.195	%FSO
Input bias current			5		nA

(1) Specified by design

P Gain (Chopper Stabilized) (continued)

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response (1)	Gain = 400 V/V, <1 kHz			±0.1	%V/V
Common-mode voltage range			Depends on selected gain, bridge supply and sensor span (2)		V
Common-mode rejection ratio	F_{CM}= 50 Hz at Gain = 5 V/V		110		dB
Input impedance		10			MΩ

(2) **Common Mode at P Gain Input and Output** has two constraints:
(a) The single-ended voltage of positive/negative pin at the P Gain input must be between 0.3 and 1.8 V.
(b) The single-ended voltage of positive/negative pin at the P Gain output must be between 0.1 and 2 V.

6.14 P Analog-to-Digital Converter

over operating free-air temperature range at VDD = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sigma delta modulator frequency			1		MHz
ADC voltage input range		–2.5		2.5	V
Number of bits			24		bits
ENOB (1)	VINPP = VINPN, including gain noise, ADC reference noise, ADC thermal noise, and ADC quantization noise, sampling rate = 128 µs, across temperature				
	PGAIN = 5 V/V		15		bits
	PGAIN = 400 V/V		11		bits
ADC 2's complement code for –2.5-V differential input	2's complement		800000_{hex}		
ADC 2's complement code for 0-V differential input			000000_{hex}		
ADC 2's complement code for 2.5-V differential input			$7FFFFF_{hex}$		
Output sample period	Sample period control bit = 0b0		64		µs
	Sample period control bit = 0b1		128		
Output sample interrupt	Sample interrupt control bit = 0b0		1		samples
	Sample interrupt control bit = 0b1		4		

(1) $$ENOB = \frac{SNR - 1.76\ dB}{6.02}$$

6.15 T Gain (Chopper Stabilized)

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain steps (2 bits)	Gain control bits = 0b00 at DC		1.33		V/V
	Gain control bits = 0b01		2.00		
	Gain control bits = 0b10		5.00		
	Gain control bits = 0b11		20.00		
Gain bandwidth product(1)			350		kHz
Input-referred noise density	f = 0.1 Hz to 2 kHz Total Input-referred noise including gain noise, ADC reference noise, ADC thermal noise, and ADC quantization noise at gain = 5 V/V, sampling rate = 128 µs, across temperature		110		nV/√Hz
Input offset voltage			95		µV
Input offset voltage temperature drift			0.4		µV/°C
Gain temperature drift(1)	Gain = 1.33 V/V		0.12		ppm/°C
Gain nonlinearity(1)	Gain = 5 V/V		6.6		m%FSO
Total unadjusted error	Includes offset error, gain error and INL across temperature		0.04	0.195	%FSO
Input bias current			5		nA
Frequency response(1)	Gain = 20 V/V, <100 Hz			0.335	%V/V
Common-mode voltage range			Depends on selected gain and current supply(2)		
Common-mode rejection ratio	F_{CM} = 50 Hz at Gain = 5 V/V		110		dB
Input impedance		1			MΩ

(1) Specified by design
(2) **Common Mode at T Gain Input and Output** has two constraints:
(a) The single-ended voltage of positive/negative pin at the T gain input must be between 5 mV and 1.8 V.
(b) The single-ended voltage of positive/negative pin at the T gain output must be between 0.1 and 2 V.

6.16 T Analog-to-Digital Converter

over operating free-air temperature range at VDD = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sigma delta modulator frequency			1		MHz
ADC voltage input range		–2.5		2.5	V
Number of bits			24		bits
ADC 2's complement code for –2.5-V differential input	2's complement		800000_{hex}		LSB
ADC 2's complement code for 0-V differential input			000000_{hex}		LSB
ADC 2's complement code for 2.5-V differential input			$7FFFFF_{hex}$		LSB
ENOB(1)	VINTP = VINTN, including gain noise, ADC reference noise, ADC thermal noise, and ADC quantization noise at TGAIN = 5 V/V, sampling rate = 128 µs, across temperature		14		bits
Output sample period	Sample period control bit = 0b0		64		µs
	Sample period control bit = 0b1		128		
Output sample interrupt	Sample interrupt control bit = 0b0		1		samples
	Sample interrupt control bit = 0b1		4		

(1) $$ENOB = \frac{SNR - 1.76\ dB}{6.02}$$

6.17 OWI

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Communication baud rate(1)		320		9600	bits per second
OWI_ENH	OWI activation high		5.95			V
OWI_ENL	OWI activation low				5.75	V
OWI_VIH	OWI transceiver Rx threshold for high		4.8			V
OWI_VIL	OWI transceiver Rx threshold for low				4.2	V
OWI_IOH	OWI transceiver Tx threshold for hIgh		500		1379	µA
OWI_IOL	OWI transceiver Tx threshold for low		2		5	µA

(1) **OWI over power line does not work if there is an LDO between supply to the sensor and VDD pin and if the OWI high/low voltages are greater than the regulated voltage**

6.18 SPI

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
V_{IH}	High-level voltage (CSN, SCK, MOSI)	2			V
V_{IL}	Low-level voltage (CSN, SCK, MOSI)			0.8	V
V_{OH}	High-level output voltage	2.4			V
V_{OL}	Low-level output voltage			0.4	V
F_{SCK}	SPI frequency			1	MHz
$C_{L(MISO)}$	Capacitive load for data output (MISO)		10		pF

6.19 I²C Interface

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		0.7 × AVDD			V
V_{IL}	Low-level input voltage				0.3 × AVDD	V
V_{OL}	Low-level output voltage	I_{OL} = 3 mA, I²C RATE configuration bit = 0			0.4	V
V_{OL}	Low-level output voltage	I_{OL} = 20 mA, I²C RATE configuration bit = 1			0.4	V
f_{SCL}	SCL clock frequency				800	KBPS

6.20 PWM Output

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM timer			4		MHz
PWM timer bits			16		bits

6.21 DAC Output

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC reference voltage	Reference bit = 1		1.25		V
	Reference bit = 0 (ratiometric)		0.25 × Vddp		
DAC resolution			14		bits

6.22 DAC Gain

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Buffer gain (see Figure 3)	2X		2		V/V
	4X		4		
	6.67X		6.67		
	10X		10		
Current loop gain			1001		mA/mA
Gain bandwidth product(1)			1		MHz
Offset error	Gain = 4X, ratiometric output measured at VOUT		±13		mV
Gain error	Gain = 4X, ratiometric output measured at VOUT		±0.3		%FSR
Ratiometric error	For ratiometric applications, across temperature			±0.1	%FSO
Total unadjusted error	Current mode output		3.5		%FSO
	Includes offset error, gain error and INL across temperature				
	Voltage mode output		0.15		%FSO
	Includes offset error, gain error and INL across temperature				

(1) Specified by design

DAC Gain (continued)

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ratiometric error due to change in temperature and load current for DAC Code = 8192d (Mid-Code).	Calculate ratiometric error at VDD = 5 V and at DAC codes as follows: 1. Apply DAC Code at 25°C and 0-mA load, and measure voltage at VOUT 2. Change temperature between –40°C to 125°C, and measure voltage at VOUT 3. Change load current between 0 mA to 2.5 mA, and measure voltage at VOUT 4. Ratiometric Error = ((VOUT at TEMPERATURE at LOAD) – (VOUT at 25°C at 0 mA))		3		mV
DAC gain noise	f = 10 Hz to 1 kHz, V_{DD} = 4.5 V, ratiometric mode, gain = 4 V/V, no capacitors for COMP or DACCAP pins, 25°C		10		uVpp
Settling time (first order response)(1)	DAC code 0000h to 1FFFh step. Output is 90% of full scale. R_{LOAD} = 5 kΩ, C_{LOAD} = 500 pF			7	µs
Zero code voltage (Gain = 4X)	DAC code = 0000h, I_{DAC} = –2.5 mA			20	mV
Full code voltage (Gain = 4X)	Output when DAC code is 1FFFh, I_{DAC} = 2.5 mA	4.8			V
Absolute mode voltage half code temperature drift, I_{DAC} = 2.5 mA(2)	Gain = 2X		6	25	ppm/°C
	Gain = 4X		6	26.5	
	Gain = 6.67X		6	28.5	
	Gain = 10X		7	30	
Ratiometric mode voltage half code temperature drift, Gain = 4X(2)	No load		21.5	38	ppm/°C
	I_{DAC} = 1.25 mA		30.5	49.5	
Output current	DAC code = 1FFFh , DAC code = 0000h			±2.5	mA
Short-circuit source current	DAC code = 0000h		27		mA
Short-circuit sink current	DAC code = 1FFFh		27		mA
Max capacitance	Without compensation			100	pF
	With compensation			100	nF

(2) $$\text{TEMP DRIFT} = \frac{\text{Value at TEMP} - \text{Value at 25°C}}{\text{Value at 25°C} \times \Delta\text{TEMP}} \times 10^6$$

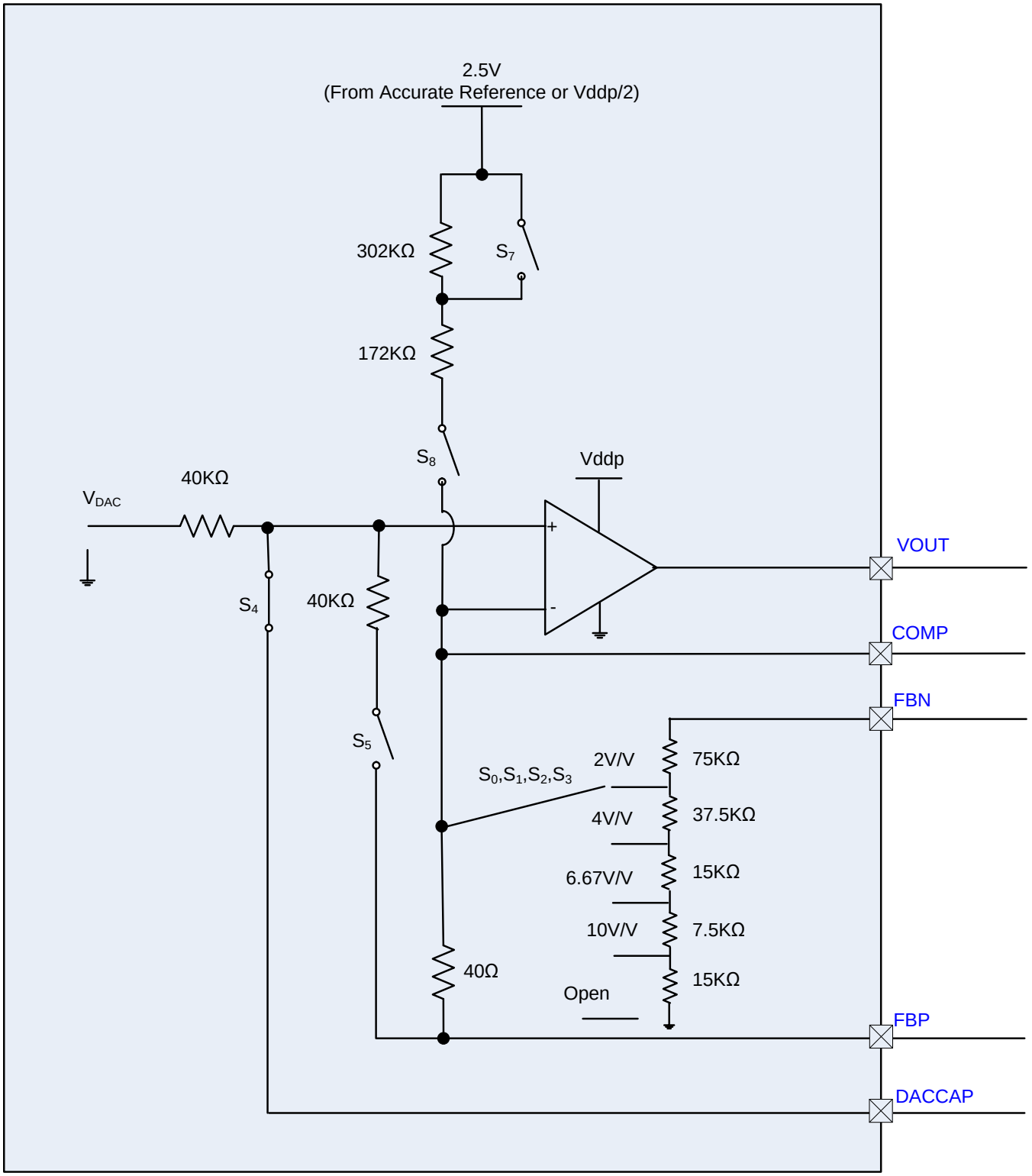


Figure 3. PGA900 Output Buffer

6.23 GPIO, Digital Test In-Test Out, UART TX/RX Buffers

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	R_{LOAD} ≥ 10 kΩ to V_{DD} or to 0 V	2.0			V
V_{IL}	Low-level input voltage	R_{LOAD} ≥ 10 kΩ to V_{DD} or to 0 V			0.8	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_{OH}	High-level output current	V_{OH} = 2.4 V	–2			mA
I_{OL}	Low-level output current	V_{OL} = 0.4 V			2	mA

6.24 Non-Volatile Memory

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OTP	Size			8		KB
	Number of erase/write cycles				1	cycle
	Programming time	1 byte			200	µS
	Data retention		10			years
EEPROM	Size			128		bytes
	Erase/write cycles				1000	cycles
	Programming time	1 8-byte page			8	ms
	Data retention		10			years

6.25 Diagnostics

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Software watchdog timer resolution			2		ms
	Software watchdog timer range			8		bits
OSC_VDD_OV	Oscillator circuit supply overvoltage threshold			3.3		V
OSC_VDD_UV	Oscillator circuit supply undervoltage threshold			2.7		V
VBRG_OV	Resistive bridge sensor supply over voltage threshold			10		%Prog. VBRG
VBRG_UV	Resistive bridge sensor supply under voltage threshold			–10		%Prog. VBRG
AVDD_OV	AVDD OV threshold			3.3		V
AVDD_UV	AVDD UV threshold			2.7		V
DVDD_OV	DVDD OV threshold			2		V
DVDD_UV	DVDD UV threshold			1.53		V
REF_OV	Reference overvoltage threshold			2.75		V

Diagnostics (continued)

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
REF_UV	Reference undervoltage threshold						2.25		V
P_DIAG_PU	P gain input diagnostics pulldown resistor value	VINPP and VINPN each has pulldown resistor					1		MΩ
							2		
							3		
							4		
VINP_OV	P gain input overvoltage threshold value	VINPP and VINPN each has threshold comparator	FAULT_THRS[2]	FAULT_THRS[1]	FAULT_THRS[0]				% VBRDG
		VBRDG = 2.5 V	0	0	0		72.5		
			0	0	1		70		
			0	1	0		65		
		VBRDG = 2 V	0	1	1		90		
			1	0	0		87.5		
			1	0	1		82.5		
		VBRDG = 1.25 V	1	1	0		100		
			1	1	1		95		
VINP_UV	P gain input undervoltage threshold value	VINPP and VINPN each has threshold comparator	FAULT_THRS[2]	FAULT_THRS[1]	FAULT_THRS[0]				% VBRDG
		VBRDG = 2.5 V	0	0	0		7.5		
			0	0	1		10		
			0	1	0		15		
		VBRDG = 2 V	0	1	1		10		
			1	0	0		12.5		
			1	0	1		17.5		
		VBRDG = 1.25 V	1	1	0		17.5		
			1	1	1		22.5		
VINT_OV	T gain input overvoltage	VINTP and VINTN					2.1		V
PGAIN_OV	Output overvoltage (single-ended) threshold for P gain						2.25		V
PGAIN_UV	Output undervoltage (single-ended) threshold for P gain						0.15		V
TGAIN_OV	Output overvoltage (single-ended) threshold for T gain						2.25		V
TGAIN_UV	Output undervoltage (single-ended) threshold for T gain						0.15		V
DAC_LB	DAC loop back voltage gain						0.2		V/V
	DAC loop back driving capability						10		µA
HARNESS_FAULT1	Open wire leakage current 1 - open VDD with pullup on VOUT1						2		µA

Diagnostics (continued)

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HARNESS_FAULT2	Open wire leakage current 2 - open GND with pulldown on VOUT1			20		µA

6.26 M0

over operating free-air temperature range at V_{DD} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
M0 core frequency (including OTP and RAM)	M0 frequency control bit = 0b00		0.5		MHz
	M0 frequency control bit = 0b01		1		
	M0 frequency control bit = 0b10		2		
	M0 frequency control bit = 0b11		4		

6.27 OWI Timing Requirements

	MIN	TYP	MAX	UNIT
Activation signal pulse low time	1 10			ms
Activation signal pulse high time	1 10			ms

6.28 SPI Timing Requirements

		MIN	TYP	MAX	UNIT
t_{CSNSCK}	CSN low to first SCK rising edge	25			ns
t_{SCKCSN}	Last SCK rising edge to CSN rising edge	125			ns
t_{CSND}	CSN disable time	4000			ns
t_{DS}	MOSI setup time	25			ns
t_{DH}	MOSI hold time	25			ns
t_{MOSIS}	MOSI fall/rise time			7	ns
t_{SCKR}	SCK rise time			7	ns
t_{SCKF}	SCK fall time			7	ns
t_{SCKH}	SCK high time	125			ns
t_{SCKL}	SCK low time	125			ns
t_{MISOE}	MISO enable time	15			ns
t_{ACCS}	SCK rising edge to MISO data valid	15			ns
t_{MISOD}	MISO disable time			15	ns
t_{MISOS}	MISO rise/fall time	3		11	ns

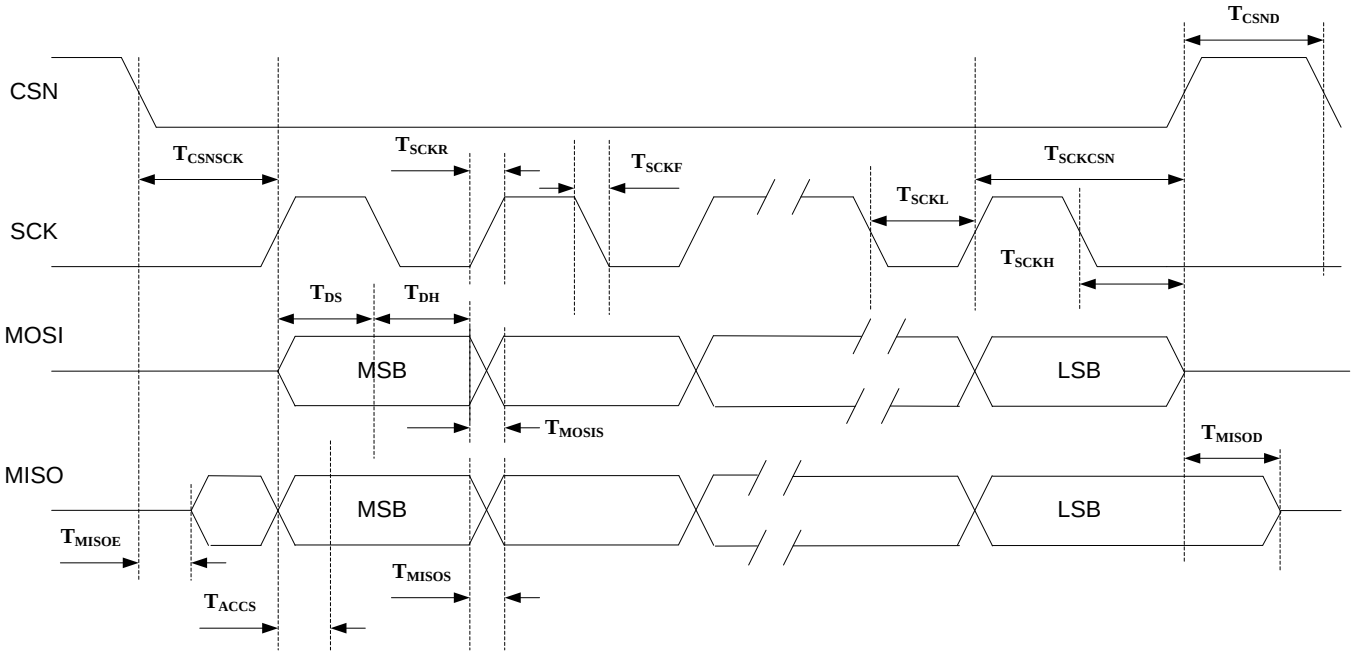


Figure 4. SPI Timing

6.29 I²C Interface Timing Requirements

		MIN	TYP	MAX	UNIT
t_{STASU}	START condition set-up time	500			ns
t_{STAHD}	START condition hold time	500			ns
t_{LOW}	SCL low time	1.25			µs
t_{HIGH}	SCL high time	1.25			µs
t_{RISE}	SCL and SDA rise time			120	ns
t_{FALL}	SCL and SDA fall time			120	ns
t_{DATSU}	Data setup time	500			ns
t_{DATHD}	Data hold time	500			ns
t_{STOSU}	STOP condition set-up time	500			ns

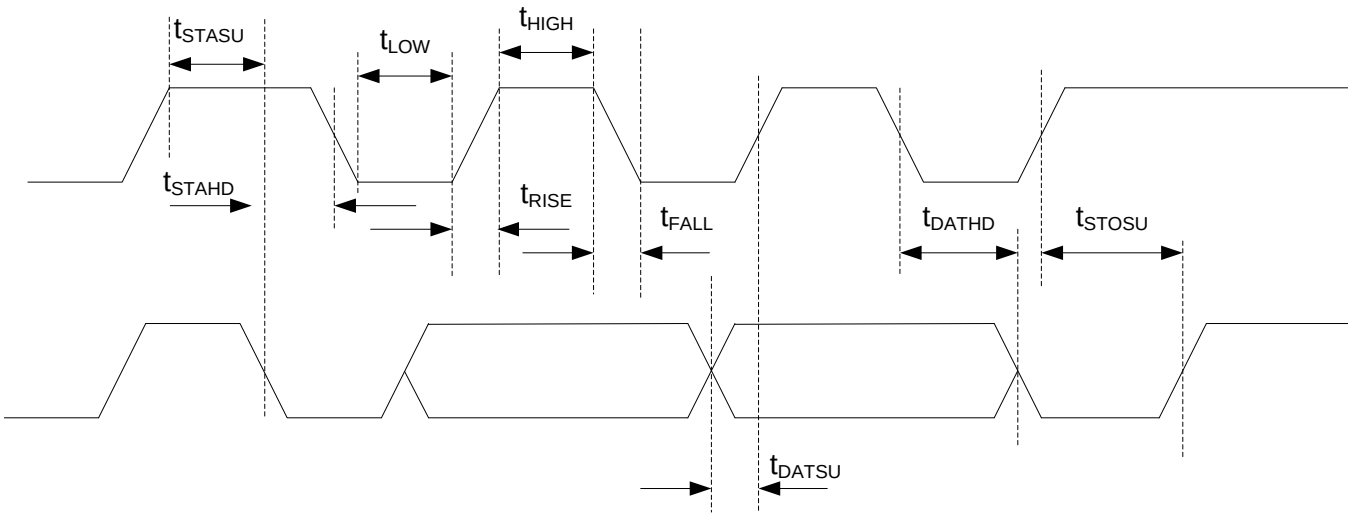


Figure 5. I²C Timing

6.30 Typical Characteristics

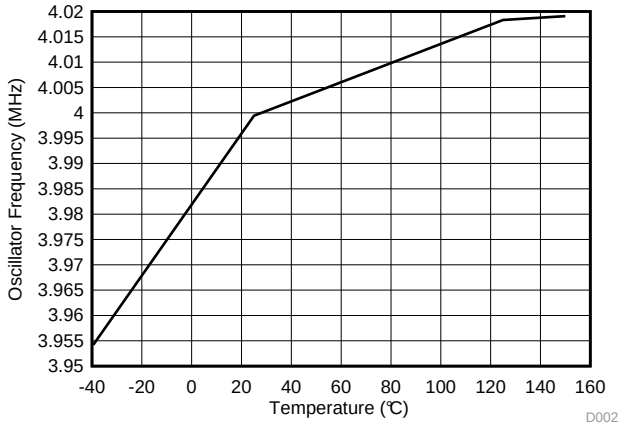


Figure 6. Oscillator Frequency vs Temperature

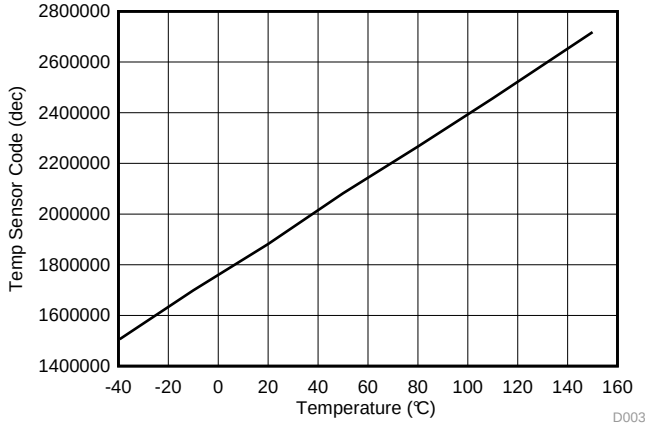


Figure 7. Temperature Sensor Code vs Temperature

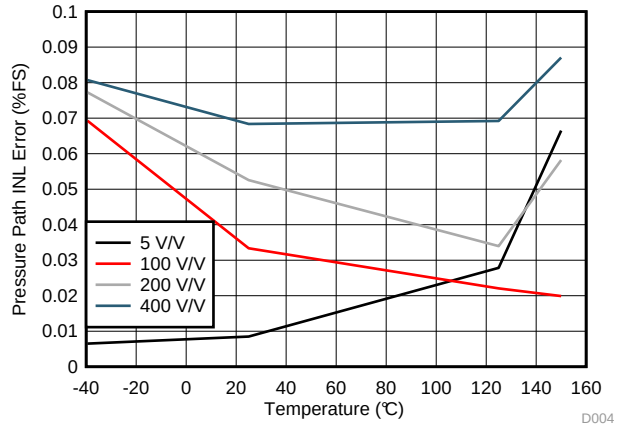


Figure 8. Pressure Path INL Error (Differential) vs Temperature

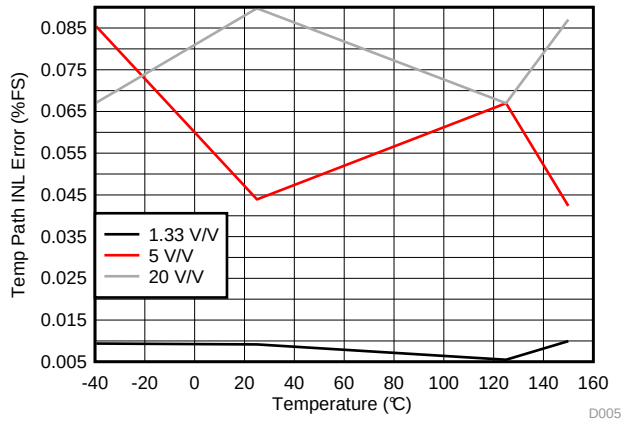


Figure 9. Temperature Path INL Error (Differential) vs Temperature

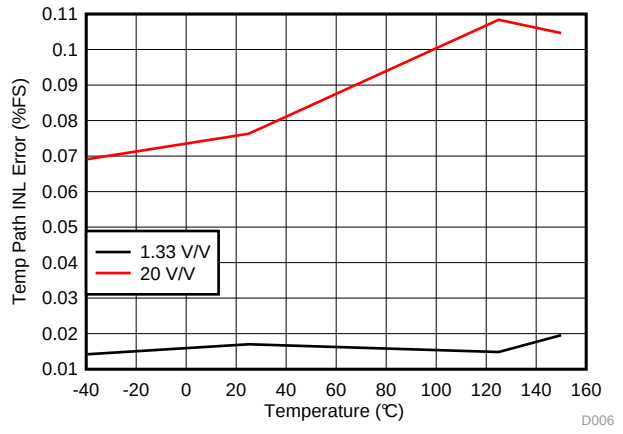


Figure 10. Temperature Path INL Error (Single-Ended) vs Temperature

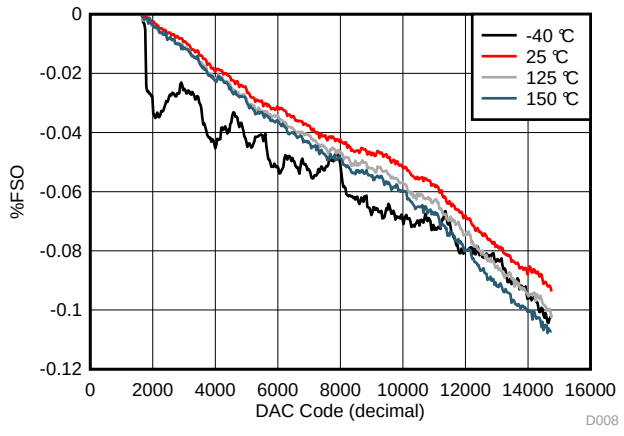


Figure 11. Voltage Mode DAC Output Across Temperature

Typical Characteristics (continued)

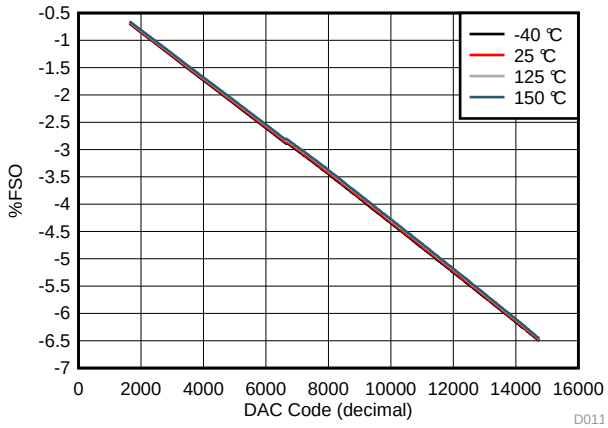
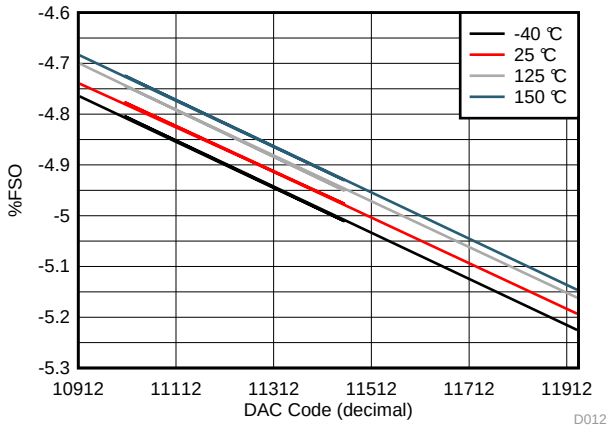
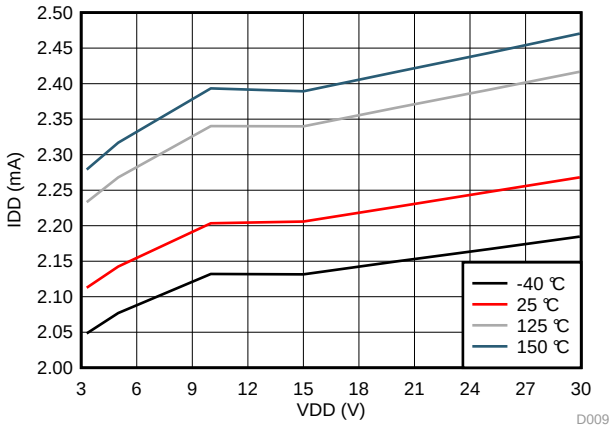


Figure 12. Current Mode DAC Output Across Temperature



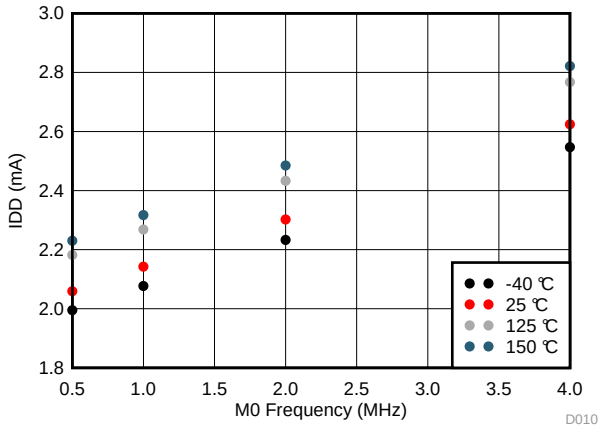
Zoomed in section of Figure 12 to indicate drift across temperature

Figure 13. Current Mode DAC Output Across Temperature



M0 Frequency = 1 MHz

Figure 14. IDD vs VDD Across Temperature



VDD = 5 V, code through OTP

Figure 15. IDD vs Frequency Across Temperature

7 Detailed Description

7.1 Overview

The PGA900 is a high accuracy, extreme low drift, low noise, low power, and versatile signal conditioner device for resistive bridge pressure and temperature-sensing applications. The PGA900 accommodates various sensing element types, such as piezoresistive, ceramic film, and steel membrane. It supports the sensing element spans from 1 mV/V to 135 mV/V. The typical applications supported are pressure sensor transmitter, transducer, liquid level meter, flow meter, strain gauge, weight scale, thermocouple, thermistor, 2-wire resistance thermometer (RTD), and resistive field transmitters. It can also be used in accelerometer and humidity sensor signal conditioning applications.

The PGA900 provides bridge excitation voltages of 2.5 V, 2 V, and 1.25 V, all ratiometric to the ADC reference level. The PGA900 conditions sensing and temperature signals by amplification and digitization through the analog front-end chain, and performs linearization and temperature compensation within an on-chip ARM Cortex M0 processor which is open core and programmable by users. The conditioned signals can be output in analog or digital form. The signal data can also be accessed by multiple digital interfaces, including SPI, I^2C, UART, and the two GPIO ports. The digital interfaces can also be used to configure other function blocks inside the device. The PGA900 has the unique One-Wire Interface (OWI) that supports the communication and configuration through the power supply line. This feature allows to minimize the number of wires necessary.

The PGA900 contains two separated analog-front end (AFE) chains for resistive bridge inputs and temperature sensing inputs. Each AFE chain has its own gain amplifier and a 24-bit ADC with 7.8-KHz and 15.6-KHz selectable output rates. The resistive bridge input AFE chain consists of a programmable gain with 32 steps from 5 V/V to 400 V/V. For the temperature-sensing input AFE chain, the PGA900 provides a current source that can source up to 500 µA for the optional external temperature sensing. This current source can also be used as a constant current bridge excitation. The programmable gain in the temperature-sensing chain has 4 steps from 1.33 V/V to 20 V/V. In addition, the PGA900 integrates an internal temperature sensor which can be configured as the input of the temperature-sensing AFE chain. The digitalized signals after the ADC decimation filters are sent to the M0 processor for linearization and compensation calculation.

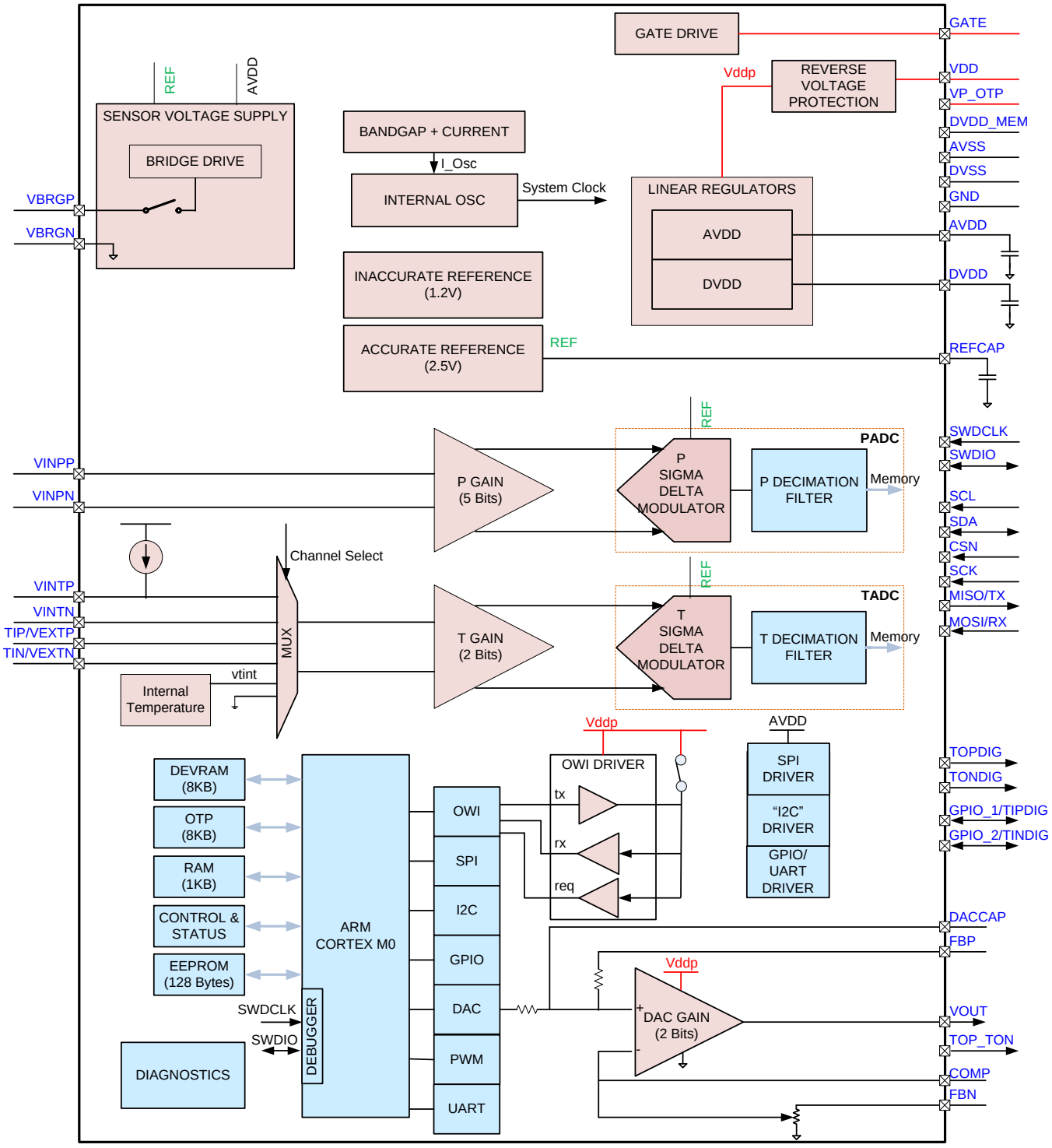
The on-chip ARM Cortex M0 processor is available for programming by the user through an on-chip 8-kb One Time Programmable (OTP) memory. The PGA900 has the option to incorporate a built-in 8-kB develop RAM (DEVRAM) to map OTP memory to minimize the risk in the programming development. A 1-kB data RAM memory can be used for M0 operation. A 128-byte EEPROM is integrated in the PGA900 to store sensor calibration coefficients and PGA900 configuration settings as needed. These memory spaces are accessible by the M0 and the digital interfaces. See the PGA900*PGA900 Software User's Guide* (SLDU013) for more information and examples.

The PGA900 outputs the M0 processed data in either analog or digital forms, or both. The PGA900 has a 14-bit DAC followed by a buffer gain stage of 2 V/V to 10 V/V. It supports industrial standard ratiometric voltage output, absolute voltage output, and 4- to 20-mA current loop. The PGA900 also can send out the data in PWM form or through the SPI, I^2C, OWI and UART digital interfaces. Two GPIO ports are also available.

The diagnostic function monitors the operating condition of the PGA900, including power supplies overvoltage, undervoltage, and open, AFE faults, DAC faults, and a DAC loopback option to check the integrity of the signal chains. The PGA900 also integrates an oscillator and power management. It can operate with 3.3-V to 30-V power supply directly without using external LDO. The PGA900 has a wide ambient temperature operating range from –40°C to +150°C. The package form is 6-mm × 6-mm 36-pin VQFN. Within this small package size, PGA900 has integrated all the functions needed for resistive bridge sensing applications to minimize PCB area and simplify the overall application design.

The evaluation module for the PGA900 is available at www.ti.com/tool/pga900evm. Users can use this EVM to fully evaluate the features of the PGA900. The EVM comes with a socket, allowing users to easily replace the device if needed or for software development. Visit www.ti.com for additional technical documents and reference design information. For any question or support, please contact TI at Pressure Sensing E2E forum http://e2e.ti.com/support/sensor/pressure/.

7.2 Functional Block Diagram



7.3 Feature Description

This section describes individual functional blocks.

7.3.1 Gate Drive for N-Channel Depletion NMOS

The PGA900 includes gate control for an external N-channel depletion MOSFET used as the pass element for a LDO. The gate threshold voltage for the MOSFET must be less than –1.5 V. When the device is used in this mode, VDD is regulated to 3.5 V by PGA900. A capacitor of 1 nF or less is recommended to be added to the GATE pin. Figure 16 shows a block diagram representation of the MOSFET gate drive.

If gate drive mode is not used, then the user must do the following:

1. Connect GATE pin to ground.
2. Disable gate control by setting GATE_CTRL_SD bit in ALPWR register to 1.

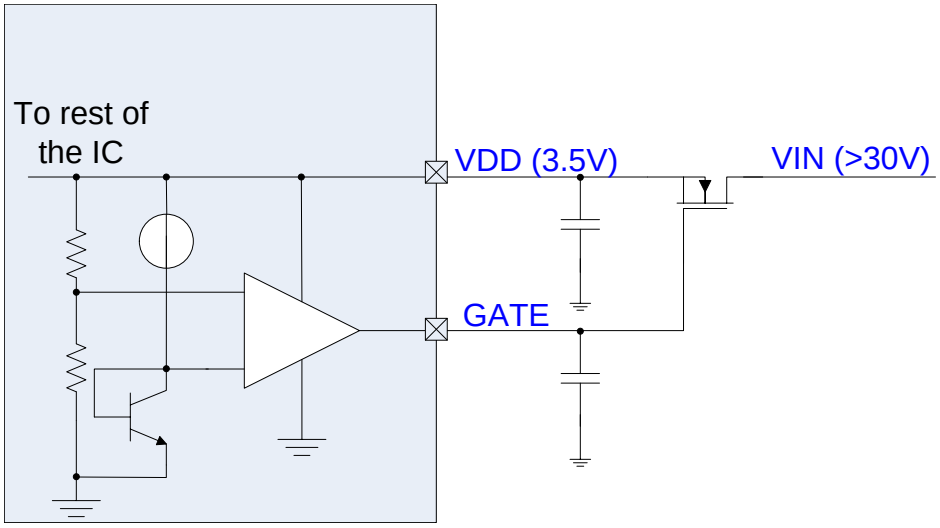


Figure 16. Gate Drive for N-Channel Depletion MOSFET

NOTE

If PGA900 is operated in gate drive mode, then VDD cannot be driven directly from an external voltage source.

Feature Description (continued)

7.3.2 Reverse Voltage Protection Block

The PGA900 includes reverse voltage protection block. This block protects the device from reverse-battery conditions on the external power supply. Figure 17 shows a schematic of the reverse protection block.

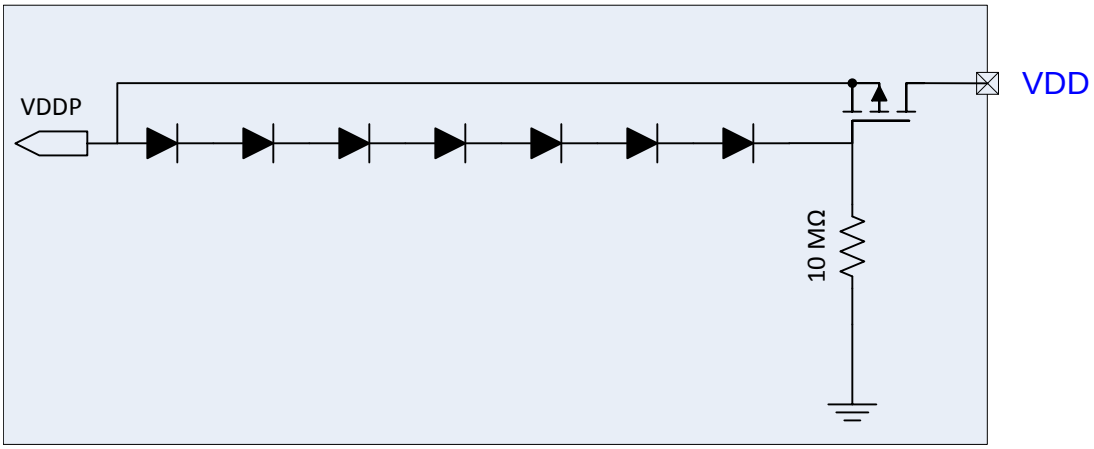


Figure 17. Reverse Voltage Protection Block

7.3.3 Linear Regulators

The PGA900 has two main linear regulators: AVDD regulator and DVDD regulator. The AVDD regulator provides the 3-V voltage source for internal analog circuitry while the DVDD regulator provides the 1.8-V regulated voltage for the digital circuitry. The user needs to connect bypass capacitors of 100 nF each on the AVDD and DVDD pins of the device.

The power-on reset (POR) signal to the digital core are de-asserted when both AVDD and DVDD are in regulation. Figure 18 shows the block diagram representation of the digital POR signal generation and Figure 19 shows the digital POR signal assertion/deassertion timing during VDD ramp up and ramp down. This timing shows that during power up, the digital core and the microprocessor remain in reset state until both AVDD and DVDD are at stable levels.

Feature Description (continued)

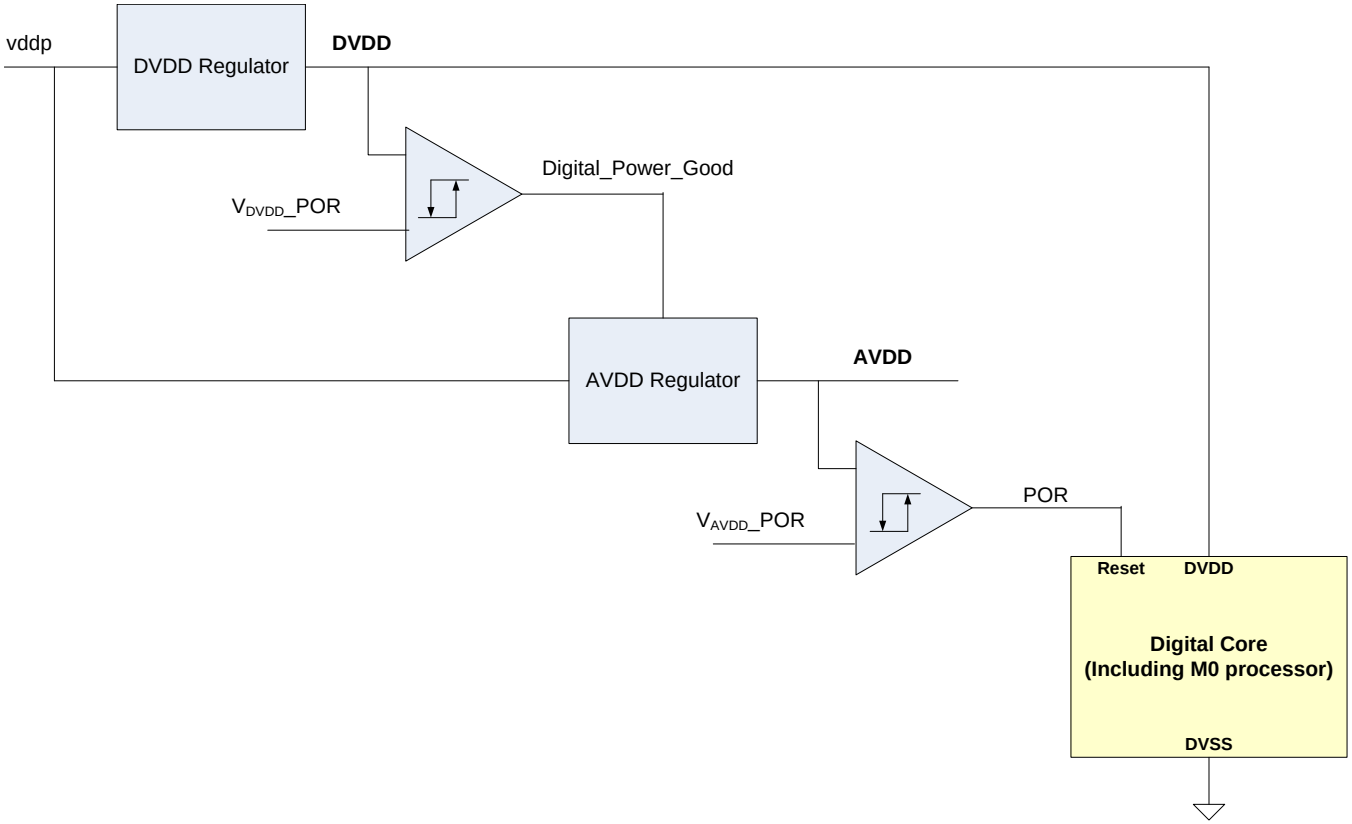


Figure 18. Digital POR Signal Generation

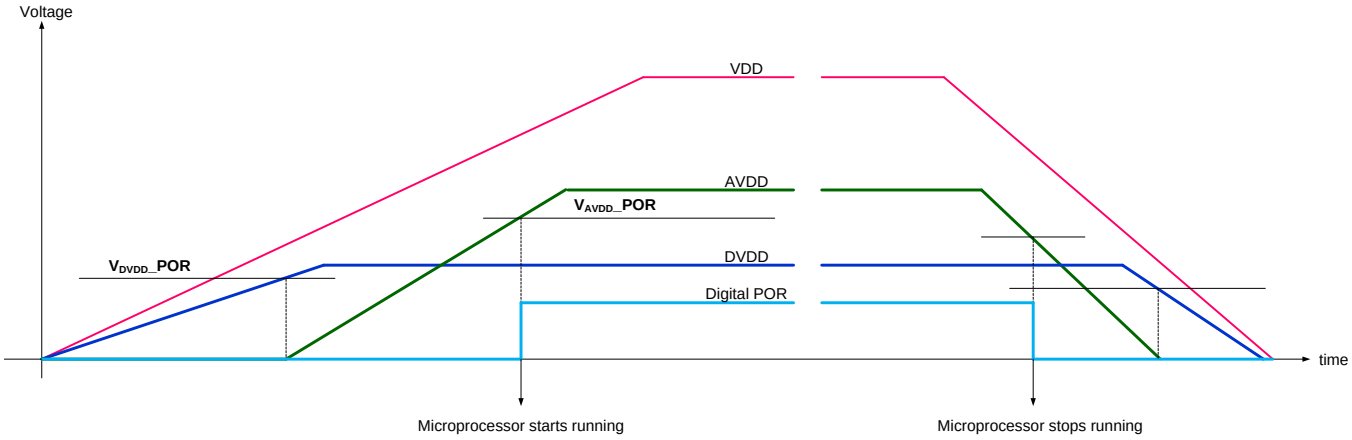


Figure 19. Digital POR Signal Generation

7.3.4 Internal Reference

PGA900 has two internal references. The following sections describe each of these references.

7.3.4.1 Inaccurate Reference

The inaccurate reference is an inaccurate reference used in the gate drive circuit as well as diagnostic thresholds.

Feature Description (continued)

7.3.4.2 Accurate Reference

The accurate reference is used to generate reference voltage for P ADC, T ADC, and the DAC. TI recommends placing a 100-nF capacitor on REFCAP pin to bandwidth limit the reference noise.

The accurate reference buffer can be disabled by setting ADC_EN_VREF bit in ALPWR register to 0. This allows the user to connect an external single-ended reference voltage to REFCAP pin, and thus provide the reference voltage to the ADCs and the DAC. Note that the default power-up state of ADC_EN_VREF is such that the reference buffer is disabled.

NOTE

The accurate reference is valid 50 µs after digital core starts running at power up.

7.3.5 Internal Oscillator

The device includes an internal 4-MHz oscillator. This oscillator provides the internal clock required for the various circuits in PGA900.

7.3.6 VBRGP/VBRGN Supply for Resistive Bridge

The sensor voltage supply block of the PGA900 supplies power to the resistive sense element. The sensor supply in the PGA900 is configurable to 2.5-V, 2-V, and 1.2-V nominal output supply using the VBRDG_CTRL bits in BRDG_CTRL register to accommodate bridge sense elements with different resistance values. This nominal supply is ratiometric to the precise internal accurate reference.

The sensor drive includes a switch. This switch can be used to turn off power to the sensing element.

7.3.7 ITEMP Supply for Temperature Sensor

The ITEMP block in PGA900 supplies programmable current to an external temperature sensor such as PTC. The temperature sensor current source is ratiometric to the accurate reference.

The value of the current can be programmed using the ITEMP_CTRL bits in TEMP_CTRL register.

Feature Description (continued)

7.3.8 Internal Temperature Sensor

PGA900 includes an internal temperature sensor whose voltage output is digitized by the T ADC and made available to the microprocessor. This digitized value is used to implement temperature compensation algorithms in software. Note that the voltage generated by the internal temperature sensor is proportional to the junction temperature.

Figure 20 shows the internal temperature sensor AFE.

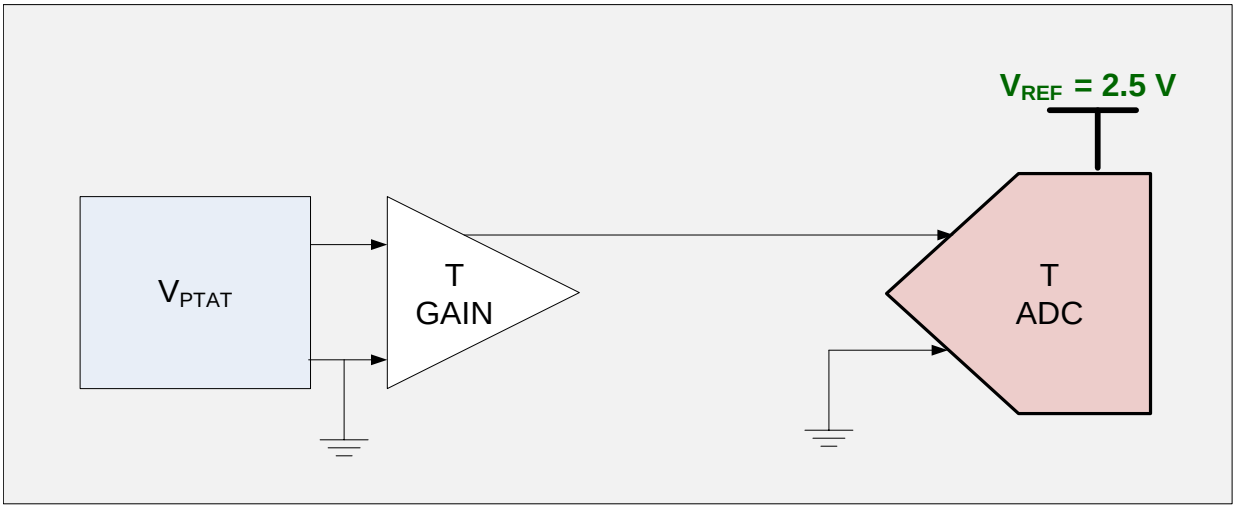


Figure 20. Internal Temperature Sensor AFE

7.3.9 P Gain

The P gain is designed with amplifiers that are precision, low drift, low flicker noise, and chopper-stabilized. The P gain is implemented as an instrument amplifier as shown in Figure 21.

The gain of this stage is adjustable using 5 bits in P_GAIN_SELECT register to accommodate sensing elements with wide-range of signal spans. These signals must meet the requirements below as shown in *P Gain (Chopper Stabilized)*:

1. 0.3 V < VINPP < 1.8 V
2. 0.3 V < VINPN < 1.8 V
3. 0.1 V < VOPP < 2 V
4. 0.1 V < VOPN < 2 V

Based on the above constraints, the Input Common-Mode Voltage, VICM, and the Input Differential Voltage, VIDIFF, can be defined in :

$$VICM = \frac{VINPP + VINPN}{2}$$

$$VIDIFF = VINPP - VINPN$$

In a similar way, the Output Common-Mode Voltage, VOCM, and the Output Differential Voltage, VODIFF, can be defined in :

$$VOCM = \frac{VINPP + VINPN}{2}$$

$$VODIFF = PGAIN \times (VINPP - VINPN)$$

As a result, the single-ended outputs from the PGAIN, VOPP and VOPN, are defined in :

Feature Description (continued)

$$VOPP = \frac{VINPP + VINPN}{2} + PGAIN \times \frac{VINPP - VINPN}{2}$$

$$VOPN = \frac{VINPP + VINPN}{2} - PGAIN \times \frac{VINPP - VINPN}{2}$$

The P gain amplifier can be disconnected from the input pins by setting PGAIN_OPEN in AFE_CFG register to 1. The user must disconnect P gain amplifier pins from input pin in case of overvoltage faults at the input of P gain amplifier to prevent damage to the device.

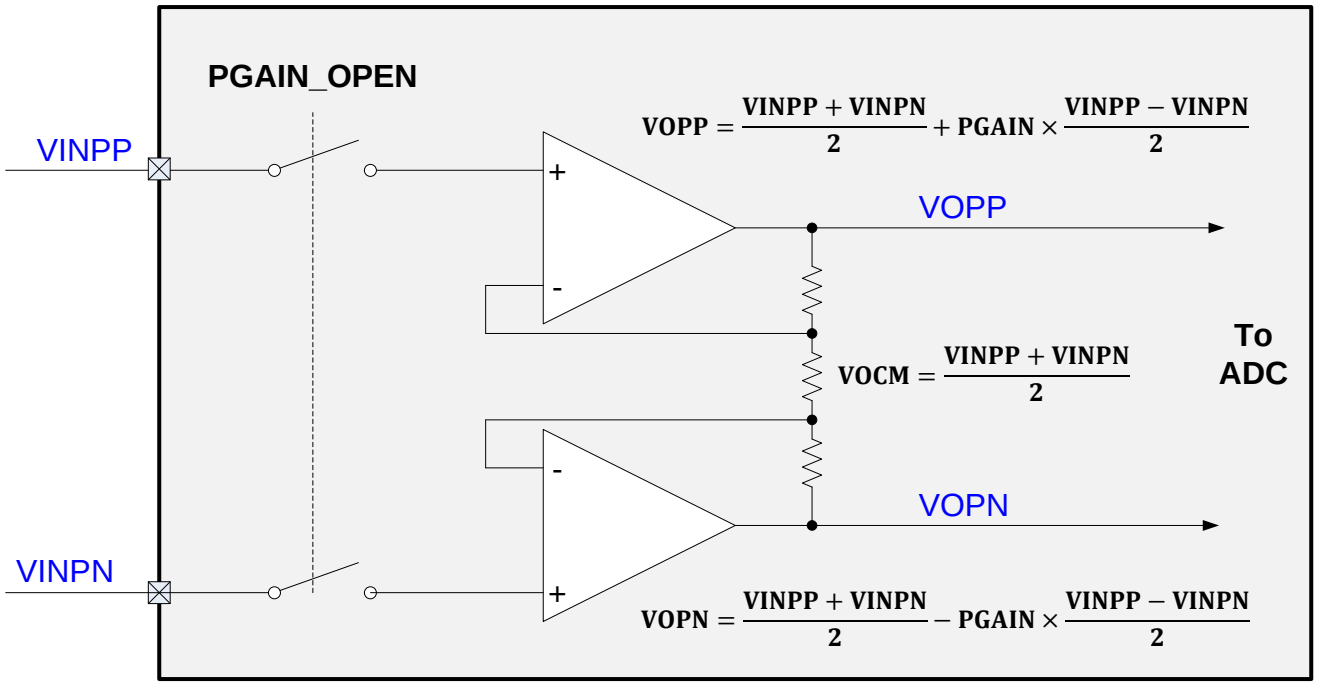


Figure 21. P Gain

7.3.10 P Analog-to-Digital Converter

The P analog-to-digital converter is used to digitize the voltage output of the P gain amplifier. The digitized value is available in PADC_DATA1-3 registers.

7.3.10.1 P Sigma Delta Modulator for P ADC

The sigma-delta modulator for P ADC is a 1-MHz, second-order, 3-bit quantizer sigma-delta modulator. The P sigma-delta modulator can be halted using the ADC_CFG_1 register.

Feature Description (continued)

7.3.10.2 P Decimation Filter for P ADC

The pressure signal path contains a decimation filter that can be configured to have output rate of either 64 or 128 µs.

The output of the decimation filter in the pressure signal path can be configured to be either 16-bit or 24-bit **signed** value. Table 1 shows some example decimation output codes for given differential voltages at the input of the sigma-delta modulator.

Table 1. Input Voltage to Output Counts for O ADC

SIGMA DELTA MODULATOR DIFFERENTIAL INPUT VOLTAGE (V)	16-BIT NOISE-FREE DECIMATOR OUTPUT	24-BIT NOISE-FREE DECIMATOR OUTPUT
–2.5	–32768 (0x8000)	–8388608 (0x800000)
–1.25	–16384 (0xC000)	–4194304 (0xC00000)
0	0 (0x0000)	0 (0x000000)
1.25	16383 (0x3FFF)	4194303 (0x3FFFFF)
2.5	32767 (0x7FFF)	8388607 (0x7FFFFF)

7.3.10.3 P ADC Configuration

The P ADC can be configured using the PADC_CONFIG register as follows:

1. Enable/Disable: The decimation filter can be disabled.
2. 16-bit/24-bit: The decimation filter can be configured to provide either 16-bit or 24-bit output. The decimator output is available in PADC_DATA1-3 registers.
3. Output rate: The decimator output rate can be configured to be either 64 or 128 µs.
4. Interrupt rate: The decimator can be configured to interrupt the microprocessor every sample or every fourth sample.

7.3.10.4 Connecting P GAIN Output to P ADC Input

The P GAIN output can either be connected to the TOP_TON test pin or to the P ADC input as shown in Figure 22. Note that P GAIN output can be connected to P ADC input by setting TEST_MUX_P_EN bit in AMUX_CTRL register to 1.

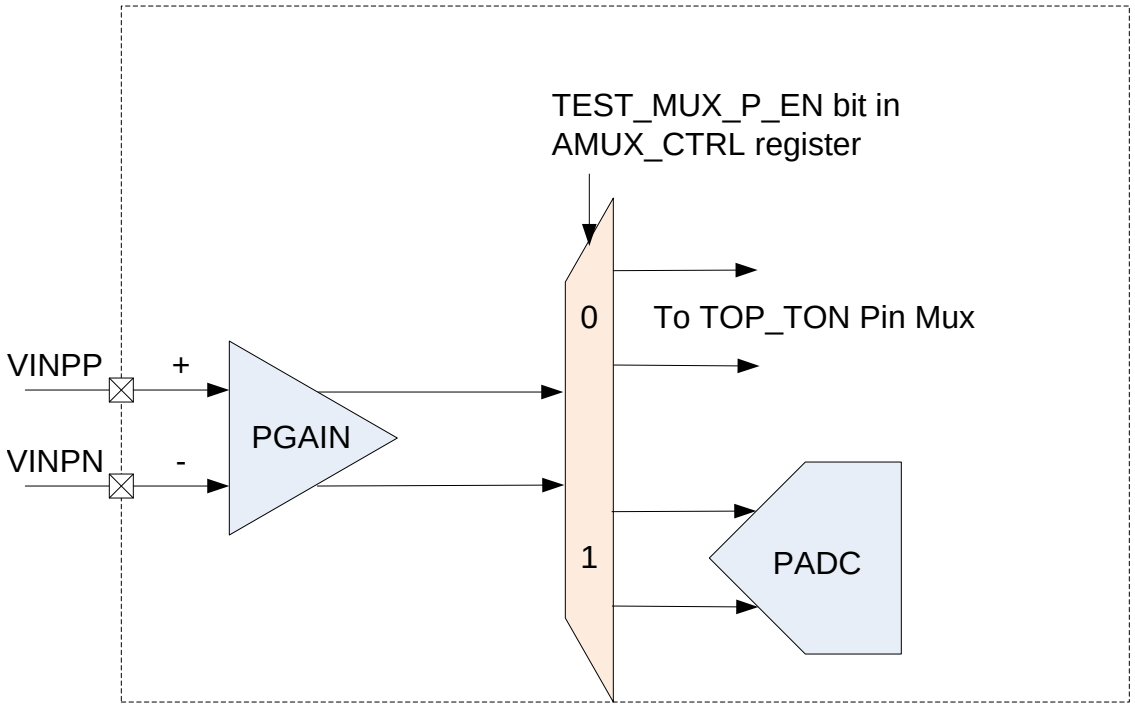


Figure 22. Connecting P GAIN to P ADC

7.3.11 T Gain

The device has the ability to perform temperature compensation through an internal or external temperature sensor. The user can select the source of the temperature measurement with the TEMP_MUX_CTRL bits in TEMP_CTRL register. Note that the device connects to an external temperature sensor through the VINTP/VINTN pins.

The T Gain block is constructed with a low-flicker noise, low offset, chopper-stabilized amplifier. The gain is configurable with 2 bits in the T_GAIN_SELECT register. Figure 23 shows the T gain amplifier topology. The gain of this stage is adjustable using 5 bits in P_GAIN_SELECT register to accommodate sensing elements with wide-range of signal spans.

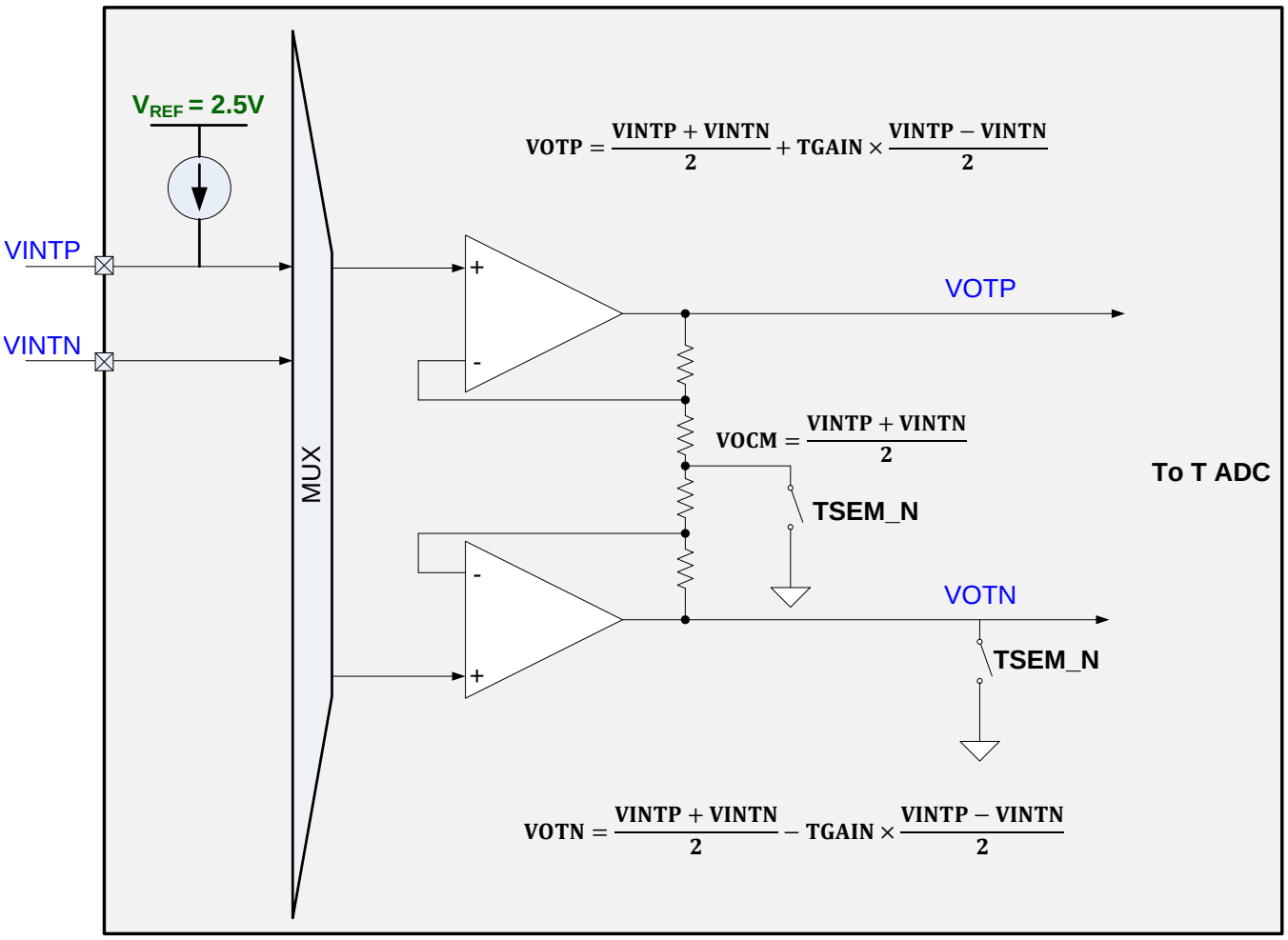


Figure 23. Temperature Sensor AFE

The T Gain amplifier can be configured for single-ended or differential operation using the TSEM_N bit in AMUX_CTRL register. Note that when the T gain amplifier is set up for single-ended operation, the differential voltage converted by T ADC is with respect to ground. Table 2 shows the configuration that the user needs to select for the different temperature sources.

Table 2. T Gain Configuration

TEMPERATURE SOURCE	T GAIN CONFIGURATION
Internal temperature sensor	Single-ended
External temperature sensor with one terminal of sensor connected to ground	Single-ended
External temperature sensor with neither terminal of the sensor connected to ground	Differential

The T Gain amplifier has to be set up for either single-ended or differential configurations depending on the source of signal to the T Gain.

The signal to the T Gain must meet the requirements below as shown in *T Gain (Chopper Stabilized)*:

1. 0.005 V < VINTP < 1.8 V
2. 0.005 V < VINTN < 1.8 V
3. 0.1 V < VOTP < 2 V
4. 0.1 V < VOTN < 2 V

If the signal is differential, based on the above constraints, the Input Common-Mode Voltage, VICM, and the Input Differential Voltage, VIDIFF, can be defined in :

$$VICM = \frac{VINTP + VINTN}{2}$$

$$VIDIFF = VINTP - VINTN$$

In a similar way, the Output Common-Mode Voltage, VOCM, and the Output Differential Voltage, VODIFF, can be defined in :

$$VOCM = \frac{VINTP + VINTN}{2}$$

$$VODIFF = TGAIN \times (VINTP - VINTN)$$

As a result, the single-ended outputs from the TGAIN, VOTP and VOTN, are defined in :

$$VOTP = \frac{VINTP + VINTN}{2} + TGAIN \times \frac{VINTP - VINTN}{2}$$

$$VOTN = \frac{VINTP + VINTN}{2} - TGAIN \times \frac{VINTP - VINTN}{2}$$

If the T Gain amplifier is setup for single-ended configuration, then the signal to the T Gain must still meet the requirements shown in *T Gain (Chopper Stabilized)* but in this case VINTN = GND. The equations for VOTP and VOTN then become :

$$VOTP = 0.1\,V < VINTP \times TGAIN < 2\,V$$

$$VOTN = GND$$

NOTE

When T GAIN is configured to measure internal temperature sensor output, T GAIN must be configured to operated in single-ended mode and must be configured for a gain of 5 V/V.

7.3.12 T Analog-to-Digital Converter

The T analog-to-digital converter digitizes the output of the T gain amplifier. The digitized value is available in TADC_DATA1-3 registers.

7.3.12.1 T Sigma-Delta Modulator for T ADC

The sigma-delta modulator for T ADC is a 1-MHz, second-order, 3-bit quantizer sigma-delta modulator. The T sigma-delta modulator can be halted using the ADC_CFG_1 register.

7.3.12.2 T Decimation Filters for T ADC

The temperature signal path contains a decimation filter that can be configured to have output rate of either 64 or 128 µs.

The output of the decimation filter in the temperature signal path can be configured to be either 16-bit or 24-bit **signed** value. Some example decimation output codes for given differential voltages at the input of the sigma-delta modulator are shown in Table 3.

Table 3. Input Voltage to Output Counts for T ADC

SIGMA DELTA MODULATOR DIFFERENTIAL INPUT VOLTAGE (V)	16-BIT NOISE-FREE DECIMATOR OUTPUT	24-BIT NOISE-FREE DECIMATOR OUTPUT
–2.5	–32768 (0x8000)	–8388608 (0x800000)
–1.25	–16384 (0xC000)	–4194304 (0xC00000)
0	0 (0x0000)	0 (0x000000)
1.25	16383 (0x3FFF)	4194303 (0x3FFFFF)
2.5	32767 (0x7FFF)	8388607 (0x7FFFFF)

The nominal relationship between the device junction temperature and 24-bit T ADC Code for T GAIN = 5 V/V is shown in Equation 1.

$$\text{T ADC Code} = 6632.1 \times \text{TEMP} + 1710281.3, \quad (1)$$

where

- TEMP is temperature in °C

Table 4 shows T ADC output for some example junction temperature values.

Table 4. Internal Temperature Sensor to T ADC Value

INTERNAL TEMPERATURE	24-BIT T ADC NOMINAL VALUE
–40°C	1444997 (0x160C85)
0°C	1710281 (0x1A18C9)
150°C	2705096 (0x2946C8)

7.3.12.2.1 T ADC Configuration

The T ADC can be configured using the TADC_CONFIG register as follows:

1. Enable/disable: The decimation filter can be disabled.
2. 16-bit/24-bit: The decimation filter can be configured to provide either 16-bit output or 24-bit output. The decimator output is available in TADC_DATA1-3 registers
3. Output rate: The decimator output rate can be configured to be either 64 or 128 µs
4. Interrupt rate: The decimator can be configured to interrupt the microprocessor every sample or every fourth sample.

7.3.12.3 Connecting T GAIN Output to T ADC Input

The T GAIN output can either be connected to TOP_TON test pin or can connected to T ADC input as shown in Figure 24. Note that T GAIN output can be connected to T ADC input by setting TEMP_MUX_T_EN bit in AMUX_CTRL register to 1.

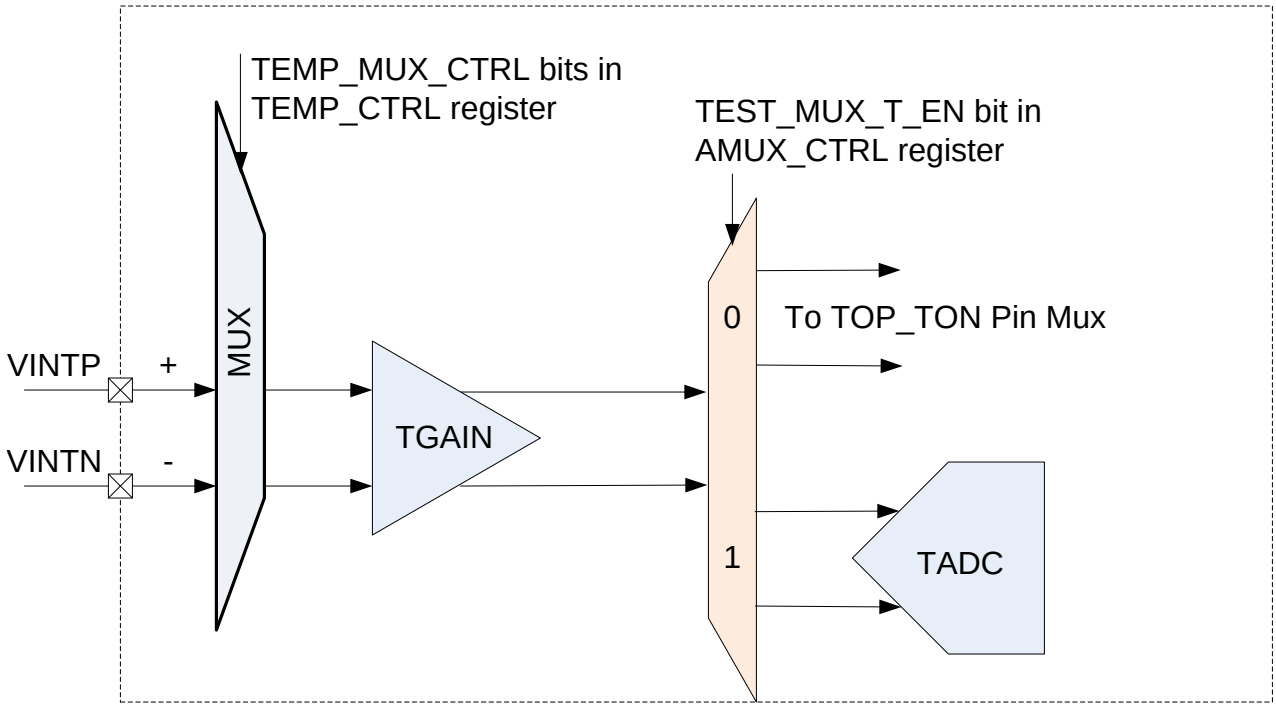


Figure 24. Connecting T GAIN to T ADC

7.3.13 Digital Interfaces

The digital interfaces are used to access (read and write) the internal memory spaces described in *Memory*. Each interface uses different pins for communication. The device has three separate modes of communication:

- OWI
- SPI
- I^2C

The three communication modes supported by PGA900 are collectively referred to as digital interfaces in this document. Each communication mode has its own protocol; however, all three access the same memory elements within the device. For all three communication modes, PGA900 device operates as a slave device.

Figure 25 shows the interface between the microprocessor, memory block, and digital interface.

All three interfaces can access the memories simultaneously. Each interface can be disabled using control bits. It is up to the user to ensure that all three interfaces do not access the device simultaneously. Note that if security lock is enabled in PGA900, then the digital interfaces cannot access any of the internal memories inside PGA900.

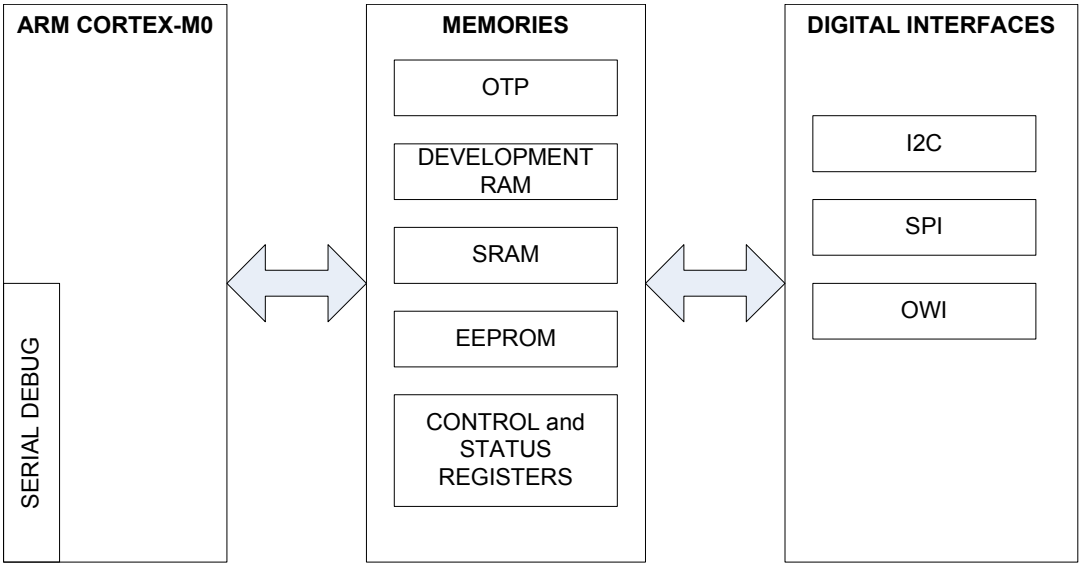


Figure 25. Digital Interface

7.3.13.1 Accessing PGA900 Memories While Microprocessor is Running

If the microprocessor is not in reset state, only the following registers are accessible to the digital interfaces:

- MICRO_INTERFACE_CONTROL
- COM_MCU_TO_DIF (which is read by digital interfaces)
- COM_DIF_TO_MCU (which is written by digital interfaces)
- COM_TX_STATUS

The COM_MCU_TO_DIF and COM_DIF_TO_MCU registers are used to communicate with the PGA900 using the digital interface while the microprocessor is running. These registers are collectively referred to as COMBUF registers. Software must be implemented inside PGA900 so that PGA900 can communicate with the digital interface master using the COMBUF registers.

The digital interface master and PGA900 slave communicate with each other in the following way:

1. The digital interface master writes data to the COM_DIF_TO_MCU register.
2. When COM_DIF_TO_MCU is written by the digital interface master, COMBUF interrupt is generated. Note that the COMBUF interrupt is enabled by writing 1 to COM_RXRDY_INT_EN bit in the COM_RX_INT_ENABLE register.
3. In the COMBUF interrupt service routine, the microprocessor clears the COMBUF interrupt by writing 1 to COM_RX_STATUS register.
4. The software then reads the COM_DIF_TO_MCU register and responds to received data by writing to the COM_MCU_TO_DIF register.
5. The master periodically polls the COM_TX_STATUS register to determine if PGA900 has updated the COM_MCU_TO_DIF register. The master reads the COM_MCU_TO_DIF register for the response from PGA900 if COM_TX_STATUS register has been updated by PGA900.

The PGA900 software can be written such that PGA900 updates the COM_MCU_TO_DIF register periodically without receiving a request from digital interface master. For example, the software in PGA900 can periodically update the processed pressure value. The master can read the processed pressure data periodically.

7.3.13.1.1 COMBUF Register Data Coherency

Both COM_MCU_TO_DIF and COM_DIF_TO_MCU registers are 16-bit registers. All 16-bits can be accessed in one transfer using SPI. However, because OWI and I^2C are 8-bit transfers, these two interfaces require two accesses to receive all 16 bits. PGA900 implements data coherency schemes to maintain data coherency for transfers from PGA900 to the digital interface master and for transfer between digital interface master to PGA900.

7.3.13.1.1.1 Coherency for Transfer From PGA900 to Master

To maintain coherency between the two 8-bit data reads by the master, PGA900 implements an 8-bit shadow register. When OWI or I^2C mater initiates a read of the COM_MCU_TO_DIF register by reading the lower 8 bits first (COM_MCU_TO_DIF_B1 register), PGA900 stores the upper 8 bits (contents of COM_MCU_TO_DIF_B2) to the shadow register. When the master reads the upper 8-bits (by reading COM_MCU_TO_DIF_B2) register, the contents of the shadow register are transmitted by PGA900.

Figure 26 shows data coherency with an example.

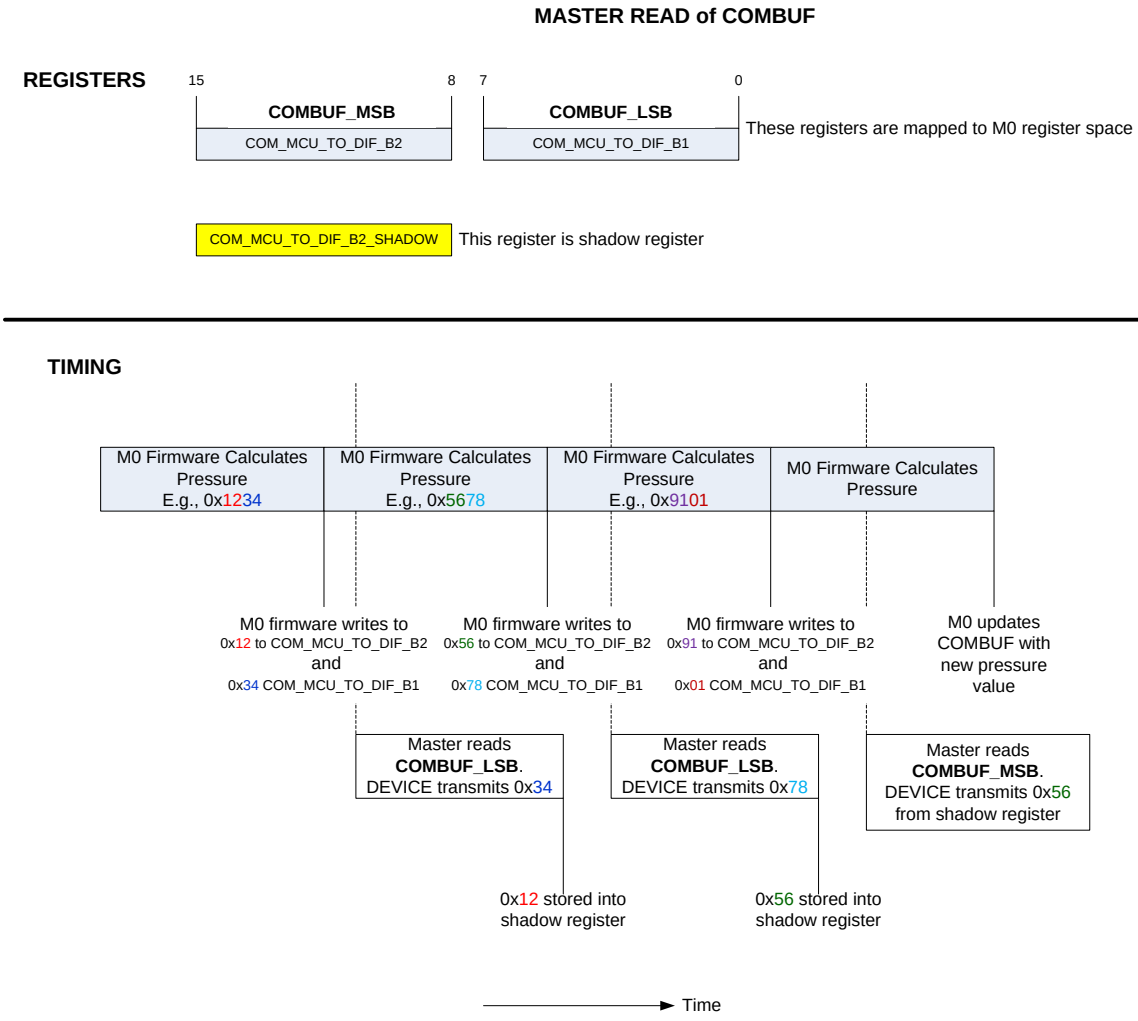


Figure 26. Digital Interface

7.3.13.1.1.2 Coherency for Transfer From Master to PGA900

To maintain coherency between the two 8-bit data reads by PGA900, COMBUF interrupt is generated only when the digital interface master writes to upper 8 bits of the COM_DIF_TO_MCU register (that is, when the master writes to COM_DIF_TO_MCU_B2 register).

Figure 27 shows data coherency with an example.

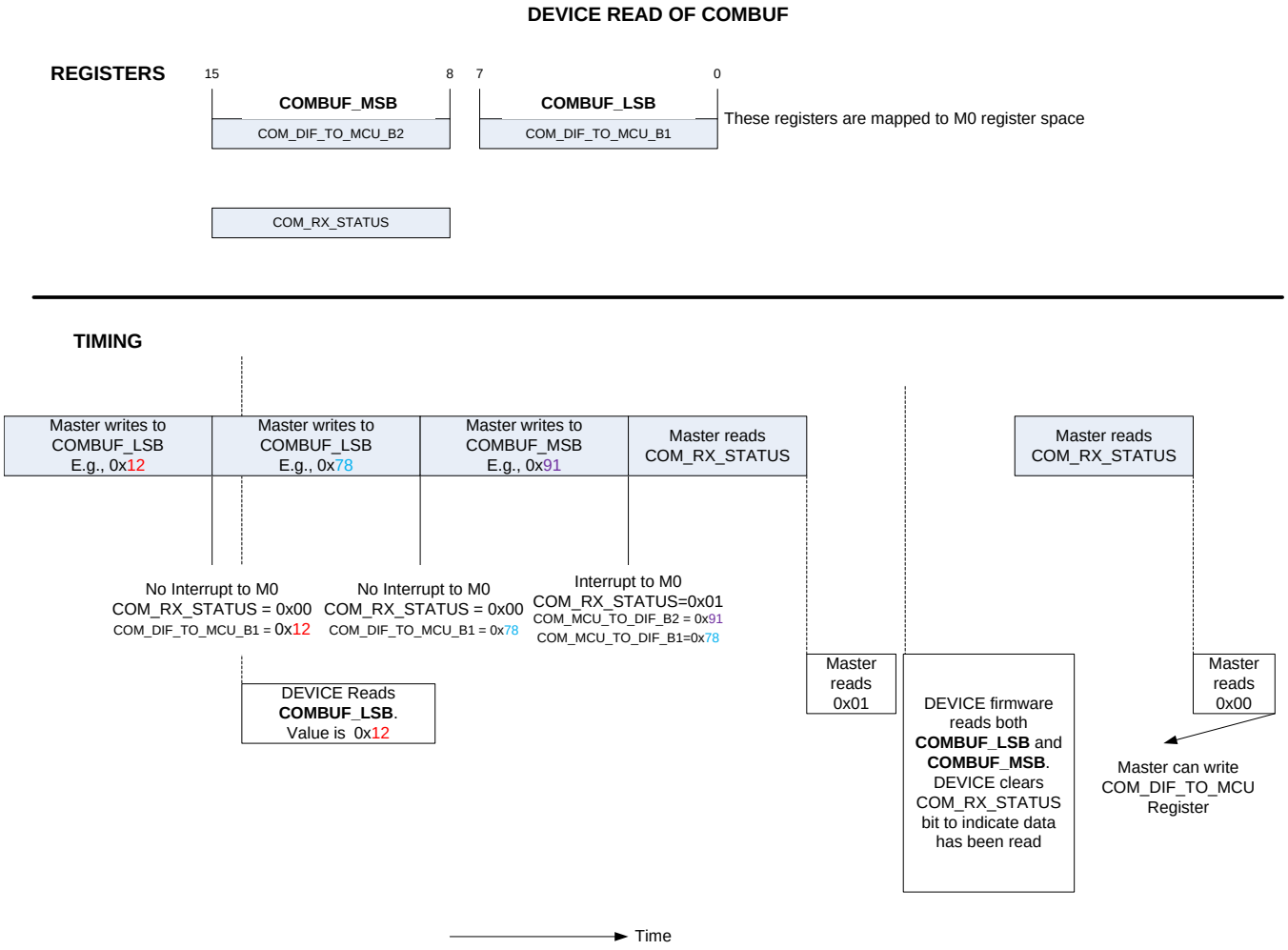


Figure 27. Digital Interface

7.3.13.2 Accessing PGA900 Memories While Microprocessor is in Reset

An alternative method to using the COMBUF registers to communicate with PGA900, is to reset the PGA900 microprocessor using the digital interface and enabling digital interface access. In this mode, all memories inside PGA900 are accessible to the digital interface without the need for software inside PGA900 to support communication.

The microprocessor can be put in reset state by writing 1 to MICRO_RESET bit in MICRO_INTERFACE_CONTROL register using any of the digital interfaces. Access to the digital interface is enabled by writing 1 to IF_SEL bit in MICRO_INTERFACE_CONTROL register.

7.3.13.3 Accessing OTP, DEVRAM, and DATARAM Using 8-Bit Addresses

The size of OTP, DEVRAM, and DATARAM in PGA900 is more than 256 bytes. Each of these memories is 8-bit addressable. To allow the digital interface to access these memories using 8-bit address, these memory spaces are organized as 256-byte pages. Table 5 lists the registers used to specify the page address for each type of memory.

Table 5. Registers Used to Set the Address

MEMORY TYPE	READ ACCESS	WRITE ACCESS
OTP	OTP_PAGE_ADDR	OTP_PROG_ADDR
DEVRAM	DEVRAM_PAGE_ADDR	DEVRAM_PAGE_ADDR
DATARAM	DATARAM_PAGE_ADDR	DATARAM_PAGE_ADDR
EEPROM	N/A	EEPROM_PAGE_ADDRESS

To address a specific memory location, the lower 8 bits of the address have to be provided as part of the digital interface 8-bit address field. The remaining upper bits (5 for OTP and DEVRAM, and 2 for DATARAM) have to be specified in the corresponding page address register. That is, to access a certain memory location, the digital interface has to first set the Page Address bits by writing to the corresponding Page Address register. In summary, the following steps are required to access the memories:

1. Select the page address by writing to the Page Address register using the Digital Interface Write command.
2. For Writing data to memory: Send the 8-bit address (corresponding to the lower 8 bits of the memory address) as part of the Write command.
3. For Reading data from memory: Send the 8-bit address (corresponding to the lower 8 bits of the memory address) as part of the Read command.

Note that for OTP writes, the OTP is 32-bit addressable, not 8-bit addressable. Therefore, OTP_PROG_ADDRESS has to be used to write to the OTP memory. EEPROM can be written 8 bytes at a time. EEPROM_PAGE_ADDRESS register is used to specify the 8 byte page to be written.

7.3.14 OWI

The device includes a OWI digital communication interface. The function of OWI is to enable writes to and reads from all memory locations inside PGA900 available for OWI access.

7.3.14.1 Overview of OWI

The OWI digital communication is a master-slave communication link in which the PGA900 operates as a slave device only. The master device controls when data transmission begins and ends. The slave device does not transmit data back to the master until it is commanded to do so by the master.

The VDD pin of PGA900 is used as OWI, so that when PGA900 is embedded inside of a system module, only two pins are needed (VDD and GND) for communication. The OWI master communicates with PGA900 by modulating the voltage on VDD pin while PGA900 communicates with the master by modulating current on VDD pin. The PGA900 microprocessor has the ability to control the activation and deactivation of the OWI based upon the OWI activation pulse driven on VDD pin.

Figure 28 shows a functional equivalent circuit for the structure of the OWI circuitry.

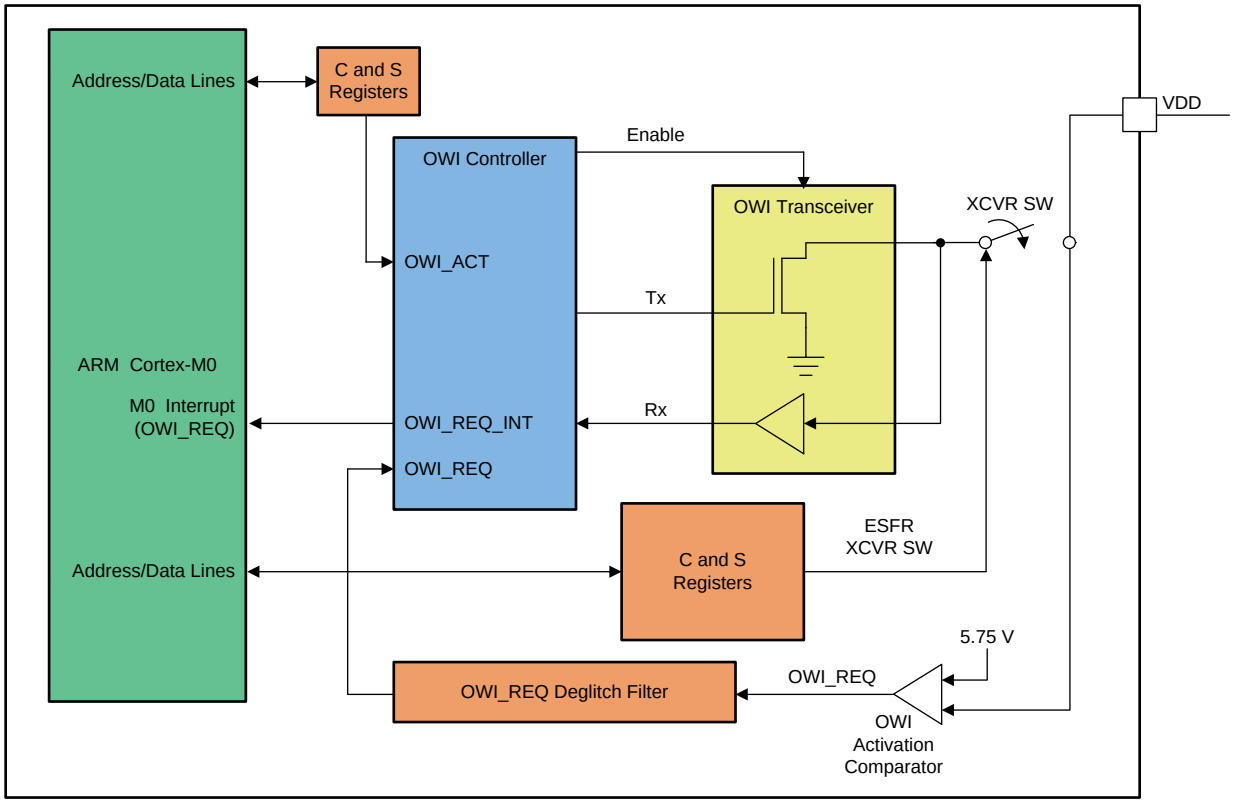


Figure 28. OWI System Components

7.3.14.2 Activating and Deactivating the OWI

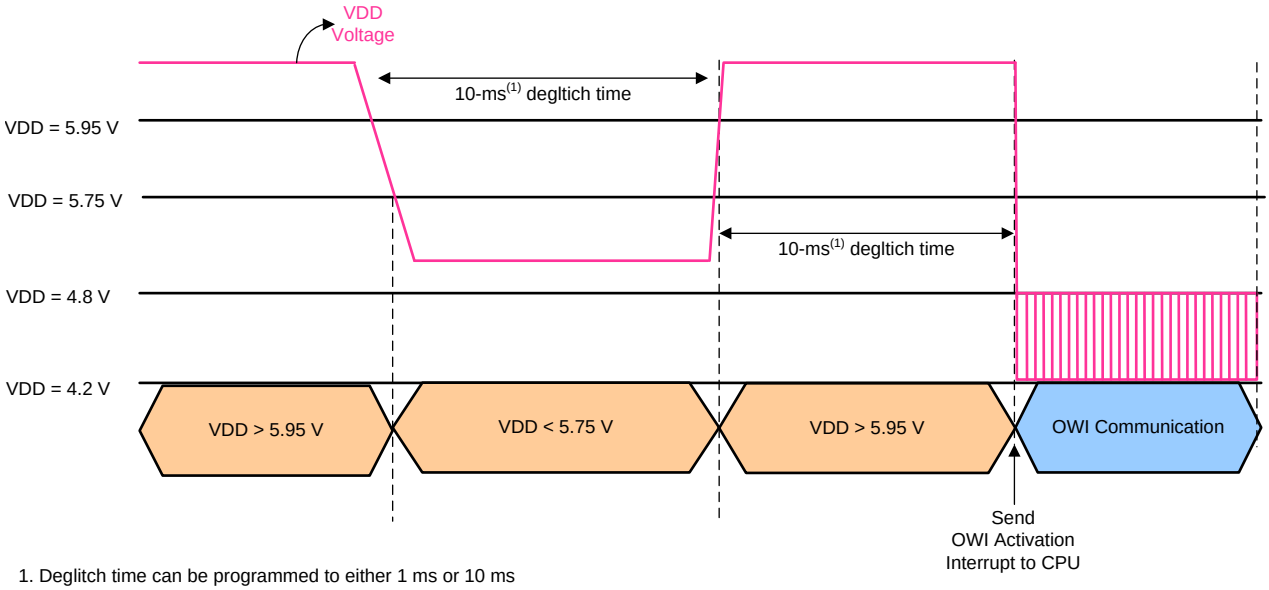
7.3.14.2.1 Activating OWI Communication

The OWI master initiates OWI communication by generating **OWI Activation Pulse** on VDD pin. When PGA900 receives a valid OWI activation pulse, it prepares itself for OWI communication.

To activate OWI communication, follow these following steps in this order:

1. OWI master: Generate an OWI activation pulse on VDD pin. Figure 28 shows the OWI activation pulse that is generated by the master. The OWI pulse is as follows:
   a. Generate a *Low* pulse by driving VDD pin to below 5.75 V. Note that the low level has to be greater than 3.3 V so that PGA900 can continue to operate. The duration of low pulse is determined by OWI_DGL_CNT_SEL bit in DIG_IF_CTRL register. This deglitch time is set by the OWI_DEGLITCH_SEL bit in the Digital Interface Control register (DIG_IF_CTRL), and has the following properties:
      – OWI_DGL_CNT_SEL = 0 → OWI Activation deglitch time = 1 ms
      – OWI_DGL_CNT_SEL = 1 → OWI Activation deglitch time = 10 ms
      – The default value for OWI_DGL_CNT_SEL bit is 0, which corresponds to deglitch time of 1 ms.
   b. Generate a *High* pulse by driving VDD to greater than 5.75 V. The duration of the high pulse is determined by OWI_DGL_CNT_SEL bit in DIG_IF_CTRL register.
2. PGA900: When PGA900 receives a valid OWI activation sequence on VDD pin, the microprocessor receives the OWI activation interrupt. Note that the OWI activation interrupt is enabled by writing 1 to OWI_INT_EN bit in the OW_INTERRUPT_EN register. The OWI activation interrupt service routine has to implement the following steps to enable OWI communication:
   a. Clear the OWI Activation Interrupt by writing 1 to OWI_INT_RW bit in OWI_INTERRUPT register.

b. Enable OWI by writing 1 to OWI_EN bit in DIG_IF_CTRL register.
c. Connect OWI transceiver to VDD pin by writing 1 to the OWI_XCR_EN bit in DIG_IF_CTRL register.
d. If the OWI master communicates to PGA900 with the microprocessor in reset, reset microprocessor by writing 1 to MICRO_RESET bit in MICRO_INTERFACE_CONTROL register and enable digital interface by writing 1 to IF_SEL bit in the MICRO_INTERFACE_CONTROL. If OWI master communicates with PGA900 while microprocessor is running, then the COMBUF registers are used for communication.



1. Deglitch time can be programmed to either 1 ms or 10 ms

A. Deglitch time programmed to 10 ms.

Figure 29. OWI Activation Using Overvoltage Drive

7.3.14.2.2 Deactivating OWI Communication

To deactivate OWI communication and restart the microprocessor inside PGA900 (if it was in reset), the microprocessor reset must be de-asserted by writing 0 to MICRO_RESET bit in MICRO_INTERFACE_CONTROL register.

7.3.14.3 OWI Protocol

7.3.14.3.1 OWI Frame Structure

7.3.14.3.1.1 Standard Field Structure

Data is transmitted on the OWI in byte-sized packets. The first bit of the OWI field is the start bit. The next 8 bits of the field are data bits to be processed by the OWI control logic. The final bit in the OWI field is the stop bit. A group of fields make up a transmission frame. A transmission frame is composed of the fields necessary to complete one transmission operation on the OWI. Figure 30 shows the standard field structure for a one-wire field.

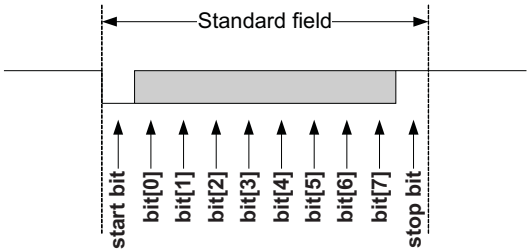


Figure 30. Standard OWI Field

7.3.14.3.1.2 Frame Structure

A complete one-wire data transmission operation is done in a frame with the structure shown in Figure 31.

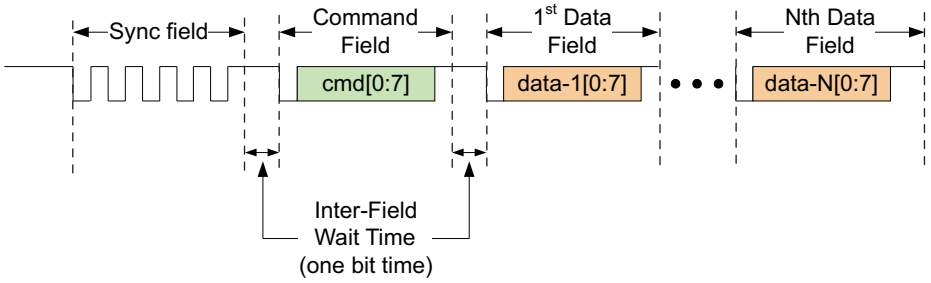


Figure 31. OWI Transmission Frame, N = 1 to 8

Each transmission frame must have a Synchronization field and command field followed by 0 to 8 data fields. The sync field and command fields are always transmitted by the master device. The data field or fields may be transmitted either by the master or the slave depending on the command given in the command field. It is the command field which determines direction of travel of the data fields (master-to-slave or slave-to-master). The number of data fields transmitted is also determined by the command in the command field. The inter-field wait time is optional and may be necessary for the slave or master to process data that has been received.

If OWI remains idle in either logic 0 or 1 state, for more than 15 ms, then the PGA900 communication resets and expects to receive a sync field as the next data transmission from the master.

7.3.14.3.1.3 SYNC Field

The SYNC field is the first field in every frame that is transmitted by the master. The SYNC field is used by the slave device to compute the bit width transmitted by the master. This bit width is used to accurately receive all subsequent fields transmitted by the master. The format of the SYNC field is shown in Figure 32.

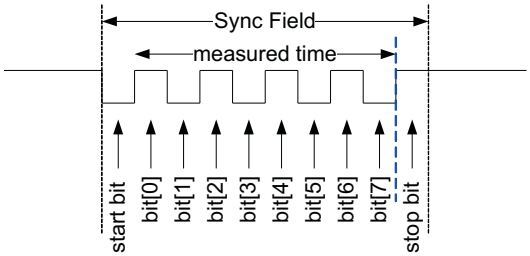


Figure 32. OWI SYNC Field

NOTE

Consecutive SYNC field bits are measured and compared to determine if a valid SYNC field is being transmitted to the PGA900. If the difference in bit widths of any two consecutive SYNC field bits is greater than ±19%, then PGA900 ignores the rest of the OWI frame; that is, the PGA900 does not respond to the OWI message.

7.3.14.3.1.4 Command Field

The command field is the second field in every frame sent by the master. The command field contains instructions about what to do with and where to send the data that is transmitted to the slave. The command field can also instruct the slave to send data back to the master during a Read operation. The number of data fields to be transmitted is also determined by the command in the command field. Figure 33 shows the format of the command field.

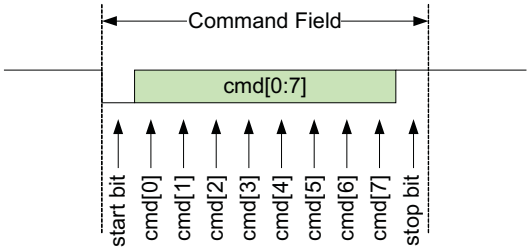


Figure 33. OWI Command Field

7.3.14.3.1.5 Data Fields

After the master has transmitted the command field in the transmission frame, 0 or more data fields are transmitted to the slave (Write operation) or to the master (Read operation). The Data fields can be raw EEPROM data or address locations in which to store data. The format of the data is determined by the command in the command field. Figure 34 shows the typical format of a data field.

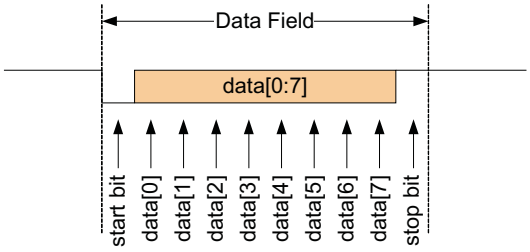


Figure 34. OWI Data Field

7.3.14.3.2 OWI Commands

The following is the list of five OWI commands supported by PGA900:

- OWI Write
- OWI Read Initialization
- OWI Read Response
- OWI Burst Write of EEPROM Cache
- OWI Burst Read from EEPROM Cache

7.3.14.3.2.1 OWI Write Command

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	Basic write command	**0**	P2	P1	P0	0	0	0	1
Data field 1	Destination address	A7	A6	A5	A4	A3	A2	A1	A0
Data field 2	Data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0

The P2, P1, P0 bits in the command field determine the memory page that is being accessed by the OWI. Table 6 shows the memory page decode.

Table 6. OWI Memory Page Decode

P2	P1	P0	MEMORY PAGE
0	0	0	Test registers
0	0	1	Data RAM
0	1	0	Control and Status registers, DI_PAGE_ADDRESS = 0x02
0	1	1	Development RAM

Table 6. OWI Memory Page Decode (continued)

P2	P1	P0	MEMORY PAGE
1	0	0	OTP
1	0	1	EEPROM cache/cells
1	1	0	Reserved
1	1	1	Control and Status registers, DI_PAGE_ADDRESS = 0x07

7.3.14.3.2.2 OWI Read Initialization Command

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	Read Init command	**0**	P2	P1	P0	0	0	1	0
Data field 1	Fetch address	A7	A6	A5	A4	A3	A2	A1	A0

The P2, P1, P0 bits in the command field determine the memory page that is being accessed by the OWI. The memory page decode is shown in Table 6.

7.3.14.3.2.3 OWI Read Response Command

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	Read response command	**0**	1	1	1	0	0	1	1
Data field 1	Data retrieved (OWI drives data out)	D7	D6	D5	D4	D3	D2	D1	D0

The P2, P1, P0 bits in the command field determine the memory page that is being accessed by the OWI. Table 6 shows the memory page decode.

7.3.14.3.2.4 OWI Burst Write Command (EEPROM Cache Access)

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	EE_CACHE write command cache bytes (0 to 7)	**1**	1	0	1	0	0	0	0
Data field 1	First data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 2	Second data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 3	Third data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 4	Fourth data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 5	Fifth data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 6	Sixth data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 7	Seventh data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 8	Eighth data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0

7.3.14.3.2.5 OWI Burst Read Command (EEPROM Cache Access)

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	Burst read response (8-bytes)	**1**	1	0	1	0	0	1	1
Data field 1	First data byte retrieved EE cache byte 0	D7	D6	D5	D4	D3	D2	D1	D0
Data field 2	Second data byte retrieved EE cache byte 1	D7	D6	D5	D4	D3	D2	D1	D0
Data field 3	Third data byte retrieved EE cache byte 2	D7	D6	D5	D4	D3	D2	D1	D0

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Data field 4	Fourth data byte retrieved EE cache byte 3	D7	D6	D5	D4	D3	D2	D1	D0
Data field 5	Fifth data byte retrieved EE cache byte 4	D7	D6	D5	D4	D3	D2	D1	D0
Data field 6	Sixth data byte retrieved EE cache byte 5	D7	D6	D5	D4	D3	D2	D1	D0
Data field 7	Seventh data byte retrieved EE cache byte 6	D7	D6	D5	D4	D3	D2	D1	D0
Data field 8	Eighth data byte retrieved EE cache byte 7	D7	D6	D5	D4	D3	D2	D1	D0

7.3.14.3.3 OWI Operations

7.3.14.3.3.1 Write Operation

The write operation on the OWI is fairly straightforward. The command field specifies the write operation, where the subsequent data bytes are to be stored in the slave, and how many data fields are going to be sent. Additional command instructions can be sent in the first few data fields if necessary. Figure 35 shows the write operation.

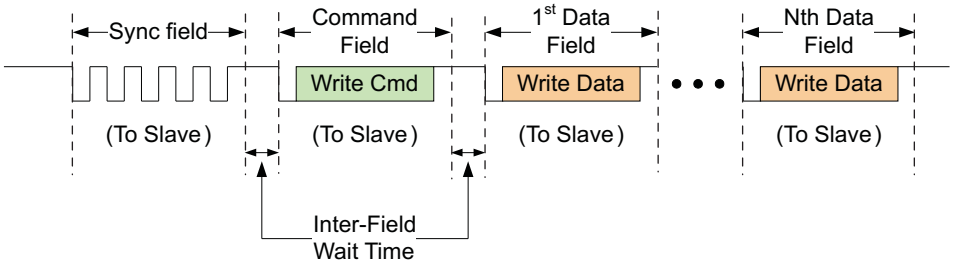


Figure 35. Write Operation, N = 1 to 8

7.3.14.3.3.2 Read Operation

The read operation requires two consecutive transmission frames to move data from the slave to the master. The first frame is the Read Initialization frame. It tells the slave to retrieve data from a particular location within the slave device and prepare to send it over the OWI. The data location may be specified in the command field or may require additional data fields for complete data location specification. The data is not sent until the master commands it to be sent in the subsequent frame called the Read Response frame. During the Read Response frame, the data direction changes from master → slave to slave → master right after the read response command field is sent. Enough time exists between the command field and data field to allow the signal drivers time to change direction. This wait time is 20 µs and the timer for this wait time is located on the slave device. After this wait time is complete, the slave transmits the requested data. The master device is expected to have switched its signal drivers and is ready to receive data. The Read frames are shown in Figure 36.

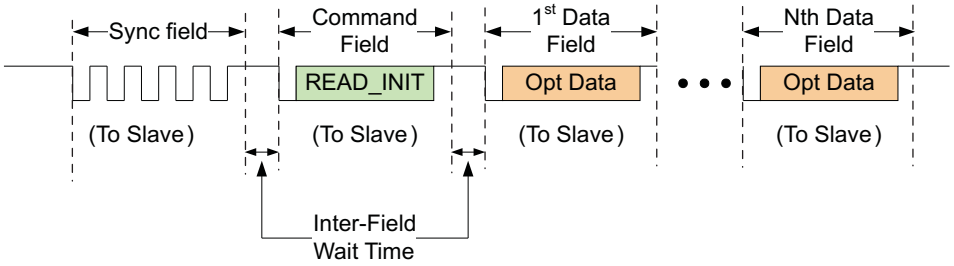


Figure 36. Read Initialization Frame, N = 1 to 8

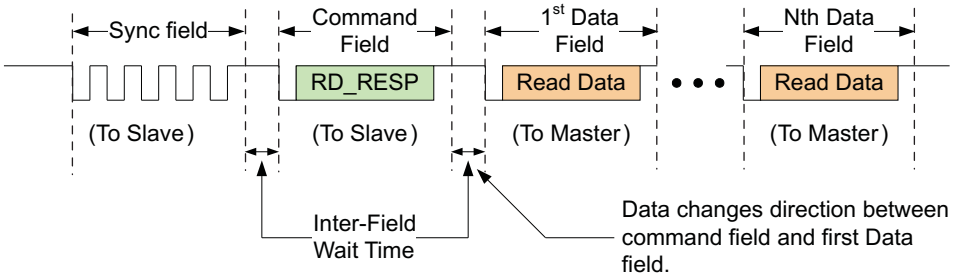


Figure 37. Read Response Frame, N = 1 to 8

7.3.14.3.3.3 EEPROM Burst Write

The EEPROM burst write is used to write 8 bytes of data to the EEPROM cache using one OWI frame. This allows fast programming of EEPROM in the manufacturing line. Note that the EEPROM page must be selected before transferring the contents of the EEPROM memory cells to the EEPROM cache.

7.3.14.3.3.4 EEPROM Burst Read

The EEPROM burst read is used to read 8 bytes of data from the EEPROM cache using one OWI frame. The Burst Read command is used for fast read the EEPROM cache contents in the manufacturing line. The read process is used to verify the writes to the EEPROM cache.

7.3.14.4 OWI Communication Error Status

PGA900 detects errors in OWI communication. OWI_ERROR_STATUS_LO and OWI_ERROR_STATUS_HI registers contain OWI communication error bits. The communication errors detected include

- Out of range communication baud rate
- Invalid SYNC field
- Invalid STOP bits in command and data
- Invalid OWI command

7.3.15 SPI

The device includes a SPI digital communication interface. The main function of the SPI is to enable writes to and reads from all addresses available for SPI access.

7.3.15.1 Overview of SPI

SPI is a synchronous, serial, master-slave, communication standard that requires the following four pins:

- MOSI: SPI master out slave in, input pin
- MISO: SPI master in slave out, serial output pin (tri-state output)
- SCK: SPI clock which controls the communication
- CSN: Chip select (active low)

SPI communicates in a master/slave style where only one device, the master, can initiate data transmissions. The PGA900 always acts as the slave in SPI communication, where whatever external device that is communicating to it becomes the master. Both devices begin data transmission with the most significant bit (MSB) first.

Because multiple slave devices can exist on one bus, the master node is able to notify the specific slave node that it is ready to begin communicating by driving the CSN line to a low logic level. In the absence of active transmission, the master SPI device places the device in reset by driving the CSN pin to a high logic level. During a reset state the MISO pin operates in tri-state mode. For the SPI interface to have access to memory locations other than test register space, the IF_SEL bit in the MICRO_INTERFACE_CONTROL register has to be set to 1.

7.3.15.2 Activating the SPI

To activate SPI communication, follow these steps in this order:

1. Enable SPI by writing 1 to SPI_EN bit in DIG_IF_CTRL register
2. If SPI master communicates to PGA900 with the microprocessor in reset, reset microprocessor by writing 1 to MICRO_RESET bit in MICRO_INTERFACE_CONTROL register and enable digital interface by writing 1 to IF_SEL bit in the MICRO_INTERFACE_CONTROL. If SPI master communicates with PGA900 while microprocessor is running, then the COMBUF registers are used for communication.

7.3.15.3 SPI Protocol

7.3.15.3.1 SPI Master to PGA900 Commands

The SPI is a 24-bit protocol with a 3-bit memory access control word, a read-write bit, an 8-bit address, and an 8-bit data word. Table 7 describes the command codes.

Table 7. SPI Command Codes

BIT	FUNCTION	DESCRIPTION
23:21	DI PAGE ADDRESS	
	TEST = 3'b000	Access to Control and Status registers with DI PAGE ADDRESS = 0x0
	DATA RAM = 3'b001	Bits [9:8] of the Data RAM address is specified by the DATARAM_PAGE_ADDR register Bits [7:0] of the Data RAM address is specified by the Data Address field of the SPI transaction
	Control and Status Registers = 3'b010	Access to Control and Status registers with DI PAGE ADDRESS = 0x2
	DEVELOPMENT RAM = 3b011	Bits [11:8] of the Development RAM address is specified by the DEVRAM_PAGE_ADDR register Bits [7:0] of the Development RAM address is specified by the Data Address field of the SPI transaction
	OTP = 3'b100	Bits [11:8] of the OTP address is specified by the OTP_PAGE_ADDR register Bits [7:0] of the OTP address is specified by the Data Address field of the SPI transaction
	EECACHE = 3'b101	Access to the EEPROM cache/cells
	RESERVED = 3b110	
	RESERVED = 3b111	Access to Control and Status registers with DI PAGE ADDRESS = 0x7
20:13	Data Address	Address of register to read or write. During Reads, bit 13 is always 0. The reads always happen to 16-bit aligned addresses.
12	Write if 1, Read if 0	
11:4	Data	
3:0	Don't Care	

7.3.15.3.2 PGA900 to SPI Master Response

For SPI transfers to all the memories, the read data is available on the next SPI transfer as shown in Figure 38. That is, when reading from a memory location, the user has to send a subsequent transfer to get the data back. Further, the SPI response contains 16 bits of data. The PGA900 returns data from a 16-bit aligned address; that is, SPI reads must not straddle the 16-bit address boundary.

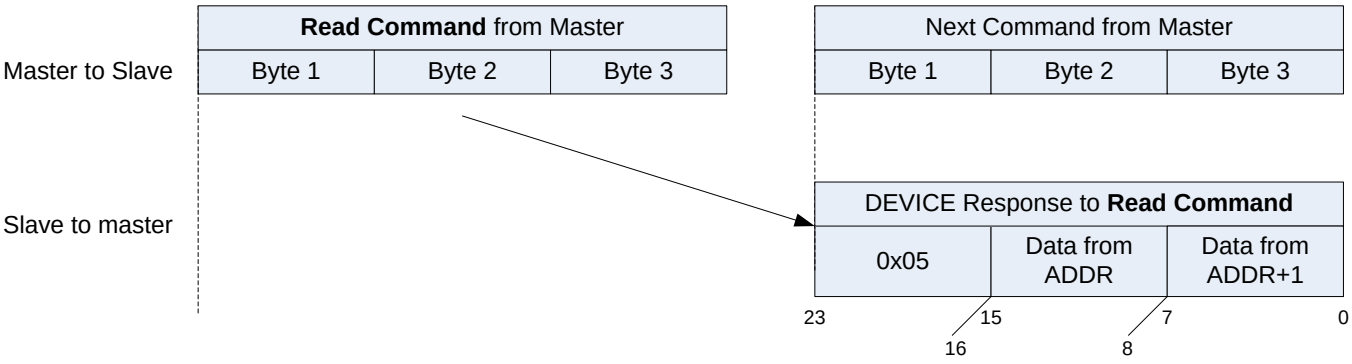


Figure 38. Response to SPI Read Commands is Available When the Next Command is Sent

Table 8 describes the SPI response. Note that only 2 bytes of data can be read with one SPI read command.

Table 8. SPI Response

BIT	FUNCTION
23:20	0b0000
19:16	0b0101
15:8	Read Data from ADDR, where ADDR is received in the previous SPI command
7:0	Read Data from ADDR + 1, where ADDR is received in the previous SPI command

7.3.15.3.3 SPI Command Examples

Table 9 lists a few examples of SPI transfers.

Table 9. SPI Transfers Examples

COMMAND	MASTER TO SLAVE DATA ON SPI MOSI
Read COM_MCU_TO_DIF_B1	000 00000100 0 XXXXXXXX 0000
Write 0x80 to Control and Status registers 0x30 (DAC_REG0_1)	010 00110000 1 10000000 0000
Write 0x34 to Data SRAM 0x7F	1. Write 0 to DATARAM_PAGE_ADDR: 010 00011001 1 00000000 0000 2. Send the following command to write data: 001 01111111 1 00110100 0000
Read from EEPROM Byte 7	101 00000111 0 XXXXXXXX 0000
Write 0xD9 to DEVRAM 0x1765	1. Write 0x17 to DEVRAM_PAGE_ADDR: 010 00011010 1 00010111 0000 2. Send the following command to write data: 011 01100101 1 11011001 0000

7.3.15.4 Clocking Details of SPI

Input data on the MOSI pin must be driven from the rising edge of the SCK clock, whereas output data on the MISO pin changes during the rising edge of the SCK clock. For SPI timing information, refer to the *SPI Timing Requirements* table.

7.3.16 I^2C Interface

The device includes an I^2C digital communication interface. The main function of the I^2C is to enable writes to and reads from all addresses available for I^2C access.

7.3.16.1 Overview of I^2C Interface

I^2C is a synchronous serial communication standard that requires the following two pins for communication:

- SDA: I^2C serial data line (SDA)
- SCL: I^2C serial clock line (SCL)

In addition, CSN pin is used to select the I^2C device address of PGA900. Specifically

- CSN - Logic 1 - Device address - 0x20:0x27
- CSN - Logic 0 - Device address - 0x40:0x47

It is noted that for valid I^2C communication to occur

- CSN must not change value during an I^2C transaction
- SPI clock (SCLK) must not be active when CSN is Logic 0 when selecting the I^2C device address

I^2C communicates in a master/slave style communication bus where one device, the master, can initiate data transmission. The device always acts as the slave device in I^2C communication, where the external device that is communicating to it acts as the master. The master device is responsible for initiating communication over the SDA line and supplying the clock signal on the SCL line. When the I^2C SDA line is pulled low it is considered a logical zero, and when the I^2C SDA line is floating high it is considered a logical one. For the I^2C interface to have access to memory locations other than test register space, the IF_SEL bit in the MICRO_INTERFACE_CONTROL register has to be set to logic one.

7.3.16.2 Activating the I²C Interface

To activate I²C communication, follow these steps in order:

1. Enable I²C by writing 1 to I2C_EN bit in DIG_IF_CTRL register
2. If I²C master communicates to PGA900 with the microprocessor in reset, reset microprocessor by writing 1 to MICRO_RESET bit in MICRO_INTERFACE_CONTROL register and enable digital interface by writing 1 to IF_SEL bit in the MICRO_INTERFACE_CONTROL register. If I²C master communicates with PGA900 while microprocessor is running, then the COMBUF registers are used for communication.
3. The default I²C interface communication speed is 100KBPS/400KBPS. The communication speed can be changed to 800KPBS mode by setting I2C_RATE bit to 1 in DIG_IF_CTRL register.
4. The I²C interfaces implements a deglitch filter as required by the I²C standard. The deglitch filters are enabled by default. The deglitch filter can be disabled by setting I2C_DEGLITCH_EN bit to 0 in DIG_IF_CTRL register.

7.3.16.3 I²C Interface Protocol

Figure 39 shows the basic protocol of the I²C frame for a Write operation.

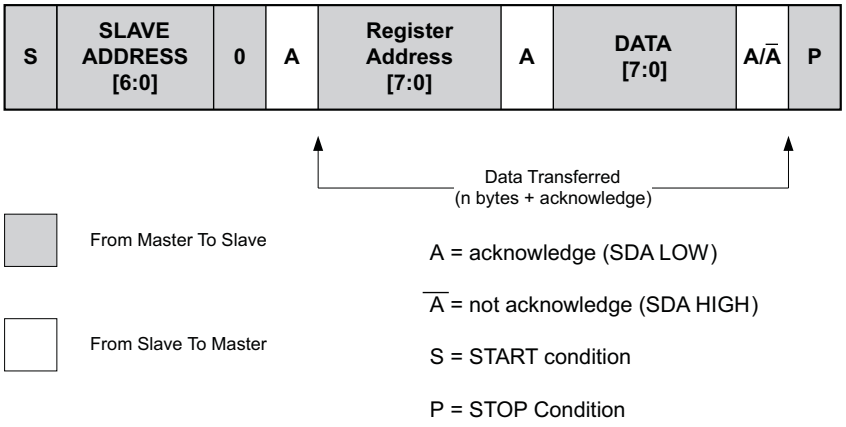


Figure 39. I²C Write Operation: A Master-Transmitter Addressing a PGA900 Slave With a 7-Bit Slave Address

The diagram represents the data fed into or out from the I²C SDA port.

The basic data transfer is to send 2 bytes of data to the specified slave address. The first data field is the register address and the second data field is the data sent or received.

The I²C slave address is used to determine which memory page is being referenced. Table 10 shows the mapping of the slave address to the memory page.

Table 10. Slave Addresses

SLAVE ADDRESS WHEN CSN = 1	SLAVE ADDRESS WHEN CSN = 0	PGA900 MEMORY PAGE
0x20	0x40	Test registers
0x21	0x41	Data RAM
0x22	0x42	Control and status registers, di_page_address = 0x02
0x23	0x43	Development RAM
0x24	0x44	OTP
0x25	0x45	EEPROM cache/cells
0x26	0x46	Reserved
0x27	0x47	Control and status registers, DI_PAGE_ADDRESS = 0x07

Figure 40 shows the basic PGA900 I²C protocol for a read operation.

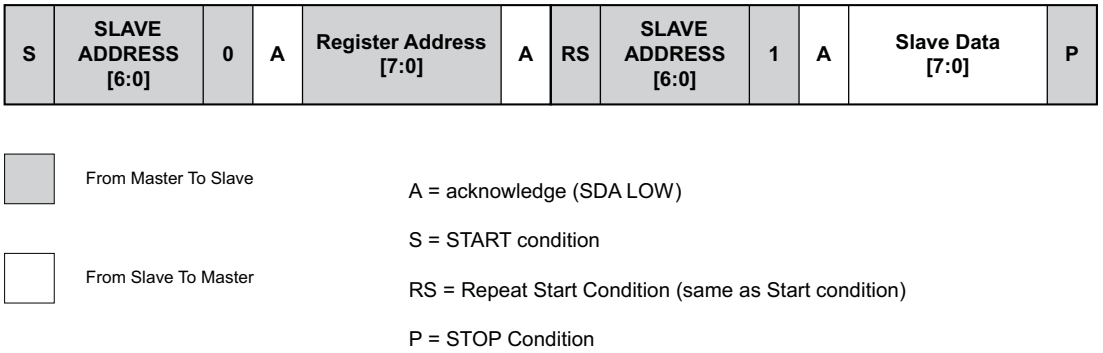


Figure 40. I²C Read Operation: A Master-Transmitter Addressing a PGA900 Slave With a 7-Bit Slave Address

The slave address determines the memory page. The R/W bit is set to 0.

The register address specifies the 8-bit address of the requested data.

The repeat start condition replaces the write data from the above write operation description. This informs the PGA900 devices that Read operation is going to take place instead of a write operation.

The second slave address contains the memory page from which the data is retrieved. The R/W bit is set to 1.

Slave data is transmitted after the acknowledge is received by the master.

Table 11 lists a few examples of I²C Transfers.

Table 11. I²C Transfers Examples

COMMAND	MASTER TO SLAVE DATA ON I²C SDA ((CSN = 1)	MASTER TO SLAVE DATA ON I²C SDA ((CSN = 0)
Read COM_MCU_TO_DIF_B0	Slave address: 010 0000 Register address: 0000 0100	Slave address: 100 0000 Register address: 0000 0100
Write 0x80 to Control and Status Registers 0x30 (DAC_REG0_1)	Slave address: 010 0010 Register address: 0011 0000 Data: 1000 0000	Slave address: 100 0010 Register address: 0011 0000 Data: 1000 0000
Write 0x34 to Data SRAM 0x7F	1. Write 0 to DATARAM_PAGE_ADDR Slave address: 010 0010 Register address 0001 1001 Data: 0000 0000 2. Send the following command to write data: Slave address: 010 0001 Register address 0111 1111 Data:0011 0100	1. Write 0 to DATARAM_PAGE_ADDR Slave address: 100 0010 Register address 0001 1001 Data: 0000 0000 2. Send the following command to write data: Slave address: 100 0001 Register address 0111 1111 Data:0011 0100
Read from EEPROM Byte 7	Slave Address: 010 0101 Register Address: 0000 0111	Slave Address: 100 0101 Register Address: 0000 0111
Write 0xD9 to DEVRAM 0x1765	1. Write 0x17 to DEVRAM_PAGE_ADDR Slave address: 010 0010 Register address: 0001 1010 Data: 0001 0111 2. Send the following command to write data Slave address: 010 0011 Register address 0110 0101 Data:1101 1001	1. Write 0x17 to DEVRAM_PAGE_ADDR Slave address: 100 0010 Register address: 0001 1010 Data: 0001 0111 2. Send the following command to write data Slave address: 100 0011 Register address 0110 0101 Data:1101 1001

7.3.16.4 Clocking Details of I²C Interface

The device samples the data on the SDA line when the rising edge of the SCL line is high, and is changed when the SCL line is low. The only exceptions to this indication are a start, stop, or repeated start condition as shown in Figure 41.

Figure 41. I²C Clocking Details

7.3.17 PWM Logic

The device has PWM logic. The PWM output is available on TOPDIG or TONDIG pins as a digital output. In addition, the PWM output is also available as an analog output at the VOUT pin; that is, the PWM logic is used to drive the DAC GAIN buffer. The PWM functionality uses a 16-bit 4-MHz free-running timer.

7.3.17.1 PWM Logic Enable

The PWM functionality can be enabled by writing a 1 to the PWM_EN bit in PWM_EN register. This enables the free-running timer used for PWM functionality

7.3.17.2 PWM ON and OFF Times

The PWM ON and OFF times can be configured by writing the ON and OFF time values to PWM_ON_TIME and PWM_OFF_TIME registers, respectively. If the PWM_ON_TIME and PWM_OFF_TIME registers are updated, the updated ON and OFF times take effect at the start of next ON time.

7.3.17.3 PWM Voltage Levels

The voltage levels of the PWM signals are configurable. The voltage level during the PWM 0 pulse is determined by the value in DAC_REG0 register while the voltage level during the PWM 1 pulse is determined by the value in DAC_REG1 register.

7.3.18 DAC Output

The device includes a 14-bit digital-to-analog converter that produces an absolute output voltage with respect to the accurate reference voltage or ratiometric output voltage with respect to the VDD supply.

When the microprocessor undergoes a reset, the DAC registers are driven to 0x000 code.

7.3.18.1 Ratiometric versus Absolute

The DAC output can be configured to be either in ratiometric-to-VDD mode or independent-of-VDD (or absolute) mode using the DAC_RATIOMETRIC bit in DAC_CONFIG.

NOTE

In ratiometric mode, changes in the VDD voltage result in a proportional change in the output voltage because the current reference for the DAC is derived from VDD.

7.3.19 DAC Gain

The DAC gain buffer is a configurable buffer stage for the DAC output. The DAC gain amplifier can be configured to operate in voltage amplification mode for voltage output or current amplification mode for 4- to 20-mA applications. In voltage output mode, DAC Gain can be configured for a specific gain value by setting the DAC_GAIN bits in DAC_CONFIG register to a specific value. The DAC gain can be configured to one of four possible gain configurations using the 2-bit DAC_GAIN field.

The final stage of DAC gain is connected to Vddp and ground. This gives the ability to drive VOUT voltage close to VDD voltage.

The DAC gain buffer also implements a COMP pin to allow implementation of compensation when driving large capacitive loads.

7.3.19.1 Connecting DAC Output to DAC GAIN Input

The DAC output can either be connected to TOP_TON test pin or can connected to DAC GAIN input as shown in Figure 42. The figure shows that the output is connected to DAC GAIN input only when TEST_MUX_DAC_EN bit in AMUX_CTRL register is set to 1.

The figure also shows how the PWM logic is enabled to drive DAC GAIN. Specifically, if PWM_EN bit in PWM_EN register is set to 1 and DAC_ENABLE bit in DAC_CTRL_STATUS register is set to 0, then DAC GAIN output is PWM output. In all other cases, the DAC GAIN output is a constant output based on the value of DAC_REG0 register.

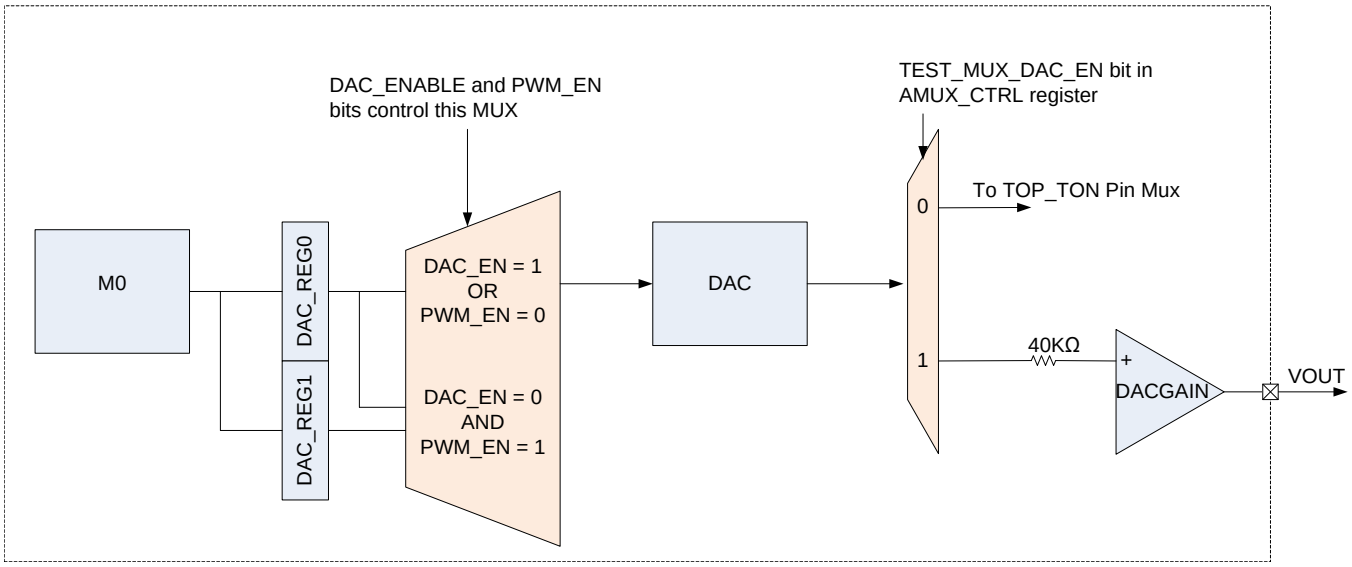


Figure 42. Connecting DAC to DAC GAIN

7.3.20 General-Purpose Input/Output (GPIO) and UART

7.3.20.1 GPIO

The device includes two general-purpose digital input/output pins. The two GPIO pins can be independently configured as input or output pins using the GPIO1_DIR bit in GPIO_DIR register for GPIO1 pin and GPIO2_DIR bit in GPIO_DIR register for GPIO2 pin. When configured as an output pin, the output buffers can be configured in either open-drain output mode or push-pull output mode using the GPIO1_CFG bit in GPIO_DIR register for GPIO1 and GPIO2_CFG bit in GPIO_DIR register for GPIO2 pin.

The microprocessor reads the state of the GPIO1 pin using the GPIO1_I bit in GPIO_INPUT register. Similarly, the state of GPIO2 pin is read using the GPIO2_I bit in GPIO_INPUT register. The state of the GPIO pins can be read in both GPIO input and output configurations.

When GPIO1/GPIO2 pins are configured as output pins, the microprocessor controls the Output state by writing the desired value to GPIO1_O bit in GPIO_OUTPUT register for GPIO1 pin and GPIO2_O bit in GPIO_OUTPUT register for GPIO2 pin.

7.3.20.2 UART

PGA900 includes a general-purpose UART with configurable baud rate. The UART transmit and receive pins are shared with MOSI and MISO SPI pins. By default, these pins are configured for SPI functionality. The MOSI and MISO pins can be configured for UART functionality by writing 1 to UART_SEL bit in the PIN_MUX register.

The UART functionality is disabled on power up. The UART functionality can be enabled by writing 1 to UART_EN bit in UART_EN register. The communication baud rate can be configured by writing the desired baud rate to BAUD_RATE registers. The formula to calculate the value to be loaded into BAUD_RATE register is given in Equation 2:

$$\text{BAUD\_RATE} = \text{round}(250000 / (\text{Desired baud rate}) - 1) \quad (2)$$

The UART in PGA900 is capable of transferring 8 bits only. Furthermore, the UART can be configured for even parity, odd parity, or parity disabled by writing to the corresponding bits in UART_CFG register. The number of stop bits is also configurable to either 1 or 2 bits using the TWO_STOP_BITS bit in the UART_CFG register. The UART in PGA900 always transmits 1 start bit.

The UART can be configured to generate interrupt to the microprocessor on TX Complete by writing 1 to the UART_TXCOMPLETE_INT_EN bit in UART_INTERRUPT_ENABLE register. Similarly, the UART can be configured to generate interrupt to the microprocessor on RX Ready by writing 1 to UART_RXRDY_INT_EN bit in UART_INTERRUPT_ENABLE register. Both TX Complete and RX Ready generate a common interrupt to the microprocessor. The source of the interrupt has to be determined in software by reading the UART_INTERRUPT_STATUS register.

Note that the interrupt status bit has to cleared in the interrupt service routine by writing 1 to UART_TX_COMPLETE_I for TX Complete interrupt and UART_RXRDY_I bit for RX Ready interrupt in UART_INTERRUPT_STATUS register.

PGA900 initiates transmission of data over UART TX line by writing data to the UART_TX_BUF. When data transmission is complete, TX Complete interrupt is generated. The data received on UART RX pin is stored in UART_RX_BUF. RX Ready interrupt is generated when data is received by PGA900.

The error status of UART communication is available in UART_LINE_STATUS register. See the description of the register for description of communication errors detected by the UART in PGA900.

7.3.21 Memory

7.3.21.1 OTP Memory

The OTP Memory space is 8 KB. This memory space contains program instructions for the M0 microprocessor. To program the OTP memory, an external VP_OTP voltage needs to be applied to the VP_OTP pin.

The device has the ability to lockout access to all memory spaces from the digital interface. This allows users to protect firmware intellectual property.

7.3.21.1.1 OTP Programming Using SPI

The OTP memory is programmed 4 bytes at a time. The program address is 4-byte aligned. That is, the OTP memory can be programmed starting at location 0x0000 4 bytes at a time. To program OTP memory, the 4 bytes to be programmed have to be first loaded into OTP Data registers. The upper 12 bits of the 14-bit 4-byte aligned OTP memory address (that is, the least two significant bits of the OTP memory address have to be 0), then has to be loaded into the program register. When the OTP_PROG bit in OTP_PROG_ADDR_2 register is set, the contents of the OTP data registers are transferred to the OTP memory cells.

The following sequence is an example to program 0x12345678 to OTP memory address 0x1764 (which is 4-byte aligned) using SPI digital interface:

1. Write 0x78 to OTP_PROG_DATA_1 register:
   010 00010000 1 01111000 0000
2. Write 0x56 to OTP_PROG_DATA_2 register:
   010 00010001 1 01010110 0000
3. Write 0x34 to OTP_PROG_DATA_3 register:
   010 00010010 1 00110100 0000
4. Write 0x12 to OTP_PROG_DATA_4 register:
   010 00010011 1 00010010 0000
5. Write 0xD9 (Least Significant Byte of (0x1764 >> 2)) to OTP_PROG_ADDR_1 register:
   010 00010100 1 11011001 0000
6. Write 0x85 (0x05 is the Most Significant Byte of (0x1764 >> 2)) to OTP_PROG_ADDR_2 register:
   010 00010101 1 10000101 0000
7. Read OTP_PROG_CTRL_STAT register:
   010 00010110 0 xxxxxxxx 0000

Wait for bit 1 of the read data to be 0 to confirm that the OTP has been programmed if necessary.

The programming sequence shows that six 24-bit commands must be transmitted to PGA900 to program 4 bytes of OTP. At 1 MHz, this translates to 144 µs. In addition, the SPI protocol requires 4 µs of chip select disable time between two consecutive commands and setup and hold times as shown in the SPI timing diagram, Figure 4. Thus, the total time to transmit 4 bytes of OTP data is 144 + (6 × 4) + 6(1) = 174 µs. To program all 8 KB, the total time is 174 × 8192 / 4 = 356.352 ms.

7.3.21.2 OTP Programming Using I²C

The OTP memory is programmed 4 bytes at a time. The program address is 4-byte aligned. That is, the OTP memory can be programmed starting at location 0x0000 4 bytes at a time. To program OTP memory, the 4 bytes to be programmed have to be first loaded into OTP Data registers. The upper 12 bits of the 14-bit 4-byte aligned OTP memory address (that is, the least two significant bits of the OTP memory address have to be 0) then has to be loaded into the program register. When the OTP_PROG bit in OTP_PROG_ADDR_2 register is set, the contents fo the OTP data registers are transferred to the OTP memory cells.

The following sequence is an example to program 0x12345678 to OTP memory address 0x1764 (which is 4-byte aligned) using I²C digital interface assuming CSN = 1:

1. Write 0x78 to OTP_PROG_DATA_1 register:
   - Slave address: 0100010
   - Register address : 00010000
   - Write data : 01111000
2. Write 0x56 to OTP_PROG_DATA_2 register:
   - Slave address: 0100010
   - Register address : 00010001
   - Write data : 01010110
3. Write 0x34 to OTP_PROG_DATA_3 register:
   - Slave address: 0100010
   - Register address : 00010010
   - Write data : 00110100
4. Write 0x12 to OTP_PROG_DATA_4 register:
   - Slave address: 0100010
   - Register address : 00010011
   - Write data : 00010010
5. Write 0xD9 (least significant byte of (0x1764 >> 2)) to OTP_PROG_ADDR_1 register:
   - Slave address: 0100010
   - Register address : 00010100
   - Write data : 11011001
6. Write 0x85 (0x05 is the most significant byte of (0x1764 >> 2), OTP_PROG = 1) to OTP_PROG_ADDR_2 register:
   - Slave address: 0100010
   - Register address : 00010101
   - Write data : 10000101
7. Read OTP_PROG_CTRL_STAT register:
   - Slave address: 0100010
   - Register address : 00010110

Wait for bit 1 of the read data to be 0 to confirm that the OTP has been programmed if necessary.

7.3.21.3 EEPROM Memory

Figure 43 shows the EEPROM structure. The contents of each EEPROM must be transferred to the EEPROM cache before writes; that is, the EEPROM can be programmed 8 bytes at a time. The EEPROM reads occur without the EEPROM cache.

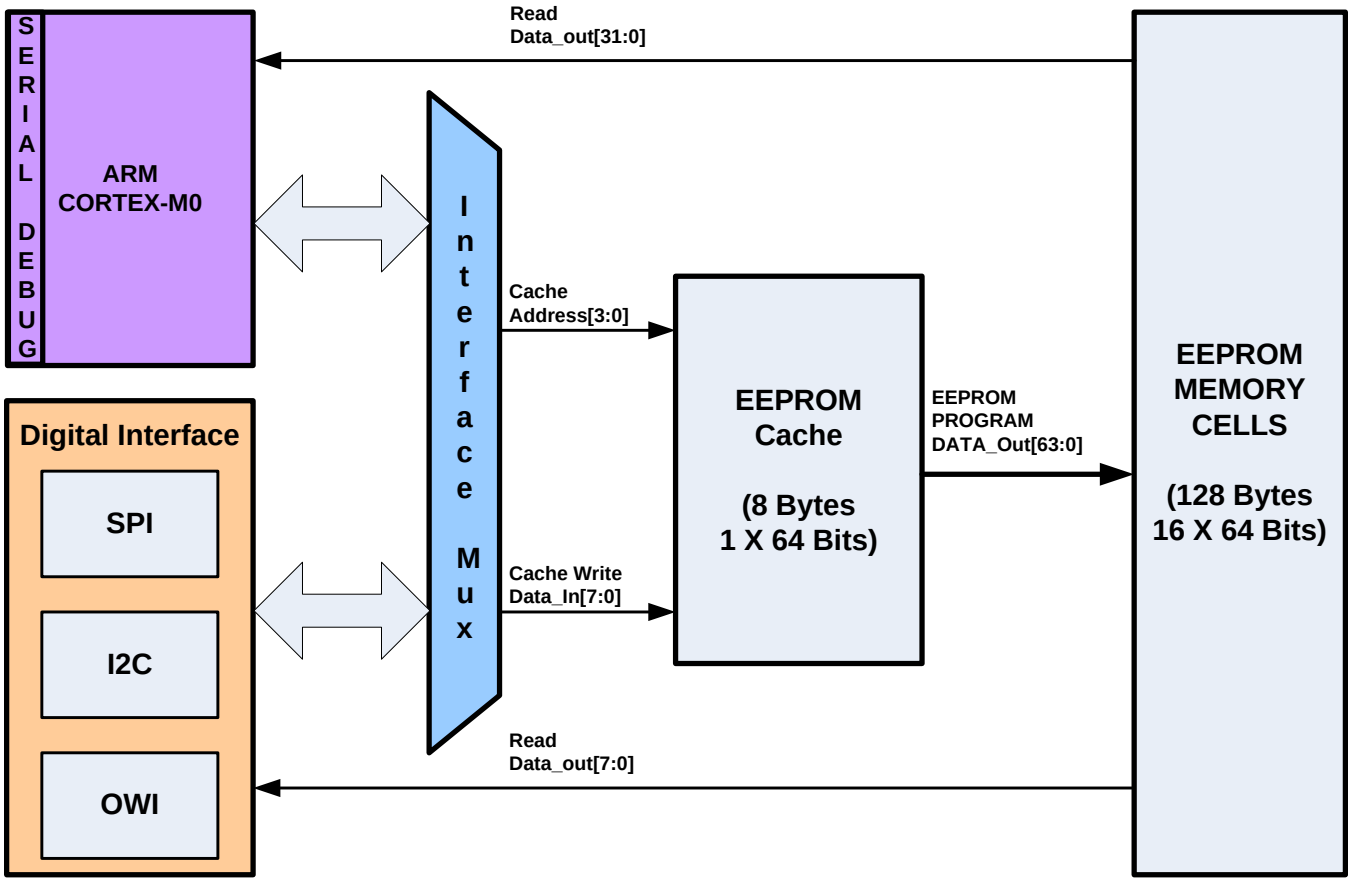


Figure 43. Structure of EEPROM Interface

7.3.21.3.1 EEPROM Cache

The EEPROM cache serves as temporary storage of data being transferred to selected EEPROM locations during the programming process.

7.3.21.3.2 EEPROM Programming Procedure

For programming the EEPROM, the EEPROM is organized in 16 pages of 8 bytes each. The EEPROM memory cells are programmed by writing to the 8-byte EEPROM cache. The contents of the cache are transferred to EEPROM memory cells by selecting the EEPROM memory page.

1. Select the EEPROM page by writing the upper 4 bits of the 7-bit EEPROM address to EEPROM_PAGE_ADDRESS register.
2. Load the 8-byte EEPROM cache by writing to the EEPROM_CACHE registers. Note that all 8 bytes have to be loaded into the EEPROM_CACHE.
3. Set the ERASE_AND_PROGRAM bit in EEPROM_CTRL register. Setting this bit automatically erases the selected EEPROM memory page and programs it with the contents of EEPROM_CACHE. Alternatively, the user can erase by writing 1 to the ERASE bit in EEPROM_CTRL register following by writing 1 to the PROGAM bit in the EEPROM_CTRL register after the erase is complete. The status of erase and program can be monitored through the EEPROM_STATUS register.

7.3.21.3.3 EEPROM Programming Current

The EEPROM programming process results in an additional 6-mA current on the VDD pin for the duration of programming.

7.3.21.3.4 CRC

The last byte of the EEPROM memory is reserved for the CRC. This CRC value covers all data in the EEPROM memory. Every time the last byte is programmed, the CRC value is automatically calculated and validated. The validation process checks the calculated CRC value with the last byte programmed in the EEPROM memory cell. If the calculated CRC matches the value programmed in the last byte, the CRC_GOOD bit is set in EEPROM_CRC_STATUS register.

The CRC check can also be initiated at any time by setting the CALCULATE_CRC bit in the EEPROM_CRC register. The status of the CRC calculation is available in the CRC_CHECK_IN_PROG bit in EEPROM_CRC_STATUS register, while the result of the CRC validation is available in the CRC_GOOD bit in EEPROM_CRC_STATUS register.

The CRC calculation pseudo code is as follows:

```
currentCRC8 = 0xFF; // Current value of CRC8

for NextData

D = NextData;

C = currentCRC8;

  begin

      nextCRC8_BIT0 = D_BIT7 ^ D_BIT6 ^ D_BIT0 ^ C_BIT0 ^ C_BIT6 ^ C_BIT7;

      nextCRC8_BIT1 = D_BIT6 ^ D_BIT1 ^ D_BIT0 ^ C_BIT0 ^ C_BIT1 ^ C_BIT6;

      nextCRC8_BIT2 = D_BIT6 ^ D_BIT2 ^ D_BIT1 ^ D_BIT0 ^ C_BIT0 ^ C_BIT1 ^ C_BIT2 ^ C_BIT6;

      nextCRC8_BIT3 = D_BIT7 ^ D_BIT3 ^ D_BIT2 ^ D_BIT1 ^ C_BIT1 ^ C_BIT2 ^ C_BIT3 ^ C_BIT7;

      nextCRC8_BIT4 = D_BIT4 ^ D_BIT3 ^ D_BIT2 ^ C_BIT2 ^ C_BIT3 ^ C_BIT4;

      nextCRC8_BIT5 = D_BIT5 ^ D_BIT4 ^ D_BIT3 ^ C_BIT3 ^ C_BIT4 ^ C_BIT5;

      nextCRC8_BIT6 = D_BIT6 ^ D_BIT5 ^ D_BIT4 ^ C_BIT4 ^ C_BIT5 ^ C_BIT6;

      nextCRC8_BIT7 = D_BIT7 ^ D_BIT6 ^ D_BIT5 ^ C_BIT5 ^ C_BIT6 ^ C_BIT7;

   end

   currentCRC8 = nextCRC8_D8;

endfor
```

NOTE

The EEPROM CRC calculation is complete 340 µs after digital core starts running at power up. After the CRC calculation completes, the EEPROM_CRC_VALUE contains the CRC value calculated and CRC_GOOD bit in the EEPROM_CRC_STATUS register indicates the status of the CRC check.

7.3.21.4 DATA RAM Memory

This memory space is used for M0 scratchpad memory, such as intermediate calculation results. It is a 1-KB memory space, and located at memory page 1.

7.3.21.5 Control and Status Registers Memory

The M0 uses control and data registers to interact with the analog blocks of the device.

7.3.21.6 Software Development RAM

7.3.21.6.1 Software Development

PGA900 has 8 KB of development RAM that can overlay the OTP memory address. This is to allow convenient development of software. The software development RAM can be configured to either overlay the OTP memory address space (that is, same address space as OTP) or assigned to non-OTP-overlay address space using the REMAP bit in the REMAP register. The REMAP can be set using a debugger.

7.3.21.6.1.1 Downloading Software into Development RAM Using Digital Interface

Follow these steps to download the software into development RAM.

1. Set REMAP bit in REMAP register to 0.
2. Select the development RAM page address by writing the appropriate page value to the DEVRAM_PAGE_ADDR register. Note that this register is at digital interface memory page address 0x02 and each development RAM page consists of 256 bytes.
3. Write to the development RAM to the byte in the 256-byte development RAM page at digital interface memory page address 0x03.

7.3.21.6.2 Trace FIFO

The PGA900 software development RAM can also be used as trace FIFO. The trace feature allows either P ADC value or T ADC value to be stored in the development RAM for post-processing. The trace source can be selected by setting the TRACE_SOURCE in the TRACE_FIFO_CTRL_STAT register. The trace function can be enabled by writing 1 to the TRACE_FIFO_ENABLE bit in TRACE_FIFO_CTRL_STAT register.

The trace capture stops after collecting 2048 ADC samples. The samples are 32-bit address aligned with the ADC value in the lower 16 or 24 bits depending on the configured number of ADC bits. The state of tracing can be monitored through TRACE_FIFO_EMPTY, TRACE_FIFO_HALF_FULL, and TRACE_FIFO_FULL bits in the TRACE_FIFO_CTRL_STAT register. Once the trace FIFO is enabled, a time equal to 2048 ADC samples × the configured decimation rate has to elapse before attempting to read the data or check the status of tracing through the TRACE_FIFO_CTRL_STAT register.

NOTE

If the trace feature is enabled, the software development RAM cannot be used to overlay the OTP for software development.

7.3.21.7 OTP Security

7.3.21.7.1 Definition of OTP Security

OTP security is defined as the inability to read OTP memory contents with digital interfaces (SPI, I^2C, and OWI) and software debugger. This feature is implemented in PGA900 to prevent the download of OTP contents after the device is deployed in the field.

7.3.21.7.2 OTP Security in PGA900

In PGA900, if OTP security is enabled, **access to all memories** is disabled. That is, after security is enabled, the digital interface cannot access OTP, EEPROM, and RAM through digital interfaces and debugger.

However, the COMBUF register is accessible even when security is enabled.

7.3.21.7.3 Enabling OTP Security in PGA900

PGA900 has two registers to enable OTP security:

1. SECLOCK register (8 bits)
   a. Writing 0x00 enables access to all memories through digital interface.
   b. Writing 0xAA disables access to all memories through digital interface.

   The reset value of the register is such that OTP security is disabled.
2. DEBUG_LOCK bit in MICRO_INTERFACE_CONTROL register

a. Writing a 0 to this bit enables access through software debugger.
b. Writing a 1 to this bit disables access through software debugger.

The reset value of the bit is 0.

7.3.21.7.4 Using OTP Security in PGA900

The M0 firmware enables OTP security by checking a EEPROM bit (or bits) reserved for OTP security. This software is executed at M0 startup after M0 reset is deasserted. The pseudocode is:

1. If (Security bit reserved in EEPROM is 1)
   a. SECLOCK = 0xAA;
   b. DEBUG_LOCK bit = 1;
2. Else
   a. SECLOCK = 0x00;
   b. DEBUG_LOCK bit = 0;
3. End

Using this method, if OTP security is enabled in the manufacturing line before calibration is complete, then all accesses to memories are disabled. That is, the manufacturing tester cannot communicate with PGA900 anymore. Hence, OTP security cannot be disabled. **Therefore, OTP security must be enabled as a last step on the manufacturing line**.

7.3.21.7.5 Sequence in Manufacturing Line

1. Ensure EEPROM bits reserved for EEPROM security correspond to *OTP Security Disable* value.
2. Program OTP with firmware.
3. Perform all calibrations.
4. As a final step on the manufacturing line, program EEPROM bits corresponding to OTP security to *OTP Security Enable* value.

7.3.22 Diagnostics

This section describes the diagnostics.

7.3.22.1 Power Supply Diagnostics

The device includes modules to monitor the power supply for faults. The internal power rails that are monitored are:

1. AVDD voltage, thresholds are generated using inaccurate reference.
2. DVDD voltage, thresholds are generated using inaccurate reference.
3. Bridge supply voltage, thresholds are generated using internal voltage reference.
4. Internal oscillator supply voltage, thresholds are generated using inaccurate reference.
5. Reference output voltage, thresholds are generated using inaccurate reference.

The electrical specifications list the voltage thresholds for each of the power rails.

When a fault is detected, an appropriate bit in the PSMON1 and PSMON2 registers is set. If the faulty condition is removed, the fault bits remain latched. To remove the fault, M0 software must read the fault bit and write a logic zero back to the bit. In addition, a system reset clears the fault.

NOTE

When bridge supply over voltage condition is detected, the user must disable the bridge supply the user by setting BRDG_EN bit BRDG_CTRL register to 0. In addition, the user must set disconnect P gain amplifier from VINPP and VINPN input pins by setting PGAIN_OPEN bit in AFE_CFG register to 1 to not damage P Gain amplifier.

7.3.22.2 Resistive Bridge Sensor and Temperature Sensor Connectivity Diagnostics

7.3.22.2.1 P Gain Input Faults

The device includes modules to monitor for sensor faults. Specifically, the device monitors the sensor pins for opens (including loss of connection from the sensor), short-to-ground, and short to sensor supply.

When a fault is detected, an appropriate bit in the AFEDIAG register is set. All three types of sensor faults result in the setting of the same bit, meaning it is not possible to distinguish the type of fault that has occurred. Even after the faulty condition is removed, the fault bits remains latched. To remove the fault the M0 software must read the fault bit and write a logic zero back to the bit. In addition a system reset clears the fault.

Open sensor faults are detected through the use of an internal pulldown resistor. The value of the resistor and the threshold can be configured using DIS_R1M and DIS_R2M bits in AFEDIAG_CFG register. Note that these diagnostics can be disabled by writing to the DIS_R_SD bit in AFEDIAG_CFG register.

The thresholds for both P Gain are derived off of VBRDG voltage.

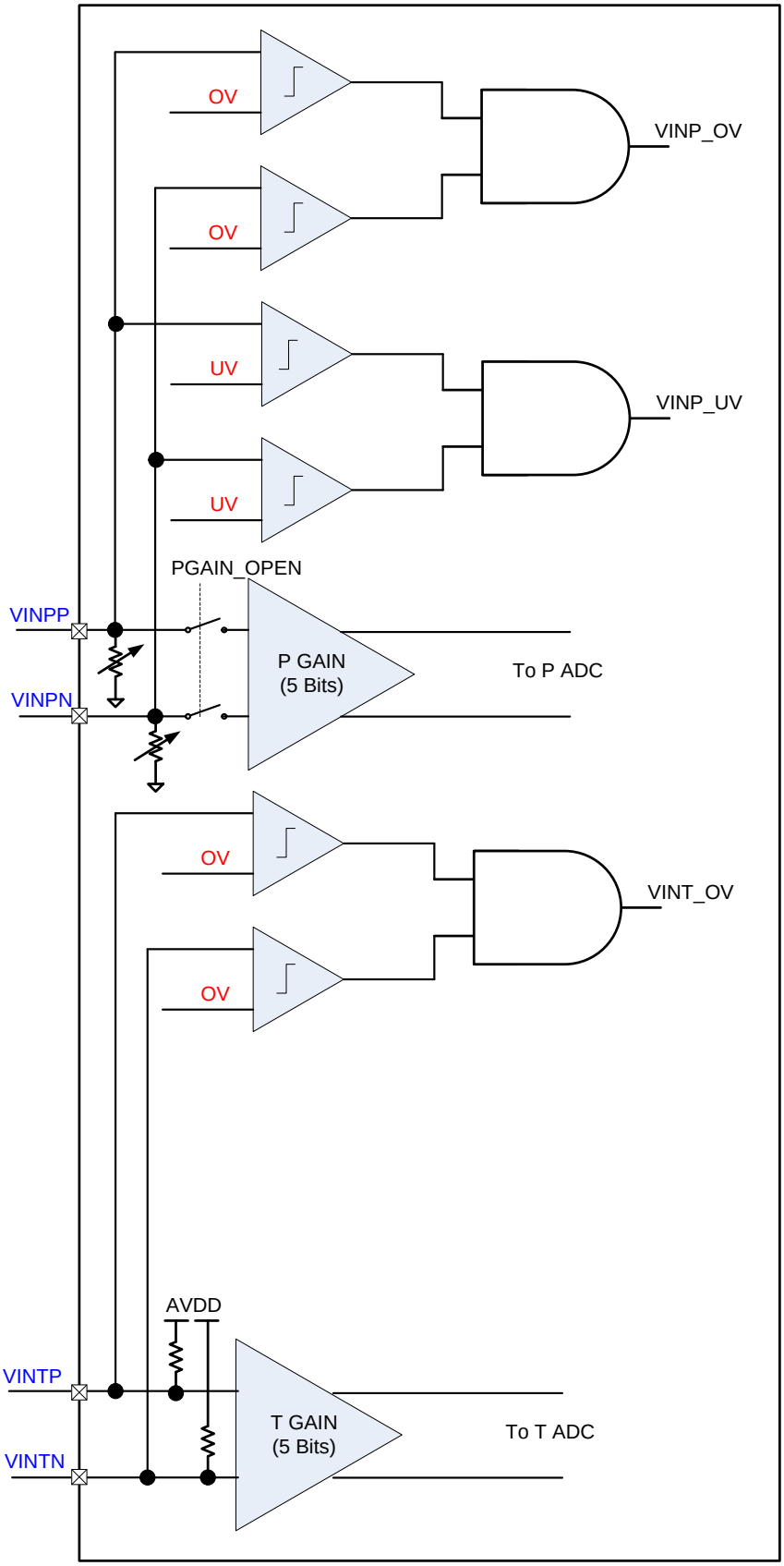


Figure 44. Block Diagram of P Gain and T Gain Diagnostics

NOTE

When an overvoltage fault is detected at the input of P gain amplifier, the user must set disconnect P gain amplifier from VINPP and VINPN input pins by setting PGAIN_OPEN bit in AFE_CFG register to 1 in order to not damage the P gain amplifier.

7.3.22.2.2 T Gain Input Faults

The device implements a comparator to detect overvoltage conditions at the input of T gain amplifier; that is, VINTP and VINTN pins. This diagnostics can be disabled by writing to the DIS_R_TEMP bit in AFEDIAG_CFG register.

7.3.22.3 P Gain and T Gain Output Diagnostics

The device includes modules that verify that the output signal of each gain is within a certain range. This ensures that gain stages in the signal chain are working correctly. AVDD voltage is used to generate the thresholds voltages for comparison.

When a fault is detected, the corresponding bit in AFEDIAG register is set. Even after the faulty condition is removed, the fault bits remain latched. To remove the fault, M0 software must read the fault bit and write a logic zero back to the bit. In addition a system reset clears the fault.

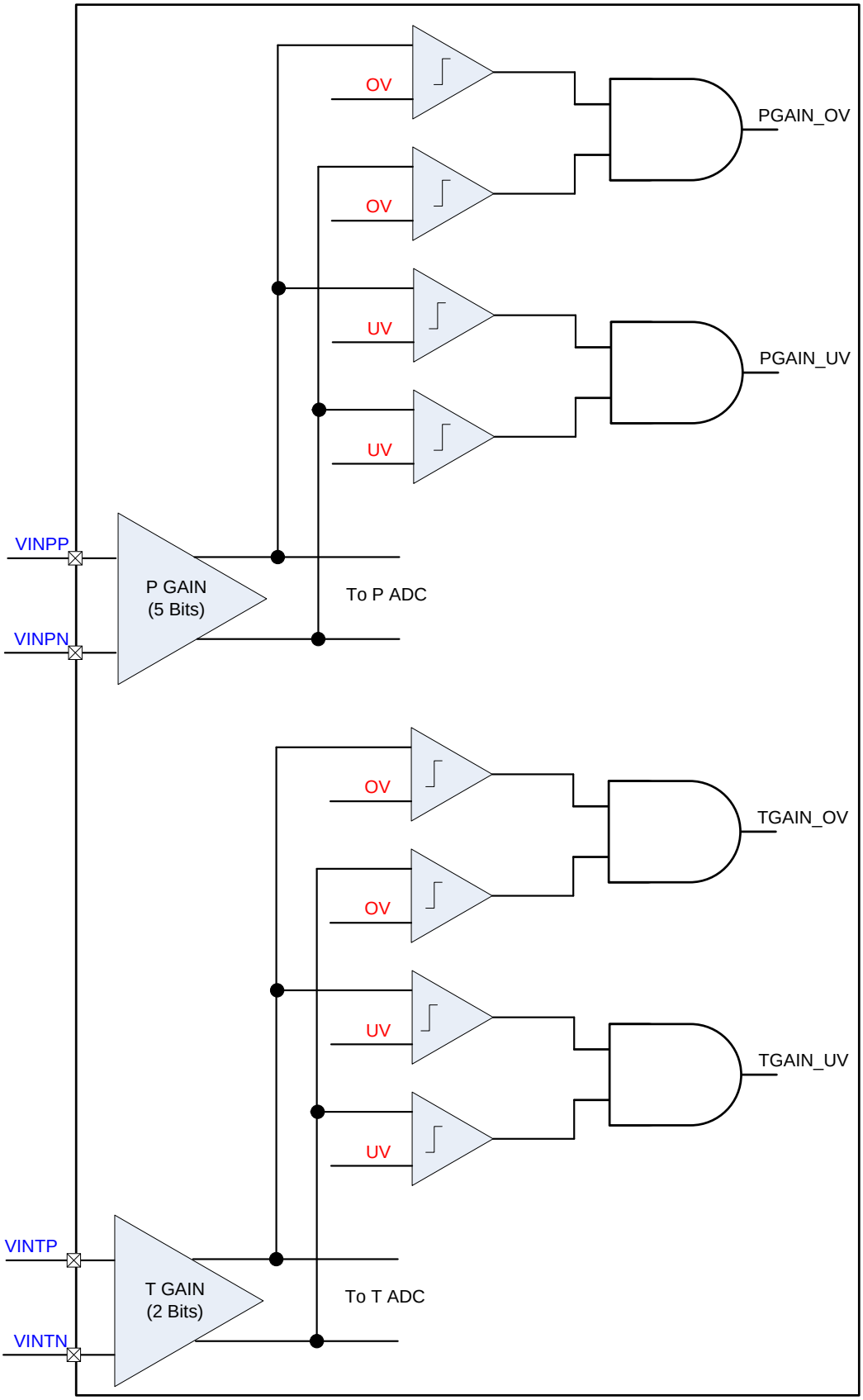


Figure 45. Block Diagram of P Gain and T Gain Output Diagnostics

NOTE

TGAIN_UV flag is ON all the time if TGAIN is configured for single-ended mode because one of the terminals is always at ground potential. In other words, TGAIN_UV flag cannot be used to detect low voltage faults in T GAIN path if the amplifier is configured for single-ended mode. Software has to use T ADC counts to determine fault.

7.3.22.4 DAC Diagnostics

The PGA900 implements loop back feature to check the integrity of the signal chain. Figure 46 shows the block diagram representation of the loop back feature. This figure shows that the DAC output is connected to positive side of the differential input while the negative side of the differential input is grounded. The common-mode for the loop back amplifier is always VBRDG/2.

The DAC outputs are voltage divided by a nominal factor of 5 before being connected to the PGAIN inputs.

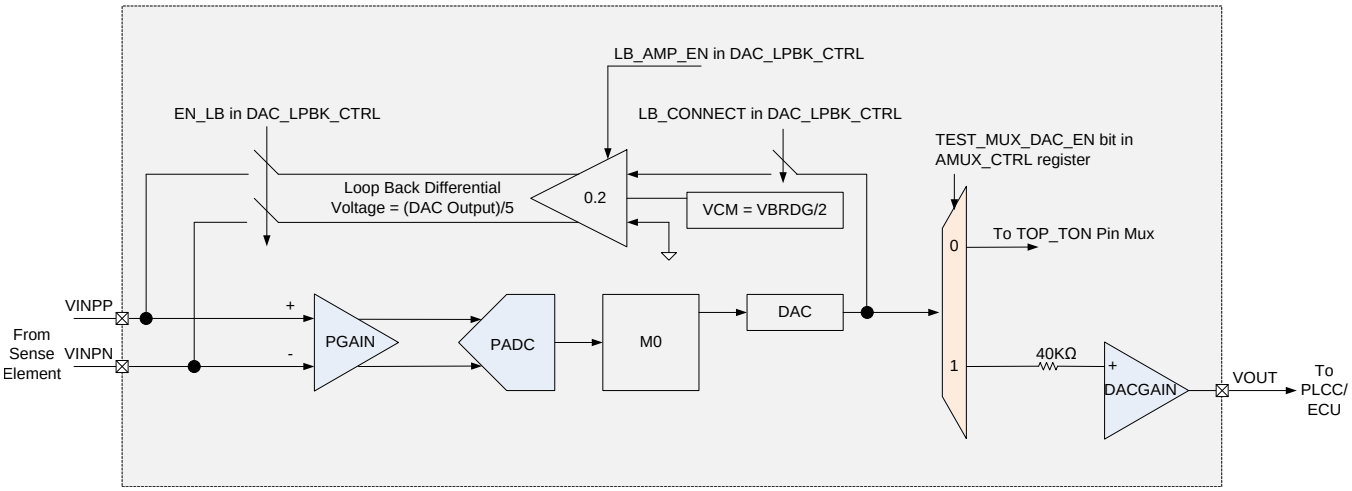


Figure 46. DAC Loop Back.

DAC loop back is enabled by setting LB_EN bit in EN_CTRL to 1. Note that ADC output represents the DAC output scaled by the voltage divider and the PGAIN.

The DAC outputs continue to be available on VOUT pin in the Loop Back mode.

7.3.22.5 Harness Open Wire Diagnostics

PGA900 allows for open wire diagnostics to be performed in the ECU. Specifically, the ECU can detect open VDD or Open GND wire by installing a pullup or pulldown on VOUT1 line.

Figure 47 shows the possible harness open-wire faults on VDD and GND pins.

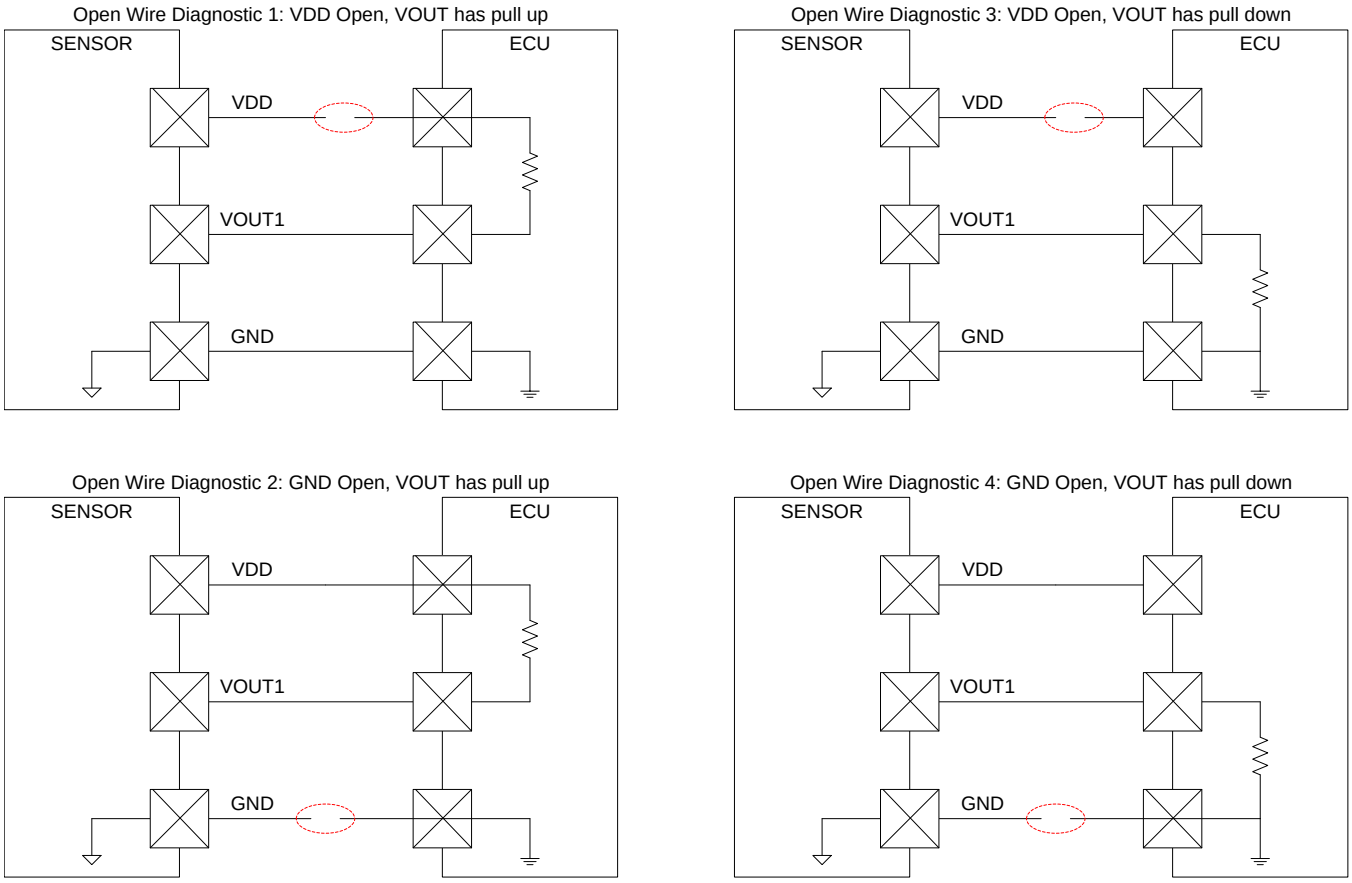


Figure 47. Harness Open-Wire Diagnostics

CAUTION

If FBN pin has intermittent disconnects, that is, the pin opens and reconnects, then the reconnect action could damage the device.

7.3.22.6 Software Watchdog

PGA900 includes a software watchdog. The software watchdog can be enabled by writing 1 to WDOG_EN bit in the WDOG_CTRL_STAT register. If the software watchdog is enabled software has to service the watchdog periodically by writing to the WDOG_TRIG register.

The value written to the WDOG_TRIG corresponds to the timeout value. The timeout value: (WDOG_TRIG+1)*2ms. If the software does not service the watchdog before timeout value, the microprocessor is reset. In this case of microprocessor reset, all peripherals (including the digital interfaces) except the software watchdog are reset. That is, all control and status registers are set to their respective reset values, and the software watchdog continues to be enabled. Furthermore, the WD_RESET bit in WDOG_CTRL_STAT is be set to 1 to indicate that the microprocessor recovered from a software watchdog timeout event. The WD_RESET bit can be cleared by writing a 1 to the WD_RESET bit.

7.3.22.7 EEPROM CRC and TRIM Error

The last Byte in the EEPROM stores the CRC for all the data in EEPROM.

The user can verify the EEPROM CRC at any time. When the last byte is loaded into the Cache, the device automatically calculates the CRC and updates the CRC_ERR bit in EE_STATUS Control and Data Registers. The validity of the CRC can also be verified by initiating the CRC check by setting the control bit CACULATE_CRC bit in EEPROM_CRC register.

The device also has analog trim values. The validity of the analog trim values is checked on power up and before the M0 reset is de-asserted. The validity of the trim values can be inferred using the TRIM_ERR bit in EE_STATUS Control and Data Registers.

7.3.22.8 DATA RAM MBIST

The device implements DATA RAM memory built-in self-test (MBIST). This diagnostic checks the integrity of the internal RAM on an on-demand basis.

The procedure to start this diagnostic and check for status is as below:

- 1. Set DATARAM_MBIST_CTRL bits in RAM_MBIST_CONTROL register to 0b11. This starts the DATARAM MBIST.
- 2. Wait for DATARAM_MBIST_DONE in RAM_MBIST_STATUS register to be set to 1 by the DATARAM MBIST algorithm
- 3. Check DATARAM_MBIST_FAIL bit in RAM_MBIST_STATUS register after DATARAM_MBIST_DONE flag is set to 1. If DATARAM_MIBIST_FAIL is 1, then DATARAM MBIST failed, indicating faulty DATARAM. If DATARAM_MBIST_FAIL is 0, then DATARAM has no faults.

The DATARAM MBIST takes 34 ms to execute. The software can continue execution as long as DATARAM is not accessed.

NOTE

While the DATARAM MBIST is running, the M0 must not access the DATARAM.

NOTE

Contents of RAM is lost when MBIST is executed. Therefore, TI recommends that MBIST be run only at power up or microprocessor reset.

7.3.22.9 Development RAM MBIST

The device implements Development RAM MBIST. This diagnostic checks the integrity of the internal RAM on an on-demand basis.

The procedure to start this diagnostic and check for status is as below:

- 1. Set DEVRAM_MBIST_CTRL bits in RAM_MBIST_CONTROL register to 0b11. This starts the DEVRAM MBIST.
- 2. Wait for DEVRAM_MBIST_DONE in RAM_MBIST_STATUS register to be set to 1 by the DEVRAM MBIST algorithm
- 3. Check DEVRAM_MBIST_FAIL bit in RAM_MBIST_STATUS register after DEVRAM_MBIST_DONE flag is set to 1. If DEVRAM_MIBIST_FAIL is 1, then DEVRAM MBIST failed, indicating faulty DEVRAM. If DEVRAM_MBIST_FAIL is 0, then DEVRAM has no faults.

The DEVRAM MBIST takes 304 ms to execute. The software can continue execution as long as DEVRAM is not accessed.

NOTE

While the DEVRAM MBIST is running, the M0 must not access the DEVRAM.

NOTE

Contents of DEVRAM are lost when MBIST is executed. Therefore, TI recommends only running the MBIST at power up or microprocessor reset.

7.3.23 ARM Cortex-M0 Microprocessor

The ARM Corext-M0 microprocessor is an exceptionally high-performance version of this popular 32-bit microcontroller.

The microprocessor can be configured to run at different frequencies by setting the M0_FREQUENCY_CONTROL register. Note that with increased clock speed, the current consumption of the device increases.

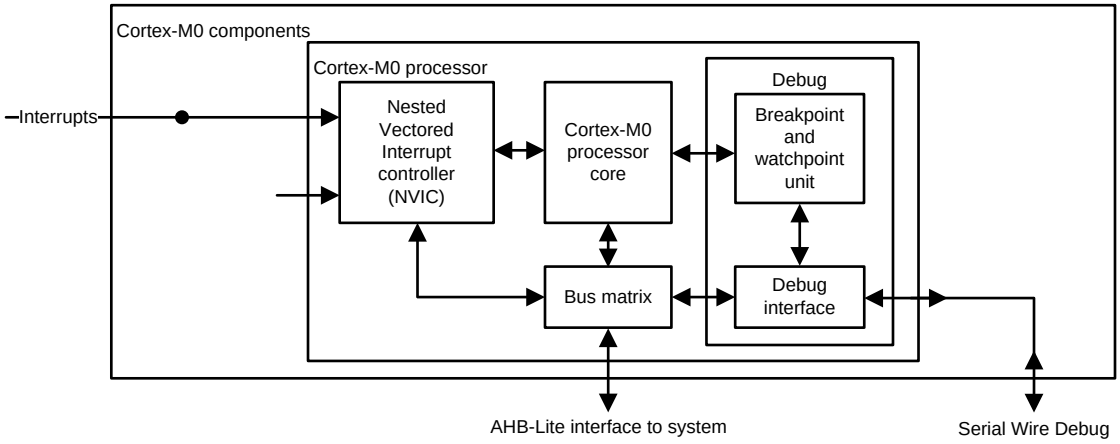


Figure 48. ARM Cortex-M0 Core

7.3.23.1 SYSTICK Timer

The Cortex M0 microprocessor includes a 24-bit timer with 1-µs update rate.

7.3.23.2 NVIC Controller

The Cortex M0 microprocessor includes the nested vectored interrupt controller (NVIC). The peripheral interrupt signals connect to the NVIC, and the NVIC prioritized the interrupts. All NVIC registers are accessible using word transfers only. The NVIC in PGA900 is configured to support 8 interrupts.

7.3.23.3 Software Debugger

The Cortex M0 microprocessor includes the debugger. The PGA900 Cortex M0 debuggers includes the following features:

- Two breakpoints
- One watchpoint

7.3.24 Revision ID

PGA900 includes Revision ID registers. These registers are read-only and represent the device revision and is not unique for every device in a certain revision.

7.3.25 Test MUX

PGA900 provides the ability to either stimulate the internal circuits from external sources and monitor the internal circuits by external sources. This is accomplished using the test pins. For more information on the MUX settings, refer to the *Control and Status Registers* section.

7.4 Device Functional Modes

There are 2 main functional modes for the PGA900: current (4- to 20-mA loop) and voltage mode. Depending on which mode is being used, the external components and connections are slightly different.

7.4.1 Voltage Mode

When configured in this mode, the FBN pin must be connected to the VOUT pin. If the VOUT pin is driving a large capacitive load, a compensation capacitor can be connected to the COMP pin and an isolation resistor can be placed between the VOUT and FBN pins. The FBP pin is not used in voltage mode.

7.4.2 Current Mode

When configured in this mode, the VOUT pin is driving the base of a BJT as shown in Figure 141. The COMP pin is connected to the emitter of the BJT and the FBP pin is connected to the return terminal of the supply. The FBN pin is not used in current mode.

7.5 Register Maps

7.5.1 Memory Map

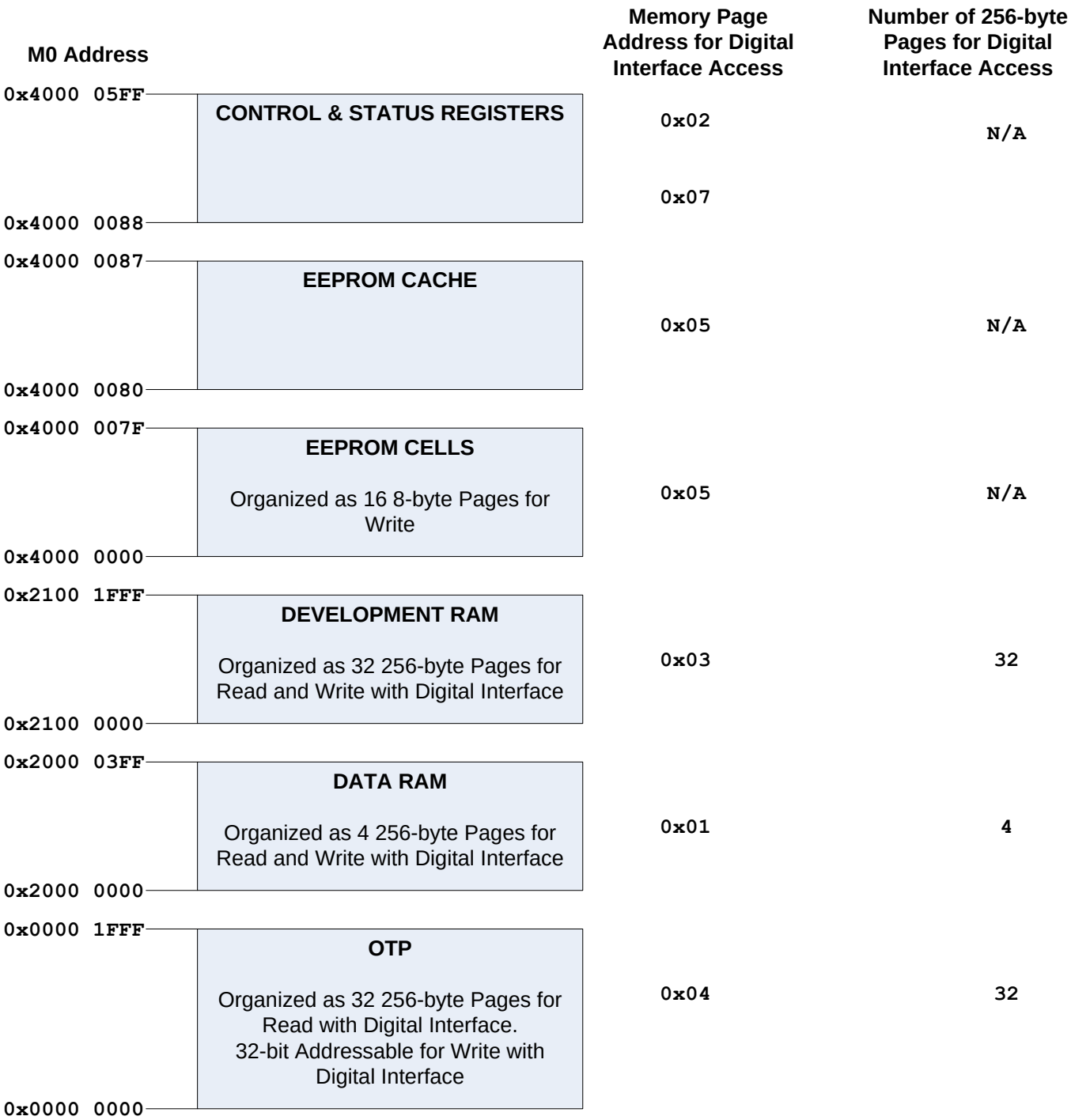


Figure 49. Memory Diagram

Refer to ARM_M0_User_guide.pdf for M0-specific register addresses

7.5.2 Control and Status Registers

Table 12. Control and Status Registers

Register Name	Description	DI Page Address	DI Offset Address	M0 Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
RAMBIST_ CONTROL	RAM MBIST CONTROL	0x2	0x02	0x40000502	RW					DEVRAM_MBIST _CTRL[1]	DEVRAM_MBIST _CTRL[0]	DATARAM_MBIST _CTRL[1]	DATARAM_MBIST _CTRL[0]
RAMBIST_ STATUS	RAM MBIST STATUS	0x2	0x03	0x40000503	R			DEVRAM_MBIST_ FAIL	DEVRAM_MBIST_ DONE			DATARAM_MBIST_ FAIL	DATARAM_MBIST_ DONE
CLK_CTRL_STATUS	M0 FREQUENCY CONTROL	0x2	0x04	0x40000504	RW			CLK_ STATUS_1	CLK_ STATUS_0			CLK_CTRL_1	CLK_CTRL_0
DIG_IF_CTRL	DIGITAL INTERFACE CONTROL	0x2	0x06	0x40000506	RW		I2C_ DEGLITCH_ EN	I2C_RATE	OWI_DGL_CNT_SEL	OWI_ XCVR_EN	OWI_EN	I2C_EN	SPI_EN
OWI_ERROR_ STATUS_LO		0x2	0x08	0x40000508	R	OWI_ERR7	OWI_ERR6	OWI_ERR5	OWI_ERR4	OWI_ERR3	OWI_ERR2	OWI_ERR1	OWI_ERR0
OWI_ERROR_ STATUS_HI		0x2	0x09	0x40000509	R	OWI_ERR_CLR						OWI_ERR9	OWI_ERR8
OWI_ INTERRUPT		0x2	0x0A	0x4000050A	RW								OWI_INT
OWI_ INTERRUPT_ ENABLE		0x2	0x0B	0x4000050B	RW								OWI_INT_EN
OTP_PROG_ DATA1		0x2	0x10	0x40000510	RW								
OTP_PROG_ DATA2		0x2	0x11	0x40000511	RW								
OTP_PROG_ DATA3		0x2	0x12	0x40000512	RW								
OTP_PROG_ DATA4		0x2	0x13	0x40000513	RW								
OTP_PROG_ ADDR1		0x2	0x14	0x40000514	RW	ADDR[7]	ADDR[6]	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
OTP_PROG_ ADDR2		0x2	0x15	0x40000515	RW	OTP_PROG					ADDR[10]	ADDR[9]	ADDR[8]
OTP_PROG_ CTRL_STAT		0x2	0x16	0x40000516	RW							OTP_ PROG_IN_ PROGRESS	OTP_ PROGTIMER_ DIS
OTP_PAGE_ ADDR		0x2	0x18	0x40000518	RW				ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
DATARAM_ PAGE_ADDR		0x2	0x19	0x40000519	RW							ADDR[1]	ADDR[0]
DEVRAM_PAGE_ ADDR		0x2	0x1A	0x4000051A	RW				ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
WDOG_CTRL_STAT		0x2	0x1C	0x4000051C	RW	WD_RESET							WDOG_EN
WDOG_TRIG		0x2	0x1D	0x4000051D	W								
PIN_MUX		0x2	0x1E	0x4000051E	RW								UART_SEL
PADC_DATA1		0x2	0x20	0x40000520	R								
PADC_DATA2		0x2	0x21	0x40000521	R								

Table 12. Control and Status Registers (continued)

Register Name	Description	DI Page Address	DI Offset Address	M0 Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
PADC_DATA3		0x2	0x22	0x40000522	R								
PADC_CONFIG		0x2	0x23	0x40000523	RW					PADC_INT_RATE	PADC_DECI_RATE	PADC_EN_24BIT	PADC_EN
TADC_DATA1		0x2	0x24	0x40000524	R								
TADC_DATA2		0x2	0x25	0x40000525	R								
TADC_DATA3		0x2	0x26	0x40000526	R								
TADC_CONFIG		0x2	0x27	0x40000527	RW					TADC_INT_RATE	TADC_DECI_RATE	TADC_EN_24BIT	TADC_EN
ADC_CFG_1		0x2	0x29	0x40000529	RW		Write 0	Write 0	ADC_EN	Write 0	Write 0	RESET_CLK	RESET_MOD
DAC_REG0_1		0x2	0x30	0x40000530	RW								
DAC_REG0_2		0x2	0x31	0x40000531	RW								
DAC_REG1_1		0x2	0x32	0x40000532	RW								
DAC_REG1_2		0x2	0x33	0x40000533	RW								
DAC_CTRL_STATUS		0x2	0x38	0x40000538	RW								DAC_ENABLE
DAC_CONFIG		0x2	0x39	0x40000539	RW								DAC_RATIOMETRIC
DAC_LPBK_CTRL		0x2	0x3A	0x4000053A	RW						EN_LB	LB_AMP_EN	LB_CONNECT
OP_STAGE_CTRL		0x2	0x3B	0x4000053B	RW			PULLUP_EN	DACCAP_EN	4_20MA_EN	DAC_GAIN[2]	DAC_GAIN[1]	DAC_GAIN[0]
AFE_CFG		0x0	0xF4	0x400004F4	RW	Write 0	Write 0	PGAIN_OPEN	Write 0	Write 0	Write 0	Write 0	Write 0
AFEDIAG_CFG		0x2	0x45	0x40000545	RW		DIS_R_TEMP	DIS_R_SD	FAULT_THRS[2]	FAULT_THRS[1]	FAULT_THRS[0]	DIS_R2M	DIS_R1M
BRDG_CTRL		0x2	0x46	0x40000546	RW						VBRDG_CTRL[1]	VBRDG_CTRL[0]	BRDG_EN
P_GAIN_SELECT		0x2	0x47	0x40000547	RW	P_INV			P_GAIN[4]	P_GAIN[3]	P_GAIN[2]	P_GAIN[1]	P_GAIN[0]
T_GAIN_SELECT		0x2	0x48	0x40000548	RW	T_INV						T_GAIN[1]	T_GAIN[0]
TEMP_CTRL		0x2	0x4C	0x4000054C	RW		ITEMP_CTRL[2]	ITEMP_CTRL[1]	ITEMP_CTRL[0]	TEMP_MUX_CTRL[3]	TEMP_MUX_CTRL[2]	TEMP_MUX_CTRL[1]	TEMP_MUX_CTRL[0]
ALPWR		0x2	0x50	0x40000550					GATE_CTRL_SD		ADC_EN_VREF		SD
DLPWR		0x2	0x54	0x40000554	RW								OWI_CLK_EN
PSMON1		0x2	0x58	0x40000558	RW	OSC_VDD_UV	OSC_VDD_OV	AVDD_UV	AVDD_OV	REF_UV	REF_OV	VBRG_UV	VBRG_OV
PSMON2		0x2	0x59	0x40000559	RW							DVDD_UV	DVDD_OV
AFEDIAG		0x2	0x5A	0x4000055A	RW	TGAIN_UV	TGAIN_OV	PGAIN_UV	PGAIN_OV		VINT_OV	VINP_UV	VINP_OV
TOPDIG_MUX_SEL		0x2	0x60	0x40000560	RW			TOPDIG[5]	TOPDIG[4]	TOPDIG[3]	TOPDIG[2]	TOPDIG[1]	TOPDIG[0]
TONDIG_MUX_SEL		0x2	0x61	0x40000561	RW			TONDIG[5]	TONDIG[4]	TONDIG[3]	TONDIG[2]	TONDIG[1]	TONDIG[0]
AMUX_ACT		0x2	0x64	0x40000564	RW							TOUT_MUX_SEL	TIN_MUX_EN

Table 12. Control and Status Registers (continued)

Register Name	Description	DI Page Address	DI Offset Address	M0 Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
AMUX_TIN_ MUX_CTRL		0x2	0x65	0x40000565	RW						AMUX_TIN _MUX_CTRL [2]	AMUX_TIN _MUX_CTRL [1]	AMUX_TIN _MUX_CTRL[0]
AMUX_TOUT_ MUX_CTRL		0x2	0x66	0x40000566	RW					AMUX_TOUT _MUX_CTRL [3]	AMUX_TOUT_ MUX_CTRL [2]	AMUX_TOUT _MUX_CTRL [1]	AMUX_TOUT _MUX_CTRL [0]
AMUX_CTRL		0x2	0x67	0x40000567	RW					TSEM_N	TEST_ MUX_T_ EN	TEST_ MUX_P_ EN	TEST_ MUX_DAC_ EN
TRACE_FIFO_ CTRL_STAT		0x2	0x70	0x40000570	RW		TRACE_ FIFO_ FULL	TRACE_ FIFO_ HALF_ FULL	TRACE_ FIFO_ EMPTY			TRACE_ SOURCE	TRACE_ FIFO_ ENABLE
REVISION_ID1		0x0	0x00	0x40000400	R	OPT_ID[2]	OPT_ID[1]	OPT_ID[0]		REV_ID[3]	REV_ID[2]	REV_ID[1]	REV_ID[0]
REVISION_ID2		0x0	0x01	0x40000401	R					DL_ID[3]	DL_ID[2]	DL_ID[1]	DL_ID[0]
COM_MCU_TO_ DIF_B1		0x0	0x04	0x40000404	RW								
COM_MCU_TO_ DIF_B2		0x0	0x05	0x40000405	RW								
COM_TX_STATUS		0x0	0x06	0x40000406	RW								COM_TXRDY
COM_DIF_TO_ MCU_B1		0x0	0x08	0x40000408	RW								
COM_DIF_TO_ MCU_B2		0x0	0x09	0x40000409	RW								
COM_RX_STATUS		0x0	0x0A	0x4000040A	RW								COM_RXRDY
COM_RX_INT_ENABL E		0x0	0x0B	0x4000040B	RW								COM_RXRDY_ INT_EN
MICRO_ INTERFACE_ CONTROL		0x0	0x0C	0x4000040C	RW						DEBUG_LOCK	MICRO_RESE T	IF_SEL
SECLOCK		0x0	0x0D	0x4000040D	RW								SECLOCK
UART_CONFIG		0x7	0x00	0x40000200	RW						TWO_STOP_ BITS	PARITY	PARITY_EN
UART_EN		0x7	0x01	0x40000201	RW								UART_EN
BAUD_RATE_LO		0x7	0x02	0x40000202	RW								
BAUD_RATE_HI		0x7	0x03	0x40000203	RW								
UART_LINE_ STATUS		0x7	0x04	0x40000204	RW				TX_COMPLET E	RX_READY	FRAMING_ ERROR	PARITY_ ERROR	OVERRUN_ ERROR
UART_INTERRUPT _STATUS		0x7	0x08	0x40000208	R							UART_ TXCOMPLETE _I	UART_ RXRDY_I
UART_INTERRUPT _ENABLE		0x7	0x0A	0x4000020A	RW							UART_ TXCOMPLET_ INT_EN	UART_ RXRDY_ INT_EN
UART_RX_BUF		0x7	0x0C	0x4000020C	R								
UART_TX_BUF		0x7	0x0E	0x4000020E	RW								
PWM_ON_TIME1		0x7	0x10	0x40000210	RW								

Table 12. Control and Status Registers (continued)

Register Name	Description	DI Page Address	DI Offset Address	M0 Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
PWM_ON_TIME2		0x7	0x11	0x40000211	RW								
PWM_OFF_TIME1		0x7	0x12	0x40000212	RW								
PWM_OFF_TIME2		0x7	0x13	0x40000213	RW								
PWM_EN		0x7	0x14	0x40000214	RW								PWM_EN
GPIO_INPUT		0x7	0x18	0x40000218	R							GPIO2_I	GPIO1_I
GPIO_OUTPUT		0x7	0x19	0x40000219	RW							GPIO2_O	GPIO1_O
GPIO_DIR		0x7	0x1A	0x4000021A	RW					GPIO2_CFG	GPIO1_CFG	GPIO2_DIR	GPIO1_DIR
REMAP		0x7	0x20	0x40000220	RW								REMAP
EEPROM ARRAY		0x5	0x00-0x7F	0x40000000-0x4000007F	RW								
EEPROM_CACHE		0x5	0x80-0x87	0x40000080-0x40000087	RW								
EEPROM_PAGE_ADDRESS		0x5	0x88	0x40000088	RW						ADDR[2]	ADDR[1]	ADDR[0]
EEPROM_CTRL		0x5	0x89	0x40000089	RW					FIXED_ERASE_PROG_TIME	ERASE_AND_PROGRAM	ERASE	PROGRAM
EEPROM_CRC		0x5	0x8A	0x4000008A	RW								CALCULATE_CRC
EEPROM_STATUS		0x5	0x8B	0x4000008B	R						PROGRAM_IN_PROGRESS	ERASE_IN_PROGRESS	READ_IN_PROGRESS
EEPROM_CRC_STATUS		0x5	0x8C	0x4000008C	R							CRC_GOOD	CRC_CHECK_IN_PROG
EEPROM_CRC_VALUE		0x5	0x8D	0x4000008D	R								

Table 13. Cortex M0 Specific Registers

Register Name	Description	M0 Address
SYST_CSR	SysTick Control and Status Register	0xE000E010
SYST_RVR	SysTick Reload Value Register	0xE000E014
SYST_CVR	SysTick Current Value Register	0xE000E018
ISER	Interrupt Set-Enable Register	0xE000E100
ICER	Interrupt Clear-Enable Register	0xE000E180
ISPR	Interrupt Set-Pending Register	0xE000E200
ICPR	Interrupt Clear-Pending Register	0xE000E280
IPR	Interrupt Priority Registers	0xE000E400-0xE000E41C

NOTE

For details of the Cortex M0 specific registers, refer to ARM_M0_User_guide.pdf that can be downloaded from the ARM website (www.arm.com).

7.5.2.1 RAM MBIST Control (M0 address = 0x40000502) (DI page address = 0x2) (DI page offset = 0x02)

Figure 50. RAMBIST_CONTROL

7	6	5	4	3	2	1	0
				DEVRAM_MBIST_CTRL[1]	DEVRAM_MBIST_CTRL[0]	DATARAM_MBIST_CTRL[1]	DATARAM_MBIST_CTRL[0]
				RW	RW	RW	RW
				0	0	0	0

Table 14. RAMBIST_CONTROL Field Descriptions

Bit Definitions	Bit			
RAMBIST_CONTROL	0: DATARAM_MBIST_CTRL[0]	**DATARAM_MBIST_CTRL[1]**	**DATARAM_MBIST_CTRL[0]**	
		0	0	DATARAM MBIST is inactive
	1: DATARAM_MBIST_CTRL[1]	0	1	Invalid
		1	0	Invalid
		1	1	DATARAM MBIST is active
	2: DEVRAM_MBIST_CTRL[0]	**DEVRAM_MBIST_CTRL[1]**	**DEVRAM_MBIST_CTRL[0]**	
		0	0	DEVRAM MBIST is inactive
		0	1	Invalid
	3: DEVRAM_MBIST_CTRL[1]	1	0	Invalid
		1	1	DEVRAM MBIST is active
	4:			
	5:			
	6:			
	7:			

7.5.2.2 RAM MBIST Status (M0 address = 0x40000503) (DI page address = 0x2) (DI page offset = 0x03)

Figure 51. RAMBIST_STATUS

7	6	5	4	3	2	1	0
		DEVRAM_MBIST_FAIL	DEVRAM_MBIST_DONE			DATARAM_MBIST_FAIL	DATARAM_MBIST_DONE
		R	R			R	R
		0	0			0	0

Table 15. RAMBIST_STATUS Field Descriptions

Bit Definitions	Bit	
RAMBIST_STATUS	0: DATARAM_MBIST_DONE	1: DATARAM MBIST is complete. 0: DATARAM MBIST has not started or has not completed.
	1: DATARAM_MBIST_FAIL	1: DATARAM MBIST has failed. 0: DATARAM MBIST has not failed. This bit is valid only when DATARAM_MBIST_DONE is 1.
	2:	
	3:	
	4: DEVRAM_MBIST_DONE	1: DEVRAM MBIST is complete. 0: DEVRAM MBIST has not started or has not completed.
	5: DEVRAM_MBIST_FAIL	1: DEVRAM MBIST has failed. 0: DEVRAM MBIST has not failed. This bit is valid only when DEVRAM_MBIST_DONE is 1.
	6:	
	7:	

7.5.2.3 M0 Frequency Control (M0 address = 0x40000504) (DI page address = 0x2) (DI page offset = 0x04)

Figure 52. CLK_CTRL_STATUS

7	6	5	4	3	2	1	0
		CLK_STATUS_1	CLK_STATUS_0			CLK_CTRL_1	CLK_CTRL_0
		R	R			RW	RW
		0	0			0	0

Table 16. CLK_CTRL_STATUS Field Descriptions

Bit Definitions	Bit			
CLK_CTRL	0: CLK_CTRL_0 1: CLK_CTRL_1	**CLK_CTRL_1**	**CLK_CTRL_0**	**DESCRIPTION**
		0	0	Microcontroller frequency is 1 MHz.
		0	1	Microcontroller frequency is 2 MHz.
		1	0	Microcontroller frequency is 4 MHz.
		1	1	Microcontroller frequency is 500 kHz.
	2:			
	3:			
CLK_STATUS	4: CLK_STATUS_0 5: CLK_STATUS_1	**CLK_STATUS_1**	**CLK_STATUS_0**	**DESCRIPTION**
		0	0	Microcontroller frequency is 1 MHz.
		0	1	Microcontroller frequency is 2 MHz.
		1	0	Microcontroller frequency is 4 MHz.
		1	1	Microcontroller frequency is 500 kHz.
	6:			
	7:			

7.5.2.4 Digital Interface Control (M0 address = 0x40000506) (DI page address = 0x2) (DI page offset = 0x06)

Figure 53. DIG_IF_CTRL

7	6	5	4	3	2	1	0
	I2C_DEGLITCH_EN	I2C_RATE	OWI_DGL_CNT_SEL	OWI_XCVR_EN	OWI_EN	I2C_EN	SPI_EN
	RW	RW	RW	RW	RW	RW	RW
	1	0	0	0	1	1	1

Table 17. DIG_IF_CTRL Field Descriptions

Bit Definitions	Bit	
DIG_IF_CTRL	0: SPI_EN	1: SPI is enabled 0: SPI is disabled
	1: I2C_EN	1: I^2C is enabled 0: I^2C is disabled
	2: OWI_EN	1: OWI is enabled 0: OWI is disabled
	3: OWI_XCVR_EN	1: Enable OWI Transceiver – OWI transceiver is connected to VDD 0: Disable OWI Transceiver – OWI transceiver is disconnected from VDD
	4: OWI_DGL_CNT_SEL	1: OWI activation deglitch filters are set to 10ms 0: OWI activation deglitch filters are set to 1ms
	5: I2C_RATE	1: I^2C transfer rate is >400 KPBPS, ≤800 KBPS 0: I^2C transfer rate is ≤400 KBPS
	6: I2C_DEGLITCH_EN	1: Enables deglitch filters on I^2C interface 0: Disables deglitch filters on I^2C interface
	7:	

7.5.2.5 OWI_ERROR_STATUS_LO (M0 address = 0x40000508) (DI page address = 0x2) (DI page offset = 0x08)

Figure 54. OWI_ERROR_STATUS_LO

7	6	5	4	3	2	1	0
OWI_ERR7	OWI_ERR6	OWI_ERR5	OWI_ERR4	OWI_ERR3	OWI_ERR2	OWI_ERR1	OWI_ERR0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Table 18. OWI_ERROR_STATUS_LO Field Descriptions

Bit Definitions	Bit	
OWI_ERROR_STATUS_LO	0: OWI_ERR0	1: SYNC field bit rate is < 320 – 5% BPS 0: No error
	1: OWI_ERR1	1: SYNC field bit rate is > 19200 + 5% BPS 0: No error
	2: OWI_ERR2	1: SYNC field stop bit too short 0: No error
	3: OWI_ERR3	1: COMMAND field: Incorrect stop bit value 0: No error
	4: OWI_ERR4	1: COMMAND field: Stop bit too short 0: No error
	5: OWI_ERR5	1: DATA field: Incorrect stop bit value 0: No error
	6: OWI_ERR6	1: DATA field: Stop bit too short 0: No error
	7: OWI_ERR7	1: DATA field: Slave transmit value overdriven to dominant value during stop bit transmit 0: No error

7.5.2.6 OWI_ERROR_STATUS_HI (M0 address = 0x40000509) (DI page address = 0x2) (DI page offset = 0x09)

Figure 55. OWI_ERROR_STATUS_HI

7	6	5	4	3	2	1	0
OWI_ERR_CLR						OWI_ERR9	OWI_ERR8
RW						R	R
0						0	0

Table 19. OWI_ERROR_STATUS_HI Field Descriptions

Bit Definitions	Bit	
OWI_ERROR_STATUS_HI	0: OWI_ERR8	1: SYNC field: Consecutive bits in the sync field are different by more than ±19% tolerance 0: No error
	1: OWI_ERR9	1: COMMAND field: Invalid command sent through OWI protocol 0: No error
	2:	
	3:	
	4:	
	5:	
	6:	
	7: OWI_ERR_CLR	1: Clear OWI_ERROR_STATUS_LO and OWI_ERROR_STATUS_HI registers 0: No action

7.5.2.7 OWI_INTERRUPT (M0 address = 0x4000050A) (DI page address = 0x2) (DI page offset = 0x0A)

Figure 56. OWI_INTERRUPT

7	6	5	4	3	2	1	0
							OWI_INT
							RW
							0

Table 20. OWI_INTERRUPT Field Descriptions

Bit Definitions	Bit		
OWI_INTERRUPT	0: OWI_INT	**Read**	**Write**
		1: OWI interrupt is active 0: No action	1: Clear OWI interrupt 0: No action
	1:		
	2:		
	3:		
	4:		
	5:		
	6:		
	7:		

7.5.2.8 OWI_INTERRUPT_EN (M0 address = 0x4000050B) (DI page address = 0x2) (DI page offset = 0x0B)

Figure 57. OWI_INTERRUPT_EN

7	6	5	4	3	2	1	0
							OWI_INT_EN
							RW
							0

Table 21. OWI_INTERRUPT_EN Field Descriptions

Bit Definitions	Bit	
OWI_INTERRUPT_EN	0: OWI_INT_EN	1: Enable OWI interrupt 0: No error
	1:	
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.9 OTP_PROG_DATA1-4

Figure 58. OTP_PROG_DATA1 (M0 address = 0x40000510) (DI page address = 0x2) (DI page offset = 0x10)

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Figure 59. OTP_PROG_DATA2 (M0 address = 0x40000511) (DI page address = 0x2) (DI page offset = 0x11)

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Figure 60. OTP_PROG_DATA3 (M0 address = 0x40000512) (DI page address = 0x2) (DI page offset = 0x12)

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Figure 61. OTP_PROG_DATA4 (M0 address = 0x40000513) (DI page address = 0x2) (DI page offset = 0x13)

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Little-endian mode.

7.5.2.10 OTP_PROG_ADDR1-2

Figure 62. OTP_PROG_ADDR1 (M0 address = 0x40000514) (DI page address = 0x2) (DI page offset = 0x14)

7	6	5	4	3	2	1	0
ADDR[7]	ADDR[6]	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Figure 63. OTP_PROG_ADDR2 (M0 address = 0x40000515) (DI page address = 0x2) (DI page offset = 0x15)

7	6	5	4	3	2	1	0
OTP_PROG					ADDR[10]	ADDR[9]	ADDR[8]
RW					RW	RW	RW
0					0	0	0

Table 22. OTP_PROG_ADDR1-2 Field Descriptions

Bit Definitions	Bit	
OTP_PROG_ADDR2	0: ADDR[8]	
	1: ADDR[9]	
	2: ADDR[10]	
	3:	
	4:	
	5:	
	6:	
	7: OTP_PROG	1: The data is programmed specified by OTP_PROG_DATA1-4 is programmed into address specified by bits OTP_PROG_ADDR bits [10:0]. The bit is automatically cleared when the internal program timer in the OTP controller is used when the programming starts. The bit retains the state until cleared by software when the program timer in the OTP controller is disabled 0: No action

7.5.2.11 OTP_PROG_CTRL_STAT (M0 address = 0x40000516) (DI page address = 0x2) (DI page offset = 0x16)

Figure 64. OTP_PROG_CTRL_STAT

7	6	5	4	3	2	1	0
						OTP_ PROG_IN_ PROGRESS	OTP_ PROGTIMER_ DIS
						R	RW
						0	0

Table 23. OTP_PROG_CTRL_STAT Field Descriptions

Bit Definitions	Bit	
OTP_PROG_CTRL_STAT	0: OTP_PROGTIMER_DIS	1: OTP programming timer is disabled. When the program timer is disabled, the program timing is controlled by assertion and de-assertion of the OTP_PROG bit in the OTP_PROG_ADDR register 0: OTP programming timer is enabled.
	1: OTP_PROG_IN_PROGRESS	1: Indicates that the programming is in progress. This bit is valid only when the OTP_PROGTIMER_DIS is 0. 0: N/A
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.12 OTP_PAGE_ADDR (M0 address = 0x40000518) (DI page address = 0x2) (DI page offset = 0x18)

Figure 65. OTP_PAGE_ADDR

7	6	5	4	3	2	1	0
			ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
			RW	RW	RW	RW	RW
			0	0	0	0	0

7.5.2.13 DATARAM_PAGE_ADDR (M0 address = 0x40000519) (DI page address = 0x2) (DI page offset = 0x19)

Figure 66. DATARAM_PAGE_ADDR

7	6	5	4	3	2	1	0
						ADDR[1]	ADDR[0]
						RW	RW
						0	0

7.5.2.14 DEVRAM_PAGE_ADDR (M0 address = 0x4000051A) (DI page address = 0x2) (DI page offset = 0x1A)

Figure 67. DEVRAM_PAGE_ADDR

7	6	5	4	3	2	1	0
			ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
			RW	RW	RW	RW	RW
			0	0	0	0	0

7.5.2.15 WDOG_CTRL_STAT (M0 address = 0x4000051C) (DI page address = 0x2) (DI page offset = 0x1C)

Figure 68. WDOG_CTRL_STAT

7	6	5	4	3	2	1	0
WD_RESET							WDOG_EN
RW							RW
0							0

Table 24. WDOG_CTRL_STAT Field Descriptions

Bit Definitions	Bit	
WDOG_CTRL_STAT	0: WDOG_EN	1:Watchdog timer is enabled 0: Watchdog timer is disabled
	1:	
	2:	
	3:	
	4:	
	5:	
	6:	
	7: WD_RESET	1: Watchdog timer is timed out. This bit is cleared when 1 is written to it. 0: N/A

7.5.2.16 WDOG_TRIG (M0 address = 0x4000051D) (DI page address = 0x2) (DI page offset = 0x1D)

Figure 69. WDOG_TRIG

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
1	1	1	1	1	1	1	1

- Writing any 8-bit value to this register, resets the watchdog timer.
- The watchdog timeout value is (WDOG_TRIG + 1) × 2 ms.

7.5.2.17 PIN_MUX (M0 address = 0x4000051E) (DI page address = 0x2) (DI page offset = 0x1E)

Figure 70. PIN_MUX

7	6	5	4	3	2	1	0
							UART_SEL
							RW
							0

Table 25. PIN_MUX Field Descriptions

Bit Definitions	Bit	
PIN_MUX	0: UART_SEL	1: MOSI/RX and MISO/TX pins are configured for UART 0: MOSI/RX and MISO/TX pins are configured for SPI
	1:	
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.18 PADC_DATA1-3

Figure 71. PADC_DATA1 (M0 address = 0x40000520) (DI page address = 0x2) (DI page offset = 0x20)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Figure 72. PADC_DATA2 (M0 address = 0x40000521) (DI page address = 0x2) (DI page offset = 0x21)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Figure 73. PADC_DATA3 (M0 address = 0x40000522) (DI page address = 0x2) (DI page offset = 0x22)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

- To read PADC_DATA from Digital Interface, the least significant byte/word must be read first. This returns the least significant byte/word. The most significant bytes are latched into a shadow register. Reads to the Digital Interface addresses 0x21, 0x22 return data from this shadow register.
- In 16-bit mode, PADC_DATA1 is the least significant byte and PADC_DATA2 is the most significant byte.
- In 24-bit mode, PADC_DATA1 is the least significant byte and PADC_DATA3 is the most significant byte.

7.5.2.19 PADC_CONFIG (M0 address = 0x40000523) (DI page address = 0x2) (DI page offset = 0x23)

Figure 74. PADC_CONFIG

7	6	5	4	3	2	1	0
				PADC_INT_RATE	PADC_DECI_RATE	PADC_EN_24BIT	PADC_EN
				RW	RW	RW	RW
				0	0	0	0

Table 26. PADC_CONFIG Field Descriptions

Bit Definitions	Bit	
PADC_CONFIG	0: PADC_EN	1: PADC decimator is enabled 0: PADC decimator is disabled
	1: PADC_EN_24BIT	1: PADC decimator output is 24 bits 0: PADC decimator output is 16 bits
	2: PADC_DECI_RATE	1: PADC output rate is one sample every 128 µs 0: PADC output rate is one sample every 64 µs
	3: PADC_INT_RATE	1: PADC interrupt occurs every fourth PADC sample 0: PADC interrupt occurs every PADC sample
	4:	
	5:	
	6:	
	7:	

7.5.2.20 TADC_DATA1-3

Figure 75. TADC_DATA1 (M0 address = 0x40000524) (DI page address = 0x2) (DI page offset = 0x24)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Figure 76. TADC_DATA2 (M0 address = 0x40000525) (DI page address = 0x2) (DI page offset = 0x25)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Figure 77. TADC_DATA3 (M0 address = 0x40000526) (DI page address = 0x2) (DI page offset = 0x26)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

- To read TADC_DATA from Digital Interface, the least significant byte/word must be read first. This returns the least significant byte/word. The most significant bytes are latched into a shadow register. Reads to the Digital Interface addresses 0x25, 0x26 return data from this shadow register.
- In 16-bit mode, TADC_DATA1 is the least significant byte and TADC_DATA2 is the most significant byte.
- In 24-bit mode, TADC_DATA1 is the least significant byte and TADC_DATA3 is the most significant byte.

7.5.2.21 TADC_CONFIG (M0 address = 0x40000527) (DI page address = 0x2) (DI page offset = 0x27)

Figure 78. TADC_CONFIG

7	6	5	4	3	2	1	0
				TADC_INT_RATE	TADC_DECI_RATE	TADC_EN_24BIT	TADC_EN
				RW	RW	RW	RW
				0	0	0	0

Table 27. TADC_CONFIG Field Descriptions

Bit Definitions	Bit	
TADC_CONFIG	0: TADC_EN	1: TADC decimator is enabled 0: TADC decimator is disabled
	1: TADC_EN_24BIT	1: TADC decimator output is 24 bits 0: TADC decimator output is 16 bits
	2: TADC_DECI_RATE	1: TADC output rate is one sample every 128 µs 0: TADC output rate is one sample every 64 µs
	3: TADC_INT_RATE	1: TADC interrupt occurs every fourth TADC sample 0: TADC interrupt occurs every TADC sample
	4:	
	5:	
	6:	
	7:	

7.5.2.22 ADC_CFG_1 (M0 address = 0x40000529) (DI page address = 0x2) (DI page offset = 0x29)

Figure 79. ADC_CFG_1

7	6	5	4	3	2	1	0
	Write 0	Write 0	ADC_EN	Write 0	Write 0	RESET_CLK	RESET_MOD
	RW	RW	RW	RW	RW	RW	RW
	0	0	0	0	0	1	1

Table 28. ADC_CFG_1 Field Descriptions

Bit Definitions	Bit	
ADC_CFG_1	0: RESET_MOD	1: PADC and TADC sigma-delta modulators are in reset 0: PADC and TADC sigma-delta modulators are not in reset
	1: RESET_CLK	1: PADC and TADC sigma-delta modulators clocks are reset 0: PADC and TADC sigma-delta modulators clocks are not in reset
	2:	Always write 0
	3:	Always write 0
	4: ADC_EN	1: ADC interfaces and decimator clocks are enabled 0: ADC interfaces and decimator clocks are disabled
	5:	Always write 0
	6:	Always write 0
	7:	

7.5.2.23 DAC_REG

Figure 80. DAC_REG0_1 (M0 address = 0x40000530) (DI page address = 0x2) (DI page offset = 0x30)

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Figure 81. DAC_REG0_2 (M0 address = 0x40000531) (DI page address = 0x2) (DI page offset = 0x31)

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Figure 82. DAC_REG1_1 (M0 address = 0x40000532) (DI page address = 0x2) (DI page offset = 0x32)

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Figure 83. DAC_REG1_2 (M0 address = 0x40000533) (DI page address = 0x2) (DI page offset = 0x33)

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

DAC Register Usage:

- When PWM is not enabled, the DAC_REG0 is driven to the DAC.
- When PWM is enabled, the DAC_REG0 is driven to the DAC when the PWM output is 0.
- When PWM is enabled, the DAC_REG1 is driven to the DAC when the PWM output is 1.

7.5.2.24 DAC_CTRL_STATUS (M0 address = 0x40000538) (DI page address = 0x2) (DI page offset = 0x38)

Figure 84. DAC_CTRL_STATUS

7	6	5	4	3	2	1	0
							DAC_ ENABLE
		R	R			RW	RW
		0	0			0	0

Table 29. DAC_CTRL_STATUS Field Descriptions

Bit Definitions	Bit	
DAC_CTRL_STATUS	0: DAC_ENABLE	1: DAC is enabled to drive DAC GAIN; that is, DAC GAIN output is based on DAC_REG0 value 0: DAC GAIN output is based on the setting of PWM_EN bit in PWM_EN register
	1:	
	3:	
	4:	
	4:	
	5:	
	6:	
	7:	

7.5.2.25 DAC_CONFIG (M0 address = 0x40000539) (DI page address = 0x2) (DI page offset = 0x39)

Figure 85. DAC_CONFIG

7	6	5	4	3	2	1	0
							DAC_ RATIOMETRIC
							RW
							0

Table 30. DAC_CONFIG Field Descriptions

Bit Definitions	Bit	
DAC_CONFIG	0: DAC_RATIOMETRIC	1: DAC is in Ratiometric mode 0: DAC is in Absolute mode
	1:	
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.26 DAC_LPBK_CTRL (M0 address = 0x4000053A) (DI page address = 0x2) (DI page offset = 0x3A)

Figure 86. DAC_LPBK_CTRL

7	6	5	4	3	2	1	0
					EN_LB	LB_AMP_EN	LB_CONNECT
					RW	RW	RW
					0	0	0

Table 31. DAC_LPBK_CTRL Field Descriptions

Bit Definitions	Bit	
DAC_LPBK_CTRL	0: LB_CONNECT	1: Connects the output of the DAC to the input of the loopback amplifier 0: Disconnects the output of the DAC from the input of the loopback amplifier
	1: LB_AMP_EN	1: Enables loopback amplifier 0: Disables loopback amplifier
	2: EN_LB	1: Connects the output of the loopback amplifier to PGA input 0: Disconnects the output of the loopback amplifier from PGA input
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.27 OP_STAGE_CTRL (M0 address = 0x4000053B) (DI page address = 0x2) (DI page offset = 0x3B)

Figure 87. OP_STAGE_CTRL

7	6	5	4	3	2	1	0
		PULLUP_EN	DACCAP_EN	4_20MA_EN	DAC_GAIN[2]	DAC_GAIN[1]	DAC_GAIN[0]
		RW	RW	RW	RW	RW	RW
		0	0	0	1	0	1

Table 32. OP_STAGE_CTRL Field Descriptions

Bit Definitions	Bit				
OP_STAGE_CTRL	0: DAC_GAIN[0]	**DAC_GAIN[2]**	**DAC_GAIN[1]**	**DAC_GAIN[0]**	**Description**
	1: DAC_GAIN[1]	0	0	0	Voltage mode disabled
	2: DAC_GAIN[2]	0	0	1	Gain = 10 V/V
		0	1	0	Gain = 4 V/V
		0	1	1	Reserved
		1	0	0	Gain = 2 V/V
		1	0	1	Reserved
		1	1	0	Gain = 6.67 V/V
		1	1	1	Reserved
	3: 4_20MA_EN	1: Enable 4- to 20-mA current loop (close switch S5 in DAC gain) 0: Disable 4- to 20-mA Current Loop (Open switch S5 in DAC gain)			
	4: DACCAP_EN	1: Enable DACCAP capacitor (close switch S4 in DAC gain) 0: Disable DACCAP capacitor (open switch S4 in DAC gain)			
	5: PULLUP_EN	1: Enable pullup at the input of DAC gain (close switch S8 in DAC gain) 0: Disable pullup at the input of DAC gain (open switch S8 in DAC gain)			
	6:				
	7:				

7.5.2.28 AFE_CFG (M0 address = 0x400004F4) (DI page address = 0x0) (DI page offset = 0xF4)

Figure 88. AFE_CFG

7	6	5	4	3	2	1	0
Write 0	Write 0	PGAIN_OPEN	Write 0	Write 0	Write 0	Write 0	Write 0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Table 33. AFE_CFG Field Descriptions

Bit Definitions	Bit	
AFE_CFG	0:	
	1:	
	2:	
	3:	
	4:	
	5: PGAIN_OPEN	0: PGAIN is disconnected from VINPP/VINPN pins. 1: PGAIN is connected to VINPP/VINPN pins.
	6:	
	7:	

7.5.2.29 AFEDIAG_CFG (M0 address = 0x40000545) (DI page address = 0x2) (DI page offset = 0x45)

Figure 89. AFEDIAG_CFG

7	6	5	4	3	2	1	0
	DIS_R_TEMP	DIS_R_SD	FAULT_THRS[2]	FAULT_THRS[1]	FAULT_THRS[0]	DIS_R2M	DIS_R1M
	RW	RW	RW	RW	RW	RW	RW
	0	0	0	0	0	0	0

Table 34. AFEDIAG_CFG Field Descriptions

Bit Definitions	Bit						
AFEDIAG_CFG	0: DIS_R1M	**DIS_R2M**				**DIS_R1M**	**Pulldown Resistor Value**
	1: DIS_R2M	0				0	4 MΩ
		1				0	3 MΩ
		0				1	2 MΩ
		1				1	1 MΩ
	2: FAULT_THRS[0]	**VBRDG**	**FAULT_THRS[2]**	**FAULT_THRS[1]**	**FAULT_THRS[0]**	**VINP_UV Threshold**	**VINP_OV Threshold**
	3: FAULT_THRS[1]	2.5 V	0	0	0	7.5% of Programmed VBRDG	72.5% of programmed VBRDG
	4: FAULT_THRS[2]		0	0	1	10% of programmed VBRDG	70% if programmed VBRDG
			0	1	0	15% of programmed VBRDG	65% of programmed VBRDG
		2 V	0	1	1	10% of programmed VBRDG	90% of programmed VBRDG
			1	0	0	12.5% of programmed VBRDG	87.5% of programmed VBRDG
			1	0	1	17.5% of programmed VBRDG	82.5% of programmed VBRDG
		1.25 V	1	1	0	17.5% of programmed VBRDG	100% of programmed VBRDG
			1	1	1	22.5% of programmed VBRDG	95% of programmed VBRDG
	5: DIS_R_SD	1: Disables pulldowns used for open/short diagnostics on VINPP/VINPN pins. 0: Enables pulldowns used for open/short diagnostics on VINPP/VINPN pins.					
	6: DIS_R_TEMP	1: Disables pullups used for open/short diagnostics on VINTP/VINTN pins. 0: Enables pullups used for open/short diagnostics on VINTP/VINTN pins.					
	7:						

7.5.2.30 BRDG_CTRL (M0 address = 0x40000546) (DI page address = 0x2) (DI page offset = 0x46)

Figure 90. BRDG_CTRL

7	6	5	4	3	2	1	0
					VBRDG_CTRL[1]	VBRDG_CTRL[0]	BRDG_EN
					RW	RW	RW
					0	0	0

Table 35. BRDG_CTRL Field Descriptions

Bit Definitions	Bit			
BRDG_CTRL	0: BRDG_EN	1: Bridge supply (VBRDGP-VBRDGN) is enabled 0: Bridge supply (VBRDGP-VBRDGN) is disabled		
	1: VBRDG_CTRL[0] 2: VBRDG_CTRL[1]	**VBRDG_CTRL[1]**	**VBRDG_CTRL[0]**	**Bridge Supply Voltage**
		0	0	2.5V
		0	1	2.0V
		1	0	1.25V
		1	1	1.25V
	3:			
	4:			
	5:			
	6:			
	7:			

7.5.2.31 P_GAIN_SELECT (M0 address = 0x40000547) (DI page address = 0x2) (DI page offset = 0x47)

Figure 91. P_GAIN_SELECT

7	6	5	4	3	2	1	0
P_INV			P_GAIN[4]	P_GAIN[3]	P_GAIN[2]	P_GAIN[1]	P_GAIN[0]
RW			RW	RW	RW	RW	RW
0			0	0	0	0	0

Table 36. P_GAIN_SELECT Field Descriptions

Bit Definitions	Bit	
P_GAIN_SELECT	0: P_GAIN[0] 1: P_GAIN[1] 2: P_GAIN[2] 3: P_GAIN[3] 4: P_GAIN[4]	See electrical parameters for gain selectors
	5:	
	6:	
	7: P_INV	1: Inverts the output of the PGAIN output 0: No inversion

7.5.2.32 T_GAIN_SELECT (M0 address = 0x40000548) (DI page address = 0x2) (DI page offset = 0x48)

Figure 92. T_GAIN_SELECT

7	6	5	4	3	2	1	0
T_INV						T_GAIN[1]	T_GAIN[0]
RW						RW	RW
0						0	0

Table 37. T_GAIN_SELECT Field Descriptions

Bit Definitions	Bit	
T_GAIN_SELECT	0: T_GAIN[0] 1: T_GAIN[1]	See electrical parameters for gain selectors
	2:	
	3:	
	4:	
	5:	
	6:	
	7: T_INV	1: Inverts the output of the T GAIN output 0: No inversion

7.5.2.33 TEMP_CTRL (M0 address = 0x4000054C) (DI page address = 0x2) (DI page offset = 0x4C)

Figure 93. TEMP_CTRL

7	6	5	4	3	2	1	0
	ITEMP_CTRL[2]	ITEMP_CTRL[1]	ITEMP_CTRL[0]	TEMP_MUX_CTRL[3]	TEMP_MUX_CTRL[2]	TEMP_MUX_CTRL[1]	TEMP_MUX_CTRL[0]
	RW	RW	RW	RW	RW	RW	RW
	1	0	0	0	0	0	0

Table 38. TEMP_CTRL Field Descriptions

Bit Definitions	Bit					
TEMP_CTRL	0: TEMP_MUX_CTRL[0]	**TEMP_MUX_CTRL[3]**	**TEMP_MUX_CTRL[2]**	**TEMP_MUX_CTRL[1]**	**TEMP_MUX_CTRL[0]**	**Description**
	1: TEMP_MUX_CTRL[1]	0	0	0	0	VINTP-VINTN
	2: TEMP_MUX_CTRL[2]	0	0	0	1	VEXTP-VEXTN
	3: TEMP_MUX_CTRL[3]	0	0	1	1	VTEMP_INT-GND (Internal Temperature Sensor)
	4: ITEMP_CTRL[0]	**ITEMP_CTRL[2]**		**ITEMP_CTRL[1]**	**ITEMP_CTRL[0]**	**Description**
	5: ITEMP_CTRL[1]	0		0	0	25 µA
	6: ITEMP_CTRL[2]	0		0	1	50 µA
		0		1	0	100 µA
		0		1	1	500 µA
		1		X	X	OFF
	7:					

7.5.2.34 ALPWR (M0 address = 0x40000550) (DI page address = 0x2) (DI page offset = 0x50)

Figure 94. ALPWR

7	6	5	4	3	2	1	0
			GATE_CTRL_SD	Write 0	ADC_EN_VREF	Write 0	SD
			RW	RW	RW	RW	RW
			0	0	0	0	1

Table 39. ALPWR Field Descriptions

Bit Definitions	Bit	
ALPWR	0: SD	1:Shuts down pressure PGA, temperature PGA, and fault detection 0: Powers up pressure PGA, temperature PGA, and fault detection
	1:	
	2: ADC_EN_VREF	1: Enables VREF 0: Disables VREF
	3:	
	4: GATE_CTRL_SD	1: Gate drive disabled 0: Gate drive enabled
	5:	
	6:	
	7:	

7.5.2.35 DLPWR (M0 address = 0x40000554) (DI page address = 0x2) (DI page offset = 0x54)

Figure 95. DLPWR

7	6	5	4	3	2	1	0
							OWI_CLK_EN
							RW
							0

Table 40. DLPWR Field Descriptions

Bit Definitions	Bit	
DLPWR	0: OWI_CLK_EN	1: Enables OWI clock to the OWI controller 0: Disables OWI clock to the OWI controller
	1:	
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.36 PSMON1 (M0 address = 0x40000558) (DI page address = 0x2) (DI page offset = 0x58)

Figure 96. PSMON1

7	6	5	4	3	2	1	0
OSC_VDD_UV	OSC_VDD_OV	AVDD_UV	AVDD_OV	REF_UV	REF_OV	VBRG_UV	VBRG_OV
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Table 41. PSMON1 Field Descriptions

Bit Definitions	Bit		
PSMON1	0: VBRG_OV	**Read:** 1: VBRG is overvoltage. 0: VBRG is not overvoltage.	**Write:** 1: Clears VBRG_OV bit 0: No action
	1: VBRG_UV	**Read:** 1: VBRG is undervoltage. 0: VBRG is not undervoltage.	**Write:** 1: Clears VBRG_UV bit 0: No action
	2: REF_OV	**Read:** 1: Reference is overvoltage. 0: Reference is not overvoltage.	**Write:** 1: Clears REF_OV bit 0: No action
	3: REF_UV	**Read:** 1: Reference is undervoltage. 0: Reference is not undervoltage.	**Write:** 1: Clears REF_UV bit 0: No action
	4: AVDD_OV	**Read:** 1: AVDD is overvoltage. 0: AVDD is not overvoltage.	**Write:** 1: Clears AVDD_OV bit 0: No action
	5: AVDD_UV	**Read:** 1: AVDD is undervoltage. 0: AVDD is not undervoltage.	**Write:** 1: Clears AVDD_UV bit 0: No action
	6: OSC_VDD_OV	**Read:** 1: OSC_VDD_OV is overvoltage. 0: OSC_VDD_OV is not overvoltage.	**Write:** 1: Clears OSC_VDD_OV bit 0: No action
	7: OSC_VDD_UV	**Read:** 1: OSC_VDD_UV is undervoltage. 0: OSC_VDD_UV is not undervoltage.	**Write:** 1: Clears OSC_VDD_UV bit 0: No action

7.5.2.37 PSMON2 (M0 address = 0x40000559) (DI page address = 0x2) (DI page offset = 0x59)

Figure 97. PSMON2

7	6	5	4	3	2	1	0
						DVDD_UV	DVDD_OV
						RW	RW
						0	0

Table 42. PSMON2 Field Descriptions

Bit Definitions	Bit		
PSMON2	0: DVDD_OV	**Read:** 1: DVDD is overvoltage. 0: DVDD is not overvoltage.	**Write:** 1: Clears DVDD_OV bit 0: No action
	1: DVDD_UV	**Read:** 1: DVDD is undervoltage. 0: DVDD is not undervoltage.	**Write:** 1: Clears DVDD_UV bit 0: No action
	2:		
	3:		
	4:		
	5:		
	6:		
	7:		

7.5.2.38 AFEDIAG (M0 address = 0x4000055A) (DI page address = 0x2) (DI page offset = 0x5A)

Figure 98. AFEDIAG

7	6	5	4	3	2	1	0
TGAIN_UV	TGAIN_OV	PGAIN_UV	PGAIN_OV		VINT_OV	VINP_UV	VINP_OV
RW	RW	RW	RW		RW	RW	RW
0	0	0	0		0	0	0

Table 43. AFEDIAG Field Descriptions

Bit Definitions	Bit		
AFEDIAG	0: VINP_OV	**Read:** 1: Indicates overvoltage at input pins of P gain 0: Indicates no overvoltage at input pins of P gain	**Write:** 1: Clears VINP_OV bit 0: No action
	1: VINP_UV	**Read:** 1: Indicates undervoltage at input pins of P gain 0: Indicates no undervoltage at input pins of P gain	**Write:** 1: Clears VINP_UV bit 0: No action
	2: VINT_OV	**Read:** 1: Indicates overvoltage at input pins of T gain 0: Indicates no overvoltage at input pins of T gain	**Write:** 1: Clears VINT_OV bit 0: No action
	3:		
	4: PGAIN_OV	**Read:** 1: Indicates overvoltage at output pins of P gain 0: Indicates no overvoltage at output pins of P gain	**Write:** 1: Clears PGAIN_OV bit 0: No action
	5: PGAIN_UV	**Read:** 1: Indicates undervoltage at output pins of P gain 0: Indicates no undervoltage at output pins of P gain	**Write:** 1: Clears PGAIN_UV bit 0: No action
	6: TGAIN_OV	**Read:** 1: Indicates overvoltage at output pins of T gain 0: Indicates no overvoltage at output pins of T gain	**Write:** 1: Clears TGAIN_OV bit 0: No action
	7: TGAIN_UV	**Read:** 1: Indicates undervoltage at output pins of T gain 0: Indicates no undervoltage at output pins of T gain **NOTE** TGAIN_UV flag is ON all the time if TGAIN is configured for single-ended mode because one of the terminals is always at ground potential.	**Write:** 1: Clears TGAIN_UV bit 0: No action

7.5.2.39 TOPDIG_MUX_SEL (M0 address = 0x40000560) (DI page address = 0x2) (DI page offset = 0x60)

Figure 99. TOPDIG_MUX_SEL

7	6	5	4	3	2	1	0
		TOPDIG[5]	TOPDIG[4]	TOPDIG[3]	TOPDIG[2]	TOPDIG[1]	TOPDIG[0]
		RW	RW	RW	RW	RW	RW
		0	0	0	0	0	0

Table 44. TOPDIG_MUX_SEL Field Descriptions

Bit Definitions	Bit	
TOPDIG_MUX_SEL	0: TOPDIG[0]	See next table or encoding
	1: TOPDIG[1]	
	2: TOPDIG[2]	
	3: TOPDIG[3]	
	4: TOPDIG[4]	
	5: TOPDIG[5]	
	6:	
	7:	

Table 45. TOPDIG[5:0] and TONDIG[5:0]

TOPDIG[5:0]/TONDIG[5:0]	INTERNAL SIGNAL
0x01	VBRDG_OV
0x02	VBRDG_UV
0x03	REF_OV
0x04	REF_UV
0x05	AVDD_OV
0x06	AVDD_UV
0x07	OSC_VDD_OV
0x08	OSC_VDD_UV
0x09	BRDG_OV
0x0A	BRDG_UV
0x0B	TEMP_OV
0x0C	TEMP_UV
0x0D	PGAIN_OV
0x0E	PGAIN_UV
0x0F	TGAIN_OV
0x10	TGAIN_UV
0x11	OWI_ERROR_STATUS_LO[0]
0x12	OWI_ERROR_STATUS_LO[1]
0x13	OWI_ERROR_STATUS_LO[2]
0x14	OWI_ERROR_STATUS_LO[3]
0x15	OWI_ERROR_STATUS_LO[4]
0x16	OWI_ERROR_STATUS_LO[5]
0x17	OWI_ERROR_STATUS_LO[6]
0x18	OWI_ERROR_STATUS_LO[6]
0x19	OWI_ERROR_STATUS_HI[0]
0x1A	OWI_ERROR_STATUS_HI[1]
0x1B	OWI receive data
0x1E	OWI transmit data
0x1F	PWM output

Table 45. TOPDIG[5:0] and TONDIG[5:0] (continued)

TOPDIG[5:0]/TONDIG[5:0]	INTERNAL SIGNAL
0x20	PADC INTERRUPT
0x21	TADC INTERRUPT
0x22	OWI ACTIVATION INTERRUPT
0x23	OWI COMBUF INTERRUPT
0x24	UART INTERRUPT
0x29	OSC4MHz
0x2A	Cortex M0 clock
0x2B	ADC clock
0x2C	PADC decimator clock
0x2D	TADC decimator clock
0x2F	DATASRAM_MBIST_DONE
0x30	DATASRAM_MBIST_FAIL
0x31	DEVSRAM_MBIST_DONE
0x32	DEVSRAM_MBIST_FAIL
0x33	DVDD_OV
0x34	DVDD_UV

7.5.2.40 TONDIG_MUX_SEL (M0 address = 0x40000561) (DI page address = 0x2) (DI page offset = 0x61)

Figure 100. TONDIG_MUX_SEL

7	6	5	4	3	2	1	0
		TONDIG[5]	TONDIG[4]	TONDIG[3]	TONDIG[2]	TONDIG[1]	TONDIG[0]
		RW	RW	RW	RW	RW	RW
		0	0	0	0	0	0

Table 46. TONDIG_MUX_SEL Field Descriptions

Bit Definitions	Bit	
TONDIG_MUX_SEL	0: TONDIG[0]	See table in TOPDIG_MUX_SEL register description
	1: TONDIG[1]	
	2: TONDIG[2]	
	3: TONDIG[3]	
	4: TONDIG[4]	
	5: TONDIG[5]	
	6:	
	7:	

7.5.2.41 AMUX_ACT (M0 address = 0x40000564) (DI page address = 0x2) (DI page offset = 0x64)

Figure 101. AMUX_ACT

7	6	5	4	3	2	1	0
						TOUT_MUX_SEL	TIN_MUX_EN
						RW	RW
						0	0

Table 47. AMUX_ACT Field Descriptions

Bit Definitions	Bit	Description
AMUX_ACT	0: TIN_MUX_EN	1: Enables the analog input test MUX 0: Disables the analog input test MUX
	1: TOUT_MUX_SEL	1: Enables Internal TOP Test Signal to TOP_TON output 0: Enables Internal TON Test Signal to TOP_TON output
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.42 AMUX_TIN_MUX_CTRL (M0 address = 0x40000565) (DI page address = 0x2) (DI page offset = 0x65)

Figure 102. AMUX_TIN_MUX_CTRL

7	6	5	4	3	2	1	0
					AMUX_TIN_MUX_CTRL[2]	AMUX_TIN_MUX_CTRL[1]	AMUX_TIN_MUX_CTRL[0]
					RW	RW	RW
					0	0	0

Table 48. AMUX_TIN_MUX_CTRL Field Descriptions

Bit Definitions	Bit	
AMUX_TIN_MUX_CTRL	0: AMUX_TIN_MUX_CTRL[0]	See next table for encoding
	1: AMUX_TIN_MUX_CTRL[1]	
	2: AMUX_TIN_MUX_CTRL[2]	
	3:	
	4:	
	5:	
	6:	
	7:	

Table 49. AMUX_TIN_MUX_CTRL[2:0]

AMUX_TIN_MUX_CTRL[2:0]	INTERNAL SIGNAL ON TIP	INTERNAL SIGNAL ON TIN
0x00	DAC buffer for ratiometric output	External test clock
0x01	ADC OTA common mode buffer	ADC reference common mode buffer
0x02	Output buffer	None
0x03	Test MUX oscillator	None
0x04	Loop back amplifier	None
0x05	Pressure ADC input 1	Pressure ADC input 2
0x06	Bridge buffer	ADC reference buffer
0x07	Temperature ADC input 1	Temperature ADC input 2

7.5.2.43 AMUX_TOUT_MUX_CTRL (M0 address = 0x40000566) (DI page address = 0x2) (DI page offset = 0x66)

Figure 103. AMUX_TOUT_MUX_CTRL

7	6	5	4	3	2	1	0
				AMUX_TOUT_MUX_CTRL[3]	AMUX_TOUT_MUX_CTRL[2]	AMUX_TOUT_MUX_CTRL[1]	AMUX_TOUT_MUX_CTRL[0]
				RW	RW	RW	RW
				0	0	0	0

Table 50. AMUX_TOUT_MUX_CTRL Field Descriptions

Bit Definitions	Bit	
AMUX_TOUT_MUX_CTRL	0: AMUX_TOUT_MUX_CTRL[0]	See next table for encoding
	1: AMUX_TOUT_MUX_CTRL[1]	
	2: AMUX_TOUT_MUX_CTRL[2]	
	3: AMUX_TOUT_MUX_CTRL[3]	
	4:	
	5:	
	6:	
	7:	

Table 51. AMUX_TOUT_MUX_CTRL[0:3]

AMUX_TOUT_MUX_CTRL[0:3]	Internal TOP Test Signal	Internal TON Test Signal
0x00	Bridge voltage	ADC reference
0x01	Temperature PGA output 1	Temperature PGA output 2
0x02	Spare	Oscillator
0x03	Inaccurate reference	AVSS
0x04	DAC buffer for ratiometric output	2.5-V reference
0x05	DAC output	Reference GND
0x06	Reference current to trim V-I	AVSS
0x07	AVSS	AVSS
0x08	ADC OTA common mode	ACD reference common mode
0x09	Loop back output P	Loop back output N
0x0A	Pressure PGA output 1	Pressure PGA output 2
0x0B	AVSS	AVSS
0x0C	AVDD	Oscillator VDD
0x0D	TIP	TIN
0x0E	Pressure PGA VCM	Temperature PGA VCM
0x0F	AVSS	AVSS

7.5.2.44 AMUX_CTRL (M0 address = 0x40000567) (DI page address = 0x2) (DI page offset = 0x67)

Figure 104. AMUX_CTRL

7	6	5	4	3	2	1	0
				TSEM_N	TEST_ MUX_T_ EN	TEST_ MUX_P_ EN	TEST_ MUX_DAC_ EN
				RW	RW	RW	RW
				0	0	0	0

Table 52. AMUX_CTRL Field Descriptions

Bit Definitions	Bit	
AMUX_CTRL	0: TEST_MUX_DAC_EN	1: Connects DAC output to DAC gain 0: Connects DAC output to TOP/TON pins
	1: TEST_MUX_P_EN	1: Connects PGAIN output to PADC 0: Connects PGAIN output to TOP/TON pins
	2: TEST_MUX_T_EN	1: Connects TGAIN output to TADC 0: Connects TGAIN output to TOP/TON pins
	3:TSEM_N	1: Output of temperature MUX is differential 0: Output of temperature MUX is single ended
	4:	
	5:	
	5:	
	6:	
	7:	

7.5.2.45 TRACE_FIFO_CTRL_STAT (M0 address = 0x40000570) (DI page address = 0x2) (DI page offset = 0x70)

Figure 105. TRACE_FIFO_CTRL_STAT

7	6	5	4	3	2	1	0
	TRACE_ FIFO_ FULL	TRACE_ FIFO_ HALF_ FULL	TRACE_ FIFO_ EMPTY			TRACE_ SOURCE	TRACE_ FIFO_ ENABLE
	R	R	R			RW	RW
	0	0	1			0	0

Table 53. TRACE_FIFO_CTRL_STAT Field Descriptions

Bit Definitions	Bit	Description
TRACE_FIFO_CTRL_STAT	0: TRACE_FIFO_ENABLE	1: Enables trace FIFO 0: Disables trace FIFO
	1: TRACE_SOURCE	1: TADC 0: PADC
	2:	
	3:	
	4: TRACE_FIFO_EMPTY	1: Trace FIFO is empty 0: Trace FIFO is not empty
	5: TRACE_FIFO_HALF_FULL	1: Trace FIFO is half full 0: Trace FIFO is less than half full
	6: TRACE_FIFO_FULL	1: Trace FIFO is full 0: Trace FIFO is not full
	7:	

7.5.2.46 REVISION_ID1 (M0 address = 0x40000400) (DI page address = 0x0) (DI page offset = 0x00)

Figure 106. REVISION_ID1

7	6	5	4	3	2	1	0
OPT_ID[2]	OPT_ID[1]	OPT_ID[0]		REV_ID[3]	REV_ID[2]	REV_ID[1]	REV_ID[0]
R	R	R		R	R	R	R
Encoded				Encoded			

Table 54. REVISION_ID1 Field Descriptions

Bit Definitions	Bit	Description
REVISION_ID1	0: REV_ID[0]	Device Revision
	1: REV_ID[1]	
	2: REV_ID[2]	
	3: REV_ID[3]	
	4:	
	5: OPT_ID[0]	Device Option
	6: OPT_ID[1]	
	7: OPT_ID[2]	

7.5.2.47 REVISION_ID2 (M0 address = 0x40000401) (DI page address = 0x0) (DI page offset = 0x01)

Figure 107. REVISION_ID2

7	6	5	4	3	2	1	0
				DL_ID[3]	DL_ID[2]	DL_ID[1]	DL_ID[0]
				R	R	R	R
				Encoded			

Table 55. REVISION_ID2 Field Descriptions

Bit Definitions	Bit	Description
REVISION_ID2	0: DL_ID[0]	Digital Logic Revision
	1: DL_ID[1]	
	2: DL_ID[2]	
	3: DL_ID[3]	
	4:	
	5:	
	6:	
	7:	

7.5.2.48 COM_MCU_TO_DIF_B1 (M0 address = 0x40000404) (DI page address = 0x0) (DI page offset = 0x04)

Figure 108. COM_MCU_TO_DIF_B1 Field Descriptions

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Bits 7:0 of the data written by the microcontroller for communication with the digital interface. This register can be written only by the microcontroller.

7.5.2.49 COM_MCU_TO_DIF_B2 (M0 address = 0x40000405) (DI page address = 0x0) (DI page offset = 0x05)

Figure 109. COM_MCU_TO_DIF_B2

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Bits 15:8 of the data written by the microcontroller for communication with the digital interface. This register can be written only by the microcontroller.

7.5.2.50 COM_TX_STATUS (M0 address = 0x40000406) (DI page address = 0x0) (DI page offset = 0x06)

Figure 110. COM_TX_STATUS

7	6	5	4	3	2	1	0
							COM_TXRDY
							RW
							0

Table 56. COM_TX_STATUS Field Descriptions

Bit Definitions	Bit	Description	
COM_TX_STATUS	0: COM_TXRDY	**Read** 1: COM_MCU_TO_DIF_B2 has been written by the microcontroller 0: COM_MCU_TO_DIF_B2 has not been written by the microcontroller	**Write** 1: COM_TXRDY is cleared 0: No action
	1:		
	2:		
	3:		
	4:		
	5:		
	6:		
	7:		

7.5.2.51 COM_DIF_TO_MCU_B1 (M0 address = 0x40000408) (DI page address = 0x0) (DI page offset = 0x08)

Figure 111. COM_DIF_TO_MCU_B1

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Bit 7:0 of the data written by the digital interface for communication with the microcontroller. This register can be written only by the digital interface.

7.5.2.52 COM_DIF_TO_MCU_B2 (M0 address = 0x40000409) (DI page address = 0x0) (DI page offset = 0x09)

Figure 112. COM_DIF_TO_MCU_B1

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Bits 15:8 of the data written by the digital interface for communication with the microcontroller. This register can be written only by the digital interface.

7.5.2.53 COM_RX_STATUS (M0 address = 0x4000040A) (DI page address = 0x0) (DI page offset = 0x0A)

Figure 113. COM_RX_STATUS

7	6	5	4	3	2	1	0
							COM_RXRDY
							RW
							0

Table 57. COM_RX_STATUS Field Descriptions

Bit Definitions	Bit	Description	
COM_RX_STATUS	0: COM_RXRDY	**Read** 1: COM_DIF_TO_MCU_B2 has been written by the digital interface 0: COM_DIF_TO_MCU_B2 has not been written by the digital interface	**Write** 1: COM_RXRDY is cleared 0: No action
	1:		
	2:		
	3:		
	4:		
	5:		
	6:		
	7:		

7.5.2.54 COM_RX_INT_ENABLE (M0 address = 0x4000040B) (DI page address = 0x0) (DI page offset = 0x0B)

Figure 114. COM_RX_INT_ENABLE

7	6	5	4	3	2	1	0
							COM_RXRDY_ INT_EN
							RW
							0

Table 58. COM_RX_INT_ENABLE Field Descriptions

Bit Definitions	Bit	Description
COM_RX_INT_ENABLE	0: COM_RXRDY_ INT_EN	1: COM_RXRDY interrupt is enabled and propagated to the microcontroller 0: COM_RXRDY interrupt is disabled and not propagated to the microcontroller
	1:	
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.55 MICRO_INTERFACE_CONTROL (M0 address = 0x4000040C) (DI page address = 0x0) (DI page offset = 0x0C)

Figure 115. MICRO_INTERFACE_CONTROL

7	6	5	4	3	2	1	0
					DEBUG_LOCK	MICRO_RESET	IF_SEL
					RW	RW	RW
					0	0	0

Table 59. MICRO_INTERFACE_CONTROL Field Descriptions

Bit Definitions	Bit	Description
MICRO_INTERFACE_CONTROL	0: IF_SEL	1: Digital interface accesses the PGA900 resources 0: Microcontroller accesses the PGA900 resources
	1: MICRO_RESET	1: Microcontroller reset 0: Microcontroller running
	2: DEBUG_LOCK	1: Debugger cannot access PGA900 resources 0: Debugger can access the PGA900 resources if IF_SEL is 0
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.56 SECLOCK (M0 address = 0x4000040D) (DI page address = 0x0) (DI page offset = 0x0D)

Figure 116. SECLOCK

7	6	5	4	3	2	1	0
							SECLOCK
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

- Write pattern 0xAA to enable OTP security
- Write pattern 0x00 to disable OTP security

Table 60. SECLOCK Field Descriptions

Bit Definitions	Bit	Description
SECLOCK	0: SECLOCK	**Read** 1: OTP security is enabled 0: OTP security is disabled
	1:	
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.57 UART_CFG (M0 address = 0x40000200) (DI page address = 0x7) (DI page offset = 0x00)

Figure 117. UART_CFG

7	6	5	4	3	2	1	0
					TWO_STOP_BITS	PARITY	PARITY_EN
					RW	RW	RW
					0	0	0

Table 61. UART_CFG Field Descriptions

Bit Definitions	Bit	Description
UART_CFG	0: PARITY_EN	1: Parity is enabled 0: Parity is disabled
	1: PARITY	1: Parity is EVEN 0: Parity is ODD
	2: TWO_STOP_BITS	1: Two stop bits are transmitted 0: One stop bit is transmitted
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.58 UART_EN (M0 address = 0x40000201) (DI page address = 0x7) (DI page offset = 0x01)

Figure 118. UART_EN

7	6	5	4	3	2	1	0
							UART_EN
							RW
							0

Table 62. UART_EN Field Descriptions

Bit Definitions	Bit	Description
UART_EN	0: UART_EN	1: UART is enabled 0: UART is disabled
	1:	
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.59 BAUD_RATE_LO (M0 address = 0x40000202) (DI page address = 0x7) (DI page offset = 0x02)

Figure 119. BAUD_RATE_LO

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

7.5.2.60 BAUD_RATE_HI (M0 address = 0x40000203) (DI page address = 0x7) (DI page offset = 0x03)

Figure 120. BAUD_RATE_HI

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

7.5.2.61 UART_LINE_STATUS (M0 address = 0x40000204) (DI page address = 0x7) (DI page offset = 0x04)

Figure 121. UART_LINE_STATUS

7	6	5	4	3	2	1	0
			TX_COMPLETE	RX_READY	FRAMING_ERROR	PARITY_ERROR	OVERRUN_ERROR
			R	R	R	R	RW
			0	0	0	0	0

Table 63. UART_LINE_STATUS Field Descriptions

Bit Definitions	Bit	Description
UART_EN	0: OVERRUN_ERROR	1: Receive buffer was not read before it was overwritten by another character received The bit is cleared when the UART_LINE_STATUS register is read 0: No error UART_EN OVERRUN_ERROR cleared when the UART_LINE_STATUS register is read after the UART_RX_BUF is read.
	1: PARITY_ERROR	1: Receive data has parity error 0: No error PARITY_ERROR is cleared when the UART_LINE_STATUS register is read after the UART_RX_BUF is read
	2: FRAMING_ERROR	1: Receive data has framing error (stop bits were not received as expected) 0: No error FRAMING_ERROR is cleared when the UART_LINE_STATUS register is read after the UART_RX_BUF is read
	3: RX_READY	1: Receive buffer has data 0: Receive buffer is empty RX_READY is cleared when the UART_RX_BUF is read
	4: TX_COMPLETE	1: Data in the transmit buffer has been transmitted 0: Data in the transmit buffer has not been transmitted yet TX_COMPLETE is cleared when the UART_TX_BUF is written
	5:	
	6:	
	7:	

7.5.2.62 UART_INTERRUPT_STATUS (M0 address = 0x40000208) (DI page address = 0x7) (DI page offset = 0x08)

Figure 122. UART_INTERRUPT_STATUS

7	6	5	4	3	2	1	0
						UART_ TXCOMPLETE _I	UART_ RXRDY_I
						R	R
						0	0

Table 64. UART_INTERRUPT_STATUS Field Descriptions

Bit Definitions	Bit	Description	
UART_INTERRUPT_STATUS	0: UART_ RXRDY_I	**Read** 1: UART_RX_BUF has data ready 0: UART_RX_BUF does not have valid data	**Write** 1: UART_RXRDY_I is cleared 0: No effect
	1: UART_ TXCOMPLETE_I	**Read** 1: UART_TX_BUF is empty 0: UART_TX_BUF is not empty	**Write** 1: UART_TXRCOMPLTE_I is cleared 0: No effect
	2:		
	3:		
	4:		
	5:		
	6:		
	7:		

7.5.2.63 UART_INTERRUPT_ENABLE (M0 address = 0x4000020A) (DI page address = 0x7) (DI page offset = 0x0A)

Figure 123. UART_INTERRUPT_ENABLE

7	6	5	4	3	2	1	0
						UART_ TXCOMPLET_ INT_EN	UART_ RXRDY_ INT_EN
						RW	RW
						0	0

Table 65. UART_INTERRUPT_ENABLE Field Descriptions

Bit Definitions	Bit	Description
UART_INTERRUPT_ENABLE	0: UART_RXRDY_INT_EN	1: RX ready interrupt is enabled 0: RX ready interrupt is disabled
	1: UART_TXCOMPLET_INT_EN	1: TX ready interrupt is enabled 0: TX ready interrupt is disabled
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.64 UART_RX_BUF (M0 address = 0x4000020C) (DI page address = 0x7) (DI page offset = 0x0C)

Figure 124. UART_RX_BUF

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

The receive buffer contains the character received by the UART.

7.5.2.65 UART_TX_BUF (M0 address = 0x4000020E) (DI page address = 0x7) (DI page offset = 0x0E)

Figure 125. UART_TX_BUF

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Data written to this register is transmitted by the UART.

7.5.2.66 PWM_ON_TIME1-2

Figure 126. PWM_ON_TIME1 (M0 address = 0x40000210) (DI page address = 0x7) (DI page offset = 0x10)

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Figure 127. PWM_ON_TIME2 (M0 address = 0x40000211) (DI page address = 0x7) (DI page offset = 0x11)

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

- PWM_ON_TIME is 16 bits. PWM_ON_TIME1 is least significant byte and PWM_ON_TIME2 is most significant byte.
- The PWM_ON_TIME determines when the PWM output is at 1. The PWM output is high for PWM_ON_TIME × 4 MHZ clock period.

7.5.2.67 PWM_OFF_TIME1-2

Figure 128. PWM_OFF_TIME1 (M0 address = 0x40000212) (DI page address = 0x7) (DI page offset = 0x12)

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Figure 129. PWM_OFF_TIME2 (M0 address = 0x40000213) (DI page address = 0x7) (DI page offset = 0x13)

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

- PWM_OFF_TIME is 16 bits. PWM_OFF_TIME1 is least significant byte and PWM_OFF_TIME2 is most significant byte.
- The PWM_OFF_TIME determines when the PWM output is at 0. The PWM output is high for PWM_OFF_TIME × 4 MHZ clock period.

7.5.2.68 PWM_EN (M0 address = 0x40000214) (DI page address = 0x7) (DI page offset = 0x14)

Figure 130. PWM_EN

7	6	5	4	3	2	1	0
							PWM_EN
							RW
							0

Table 66. PWM_EN Field Descriptions

Bit Definitions	Bit	
PWM_EN	0: PWM_EN	1: PWM is enabled to drive DAC GAIN if DAC_ENABLE is 0; that is, DAC_REG0 and DAC_REG1 are output as DAC GAIN output to generate PWM signal at VOUT pin of device 0: PWM is disabled to drive DAC GAIN; that is, DAC_REG0 are output of DAC GAIN to generate constant voltage at VOUT pin of device
	1:	
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.69 GPIO_INPUT (M0 address = 0x40000218) (DI page address = 0x7) (DI page offset = 0x18)

Figure 131. GPIO_INPUT

7	6	5	4	3	2	1	0
						GPIO2_I	GPIO1_I
						R	R
						X	X

Table 67. GPIO_INPUT Field Descriptions

Bit Definitions	Bit	Description
GPIO_INPUT	0: GPIO1_I	GPIO1 pin state both in INPUT and OUTPUT mode
	1: GPIO2_I	GPIO2 pin state both in INPUT and OUTPUT mode
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.70 GPIO_OUTPUT (M0 address = 0x40000219) (DI page address = 0x7) (DI page offset = 0x19)

Figure 132. GPIO_OUTPUT

7	6	5	4	3	2	1	0
						GPIO2_O	GPIO1_O
						RW	RW
						0	0

Table 68. GPIO_OUTPUT Field Descriptions

Bit Definitions	Bit	Description
GPIO_OUTPUT	0: GPIO1_O	GPIO1 output state
	1: GPIO2_O	GPIO2 output state
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.71 GPIO_DIR (M0 address = 0x4000021A) (DI page address = 0x7) (DI page offset = 0x1A)

Figure 133. GPIO_DIR

7	6	5	4	3	2	1	0
				GPIO2_CFG	GPIO1_CFG	GPIO2_DIR	GPIO1_DIR
				RW	RW	RW	RW
				0	0	1	1

Table 69. GPIO_DIR Field Descriptions

Bit Definitions	Bit	Description
GPIO_DIR	0: GPIO1_DIR	1: GPIO1 is input. 0: GPIO1 is output.
	1: GPIO2_DIR	1: GPIO2 is input. 0: GPIO2 is output.
	2: GPIO1_CFG	1: GPIO1 is open-drain mode in OUTPUT mode. 0: GPIO1 is push-pull mode in OUTPUT mode.
	3: GPIO2_CFG	1: GPIO2 is open-drain mode in OUTPUT mode. 0: GPIO2 is push-pull mode in OUTPUT mode.
	4:	
	5:	
	6:	
	7:	

7.5.2.72 REMAP (M0 address = 0x40000220) (DI page address = 0x7) (DI page offset = 0x20)

Figure 134. REMAP

7	6	5	4	3	2	1	0
							REMAP
							RW
							0

Table 70. REMAP Field Descriptions

Bit Definitions	Bit	Description
REMAP	0: REMAP	1: DEVRAM overlays OTP; that is, DEVRAM is located starting at address 0x0000 0000 0: DEVRAM does not overlay OTP; that is, DEVRAM is located started at address 0x2100 0000
	1:	
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.73 EEPROM_PAGE_ADDRESS (M0 address = 0x40000088) (DI page address = 0x5) (DI page offset = 0x88)

Figure 135. EEPROM_PAGE_ADDRESS

7	6	5	4	3	2	1	0
				ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
				RW	RW	RW	RW
				0	0	0	0

7.5.2.74 EEPROM_CTRL (M0 address = 0x40000089) (DI page address = 0x5) (DI page offset = 0x89)

Figure 136. EEPROM_CTRL

7	6	5	4	3	2	1	0
				FIXED_ ERASE_ PROG_TIME	ERASE_AND _PROGRAM	ERASE	PROGRAM
				RW	RW	RW	RW
				0	0	0	0

Table 71. EEPROM_CTRL Field Descriptions

Bit Definitions	Bit	Description
EEPROM_CTRL	0: PROGRAM	1: Program contents of EEPROM cache into EEPROM memory pointed to by EEPROM_PAGE_ADDRESS 0: No action
	1: ERASE	1: Erase contents of EEPROM memory pointed to by EEPROM_PAGE_ADDRESS 0: No action
	2: ERASE_AND_PROGRAM	1: Erase contents of EEPROM memory pointed to by EEPROM_PAGE_ADDRESS and program of contents of EEPROM cache 0: No action
	3: FIXED_ERASE_PROG_TIME	1: Use fixed 8 ms as the erase/program time 0: Use Variable time <8 ms as the erase/program time. The EEPROM programming logic determines the duration to program the EEPROM memory
	4:	
	5:	
	6:	
	7:	

7.5.2.75 EEPROM_CRC (M0 address = 0x4000008A) (DI page address = 0x5) (DI page offset = 0x8A)

Figure 137. EEPROM_CRC

7	6	5	4	3	2	1	0
							CALCULATE _CRC
							RW
							0

Table 72. EEPROM_CRC Field Descriptions

Bit Definitions	Bit	Description
EEPROM_CRC	0: CALCULATE_CRC	1: Calculate EEPROM CRC 0: No action
	1:	
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.76 EEPROM_STATUS (M0 address = 0x4000008B) (DI page address = 0x5) (DI page offset = 0x8B)

Figure 138. EEPROM_STATUS

7	6	5	4	3	2	1	0
					PROGRAM_IN_PROGRESS	ERASE_IN_PROGRESS	READ_IN_PROGRESS
					R	R	R
					0	0	0

Table 73. EEPROM_STATUS Field Descriptions

Bit Definitions	Bit	Description
EEPROM_STATUS	0: READ_IN_PROGRESS	1: EEPROM read in progress 0: EEPROM read not in progress
	1: ERASE_IN_PROGRESS	1: EEPROM erase in progress 0: EEPROM erase not in progress
	2: PROGRAM_IN_PROGRESS	1: EEPROM program in progress 0: EEPROM program not in progress
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.77 EEPROM_CRC_STATUS (M0 address = 0x4000008C) (DI page address = 0x5) (DI page offset = 0x8C)

Figure 139. EEPROM_CRC_STATUS

7	6	5	4	3	2	1	0
						CRC_GOOD	CRC_CHECK_IN_PROG
						R	R
						0	0

Table 74. EEPROM_CRC_STATUS Field Descriptions

Bit Definitions	Bit	Description
EEPROM_STATUS	0: CRC_CHECK_IN_PROGRESS	1: EEPROM CRC check in progress 0: EEPROM CRC check not in progress
	1: CRC_GOOD	1: EEPROM programmed CRC matches calculated CRC 0: EEPROM programmed CRC does not match calculated CRC
	2:	
	3:	
	4:	
	5:	
	6:	
	7:	

7.5.2.78 EEPROM_CRC_VALUE (M0 address = 0x4000008D) (DI page address = 0x5) (DI page offset = 0x8D)

Figure 140. EEPROM_CRC_VALUE

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
1	1	1	1	1	1	1	1

EEPROM CRC value must be located in the last byte of the EEPROM

7.5.3 Interrupt Sources

Table 75. Interrupt Sources

Interrupt Source	IRQ Number
M0 SYSTICK	Standard cortex M0 interrupt
P ADC	0
T ADC	1
OWI activation	2
COMBUF RX	3
UART TX complete/RX	4

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The PGA900 can be used in a variety of applications to measure pressure and temperature. Depending on the application, the device can be configured in different modes as illustrated in the following section.

8.2 Typical Applications

8.2.1 4- to 20-mA Output With Internal Sense Resistor

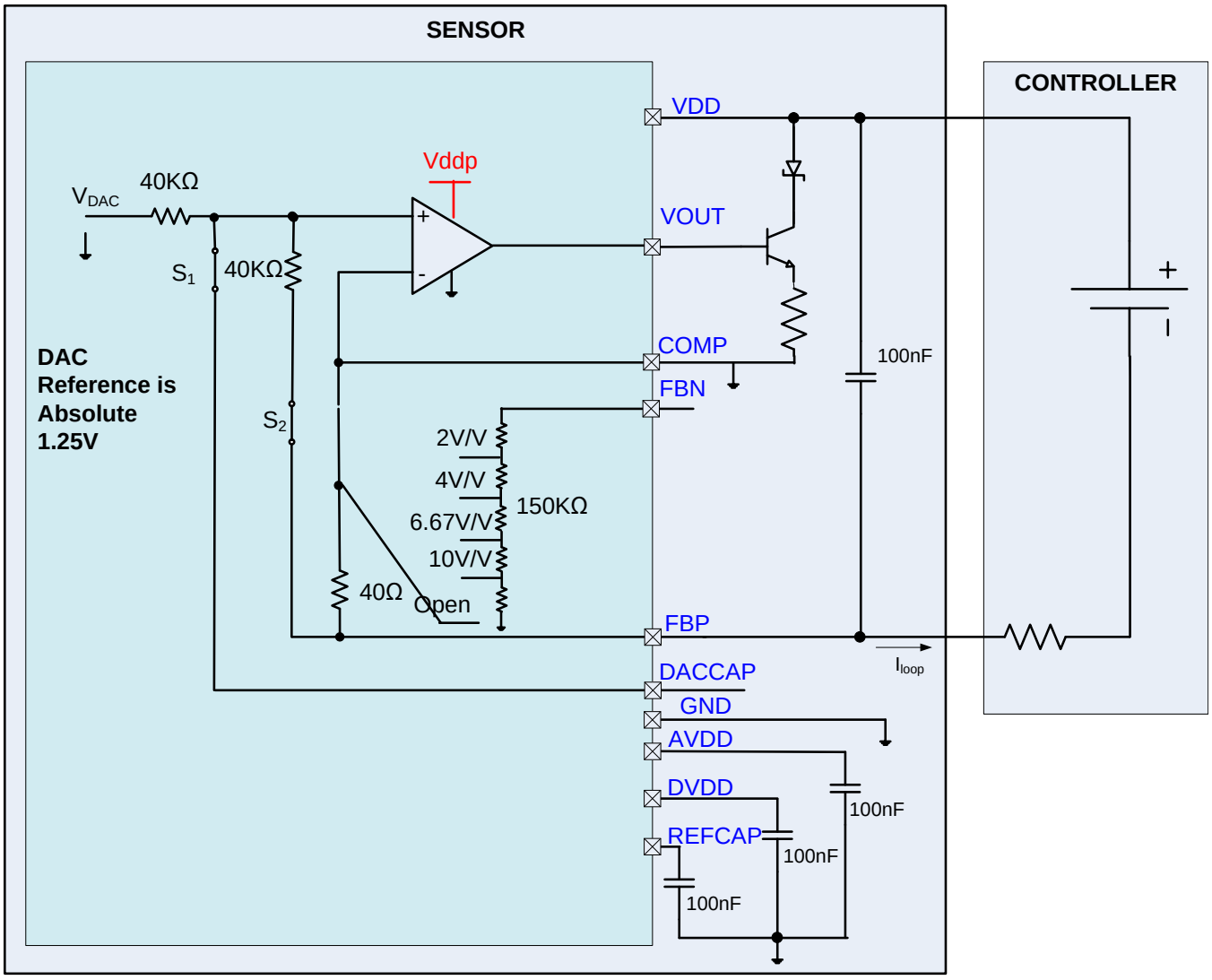


Figure 141. 4- to 20-mA Output With Internal Sense Resistor Diagram

Typical Applications (continued)

8.2.1.1 Design Requirements

There are only a few requirements to take into account when using the PGA900 in a design:

- Do not exceed the maximum slew rate of 0.5 V/µs at the VDD pin.
- Place a 100-nF capacitor as close as possible to the AVDD pin.
- Place a 100-nF capacitor as close as possible to the DVDD pin.
- Place a capacitor between 10 nF and 1000 nF as close as possible to the REFCAP pin.
- Place a 150-Ω resistor between the COMP pin and the emitter of the BJT for current loop stability purposes.
- Place a 10-Ω resistor between the FBP pin and the negative terminal of the controller for current measurement.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Programmer Tips

8.2.1.2.1.1 Resetting the Microprocessor and Enable Digital Interface

The following bits have to be configured to reset the M0 microprocessor and to enable digital interface:

1. Set IF_SEL bit in MICRO_INTERFACE_CONTROL register to 1.
2. Set MICRO_RESET bit in MICRO_INTERFACE_CONTROL register to 1.

8.2.1.2.1.2 Turning on Accurate Reference Buffer (REFCAP Voltage)

The following bits have to be configured to turn ON the accurate reference buffer:

1. Set SD bit in ALPWR register to 0.
2. Set ADC_EN_VREF bit in ALPWR register to 1.

By turning on the accurate reference buffer, the reference voltage can be measured on REFCAP pin. Further, the capacitor on REFCAP pin is connected to the reference buffer.

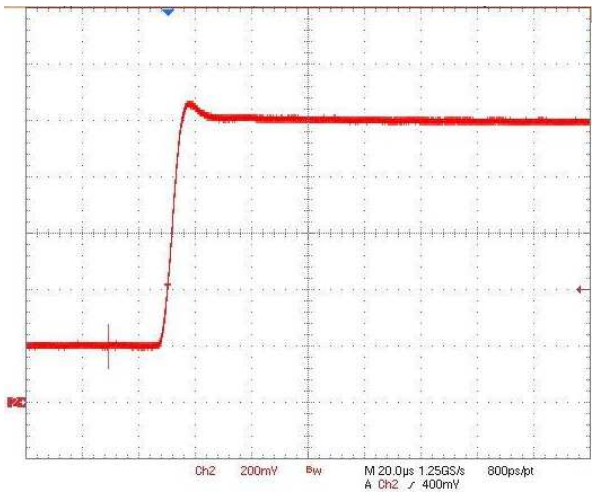
8.2.1.2.1.3 Turning on DAC and DAC GAIN

The following bits have to be configured to turn ON DAC and DAC GAIN:

1. Set SD bit in ALPWR register to 0.
2. Set ADC_EN_VREF bit in ALPWR register to 1.
3. Set DAC_ENABLE in DAC_CTRL_STATUS to 1.
4. Set 4_20_MA_EN bit in OP_STAGE_CTRL for voltage output or current output mode.
5. Set DACCAP_EN bit in OP_STAGE_CTRL to connect or disconnect external capacitor at DAC output.
6. Set DAC_RATIOMETRIC bit in DAC_CONFIG register for ratiometric or absolute voltage output mode.
7. Set TEST_MUX_DAC_EN in AMUX_CTRL to 1.
8. Set the loop current by writing to the DAC_REG0 register.

Typical Applications (continued)

8.2.1.3 Application Curve



Voltage measured between GND pin in the PGA900 and negative terminal of the controller. This includes the internal 40-Ω resistor and an external 10-Ω resistor, VDD = 15 V. The DAC codes used were 0x880 and 0x2760 for 4 and 20 mA respectively.

Figure 142. Loop Current Step From 4 to 20 mA

Typical Applications (continued)

8.2.2 Using External Depletion MOSFET When Supply to Sensor >30 V With GATE Control

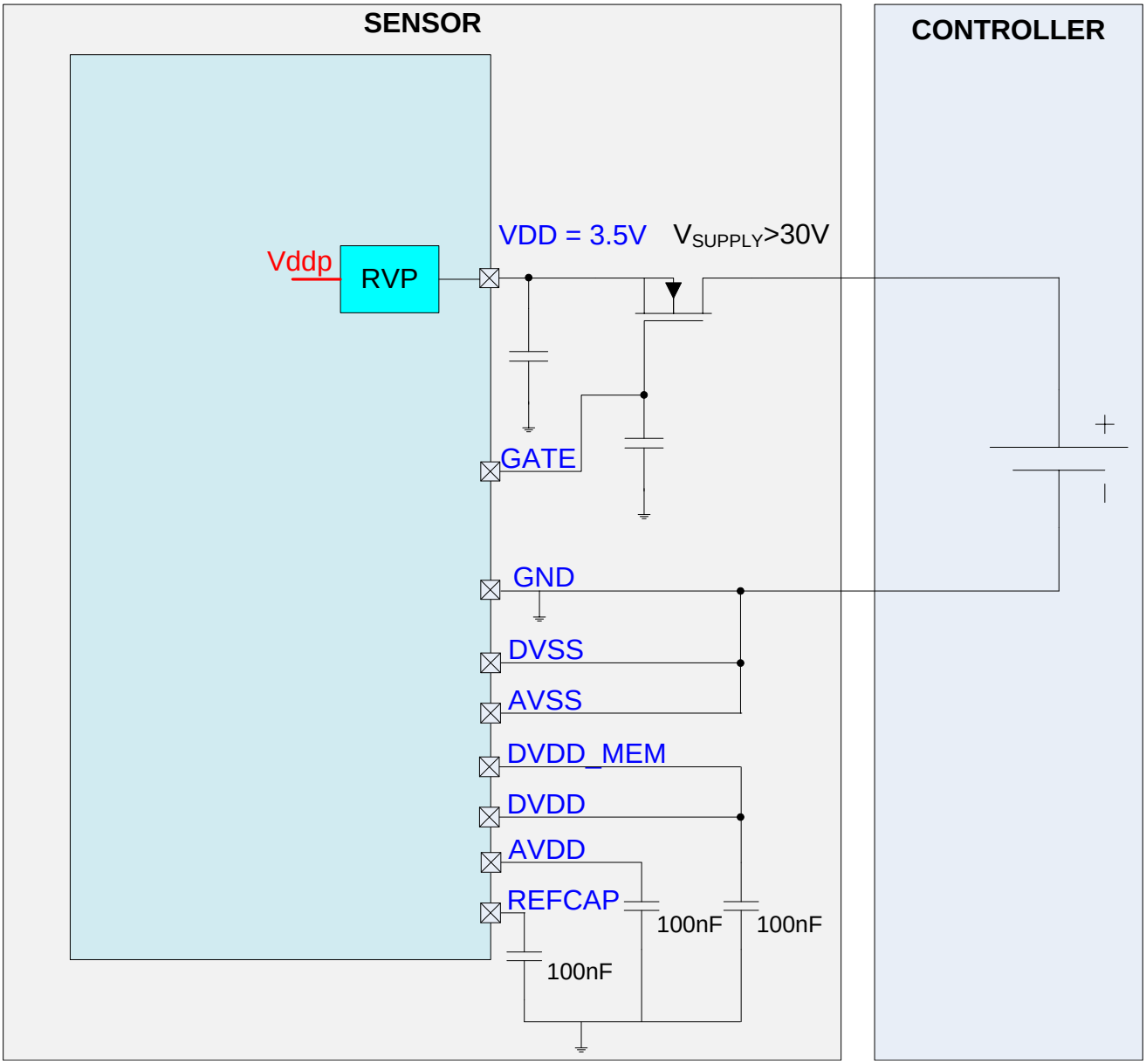


Figure 143. Using External Depletion MOSFET When Supply to Sensor >30 V With GATE Control Diagram

8.2.2.1 Design Requirements

There are only a few requirements to take into account when using the PGA900 in a design:

- Do not exceed the maximum slew rate of 0.5 V/µs at the VDD pin.
- Select an N-channel depletion MOSFET with a gate threshold voltage less than –1.5 V.
- A capacitor of 1-nF or less is recommended to be added to the GATE pin.
- Place a 100-nF capacitor as close as possible to the AVDD pin.
- Place a 100-nF capacitor as close as possible to the DVDD pin.
- Place a capacitor between 10 nF and 1000 nF as close as possible to the REFCAP pin.

Typical Applications (continued)

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Programmer Tips

Gate control is enabled at power up. If gate drive mode is not used, then the GATE pin must be connected to ground and the gate control must be disabled by setting GATE_CTRL_SD bit in ALPWR register to 1.

8.2.3 0- to 10-V Absolute Output With Internal Drive

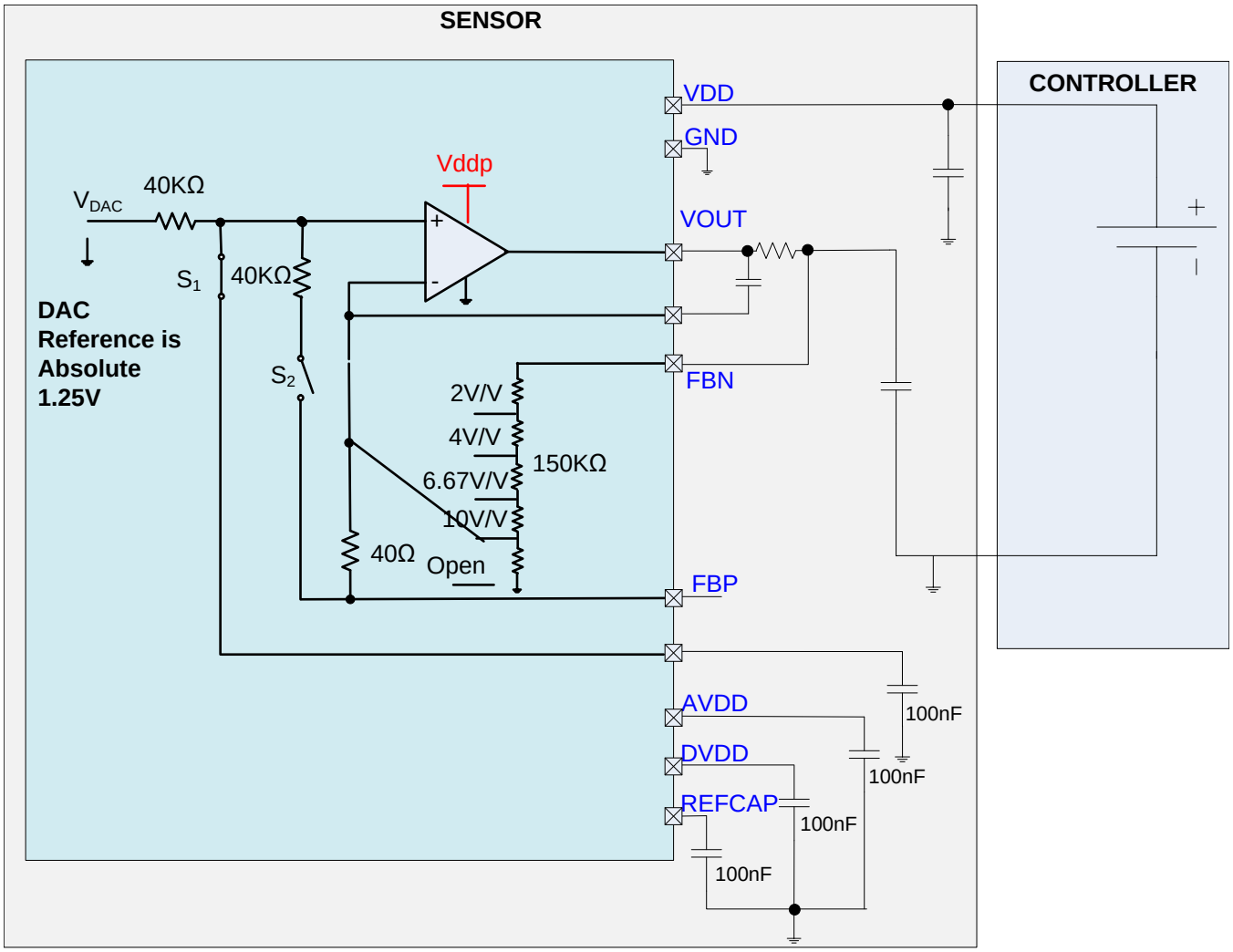


Figure 144. 0- to 10-V Absolute Output With Internal Drive Diagram

8.2.3.1 Design Requirements

There are only a few requirements to take into account when using the PGA900 in a design:

- Do not exceed the maximum slew rate of 0.5 V/µs at the VDD pin.
- Place a 100-nF capacitor as close as possible to the AVDD pin.
- Place a 100-nF capacitor as close as possible to the DVDD pin.
- Place a capacitor between 10 nF and 1000 nF as close as possible to the REFCAP pin.
- Implement compensation, using the COMP pin and an isolation resistor, when driving large capacitive loads with the VOUT pin.

Typical Applications (continued)

8.2.3.2 Detailed Design Procedure

8.2.3.2.1 Programmer Tips

8.2.3.2.1.1 Resetting the Microprocessor and Enable Digital Interface

The following bits have to be configured to reset the M0 microprocessor and to enable digital interface:

1. Set IF_SEL bit in MICRO_INTERFACE_CONTROL register to 1.
2. Set MICRO_RESET bit in MICRO_INTERFACE_CONTROL register to 1.

8.2.3.2.1.2 Turning on Accurate Reference Buffer (REFCAP Voltage)

The following bits have to be configured to turn ON the accurate reference buffer:

1. Set SD bit in ALPWR register to 0.
2. Set ADC_EN_VREF bit in ALPWR register to 1.

By turning on the accurate reference buffer, the reference voltage can be measured on REFCAP pin. Further, the capacitor on REFCAP pin is connected to the reference buffer.

8.2.3.2.1.3 Turning on DAC and DAC GAIN

The following bits have to be configured to turn ON DAC and DAC GAIN:

1. Set SD bit in ALPWR register to 0.
2. Set ADC_EN_VREF bit in ALPWR register to 1.
3. Set DAC_ENABLE in DAC_CTRL_STATUS to 1.
4. Set 4_20_MA_EN bit in OP_STAGE_CTRL for voltage output or current output mode.
5. Set DACCAP_EN bit in OP_STAGE_CTRL to connect or disconnect external capacitor at DAC output.
6. Set DAC_RATIOMETRIC bit in DAC_CONFIG register for ratiometric or absolute voltage output mode.
7. Set TEST_MUX_DAC_EN in AMUX_CTRL to 1.

Typical Applications (continued)

8.2.4 0- to 5-V Ratiometric Output With Internal Drive

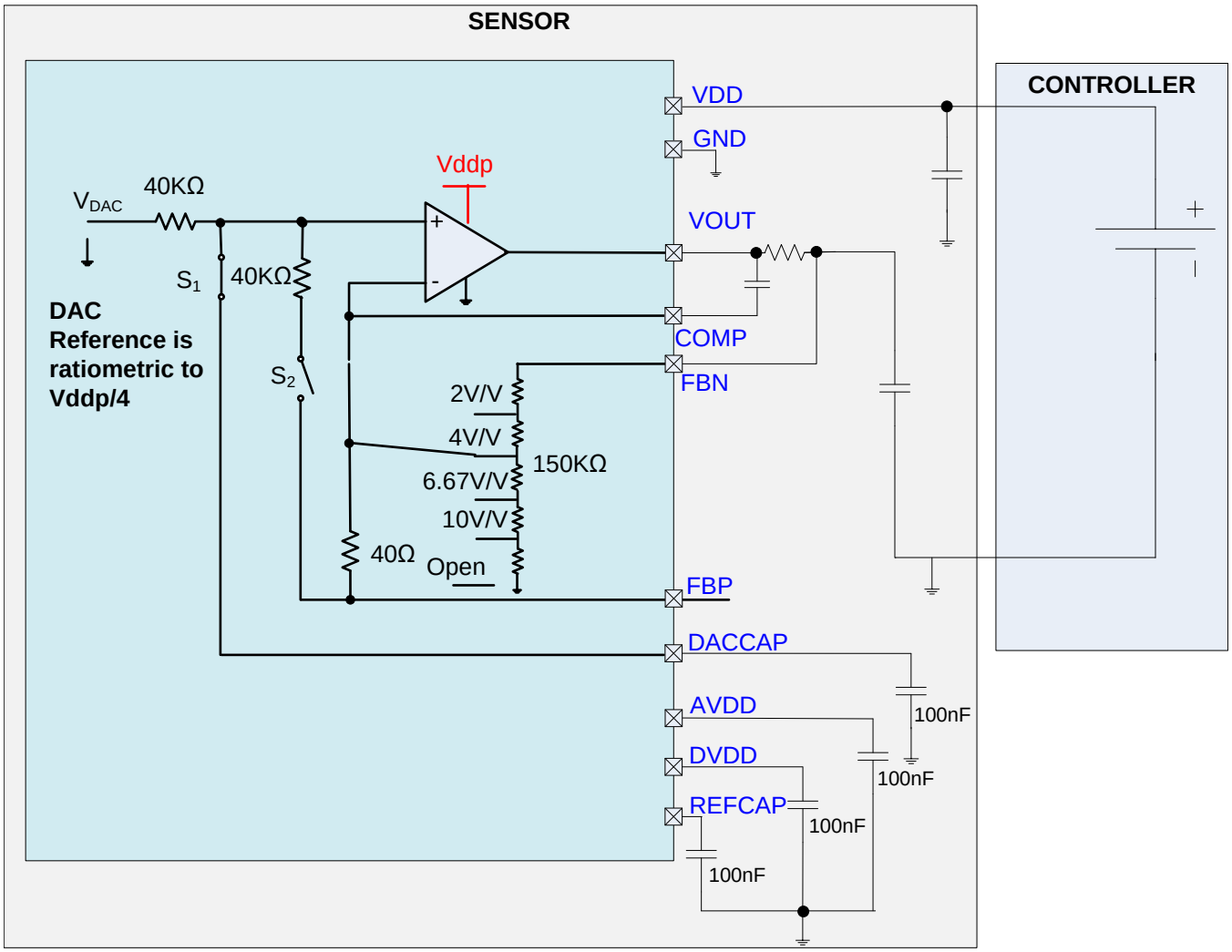


Figure 145. 0- to 5-V Ratiometric Output With Internal Drive Diagram

8.2.4.1 Design Requirements

There are only a few requirements to take into account when using the PGA900 in a design:

- Do not exceed the maximum slew rate of 0.5 V/µs at the VDD pin.
- Place a 100-nF capacitor as close as possible to the AVDD pin.
- Place a 100-nF capacitor as close as possible to the DVDD pin.
- Place a capacitor between 10 nF and 1000 nF as close as possible to the REFCAP pin.
- Implement compensation, using the COMP pin and an isolation resistor, when driving large capacitive loads with the VOUT pin.

Typical Applications (continued)

8.2.4.2 Detailed Design Procedure

8.2.4.2.1 Programmer Tips

8.2.4.2.1.1 Resetting the Microprocessor and Enable Digital Interface

The following bits have to be configured to reset the M0 microprocessor and to enable digital interface:

1. Set IF_SEL bit in MICRO_INTERFACE_CONTROL register to 1.
2. Set MICRO_RESET bit in MICRO_INTERFACE_CONTROL register to 1.

8.2.4.2.1.2 Turning on Accurate Reference Buffer (REFCAP Voltage)

The following bits have to be configured to turn ON the accurate reference buffer:

1. Set SD bit in ALPWR register to 0.
2. Set ADC_EN_VREF bit in ALPWR register to 1.

By turning on the accurate reference buffer, the reference voltage can be measured on REFCAP pin. Further, the capacitor on REFCAP pin is connected to the reference buffer.

8.2.4.2.1.3 Turning on DAC and DAC GAIN

The following bits have to be configured to turn ON DAC and DAC GAIN:

1. Set SD bit in ALPWR register to 0.
2. Set ADC_EN_VREF bit in ALPWR register to 1.
3. Set DAC_ENABLE in DAC_CTRL_STATUS to 1.
4. Set 4_20_MA_EN bit in OP_STAGE_CTRL for voltage output or current output mode.
5. Set DACCAP_EN bit in OP_STAGE_CTRL to connect or disconnect external capacitor at DAC output.
6. Set DAC_RATIOMETRIC bit in DAC_CONFIG register for ratiometric or absolute voltage output mode.
7. Set TEST_MUX_DAC_EN in AMUX_CTRL to 1.

Typical Applications (continued)

8.2.5 0- to 10-V PWM Output With Internal Drive

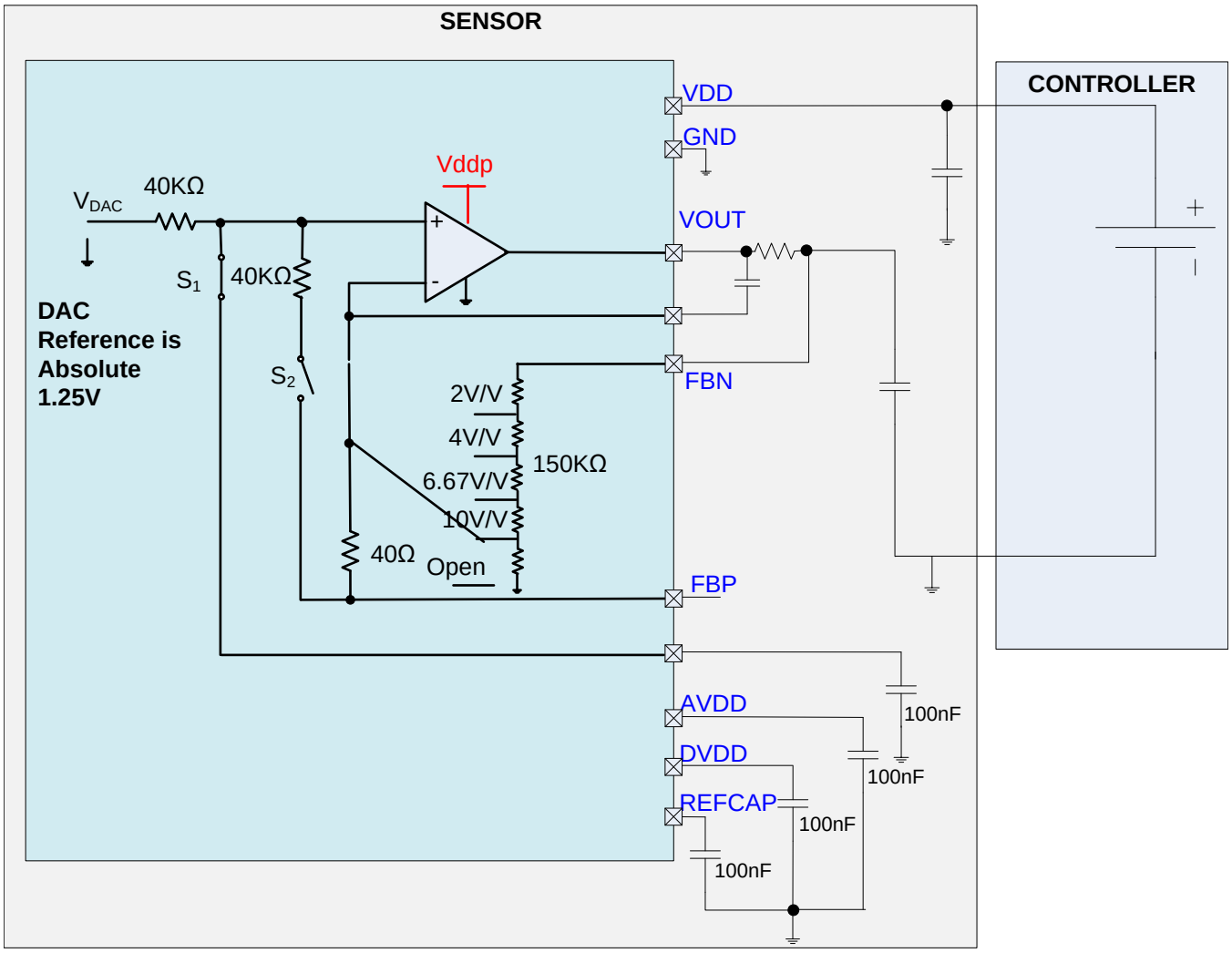


Figure 146. 0- to 10-V PWM Output With Internal Drive Diagram

8.2.5.1 Design Requirements

There are only a few requirements to take into account when using the PGA900 in a design:

- Do not exceed the maximum slew rate of 0.5 V/µs at the VDD pin.
- Place a 100-nF capacitor as close as possible to the AVDD pin.
- Place a 100-nF capacitor as close as possible to the DVDD pin.
- Place a capacitor between 10 nF and 1000 nF as close as possible to the REFCAP pin.
- Implement compensation, using the COMP pin and an isolation resistor, when driving large capacitive loads with the VOUT pin.

Typical Applications (continued)

8.2.5.2 Detailed Design Procedure

8.2.5.2.1 Programmer Tips

8.2.5.2.1.1 Resetting the Microprocessor and Enable Digital Interface

The following bits have to be configured to reset the M0 microprocessor and to enable digital interface:

1. Set IF_SEL bit in MICRO_INTERFACE_CONTROL register to 1.
2. Set MICRO_RESET bit in MICRO_INTERFACE_CONTROL register to 1.

8.2.5.2.1.2 Turning on Accurate Reference Buffer (REFCAP Voltage)

The following bits have to be configured to turn ON the accurate reference buffer:

1. Set SD bit in ALPWR register to 0.
2. Set ADC_EN_VREF bit in ALPWR register to 1.

By turning on the accurate reference buffer, the reference voltage can be measured on REFCAP pin. Further, the capacitor on REFCAP pin is connected to the reference buffer.

8.2.5.2.1.3 Turning on DAC and DAC GAIN

The following bits have to be configured to turn ON DAC and DAC GAIN:

1. Set SD bit in ALPWR register to 0.
2. Set ADC_EN_VREF bit in ALPWR register to 1.
3. Set DAC_ENABLE in DAC_CTRL_STATUS to 1.
4. Set 4_20_MA_EN bit in OP_STAGE_CTRL for voltage output or current output mode.
5. Set DACCAP_EN bit in OP_STAGE_CTRL to connect or disconnect external capacitor at DAC output.
6. Set DAC_RATIOMETRIC bit in DAC_CONFIG register for ratiometric or absolute voltage output mode.
7. Set TEST_MUX_DAC_EN in AMUX_CTRL to 1.

9 Power Supply Recommendations

The PGA900 has a single pin, VDD, for the input power supply. The maximum slew rate for the VDD pin is 0.5 V/µs as specified in the *Recommended Operating Conditions*. Faster slew rates might generate a POR. A decoupling capacitor for VDD must be placed as close as possible to the pin.

10 Layout

10.1 Layout Guidelines

Standard layout good practices must be used when designing a board to test the PGA900. Depending on the number of layers in the board, one or more GND planes must be inserted as internal layers. In addition, the VDD decoupling capacitor must be placed as close as possible to the pin. In a similar way, the 100-nF recommended capacitors for the AVDD and DVDD regulators as well as the 10- to 1000-nF recommended capacitor for REFCAP must be placed as close as possible to the respective pins.

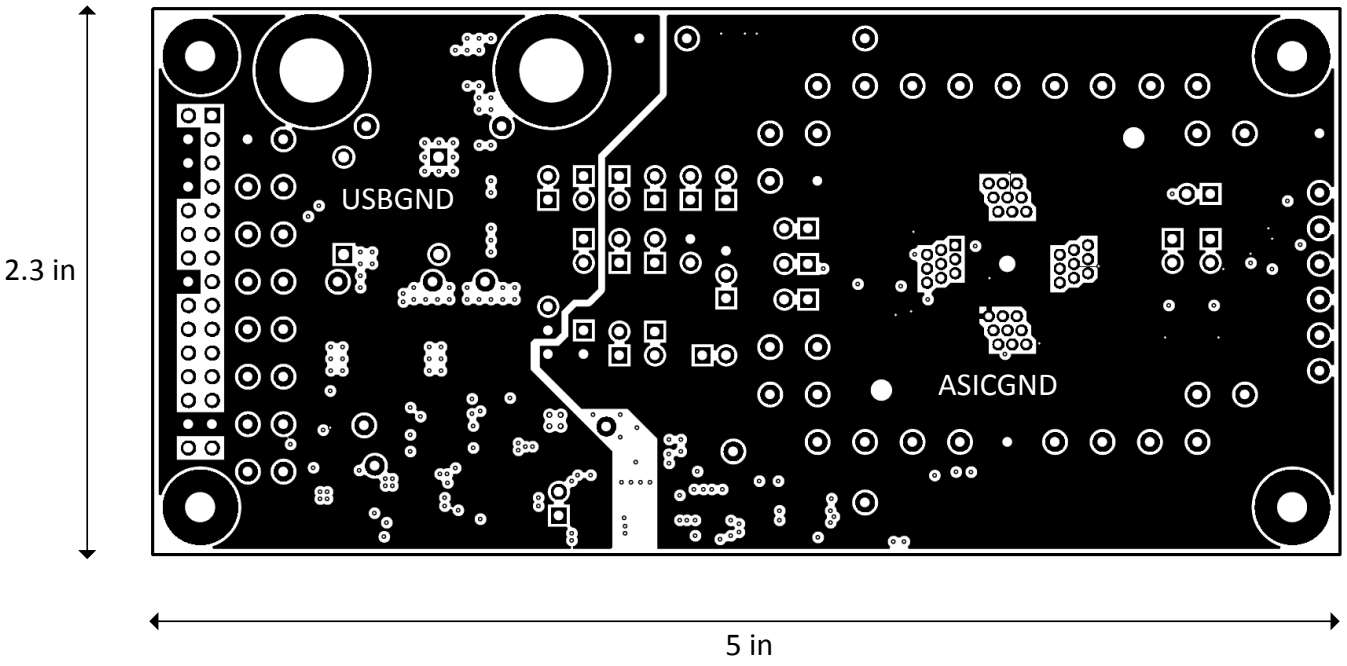
Depending on the application, the signal traces for FBN, FBP, COMP, and VOUT must be routed such that they do not cross one another to minimize coupling.

10.2 Layout Example

The following figures show the main guidelines previously discussed being implemented in a 6 layers, socketed EVM for the QFN package version of the PGA900. Two main GND planes (layer 2 and 5) were used to provide a nearby GND plane to each of the signal layers and the power plane (layer 3) in the EVM. This EVM supports voltage and current mode for the device, and as a result, GND separation is needed depending on the application. As a result, layer 2 is a solid GND plane for the majority of the circuitry in the EVM (IRETURN). Because most of the circuitry is referred to this GND plane, layers 3 and 4 also contain copper pours connected to IRETURN. This GND plane is the return path for the supply used in the 4- to 20-mA loop. Layer 5 is a split plane for the ground references for the digital communication signals used for this EVM (USBGND) and the ground pins in the device (GND, AVSS and DVSS), referred to as ASICGND. Figure 147 shows layer 5. The EVM provides jumpers to connect, or disconnect, these 3 planes one from another depending on the desired configuration.

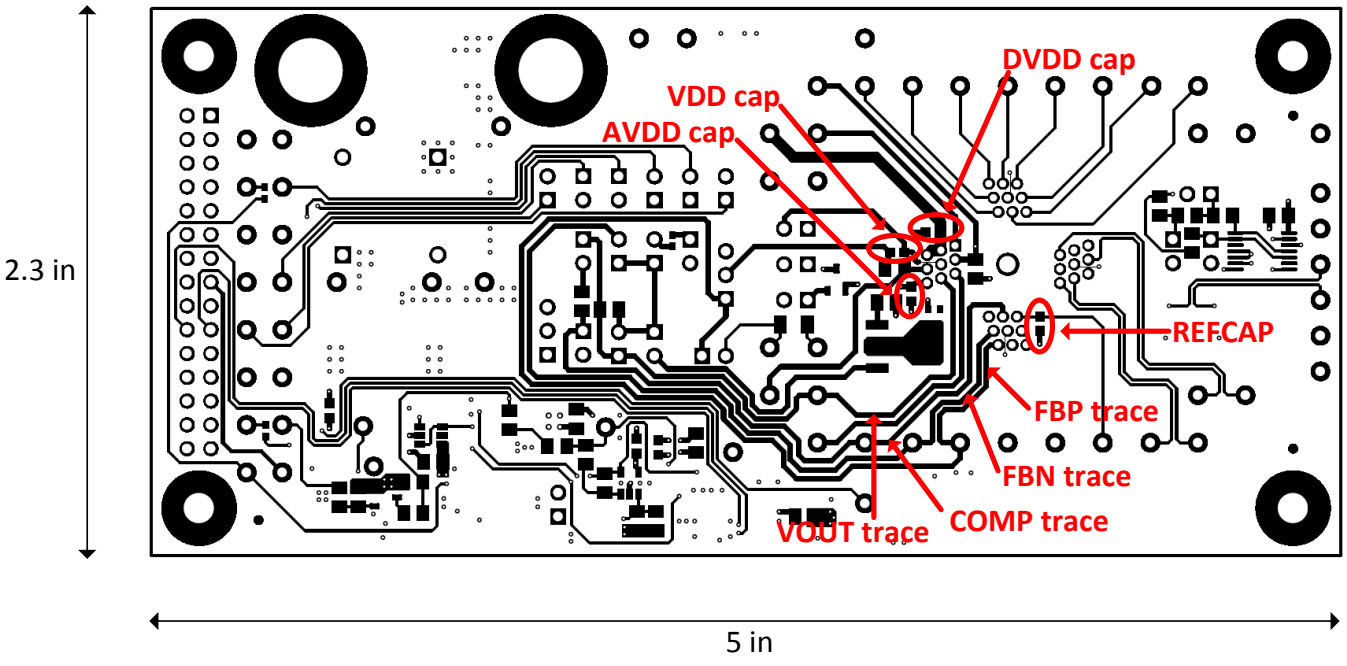
Figure 148 shows the recommended capacitors for the proper operation of the PGA900. These capacitors are placed as close as possible to the respective pins from the socket used for this particular EVM. The signal traces for FBN, FBP, COMP and VOUT can also be observed to be routed all in the same layer to avoid crossing each other and minimize coupling.

Layout Example (continued)



NOTE: Ground planes for USB2ANY and PGA900 are separated.

Figure 147. Layer 5 (GND) in PGA900EVM



NOTE: Decoupling capacitors are placed as near as possible to the socket pins and VOUT, COMP, FBN, and FBP traces are all on the same layer to avoid crossing each other and minimize coupling.

Figure 148. Bottom Layer in PGA900EVM

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *PGA900 DAC Output Stability Application Note* (SLDA020)
- *PGA900 as 4- to 20-mA Current Loop Transmitter* (SLDA030)
- *Understanding Open Loop Gain of the PGA900 DAC Gain Amplifier* (SLDA031)
- *Connecting PGA900 Instrumentation Amplifier to Resistive Bridge Sensor* (SLDA032)
- *Understanding Open Loop Output Impedance of the PGA900 DAC Gain Amplifier* (SLDA033)
- *System Noise Analysis of a Resistive Bridge Pressure Sensor Connected to the PGA* (SLDA034)
- *PGAxxxEVM-034 User's Guide* (SLDU011)
- *PGA900 Software User's Guide* (SLDU013)
- *PGA900 GUI User's Guide* (SLDU016)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
ARM, Cortex are registered trademarks of ARM Ltd.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA900ARHHR	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	PGA900A RHH	Samples
PGA900ARHHT	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	PGA900A RHH	Samples
PGA900AYZSR	ACTIVE	DSBGA	YZS	36	1500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 150	PGA900A YZS	Samples
PGA900AYZST	ACTIVE	DSBGA	YZS	36	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 150	PGA900A YZS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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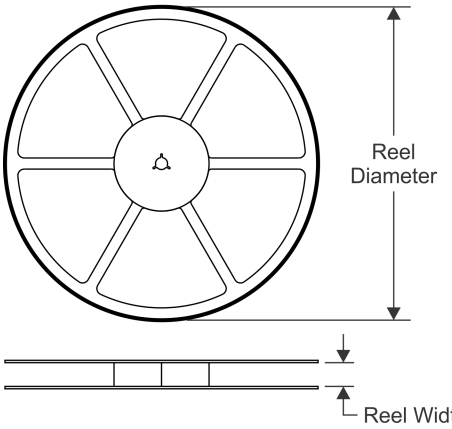
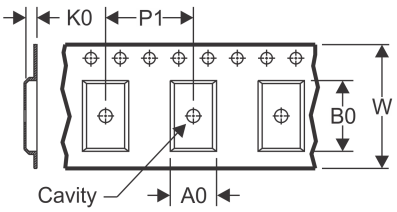
TAPE AND REEL INFORMATION

REEL DIMENSIONS

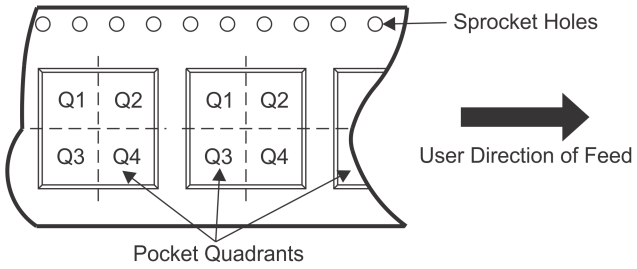


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

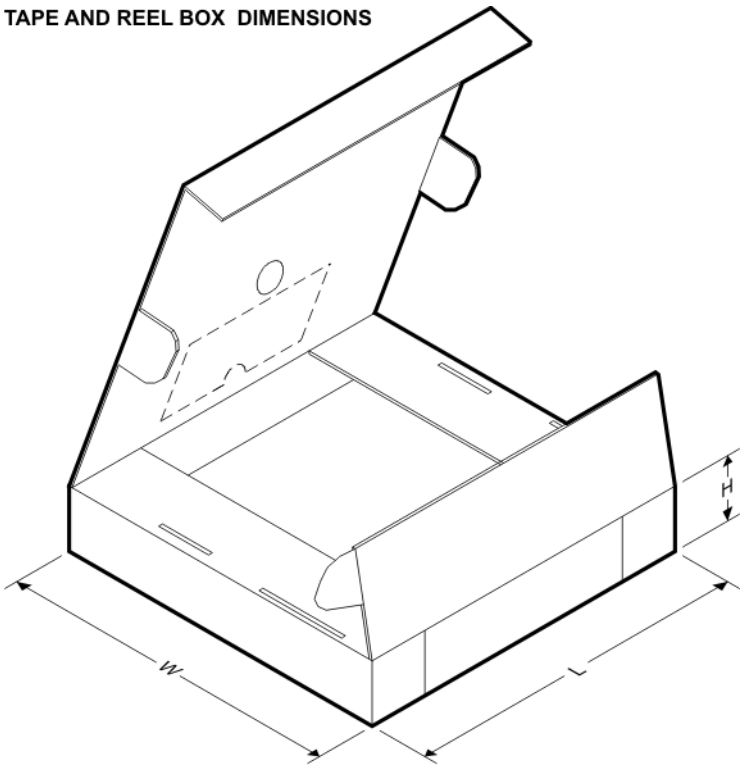
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA900ARHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
PGA900ARHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
PGA900AYZST	DSBGA	YZS	36	250	180.0	12.4	3.79	3.79	0.71	8.0	12.0	Q1

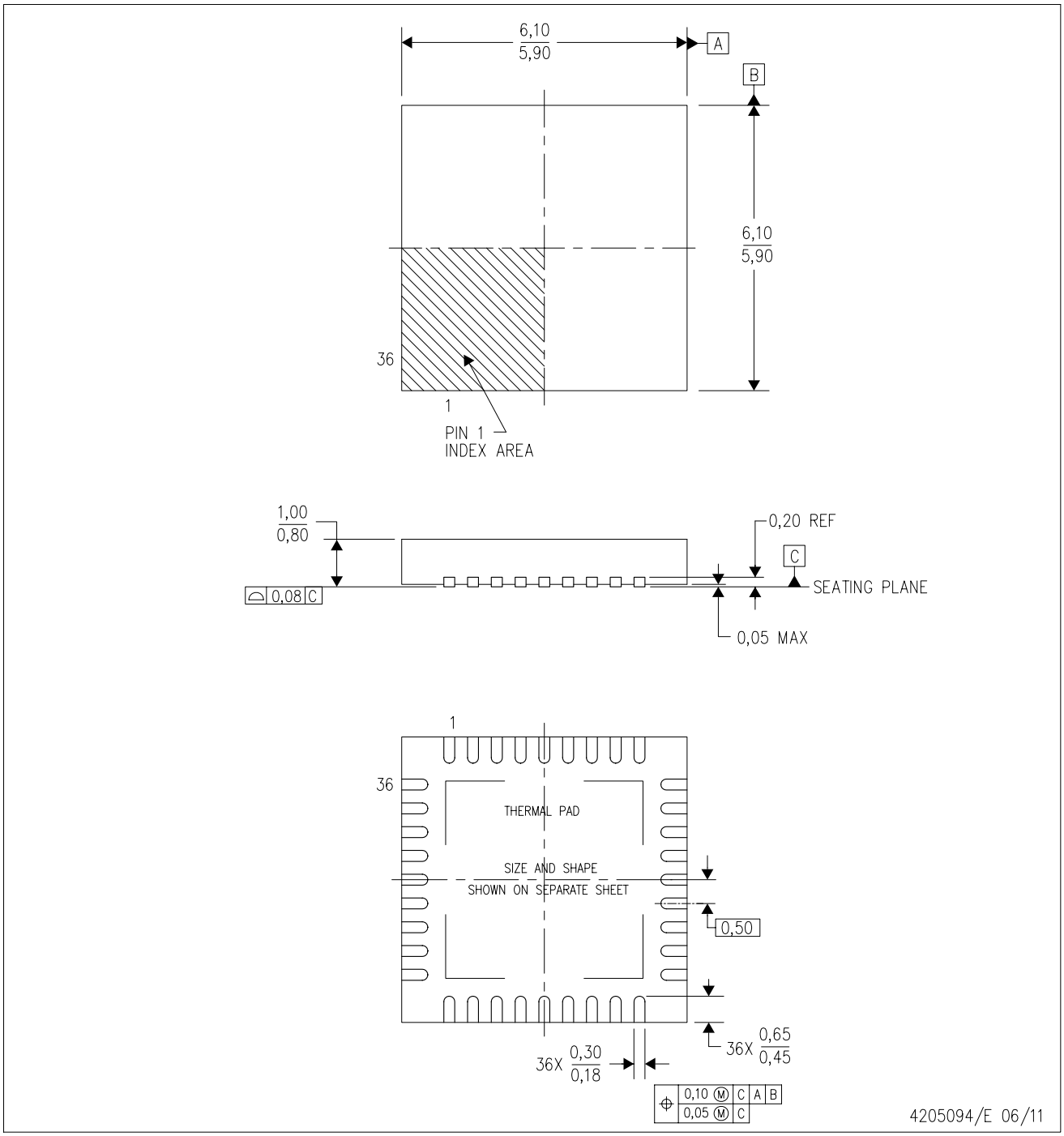
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA900ARHHR	VQFN	RHH	36	2500	367.0	367.0	38.0
PGA900ARHHT	VQFN	RHH	36	250	210.0	185.0	35.0
PGA900AYZST	DSBGA	YZS	36	250	210.0	185.0	35.0

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

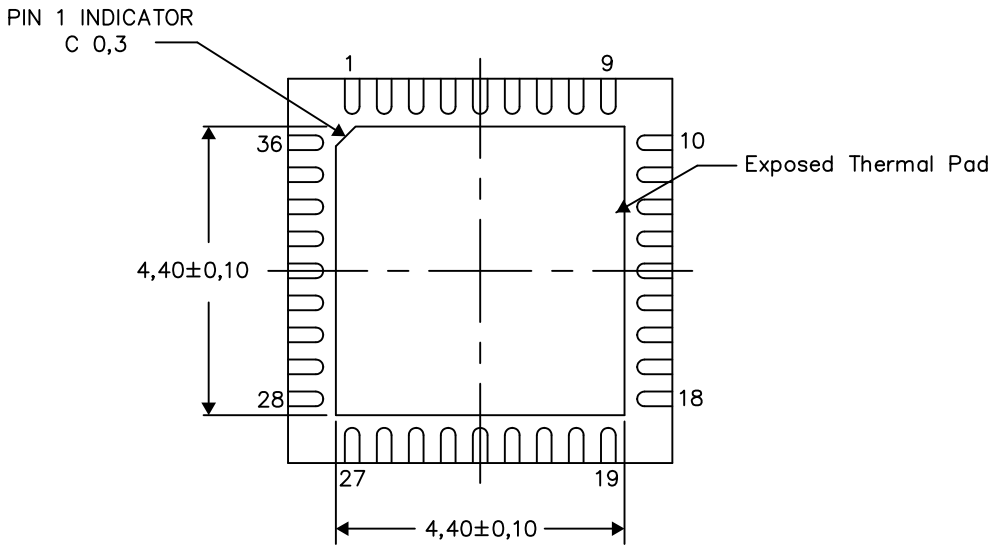
RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



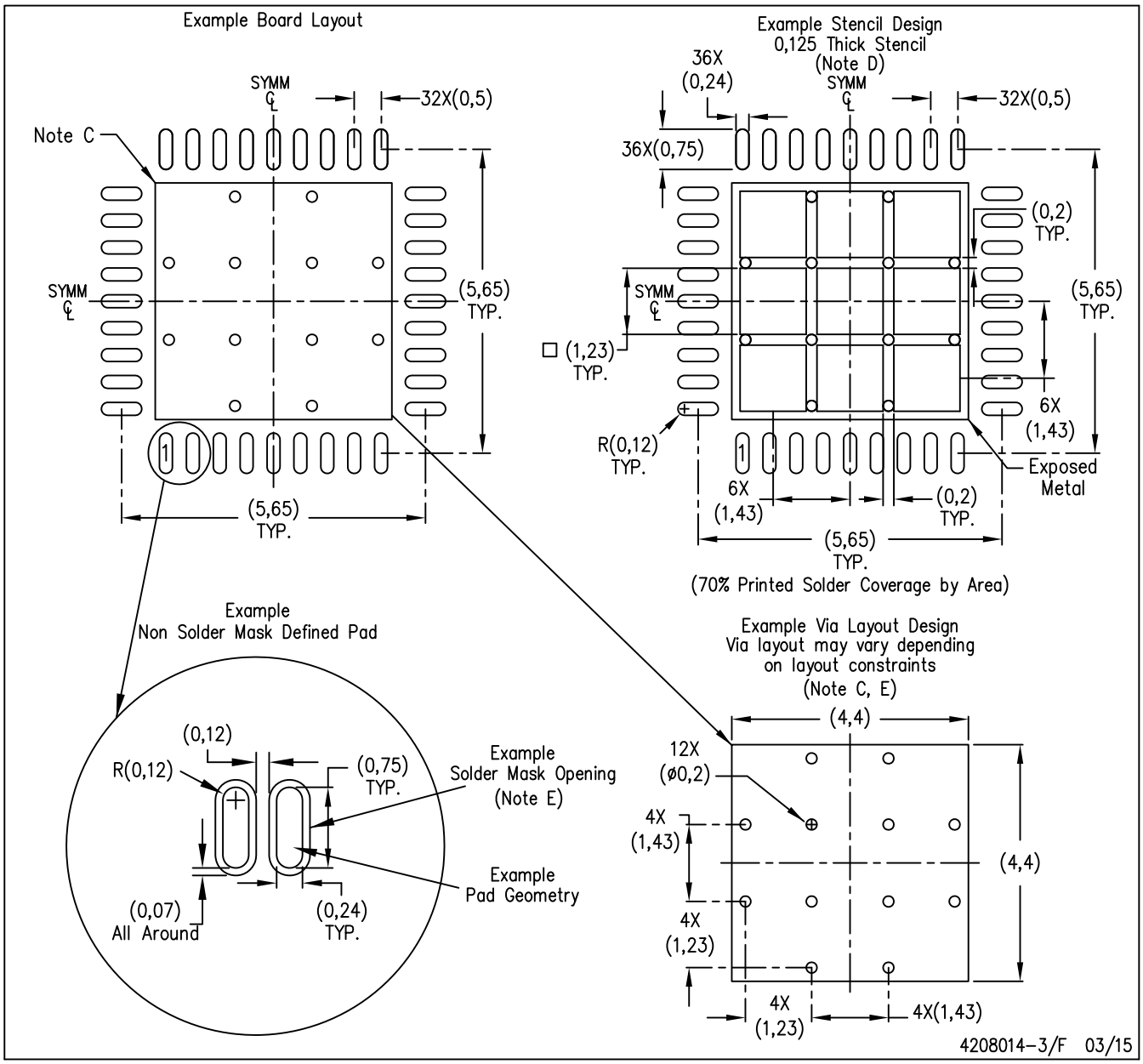
Bottom View

Exposed Thermal Pad Dimensions

4206362–5/M 11/13

NOTE: All linear dimensions are in millimeters

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



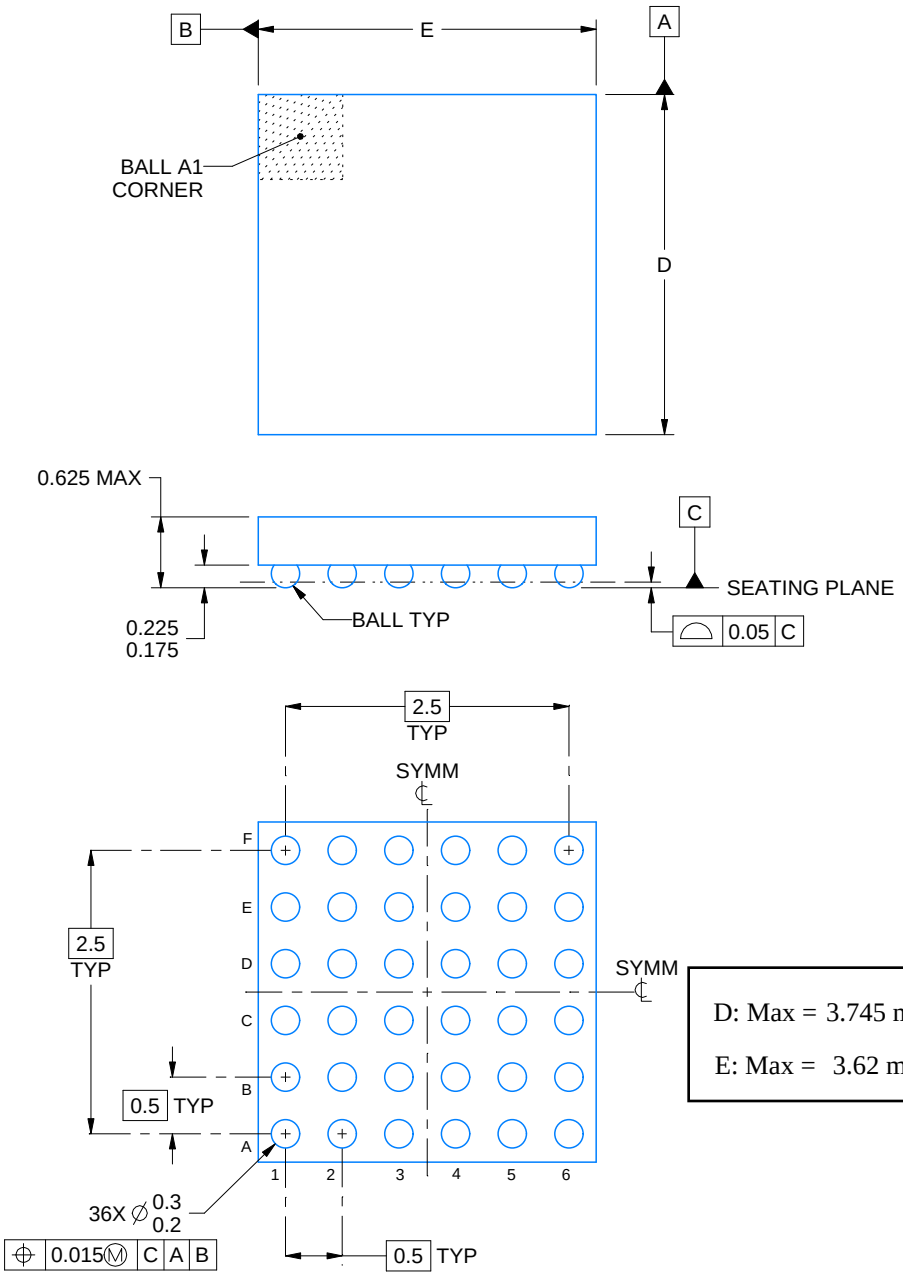
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

PACKAGE OUTLINE

YZS0036

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



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NOTES:

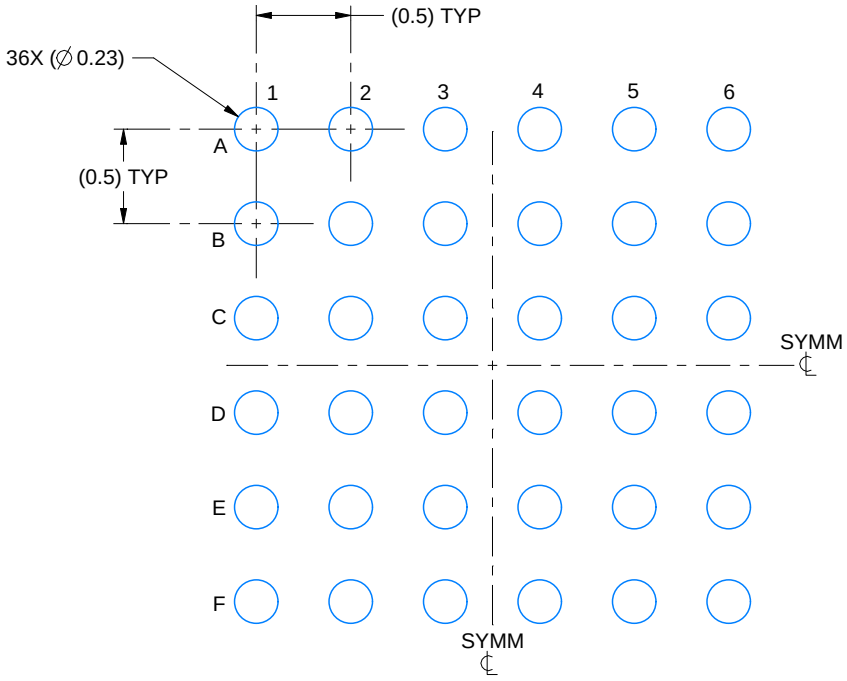
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

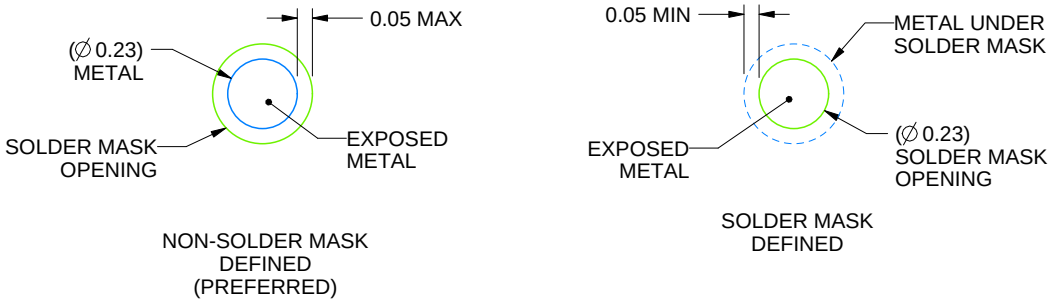
YZS0036

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS
NOT TO SCALE

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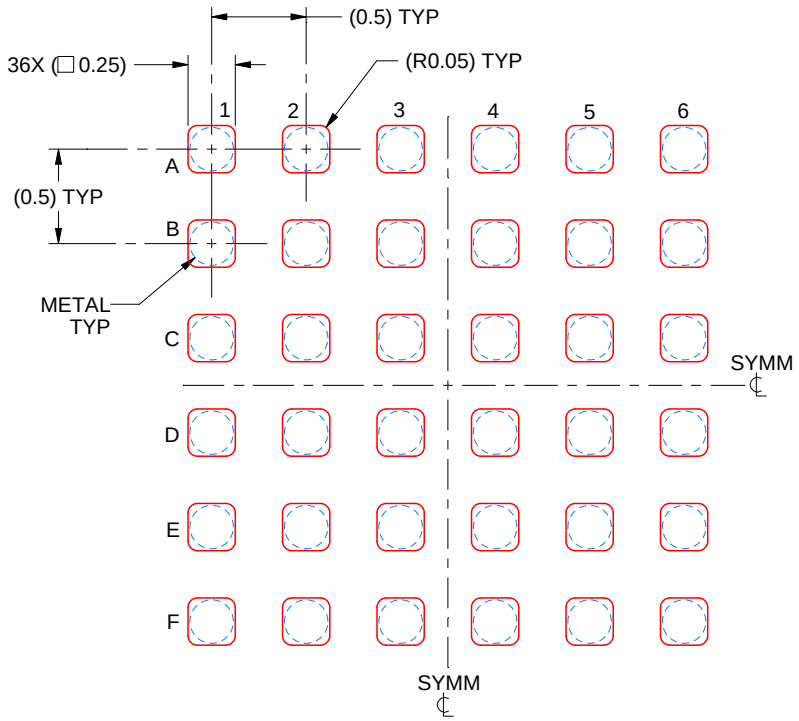
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 25X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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