PGA300 Signal Conditioner and Transmitter for Pressure Sensors

1 Features

- Analog Features
  - Analog Front-End for Resistive Bridge Sensors
  - Accommodates Sensor Sensitivities From 1 mV/V to 135 mV/V
  - On-Chip Temperature Sensor
  - Programmable Gain
  - 16-Bit Sigma-Delta Analog-to-Digital Converter for Signal Channel
  - 16-Bit Sigma-Delta Analog-to-Digital Converter for Temperature Channel
  - 14-Bit Output DAC
- Digital Features
  - <0.1% FSO Accuracy Across Temperature
  - System Response Time <220 µs
  - Third-Order Offset, Gain, and Nonlinearity Temperature Compensation
  - Diagnostic Functions
  - Integrated EEPROM for Device Operation, Calibration Data and User Data
- Peripheral Features
  - One-Wire Interface Enables Communication Through the Power Supply Pin Without Using Additional Lines
  - 4-mA to 20-mA Current Loop Interface
  - Ratiometric and Absolute Voltage Output
  - Power Management Control
  - Analog Low-Voltage Detect
- General Features
  - Industrial Temperature Range: –40°C to 150°C
  - Power Supply:
    - On-Chip Power Management Accepts Wide Power-Supply Voltage From 3.3 V to 30 V
    - Integrated Reverse-Protection Circuit

2 Applications

- Pressure-Sensor Transmitter and Transducer
- Liquid-Level Meter, Flow Meter
- Resistive Field Trasmitter

3 Description

The PGA300 device provides an interface for piezoresistive and strain-gauge pressure-sense elements. The device is a full system-on-chip (SoC) solution that incorporates programmable analog front end (AFE), ADC, and digital signal processing that enable direct connection to the sense element. Further, the PGA300 device includes integrated voltage regulators and an oscillator, thus minimizing the number of external components. The device achieves high accuracy by employing third-order temperature and nonlinearity compensation. External communication is achieved by using a one-wire serial interface (OWI) through the power-supply pin in order to simplify the system calibration process. An Integrated DAC supports absolute-voltage, ratiometric-voltage, and 4-mA to 20-mA current-loop outputs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PGA300	VQFN (36)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

PGA300 Simplified Block Diagram

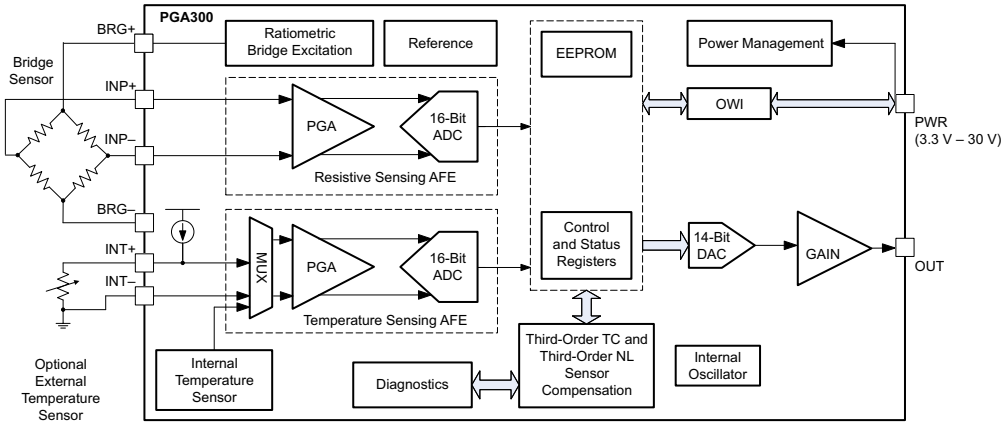


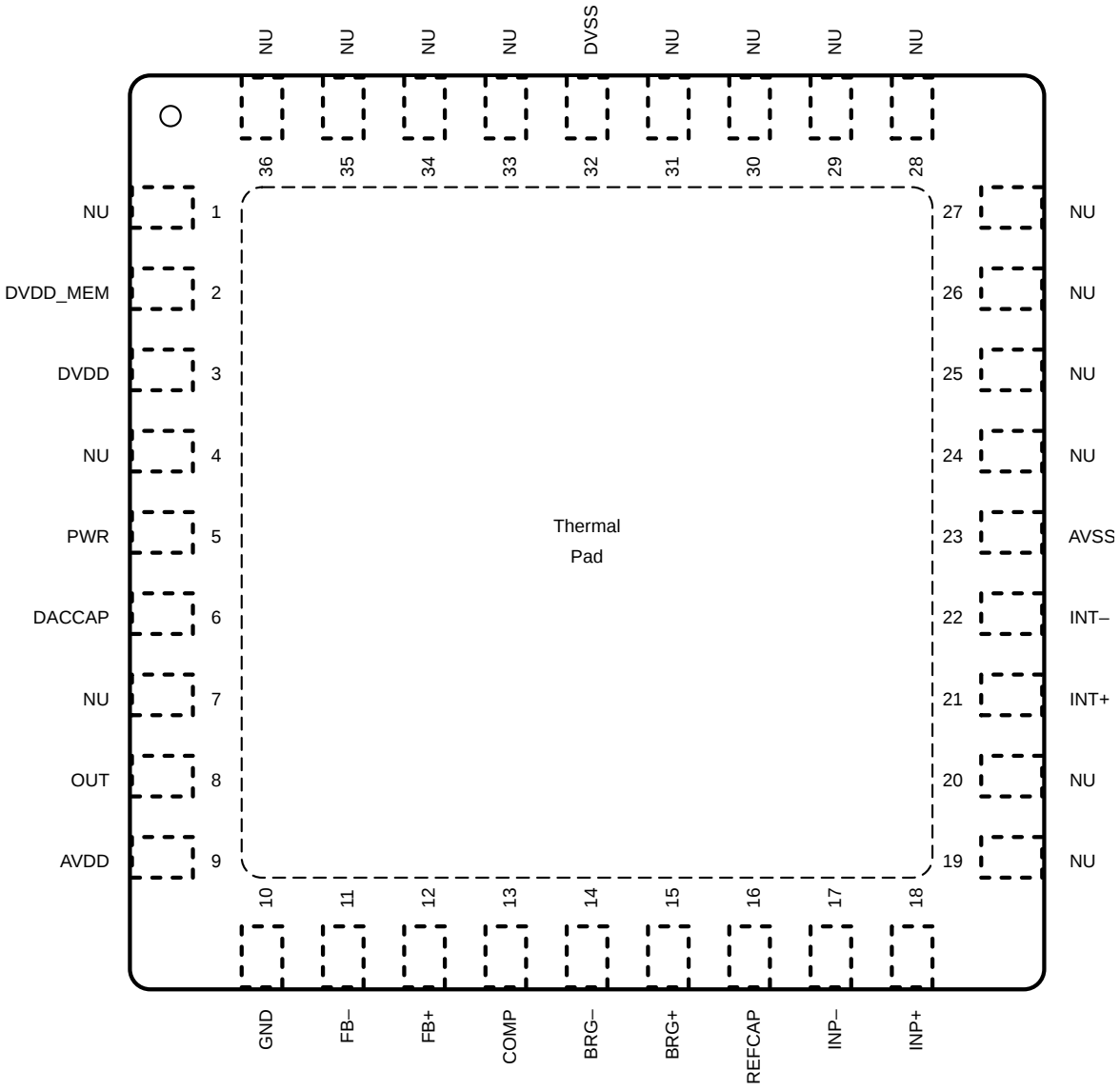
Table of Contents

4 Revision History

Changes from Original (October 2014) to Revision A	Page
• Changed data sheet from PRODUCT PREVIEW to PRODUCTION DATA	1

5 Pin Configuration and Functions

RHH Package
36-Pin VQFN With Thermal Pad
Top View



NU – Make no external connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	9	O	AVDD regulator output
AVSS	23	—	Analog ground
BRG+	15	O	Bridge drive, positive
BRG–	14	O	Bridge drive, negative
COMP	13	I	Output amplifier compensation
DACCAP	6	O	DAC capacitor
DVDD	3	O	DVDD regulator output
DVDD_MEM	2	O	Power supply for EEPROM and OTP
DVSS	32	—	Digital ground
FB+	12	I	Feedback, positive
FB–	11	I	Feedback, negative
GND	10	—	Ground
INP+	18	I	Resistive sensor positive input
INP–	17	I	Resistive sensor negative input
INT+	21	I	External temperature sensor positive input
INT–	22	I	External temperature sensor negative input
NU	1, 4, 7, 19, 20, 24 to 31, 33 to 36	—	Do not connect
OUT	8	O	DAC gain output
PWR	5	I	Input power supply
REFCAP	16	O	ADC reference capacitor
Thermal pad	—	—	Connect to analog ground

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
PWR	Supply voltage	–28	33	V
	Voltage at sensor input pins: INP+, INP–, INT+, INT–	–0.3	2	V
	Voltage at AVDD, AVSS, BRG+, BRG–, COMP, DACCAP, DVDD, DVDD_MEM, DVSS, FB–, GATE, REFCAP	–0.3	3.6	V
	Voltage at FB+ pin	–2	V_{PWR} + 0.3	V
	Voltage at OUT pin	-0.3	33	V
I_{PWR}, short on OUT pin	Supply current		25	mA
T_{Jmax}	Maximum junction temperature		155	°C
T_{stg}	Storage temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{PWR}	Power supply voltage		3.3		30	V
	Slew rate	V_{DD} = 0 to 30 V			0.5	V/µs
I_{PWR}	Power supply current - normal operation	No load on BRG, no load on DAC		2.5		mA mA
	Power supply current - EEPROM programming	While EEPROM is being programmed, no load on BRG, no load on DAC			9 (1)	
T_A	Operating ambient temperature		–40		150	°C
	Programming temperature	EEPROM	–40		140	°C
	Start-up time (including analog and digital)	V_{PWR} ramp rate 0.5 V/µs			1	ms
	Capacitor on PWR pin		10			nF

(1) Programming of the EEPROM results in an additional 6 mA of current on the PWR pin.

6.4 Thermal Information

THERMAL METRIC[1]		PGA300 RHH (VQFN) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics – Reverse Voltage Protection

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Reverse voltage		–28			V
	Voltage drop across reverse voltage protection element			20		mV

6.6 Electrical Characteristics – Regulators

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AVDD}	AVDD voltage	C_{AVDD} = 100 nF		3		V
V_{DVDD}	DVDD voltage – operating	C_{DVDD} = 100 nF		1.8		V

6.7 Electrical Characteristics – Internal Reference

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	High-voltage reference voltage[1]			1.2		V
	Accurate reference voltage			2.5		V
	Capacitor value on REFCAP pin			100		nF

(1) TEMP_DRIFT = [(Value at TEMP – Value at 25³C) / (Value at 25³C × ΔTEMP)] × 10^6

6.8 Electrical Characteristics – Bridge Sensor Supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BRG SUPPLY FOR RESISTIVE BRIDGE SENSORS						
$V_{BRG+} – V_{BRG–}$	Bridge supply voltage	Bridge supply control bit = 0b00, no load		2.5		V
		Bridge supply control bit = 0b01, no load		2		V
		Bridge supply control bit = 0b10, no load		1.25		V
I_{BRG}	Current supply to the bridge				1.5	mA
C_{BRG}	Capacitive load	R_{BRG} = 20 kΩ			2	nF

6.9 Electrical Characteristics – Temperature Sensor Supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{TEMP} SUPPLY FOR TEMPERATURE SENSOR						
I_{TEMP}	Current supply to temperature sensor	Control bit = 0b000		25		µA
		Control bit = 0b001		50		
		Control bit = 0b010		100		
		Control bit = 0b011		500		
		Control bit = 0b1xx		OFF		
C_{TEMP}	Capacitive load				100	nF
	Output impedance			15		MΩ

6.10 Electrical Characteristics – Internal Temperature Sensor

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature range		–40		150	°C

6.11 Electrical Characteristics – P Gain (Chopper Stabilized)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain steps (5 bits)	00000, at dc		5		V/V
	00001		5.48		
	00010		5.97		
	00011		6.56		
	00100		7.02		
	00101		8		
	00110		9.09		
	00111		10		
	01000		10.53		
	01001		11.11		
	01010		12.5		
	01011		13.33		
	01100		14.29		
	01101		16		
	01110		17.39		
	01111		18.18		
	10000		19.05		
	10001		20		
	10010		22.22		
	10011		25		
	10100		30.77		
	10101		36.36		
	10110		40		
	10111		44.44		
	11000		50		
	11001		57.14		
	11010		66.67		
	11011		80		
	11100		100		
	11101		133.33		
	11110		200		
	11111		400		

Electrical Characteristics – P Gain (Chopper Stabilized) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Gain bandwidth product			10		MHz
	Input-referred noise density(1)	f = 0.1 Hz to 2 kHz, gain = 400 V/V, sampling rate = 128 µs, across temperature		15		nV/√Hz
	Input offset voltage			10		µV
	Input bias current			5		nA
	Frequency response	Gain = 400 V/V, <1 kHz			±0.1	%V/V
	Common-mode voltage range			Depends on selected gain, bridge supply and sensor span (2)		V
	Common-mode rejection ratio	f_{CM} = 50 Hz at gain = 5 V/V		110		dB
	Input impedance		10			MΩ

(1) Total input-referred noise including gain noise, ADC reference noise, ADC thermal noise, and ADC quantization noise
(2) **Common Mode at P Gain Input and Output:** There are two constraints:
(a) The single-ended voltage of the positive and negative pins at the P gain input must be between 0.3 V and 1.8 V
(b) The single-ended voltage of the positive and negative pins at the P gain output must be between 0.1 V and 2 V

6.12 Electrical Characteristics – P Analog-to-Digital Converter

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Sigma-delta modulator frequency			1		MHz
	ADC voltage input range		–2.5		2.5	V
	Number of bits			16		bits
	ADC 2s complement code for –2.5-V differential input			8000_{hex}		
	ADC 2s complement code for 0-V differential input			0000_{hex}		
	ADC 2s complement code for 2.5-V differential input			$7FFF_{hex}$		
INL	Integral nonlinearity				±0.5	LSB

6.13 Electrical Characteristics – T Gain (Chopper Stabilized)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain steps (2 bits)	Gain control bits = 0b00 at dc		1.33		V/V
	Gain control bits = 0b01		2		
	Gain control bits = 0b10		5		
	Gain control bits = 0b11		20		
Gain bandwidth product			350		kHz
Noise density(1)	f = 0.1 Hz to 100 Hz at gain = 5 V/V, across temperature		110		nV/√Hz
Input offset voltage			95		µV
Input bias current			5		nA
Frequency response	Gain = 20 V/V, <100 Hz			0.335	%V/V

(1) Total input-referred noise including gain noise, ADC reference noise, ADC thermal noise, and ADC quantization noise

Electrical Characteristics – T Gain (Chopper Stabilized) (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common mode voltage range			Depends on selected gain and current supply (2)		
Common-mode rejection ratio	f_{CM} = 50 Hz		110		dB
Input impedance		1			MΩ

(2) **Common Mode at T Gain Input and Output:** There are two constraints:
(a) The single-ended voltage of positive/negative pin at the T gain input should be between 5 m V and 1.8 V
(b) The single-ended voltage of positive/negative pin at the T gain output should be between 0.1 V and 2 V

6.14 Electrical Characteristics – T Analog-to-Digital Converter

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Sigma-delta modulator frequency			1		MHz
	ADC voltage input range		–2.5		2.5	V
	Number of bits			16		bits
	ADC 2s complement code for –2.5-V differential input	2s complement		8000_{hex}		LSB
	ADC 2s complement code for 0-V differential input			0000_{hex}		LSB
	ADC 2s complement code for 2.5-V differential input			$7FFF_{hex}$		LSB
INL	Integral nonlinearity				±0.5	LSB

6.15 Electrical Characteristics – One-Wire Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Communication Baud Rate (1)		600		9600	bits per second
OWI_ENH	OWI activation high		5.95			V
OWI_ENL	OWI activation low				5.75	V
OWI_VIH	OWI transceiver Rx threshold for high		4.8		5.1	V
OWI_VIL	OWI transceiver Rx threshold for low		3.9		4.2	V
OWI_IOH	OWI transceiver Tx threshold for high		500		1379	µA
OWI_IOL	OWI transceiver Tx threshold for low		2		5	µA

(1) **OWI over power line does not work if there is an LDO between the supply to the sensor and the PWR pin, or if the OWI high and low voltages are greater than the regulated voltage.**

6.16 Electrical Characteristics – DAC Output

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC reference voltage	Reference bit = 1		1.25		V
	Reference bit = 0 (ratiometric)		0.25 × V_{PWR}		
DAC resolution			14		bits

6.17 Electrical Characteristics – DAC Gain

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Buffer gain (see Figure 16)	2×		2		V/V
	4×		4		
	6.67×		6.67		
	10×		10		

Electrical Characteristics – DAC Gain (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Current loop gain			1001		mA/mA
	Gain-bandwidth product			1		MHz
	Zero-code voltage (gain = 4×)	DAC code = 0000h, I_{DAC} = 2.5 mA			20	mV
	Full-code voltage (gain = 4×)	DAC code is 1FFFh, I_{DAC} = –2.5 mA	4.8			V
	Output current	DAC code = 1FFFh , DAC code = 0000h			±2.5	mA
	Short-circuit source current	DAC code = 1FFFh		27		mA
	Short-circuit sink current	DAC code = 0000h		27		mA
	Maximum capacitance	Without compensation			100	pF
		With compensation			100	nF

6.18 Electrical Characteristics – Non-Volatile Memory

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EEPROM	Size			128		Bytes
	Erase-write cycles				1000	Cycles
	Programming time	1 8-byte page			8	ms
	Data retention		10			Years

6.19 Electrical Characteristics – Diagnostics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSC_PWR_OV	Oscillator circuit supply overvoltage threshold			3.3		V
OSC_PWR_UV	Oscillator circuit supply undervoltage threshold			2.7		V
BRG_OV	Resistive bridge sensor supply overvoltage threshold			10		%. V_{BRG}
BRG_UV	Resistive bridge sensor supply undervoltage threshold			–10		%Prog. V_{BRG}
AVDD_OV	AVDD overvoltage threshold			3.3		V
AVDD_UV	AVDD undervoltage threshold			2.7		V
DVDD_OV	DVDD overvoltage threshold			2		V
DVDD_UV	DVDD undervoltage threshold			1.53		V
REF_OV	Reference overvoltage threshold			2.75		V
REF_UV	Reference undervoltage threshold			2.25		V

Electrical Characteristics – Diagnostics (continued)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
P_DIAG_PU	P gain input diagnostics pulldown resistor value			PD2	PD1				MΩ
				0	0		1		
				0	1		2		
				1	0		3		
				1	1		4		
INP_OV	P gain input overvoltage threshold value	INP+ and INP– each has threshold comparator	THRS[2]	THRS[1]	THRS[0]				% V_{BRG}
		V_{BRG} = 2.5 V	0	0	0		72.5		
			0	0	1		70		
			0	1	0		65		
		V_{BRG} = 2 V	0	1	1		90		
			1	0	0		87.5		
			1	0	1		82.5		
		V_{BRG} = 1.25 V	1	1	0		100		
			1	1	1		95		
INP_UV	P gain input undervoltage threshold value	INP+ and INP– each has threshold comparator	THRS[2]	THRS[1]	THRS[0]				% V_{BRG}
		V_{BRG} = 2.5 V	0	0	0		7.5		
			0	0	1		10.0		
			0	1	0		15.0		
		V_{BRG} = 2.V	0	1	1		10.0		
			1	0	0		12.5		
			1	0	1		17.5		
		V_{BRG} = 1.25 V	1	1	0		17.5		
			1	1	1		22.5		
INT_OV	T gain input overvoltage	INT+ and INT– each has threshold comparator					2.1		V
PGAIN_OV	Output overvoltage (single-ended) threshold for P gain						2.25		V
PGAIN_UV	Output undervoltage (single-ended) threshold for P gain						0.15		V
TGAIN_OV	Output overvoltage (single-ended) threshold for T gain						2.25		V
TGAIN_UV	Output undervoltage (single-ended) threshold for T gain						0.15		V
HARNESS_FAULT1	Open-wire leakage current 1. Open PWR with pullup on OUT						2		µA
HARNESS_FAULT2	Open-wire leakage current 2. Open GND with pulldown on OUT						20		µA

6.20 Operating Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time (1)	No IIR filter,		180		µs
Start-up time (2)	IIR filter = 1000 Hz		1158		µs
Output rate			128		µs
Response time (3)	No IIR filter		211		µs
Response time (4)	IIR filter = 1000 Hz		1050		µs
Absolute-voltage mode, overall accuracy (PGA300 only, no sense element) (5)	3 pressure - 1 temperature calibration, overall accuracy calculated using points different from points used for calibration		0.2		%FSO
	3 pressure - 3 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration		0.1		%FSO
	4 pressure - 4 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration		0.08		%FSO
Ratiometric-voltage mode, overall accuracy (PGA300, no sense element) (5)	3 pressure - 1 temperature calibration, overall accuracy calculated using points different from points used for calibration		0.5		%FSO
	3 pressure - 3 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration		0.25		%FSO
	4 pressure - 4 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration		0.2		%FSO
Current mode, overall accuracy (PGA300, no sense element) (5)	3 pressure - 1 temperature calibration, overall accuracy calculated using points different from points used for calibration		0.2		%FSO
	3 pressure - 3 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration		0.1		%FSO
	4 pressure - 4 temperature calibration, input voltage not subject to temperature variation, overall accuracy calculated using points different from points used for calibration		0.09		%FSO

(1) Time from power up to reach 90% of valid output
(2) Time from power up to reach valid output, including settling time
(3) Time to reach 90% of valid output
(4) Time to reach valid output, including settling time
(5) Sense element held at constant temperature while the PGA300 device was calibrated at –25ºC, 25ºC, 85ºC and 125ºC. Accuracy was then measured at –40ºC, 50ºC and 150 ºC.

6.21 Typical Characteristics

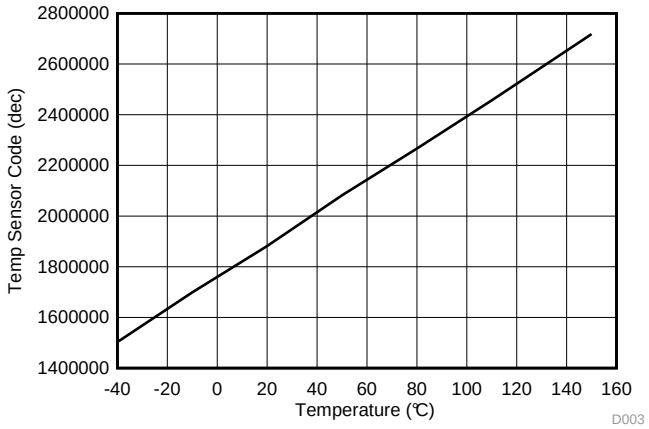


Figure 1. Temperature Sensor Code vs Temperature

7 Detailed Description

7.1 Overview

The PGA300 device can be used in a variety of applications. The most common ones are for pressure and temperature measurement. Depending on the application, the device itself can be configured in different modes. The following sections provide details regarding these configurations.

The PGA300 device is a high-accuracy, low-drift, low-noise, low-power, and easily programmable signal-conditioner device for resistive bridge pressure and temperature sensing applications. The PGA300 device implements a third-order temperature coefficient (TC) and nonlinearity (NL) algorithm to linearize the analog output. The PGA300 device accommodates various sensing element types, such as piezoresistive, ceramic film, and steel membrane. It supports the sensing element spans from 1 mV/V to 135 mV/V. The typical applications supported are pressure sensor transmitter, transducer, liquid-level meter, flow meter, strain gauge, weight scale, thermocouple, thermistor, 2-wire resistance thermometer (RTD), and resistive field transmitters. The device can also be used in accelerometer and humidity sensor signal-conditioning applications.

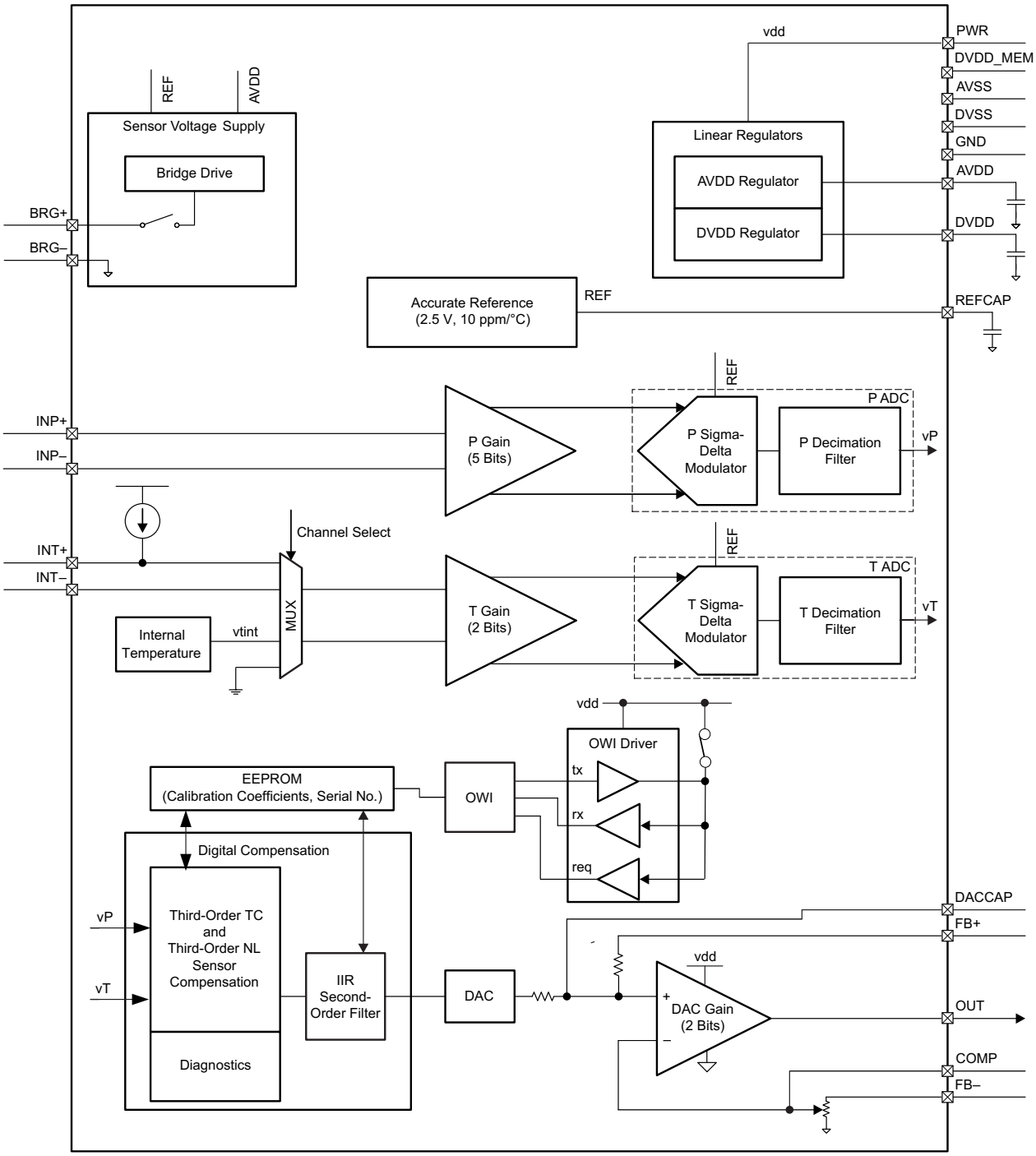
The PGA300 device provides bridge excitation voltages of 2.5 V, 2 V, and 1.25 V, all ratiometric to the ADC reference level. The PGA300 device has the unique one-wire interface (OWI) that supports communication and configuration through the power-supply line during the calibration process. This feature minimizes the number of wires needed for an application.

The PGA300 device contains two separated analog front-end (AFE) chains for resistive-bridge inputs and temperature-sensing inputs. Each AFE chain has its own gain amplifier and a 16-bit ADC at a 7.8-kHz output rate. The resistive-bridge input AFE chain consists of a programmable gain with 32 steps from 5 V/V to 400 V/V. For the temperature-sensing AFE input chain, the PGA300 device provides a current source that can supply up to 500 µA for optional external temperature sensing. This current source can also be used as constant-current bridge excitation. The programmable gain in the temperature sensing chain has four steps from 1.33 V/V to 20 V/V. In addition, the PGA300 device integrates an internal temperature sensor which can be configured as the input of the temperature-sensing AFE chain.

A 128-byte EEPROM is integrated in the PGA300 device to store the calibration coefficients and the PGA300 configuration settings as needed. The PGA300 device has a 14-bit DAC followed by a buffer gain stage of 2 V/V to 10 V/V. The device supports industrial-standard ratiometric-voltage output, absolute-voltage output, and 4-mA to 20-mA current loop.

The diagnostic function monitors the operating condition of the PGA300 device. The device can operate with a 3.3-V to 30-V power supply directly, without using an external LDO. The PGA300 device has a wide ambient-temperature operating range from –40°C to 150°C. The package form is 6-mm × 6-mm 36-pin VQFN. Within this small package size, the PGA300 device has integrated all the functions needed for resistive-bridge sensing applications to minimize PCB area and simplify the overall application design.

7.2 Functional Block Diagram



7.3 Feature Description

This section describes individual functional blocks of the PGA300 device.

7.3.1 Reverse-Voltage Protection Block

The PGA300 device includes a reverse-voltage protection block. This block protects the device from reverse-battery conditions on the external power supply.

7.3.2 Linear Regulators

The PGA300 device has two main linear regulators: an AVDD regulator and a DVDD regulator. The AVDD regulator provides the 3-V voltage source for internal analog circuitry, whereas the DVDD regulator provides the 1.8-V regulated voltage for the digital circuitry. The user must connect bypass capacitors of 100 nF each on the AVDD and DVDD pins of the device.

7.3.3 Internal Reference

The PGA300 device has two internal references. These references are described in the following subsections.

7.3.3.1 High-Voltage Reference

The high-voltage reference is an inaccurate reference used in the diagnostic thresholds.

7.3.3.2 Accurate Reference

The accurate reference is used to generate reference voltage for the P ADC, T ADC and DAC. TI recommends placing a 100-nF capacitor on the REFCAP pin to limit the bandwidth of reference noise.

The accurate reference buffer can be disabled by setting the ADC_EN_VREF bit in the ALPWR register to 0. This allows the user to connect an external single-ended reference voltage to the REFCAP pin and thus provide the reference voltage to the ADCs and the DAC. Note that the default power-up state of ADC_EN_VREF is such that the reference buffer is disabled.

NOTE

The accurate reference is valid 50 µs after digital core starts running at power up.

7.3.4 BRG+ to BRG– Supply for the Resistive Bridge

The sensor voltage-supply block of the PGA300 device supplies power to the resistive-bridge sensor. The sensor supply in the PGA300 device is configurable to a 2.5-V, 2-V, or 1.25-V nominal output supply using the BRG_CTRL bits in BRG_CTRL register to accommodate bridge sense elements with different resistor values. This nominal supply is ratiometric to the accurate reference as shown in Figure 2.

Feature Description (continued)

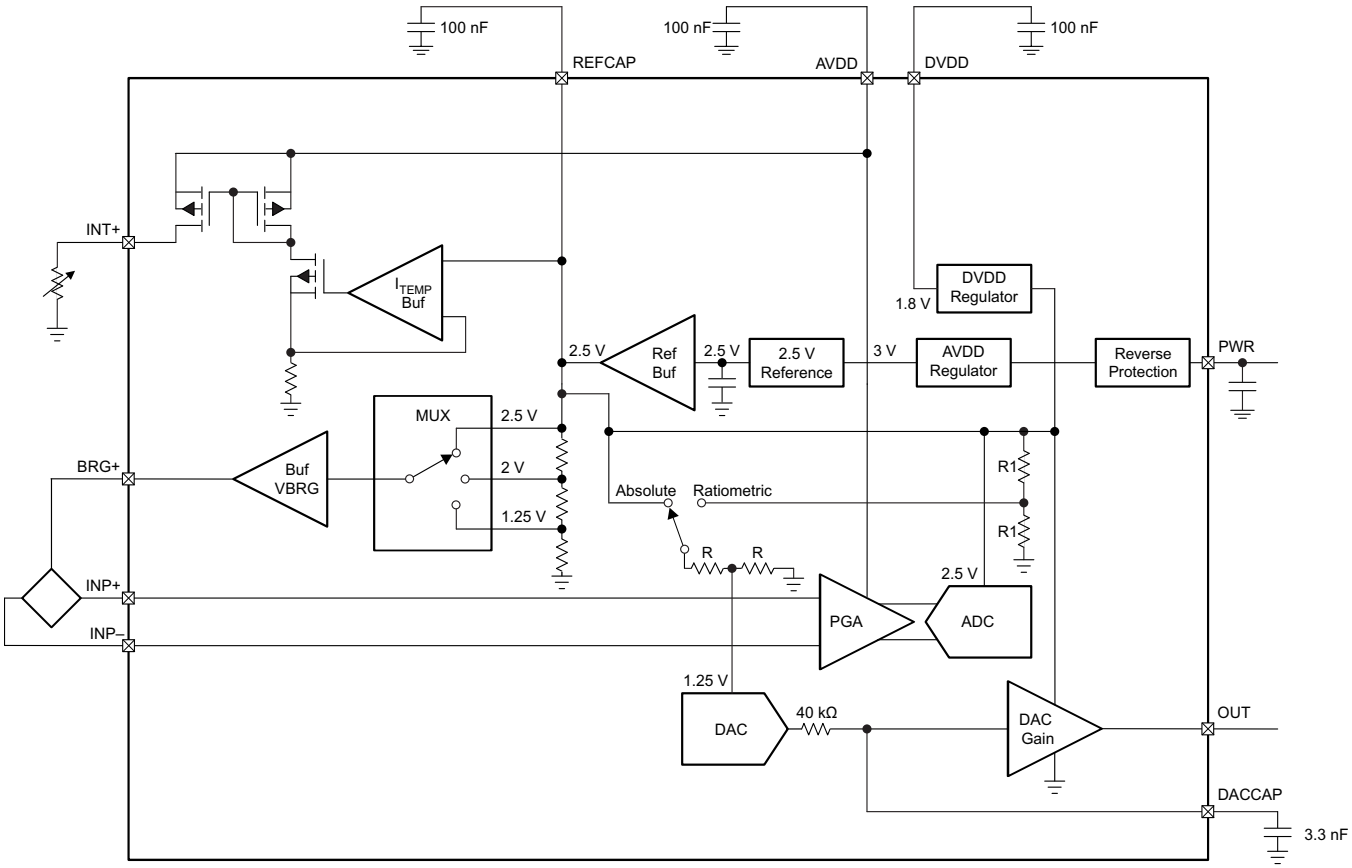


Figure 2. Bridge Supply and P ADC Reference Are Ratiometric

The sensor drive includes a switch. This switch can be used to turn off power to the sense element.

7.3.5 ITEMP Supply for the Temperature Sensor

The ITEMP block in PGA300 device supplies programmable current to an external temperature sensor such as an RTD temperature probe or NTC or PTC thermistor. The temperature-sensor current source is ratiometric to the accurate reference.

The value of the current can be programmed using the ITEMP_CTRL bits in the TEMP_CTRL register.

7.3.6 Internal Temperature Sensor

PGA300 device includes an internal temperature sensor whose voltage output is digitized by the T ADC and made available to the microprocessor. This digitized value is used to implement temperature compensation algorithms in software. Note that the voltage generated by the internal temperature sensor is proportional to the junction temperature.

Feature Description (continued)

Figure 3 shows the internal temperature sensor AFE.

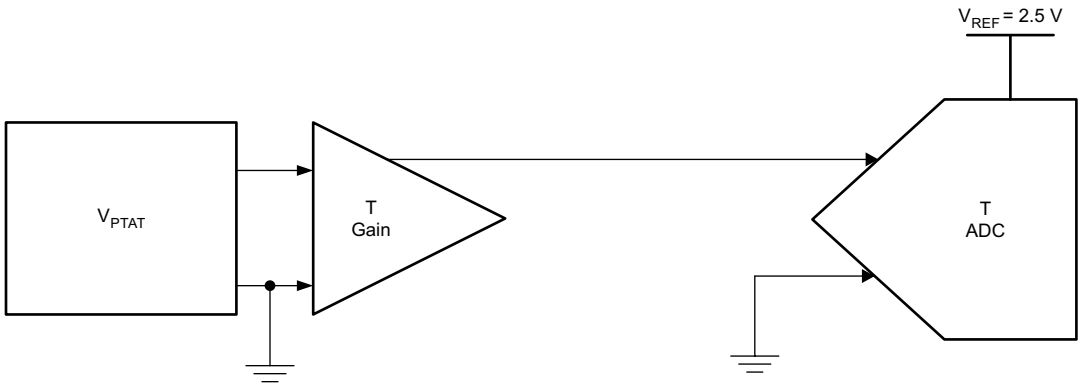


Figure 3. Temperature Sensor AFE

7.3.7 P Gain

P gain is designed with precision, low-drift, low-flicker-noise, chopper-stabilized amplifiers. P gain is implemented as an instrument amplifier as shown in Figure 4.

The gain of this stage is adjustable using 5 bits in the P_GAIN_SELECT register to accommodate sense elements with a wide range of signal spans.

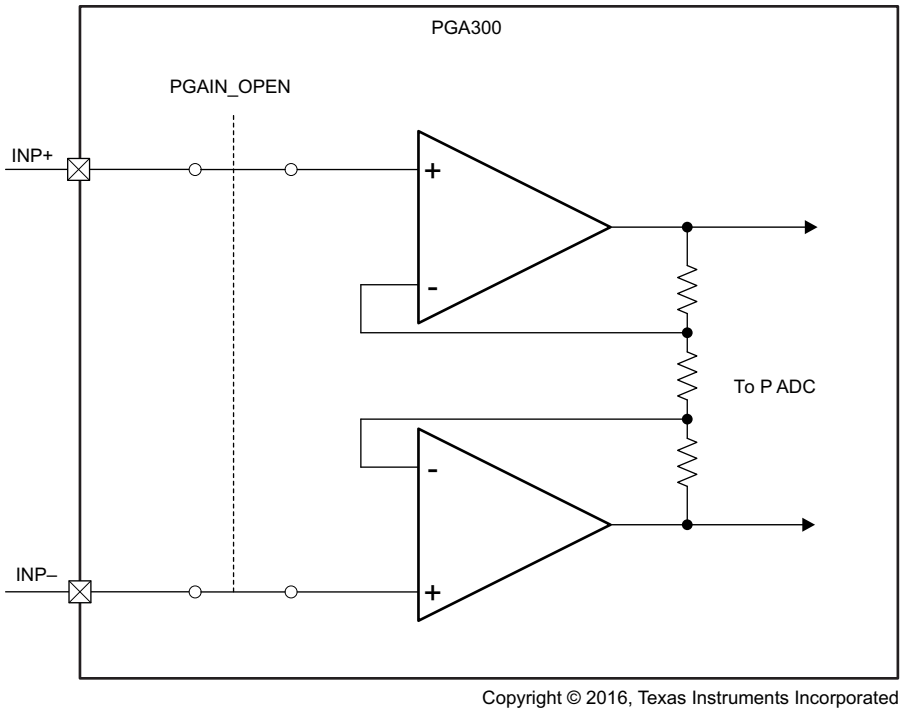


Figure 4. P Gain

7.3.8 P Analog-to-Digital Converter

The P analog-to-digital converter digitizes the voltage output of the P-gain amplifier.

7.3.8.1 P Sigma-Delta Modulator for P ADC

The sigma-delta modulator for P ADC is a 1-MHz, second-order, 3-bit quantizing sigma-delta modulator.

Feature Description (continued)

7.3.8.2 P Decimation Filter for P ADC

The pressure signal path output conversion time is 128 µs or an output rate of 7.8125 ksamples/s.

The output of the decimation filter in the pressure signal path is a 16-bit *signed* value. Some example decimation output codes for given differential voltages at the input of the sigma-delta modulator are shown in Table 1.

Table 1. Input Voltage to Output Counts for the P ADC

SIGMA-DELTA MODULATOR DIFFERENTIAL INPUT VOLTAGE (V)	16-BIT NOISE-FREE DECIMATOR OUTPUT
–2.5	–32 768 (0x8000)
–1.25	–16 384 (0xC000)
0	0 (0x0000)
1.25	16 383 (0x3FFF)
2.5	32 767 (0x7FFF)

7.3.9 T Gain

The device has the ability to perform temperature compensation via an internal or external temperature sensor. The user can select the source of the temperature measurement with the TEMP_MUX_CTRL bits in TEMP_CTRL register. Note that the device connects to an external temperature sensor via the INT+ and INT– pins.

The T gain block is constructed with a low-flicker-noise, low-offset, chopper-stabilized amplifier. The gain is configurable with 2 bits in the T_GAIN_SELECT register. Figure 5 shows the T-gain amplifier topology.

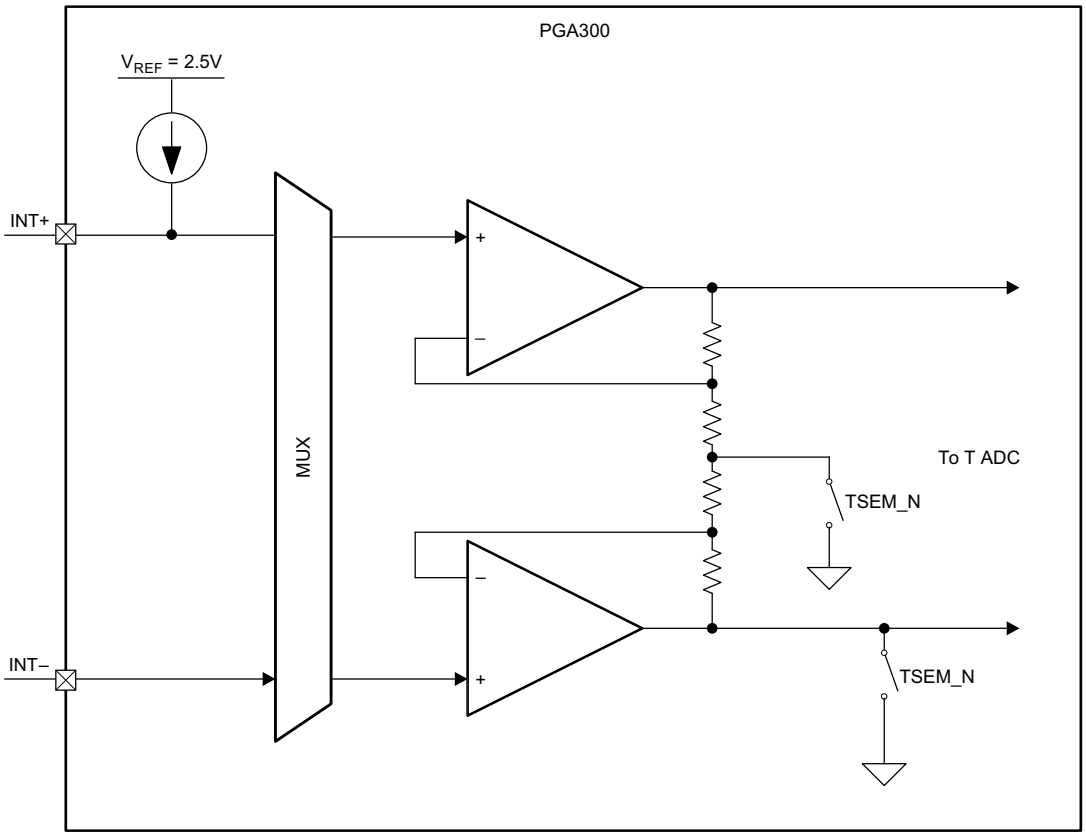


Figure 5. Temperature Sensor AFE

The T-gain amplifier can be configured for single-ended or differential operation using the TSEM_N bit in the AMUX_CTRL register. Note that when the T-gain amplifier is set up for single-ended operation, the differential voltage converted by the T ADC is with respect to ground. Table 2 shows the configuration that the user must select for the different temperature sources.

Table 2. T-Gain Configuration

TEMPERATURE SOURCE	T GAIN CONFIGURATION
Internal temperature sensor	Single-ended
External temperature sensor with one terminal of the sensor connected to ground	Single-ended
External temperature sensor with neither terminal of the sensor connected to ground	Differential

The T-gain amplifier must be set up for either the single-ended or differential configuration, depending on the source of signal to the T gain.

NOTE

When T GAIN is configured to measure the internal temperature-sensor output, T GAIN must be configured to operate in single-ended mode and with a gain of 5 V/V.

7.3.10 T Analog-to-Digital Converter

The T analog-to-digital converter is for digitizing the T-gain amplifier output. The digitized value is available in the TADC_DATA2 and TADC_DATA3 registers.

7.3.10.1 T Sigma-Delta Modulator for T ADC

The sigma-delta modulator for T ADC is a 1-MHz, second-order, 3-bit quantizing sigma-delta modulator.

7.3.10.2 T Decimation Filters for T ADC

The temperature signal path contains a decimation filter with an internal output rate of 128 µs.

The output of the decimation filter in the temperature signal path is 16-bit **signed** value. Some example decimation output codes for given differential voltages at the input of the sigma-delta modulator are shown in Table 3.

Table 3. Input Voltage to Output Counts for T ADC

SIGMA-DELTA MODULATOR DIFFERENTIAL INPUT VOLTAGE	16-BIT NOISE-FREE DECIMATOR OUTPUT
–2.5 V	–32 768 (0x8000)
–1.25 V	–16 384 (0xC000)
0 V	0 (0x0000)
1.25 V	16 383 (0x3FFF)
2.5 V	32 767 (0x7FFF)

The nominal relationship between the device junction temperature and 16-bit T ADC code for T GAIN = 5 V/V is shown in Equation 1

$$\text{T ADC code} = 25.9 \times \text{TEMP} + 6680 \quad (1)$$

where

TEMP is temperature in °C.

7.3.11 P GAIN and T GAIN Calibration

The P_GAIN value should be set based on the maximum bridge output voltage. The maximum bridge voltage is the maximum sum of bridge offset and bridge span across the entire operating temperature range.

The T GAIN value should be set based on the temperature sense element. The specific values to be used are:

- For the internal temperature sensor, set T_GAIN to 5 V/V gain
- For an external temperature sensor such as a PTC thermistor, set T_GAIN to 20 V/V gain

7.3.12 One-Wire Interface (OWI)

The device includes an OWI digital communication interface. The function of OWI is to enable writes to and reads from all memory locations inside the PGA300 device that are available for OWI access.

7.3.12.1 Overview of OWI

The OWI digital communication is a master-slave communication link in which the PGA300 device operates as a slave device only. The master device controls when data transmission begins and ends. The slave device does not transmit data back to the master until it is commanded to do so by the master.

The PWR pin of PGA300 device is used as OWI interface, so that when the PGA300 device is embedded inside of a system module, only two pins are needed (PWR and GND) for communication. The OWI master communicates with the PGA300 device by modulating the voltage on the PWR pin, whereas the PGA300 device communicates with the master by modulating the current on the PWR pin. The OWI master activates OWI communication by generating an activation pulse on the PWR pin.

Figure 6 shows a functional equivalent circuit for the structure of the OWI circuitry.

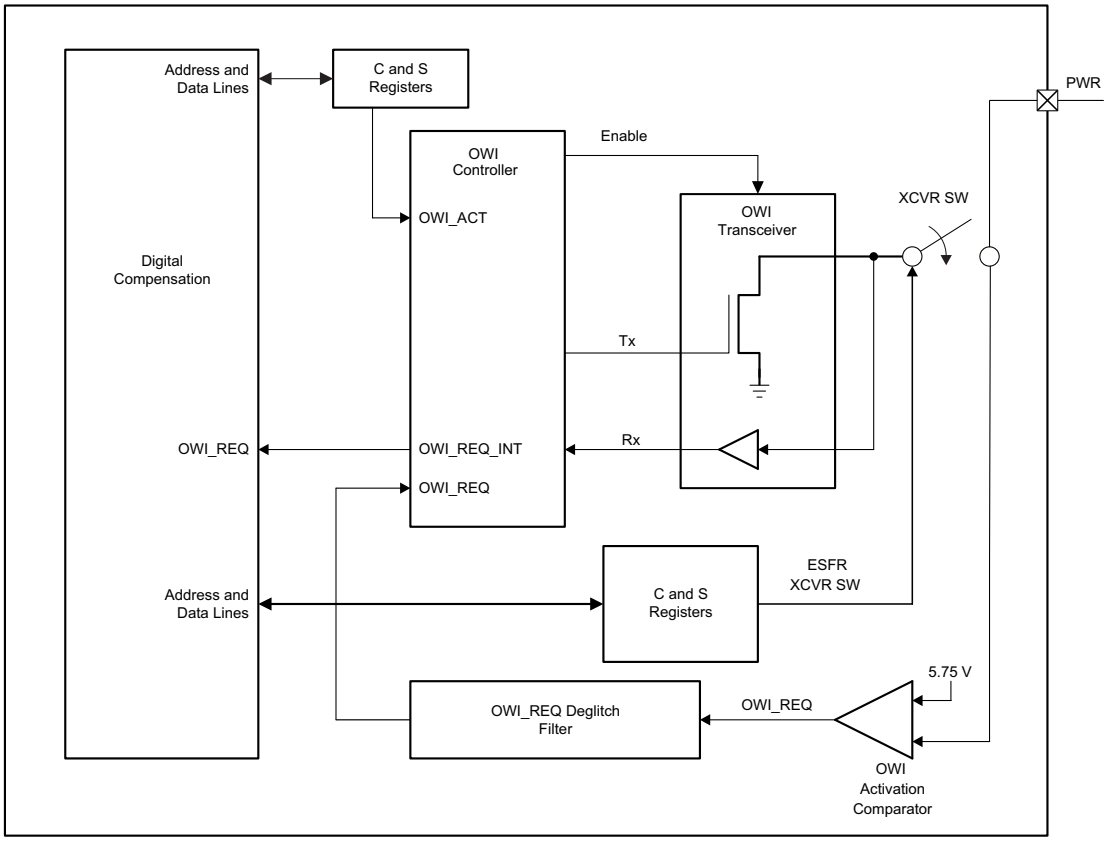


Figure 6. OWI System Components

7.3.12.2 Activating and Deactivating the OWI Interface

7.3.12.2.1 Activating OWI Communication

The OWI master initiates OWI communication by generating an **OWI activation-pulse sequence** on the PWR pin. When the PGA300 device receives a valid OWI activation-pulse sequence, it prepares itself for OWI communication. Notice that after the valid OWI activation-pulse sequence is received, the logic checks on the EEPROM lock status. If the EEPROM is locked, the sequence 0x5555 must be sent within 100 ms after the end of the activation-pulse sequence.

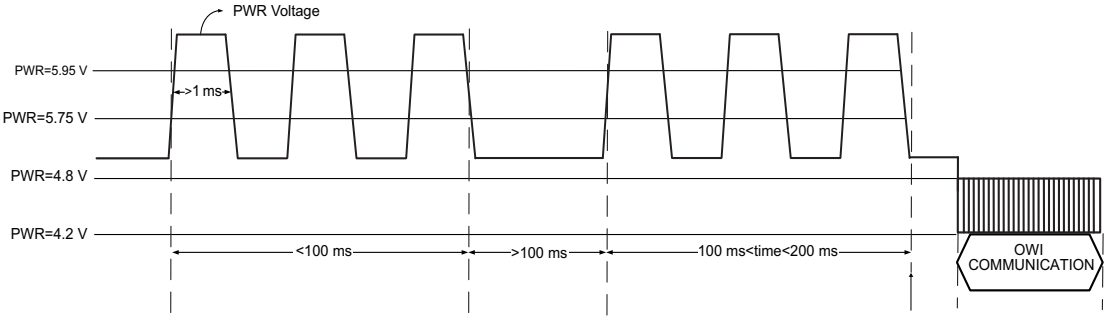


Figure 7. OWI Activation Using Overvoltage Drive

7.3.12.2.2 Deactivating OWI Communication

In order to deactivate OWI communication and restart the compensation engine inside the PGA300 device (if it was in reset), the following two steps must be performed by the OWI master:

- The OWI_XCR_EN bit in the DIG_IF_CTRL register must be set to 0. This turns off the OWI transceiver.
- The compensation engine reset should be de-asserted by writing 0 to the COMPENSATION_RESET bit in the COMPENSATION_CONTROL register.

7.3.12.3 OWI Protocol

7.3.12.3.1 OWI Frame Structure

7.3.12.3.1.1 Standard Field Structure

Data is transmitted on the one-wire interface in byte-sized packets. The first bit of the OWI field is the start bit. The next 8 bits of the field are data bits to be processed by the OWI control logic. The final bit in the OWI field is the stop bit. A group of fields make up a transmission frame. A transmission frame is composed of the fields necessary to complete one transmission operation on the one-wire interface. The standard field structure for a one-wire field is shown in Figure 8

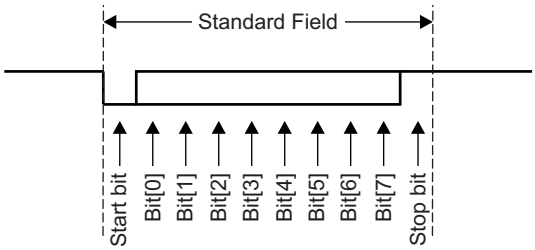


Figure 8. Standard OWI Field

7.3.12.3.1.2 Frame Structure

A complete one-wire data transmission operation is done in a frame with the structure is shown in Figure 9.

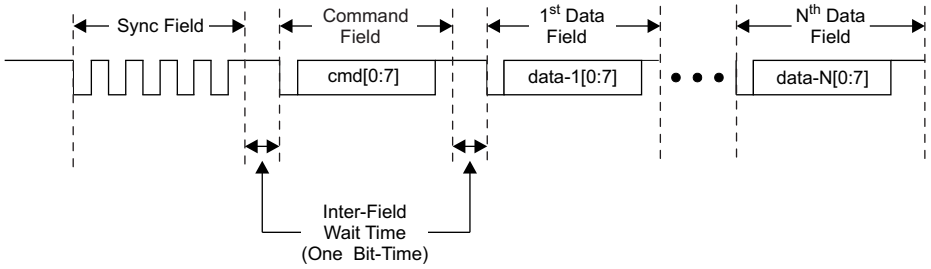


Figure 9. OWI Transmission Frame, N = 1 to 8

Each transmission frame must have a synchronization field and a command field followed by zero to a maximum of eight data fields. The sync field and command fields are always transmitted by the master device. The data fields may be transmitted either by the master or the slave, depending on the command given in the command field. It is the command field which determines direction of travel of the data fields (master-to-slave or slave-to-master). The number of data fields transmitted is also determined by the command in the command field. The inter-field wait time is optional and may be necessary for the slave or the master to process data that has been received.

NOTE

If the OWI remains idle in either the logic-0 or logic-1 state for more than 15 ms, then the PGA300 communication resets and requires a sync field as the next data transmission from the master.

7.3.12.3.1.3 Sync Field

The sync field is the first field in every frame that is transmitted by the master. The sync field is used by the slave device to compute the bit width transmitted by the master. This bit width is used to receive accurately all subsequent fields transmitted by the master. The format of the sync field is shown in Figure 10.

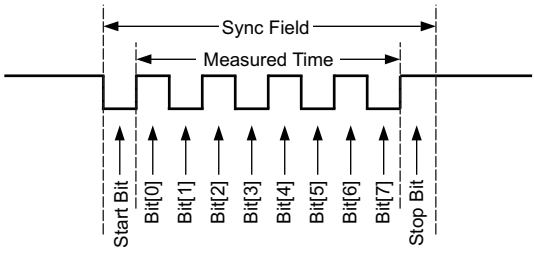


Figure 10. OWI Sync Field

NOTE

Consecutive sync-field bits are measured and compared to determine if a sync field is being transmitted to the PGA300 device is valid. If the difference in bit widths of any two consecutive SYNC field bits is greater than ±25%, then the PGA300 device ignores the rest of the OWI frame; that is, the PGA300 device does not respond to the OWI message.

7.3.12.3.1.4 Command Field

The command field is the second field in every frame sent by the master. The command field contains instructions about what to do with and where to send the data that is transmitted to the slave. The command field can also instruct the slave to send data back to the master during a read operation. The number of data fields to be transmitted is also determined by the command in the command field. The format of the command field is shown in Figure 11.

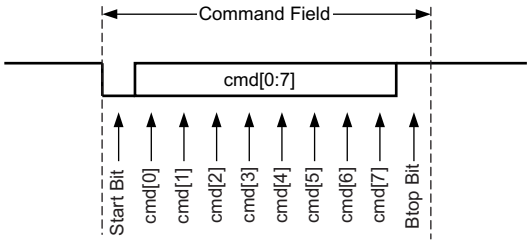


Figure 11. OWI Command Field

7.3.12.3.1.5 Data Fields

After the master has transmitted the command field in the transmission frame, zero or more data fields are transmitted to the slave (write operation) or to the master (read operation). The data fields can be raw EEPROM data or address locations in which to store data. The format of the data is determined by the command in the command field. The typical format of a data field is shown in Figure 12.

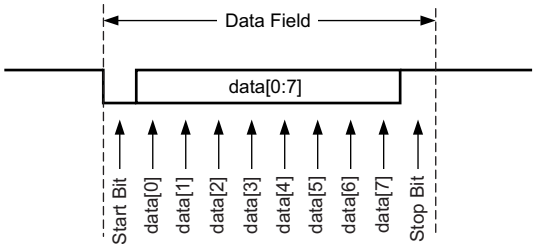


Figure 12. OWI Data Field

7.3.12.3.2 OWI Commands

The following is the list of five OWI commands supported by PGA300:

1. OWI write
2. OWI read initialization
3. OWI read response
4. OWI burst write of EEPROM cache
5. OWI burst read from EEPROM cache

7.3.12.3.2.1 OWI Write Command

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	Basic write command	**0**	P2	P1	P0	0	0	0	1
Data field 1	Destination address	A7	A6	A5	A4	A3	A2	A1	A0
Data field 2	Data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0

The P2, P1, and P0 bits in the command field determine the memory page that is being accessed by the OWI. The memory page decode is shown in Table 4.

Table 4. OWI Memory Page Decode

P2	P1	P0	MEMORY PAGE
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Control and status registers, DI_PAGE_ADDRESS = 0x02
0	1	1	Reserved
1	0	0	Reserved
1	0	1	EEPROM cache
1	1	0	Reserved
1	1	1	Control and status registers, DI_PAGE_ADDRESS = 0x07

7.3.12.3.2.2 OWI Read Initialization Command

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	Read initialization command	**0**	P2	P1	P0	0	0	1	0
Data field 1	Fetch address	A7	A6	A5	A4	A3	A2	A1	A0

The P2, P1, and P0 bits in the command field determine the memory page that is being accessed by the OWI. The memory page decode is shown in Table 4.

7.3.12.3.2.3 OWI Read-Response Command

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	Read-response command	**0**	1	1	1	0	0	1	1
Data field 1	Data retrieved (OWI drives data out)	D7	D6	D5	D4	D3	D2	D1	D0

The P2, P1, and P0 bits in the command field determine the memory page that is being accessed by the OWI. The memory page decode is shown in Table 4.

7.3.12.3.2.4 OWI Burst-Write Command (EEPROM Cache Access)

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	EE_CACHE write-command cache bytes (0–7)	**1**	1	0	1	0	0	0	0
Data field 1	First data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 2	Second data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 3	Third data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 4	Fourth data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 5	Fifth data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 6	Sixth data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 7	Seventh data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0
Data field 8	Eighth data byte to be written	D7	D6	D5	D4	D3	D2	D1	D0

7.3.12.3.2.5 OWI Burst Read Command (EEPROM Cache Access)

FIELD LOCATION	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command field	Burst-read response (8 bytes)	**1**	1	0	1	0	0	1	1
Data field 1	First data byte retrieved EEPROM cache byte 0	D7	D6	D5	D4	D3	D2	D1	D0
Data field 2	Second data byte retrieved EEPROM cache byte 1	D7	D6	D5	D4	D3	D2	D1	D0
Data field 3	Third data byte retrieved EEPROM cache byte 2	D7	D6	D5	D4	D3	D2	D1	D0
Data field 4	Fourth data byte retrieved EEPROM cache byte 3	D7	D6	D5	D4	D3	D2	D1	D0
Data field 5	Fifth data byte retrieved EEPROM cache byte 4	D7	D6	D5	D4	D3	D2	D1	D0
Data field 6	Sixth data byte retrieved EEPROM cache byte 5	D7	D6	D5	D4	D3	D2	D1	D0
Data field 7	Seventh data byte retrieved EEPROM cache byte 6	D7	D6	D5	D4	D3	D2	D1	D0
Data field 8	Eighth data byte retrieved EEPROM cache byte 7	D7	D6	D5	D4	D3	D2	D1	D0

7.3.12.3.3 OWI Operations

7.3.12.3.3.1 Write Operation

The write operation on the one-wire interface is fairly straightforward. The command field specifies the write operation, where the subsequent data bytes are to be stored in the slave, and how many data fields are going to be sent. Additional command instructions can be sent in the first few data fields if necessary. The write operation is illustrated in Figure 13.

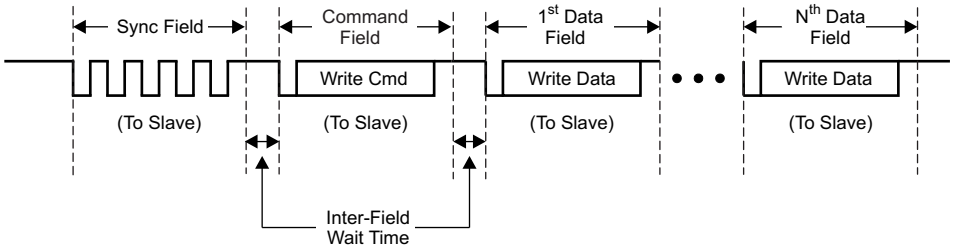


Figure 13. Write Operation, N = 1 to 8

7.3.12.3.3.2 Read Operation

The read operation requires two consecutive transmission frames to move data from the slave to the master. The first frame is the read-initialization frame. It tells the slave to retrieve data from a particular location within the slave device and prepare to send it over the OWI. The data location may be specified in the command field or may require additional data fields for complete data-location specification. The data is not sent until the master commands it to be sent in the subsequent frame called the read-response frame. During the read-response frame, the data direction changes from master → slave to slave → master immediately after the read response command field is sent. Enough time elapses between the command field and data field to allow the signal drivers to change direction. This wait time is 20 µs, and the timer for this wait time is located on the slave device. After this wait time is complete, the slave transmits the requested data. The master device is expected to have switched its signal drivers and is ready to receive data. The read frames are shown in Figure 14.

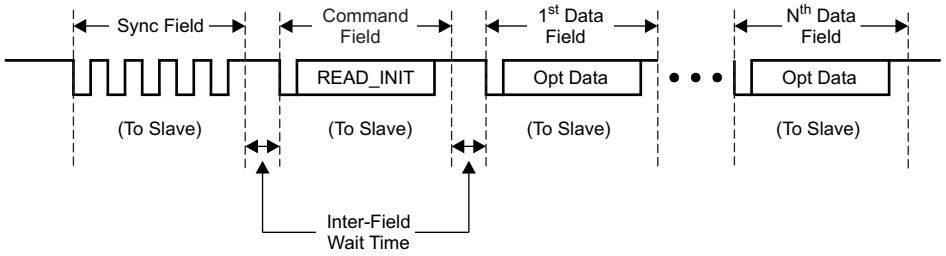


Figure 14. Read-Initialization Frame, N = 1 to 8

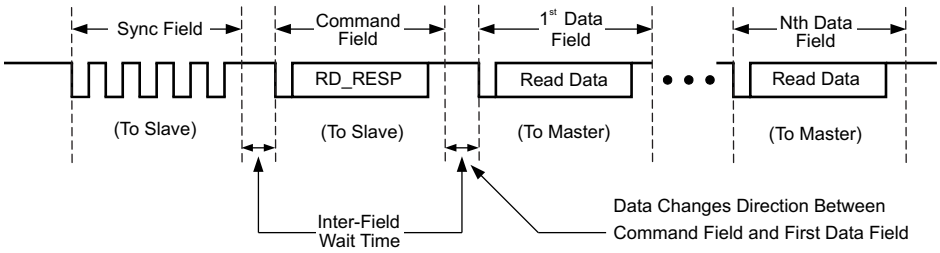


Figure 15. Read-Response Frame, N = 1 to 8

7.3.12.3.3.3 EEPROM Burst Write

The EEPROM burst write is used to write 8 bytes of data to the EEPROM cache using one OWI frame to allow fast programming of EEPROM. Note that the EEPROM page must be selected before transferring the contents of the EEPROM memory cells to the EEPROM cache.

7.3.12.3.3.4 EEPROM Burst Read

The EEPROM burst read is used to read 8 bytes of data from the EEPROM cache using one OWI frame to allow for fast reading of the EEPROM cache contents. The read process is used to verify the writes to the EEPROM cache.

7.3.12.4 OWI Communication-Error Status

The PGA300 device detects errors in OWI communication. The OWI_ERROR_STATUS_LO and OWI_ERROR_STATUS_HI registers contain OWI communication error bits. The communication errors detected include

- Out-of-range communication baud rate
- Invalid SYNC field
- Invalid STOP bits in command and data
- Invalid OWI command

7.3.13 DAC Output

The device includes a 14-bit digital-to-analog converter that produces an absolute output voltage with respect to the accurate reference voltage or a ratiometric output voltage with respect to the PWR supply.

When the microprocessor undergoes a reset, the DAC registers are driven to the 0x000 code.

7.3.13.1 Ratiometric vs Absolute

The DAC output can be configured to be either in ratiometric-to-PWR mode or independent-of-PWR (or absolute) mode using the DAC_RATIOMETRIC bit in DAC_CONFIG.

NOTE

In ratiometric mode, changes in the V_{PWR} voltage result in a proportional change in the output voltage because the current reference for the DAC is derived from V_{PWR}.

7.3.14 DAC Gain

The DAC gain buffer is a configurable buffer stage for the DAC output. The DAC gain amplifier can be configured to operate in voltage amplification mode for voltage output or current amplification mode for 4-mA to 20-mA applications. In voltage output mode, the DAC gain can be configured for a specific gain value by setting the DAC_GAIN bits in the DAC_CONFIG register to a specific value as shown in Figure 16. The DAC gain can be configured to one of four possible gain configurations using the 2-bit DAC_GAIN field.

The final stage of DAC gain is connected to PWR and ground, thus providing the ability to drive the V_{OUT} voltage close to the V_{PWR} voltage.

The DAC gain buffer also implements a COMP pin in order to allow implementing compensation when driving large capacitive loads.

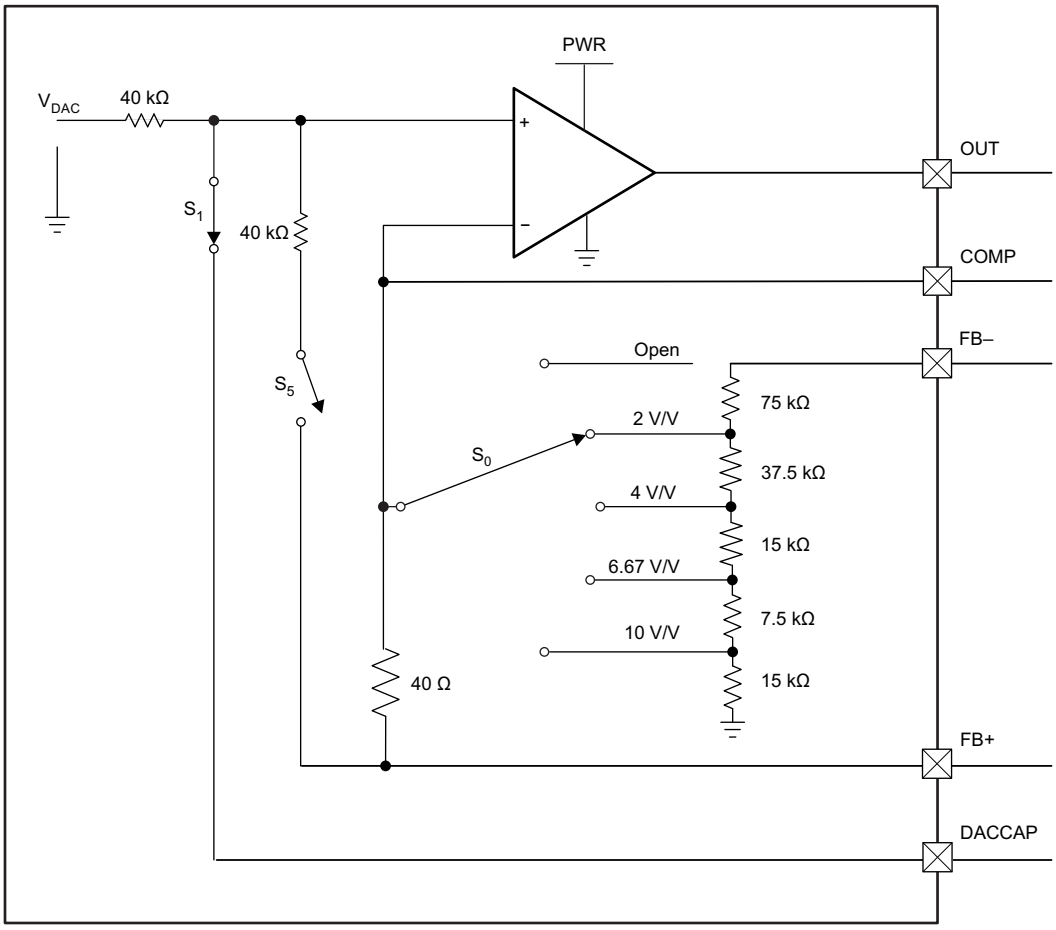


Figure 16. PGA300 Output Buffer

7.3.15 Memory

7.3.15.1 EEPROM Memory

Figure 17 shows the EEPROM structure. The contents of the EEPROM must be transferred to the EEPROM cache before writes; that is, the EEPROM can be programmed 8 bytes at a time. EEPROM reads occur without the EEPROM cache.

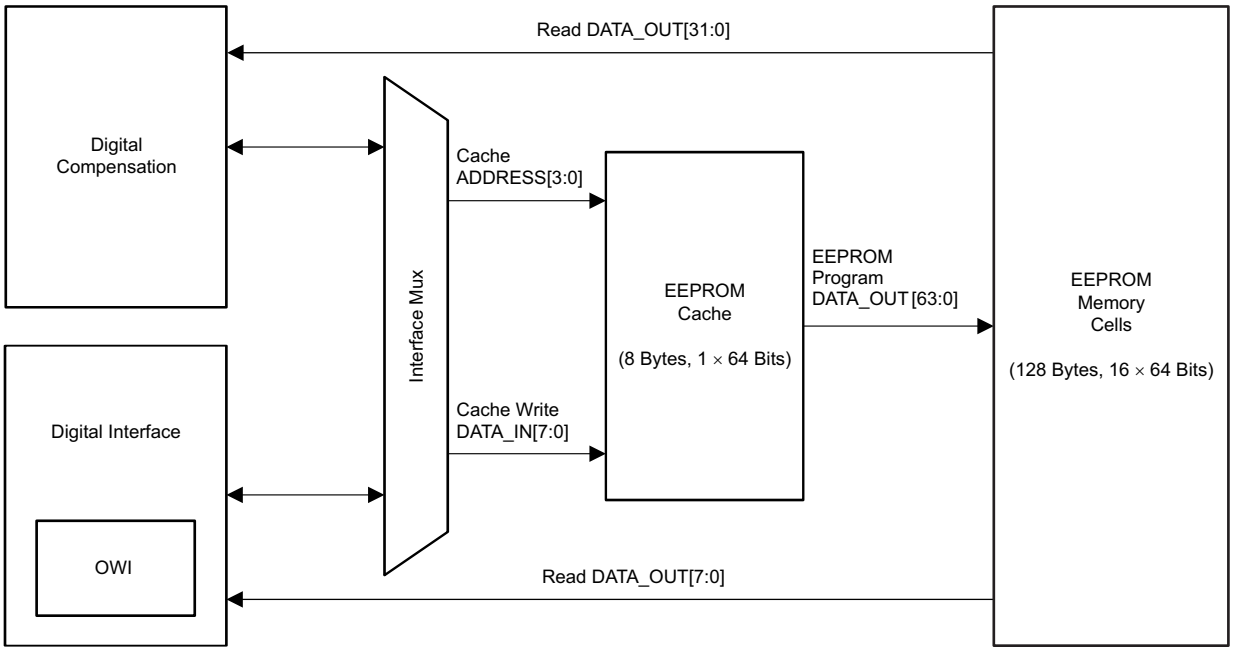


Figure 17. Structure of the EEPROM Interface

7.3.15.1.1 EEPROM Cache

The EEPROM cache serves as temporary storage of data being transferred to selected EEPROM locations during the programming process.

7.3.15.1.2 EEPROM Programming Procedure

For programming the EEPROM, the EEPROM is organized in 16 pages of 8 bytes each. The EEPROM memory cells are programmed by writing to the 8-byte EEPROM cache. The contents of the cache are transferred to EEPROM memory cells by selecting the EEPROM memory page.

1. Select the EEPROM page by writing the upper 4 bits of the 7-bit EEPROM address to the EEPROM_PAGE_ADDRESS register.
2. Load the 8-byte EEPROM cache by writing to the EEPROM_CACHE register. Note that all 8 bytes must be loaded into the EEPROM_CACHE register.
3. Set the ERASE_AND_PROGRAM bit in the EEPROM_CTRL register. Setting this bit automatically erases the selected EEPROM memory page and programs it with the contents of the EEPROM_CACHE register. Alternatively, the user can erase by writing 1 to the ERASE bit in the EEPROM_CTRL register, followed by writing 1 to the PROGAM bit in the EEPROM_CTRL register once the erase is complete. The status of the erase and program operations can be monitored through the EEPROM_STATUS register.

7.3.15.1.3 EEPROM Programming Current

The EEPROM programming process results in an additional 6-mA current on the PWR pin for the duration of programming.

7.3.15.1.4 CRC

The last byte of the EEPROM memory is reserved for the CRC. This CRC value covers all data in the EEPROM memory. Every time the last byte is programmed, the CRC value is automatically calculated and validated. The validation process checks the calculated CRC value with the last byte programmed in the EEPROM memory cell. If the calculated CRC matches the value programmed in the last byte, the CRC_GOOD bit is set in the EEPROM_CRC_STATUS register.

The CRC check can also be initiated at any time by setting the CALCULATE_CRC bit in the EEPROM_CRC register. The status of the CRC calculation is available in the CRC_CHECK_IN_PROG bit in the EEPROM_CRC_STATUS register, whereas the result of the CRC validation is available in the CRC_GOOD bit in the EEPROM_CRC_STATUS register.

The CRC calculation pseudo code is as follows:

```
currentCRC8 = 0xFF; // Current value of CRC8

for NextData

D = NextData;

C = currentCRC8;

  begin

      nextCRC8_BIT0 = D_BIT7 ^ D_BIT6 ^ D_BIT0 ^ C_BIT0 ^ C_BIT6 ^ C_BIT7;

      nextCRC8_BIT1 = D_BIT6 ^ D_BIT1 ^ D_BIT0 ^ C_BIT0 ^ C_BIT1 ^ C_BIT6;

      nextCRC8_BIT2 = D_BIT6 ^ D_BIT2 ^ D_BIT1 ^ D_BIT0 ^ C_BIT0 ^ C_BIT1 ^ C_BIT2 ^ C_BIT6;

      nextCRC8_BIT3 = D_BIT7 ^ D_BIT3 ^ D_BIT2 ^ D_BIT1 ^ C_BIT1 ^ C_BIT2 ^ C_BIT3 ^ C_BIT7;

      nextCRC8_BIT4 = D_BIT4 ^ D_BIT3 ^ D_BIT2 ^ C_BIT2 ^ C_BIT3 ^ C_BIT4;

      nextCRC8_BIT5 = D_BIT5 ^ D_BIT4 ^ D_BIT3 ^ C_BIT3 ^ C_BIT4 ^ C_BIT5;

      nextCRC8_BIT6 = D_BIT6 ^ D_BIT5 ^ D_BIT4 ^ C_BIT4 ^ C_BIT5 ^ C_BIT6;

      nextCRC8_BIT7 = D_BIT7 ^ D_BIT6 ^ D_BIT5 ^ C_BIT5 ^ C_BIT6 ^ C_BIT7;

   end

   currentCRC8 = nextCRC8_D8;

endfor
```

NOTE

The EEPROM CRC calculation is complete 340 µs after the digital core starts running at power up.

7.3.15.2 Control and Status Registers Memory

The digital compensator uses the Control and Status registers to interact with the analog blocks of the device.

7.3.16 Diagnostics

The PGA300 device implements the diagnostics described in the following table:

DIAGNOSTICS DESCRIPTION	ACTION
Digital-compensation-logic execution-timing error	DAC is disabled and compensation logic is set to reset
Digital-compensation-logic checksum error	DAC is disabled and compensation logic is set to reset
EEPROM is corrupted or EEPROM CRC = 0	DAC code is driven to 0 code
Power-supply and signal-chain errors	DAC output is driven to the value determined by the FAULT register in EEPROM

All the foregoing diagnostics can be enabled by setting the DIAG_ENABLE register in EEPROM to a non-zero value. To disable diagnostics, set the DIAG_ENABLE register in EEPROM to 0.

7.3.16.1 Power Supply Diagnostics

The PGA300 device includes circuits to monitor the reference and power supply for faults. Specifically, the following signals are monitored are:

- AVDD voltage

- DVDD voltage
- Bridge supply voltage
- Internal oscillator supply voltage
- Reference output voltage

Electrical Characteristics – Diagnostics lists the voltage thresholds for each of the power rails.

7.3.16.2 Signal Chain Faults

The PGA300 device includes circuits to monitor the P and T signal chains for faults. This section describes the faults monitored by the PGA300 device.

7.3.16.2.1 P Gain and T Gain Input Faults

The PGA300 device includes circuits to monitor for sensor connectivity faults. Specifically, the device monitors the bridge sensor pins for opens (including loss of connection from the sensor), short to ground, and short to sensor supply. The monitoring is accomplished by comparing the voltage at INP+ and INP– pins with the overvoltage and undervoltage thresholds described in Electrical Characteristics – Diagnostics.

The device also includes an overvoltage monitor at the INT+ and INT– pins through the use of 1-MΩ pullup resistors.

Figure 18 shows the block diagram of the P gain and T gain input faults.

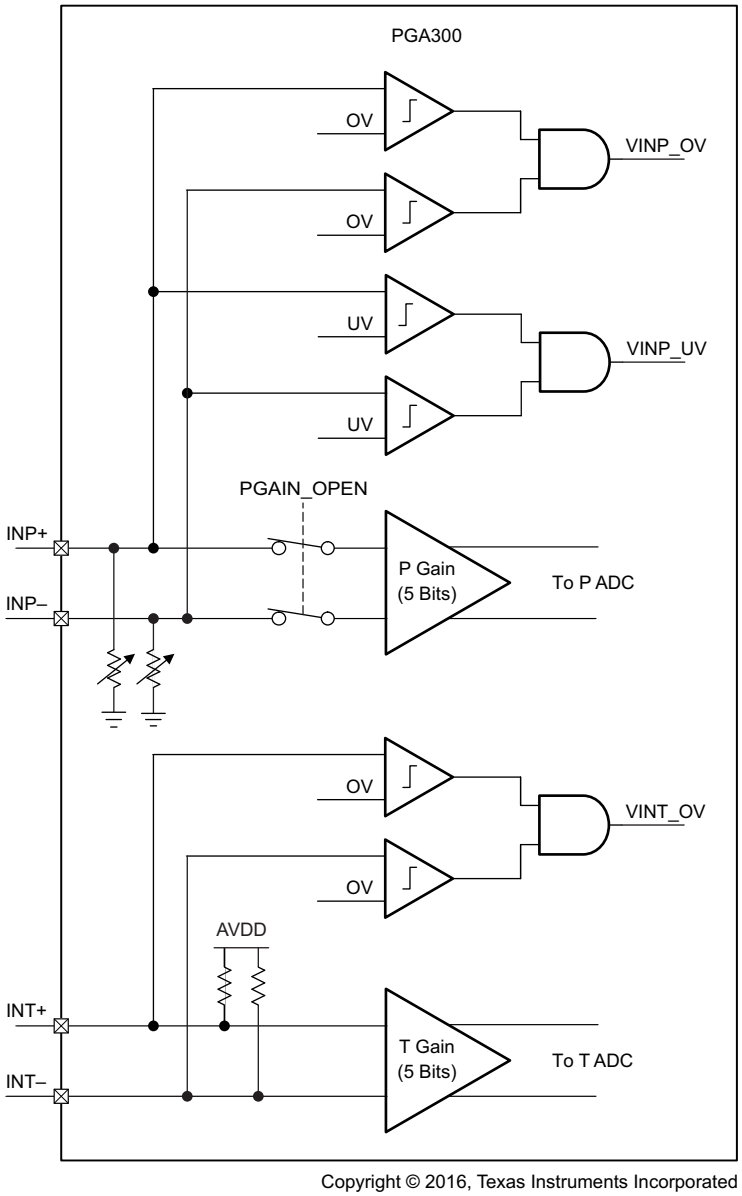


Figure 18. Block Diagram of P Gain and T Gain Diagnostics

The bridge-sensor connectivity faults are detected through the use of an internal pulldown resistor. The value of the pulldown resistor and the threshold can be configured using the AFEDIAG_CFG EEPROM register. Table Table 5 describes the possible configurations.

Table 5. Definition of AFEDIAG_CFG EEPROM Register

BITS	DESCRIPTION
0: PD1 1: PD2	See Electrical Specifications Electrical Characteristics – Diagnostics
2: THRS[0] 3: THRS[1] 4: THRS[2]	See Electrical Specifications Electrical Characteristics – Diagnostics
5: DIS_R_P	1: Disables pulldown resistors used for open and short diagnostics on the INP+ and INP– pins 0: Enables pulldown resistors used for open and short diagnostics on the INP+ and INP– pins

Table 5. Definition of AFEDIAG_CFG EEPROM Register (continued)

6: DIS_R_T	1: Disables pullup resistors used for open and short diagnostics on the INT+ and INT– pins 0: Enables pullup resistors used for open and short diagnostics on the INT+ and INT– pins
7:	—

7.3.16.2.2 P Gain and T Gain Output Diagnostics

The PGA300 device includes modules that verify that the output signal of each gain is within a certain range. This ensures that gain stages in the signal chain are working correctly.

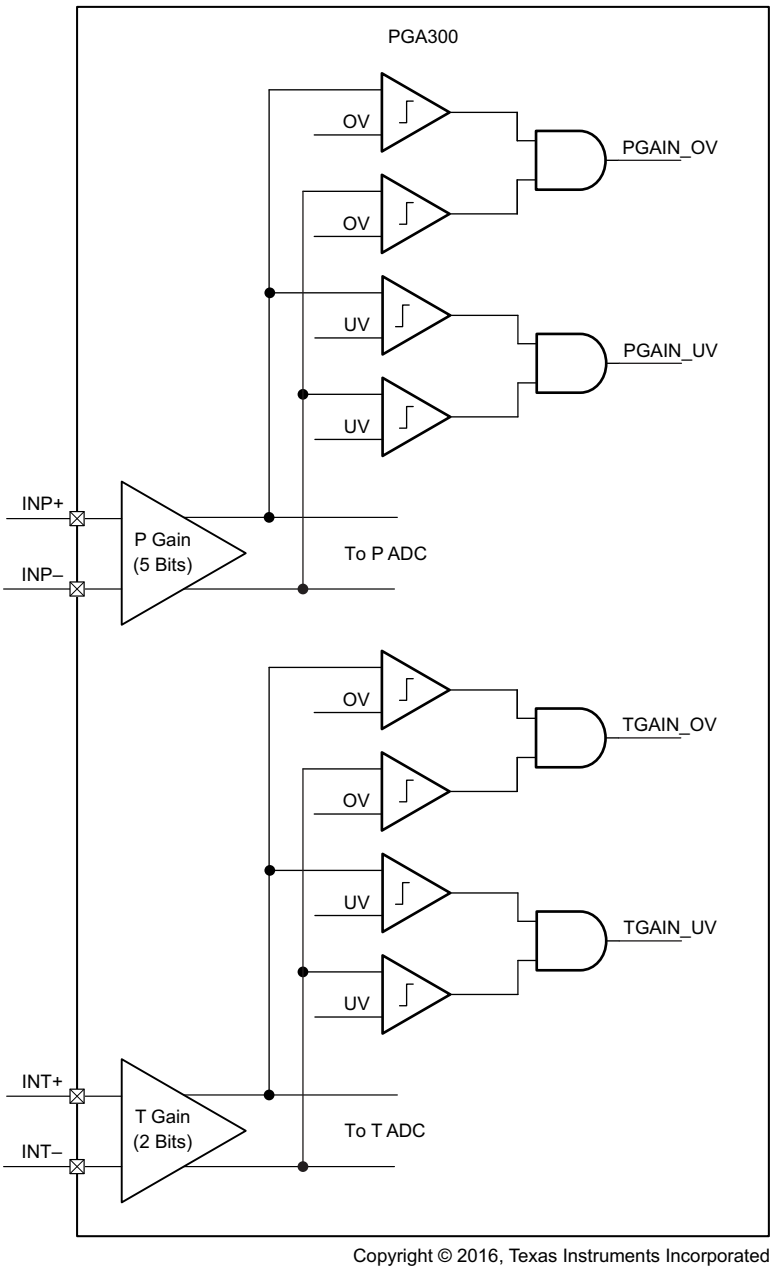


Figure 19. Block Diagram of P Gain and T Gain Output Diagnostics

7.3.16.2.3 Masking Signal Chain Faults

The signal chain diagnostics can be selectively enabled and disabled using the bits in the AFEDIAG_MASK register in EEPROM. Table Table 6 describes the mask bits. Setting a bit to 1 enables detection of the corresponding fault and setting the bit to 0 disables the detection of corresponding fault.

Table 6. Signal Chain Fault Masking Bits

BIT	DESCRIPTION
0	INP+ or INP– overvoltage
1	INP+ or INP– unvervoltage
2	INT+ or INT– overvoltage
3	N/A
4	P GAIN output overvoltage
5	P GAIN output undervoltage
6	T GAIN output overvoltage
7	T GAIN output undervoltage

7.3.16.2.4 Fault Detection Timing

The PGA300 fault-monitoring circuits monitor faults either at power up or periodically. Table 7 describes the fault-detection timing.

Table 7. Fault Detection Timing

FAULT	POWER UP OR RUN TIME	MINIMUM TIME AFTER FAULT OCCURS	MAXIMUM TIME AFTER FAULT OCCURS
Digital-compensation execution-timing error	Run time	500 ms	—
Digital-compensation checksum error	Run time	500 ms	—
EEPROM is corrupted or EEPROM CRC = 0	Power up only (EEPROM is accessed only at power up)	N/A	N/A
Power supply and signal chain errors	Run time	8 ms	16 ms

7.3.17 Digital Compensation and Filter

The PGA300 device implements a third-order TC and NL correction of the pressure and temperature inputs. The corrected output is then filtered using a second-order IIR filter and then written to the DAC as shown in Figure 20.

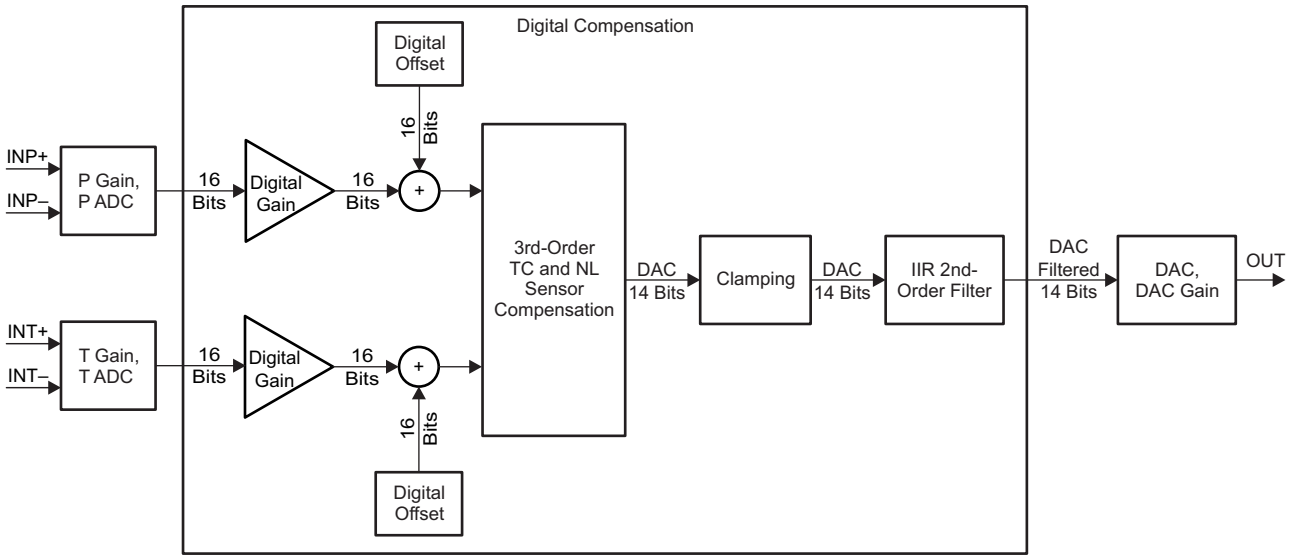


Figure 20. Digital Transfer Block Diagram

7.3.17.1 Digital Gain and Offset

The digital compensation implements digital gain and offset for both pressure and temperature. The equations are:

$P = a_0(P\ ADC + b_0)$

$T = a_1(T\ ADC + b_1)$

where

a_0 and a_1 are the digital gain

b_0 and b_1 are the digital offset

P is the pressure

T is the temperature

P ADC is the pressure digital output

T ADC is the temperature digital output

For high-offset sensors or sensor bridges with a low or high common mode, it may be useful to amplify and offset the P ADC value in the digital domain. The PGA300 device allows the ability to cancel the offset and amplify the signal further before being used in the compensation equation. The determination of the digital gain and offset values is implemented automatically by the PGA300 GUI.

7.3.17.2 TC and NL Correction

The digital compensation equation is as follows:

$$DAC = (h_0 + h_1 \times T + h_2 \times T^2 + h_3 \times T^3) + (g_0 + g_1 \times T + g_2 \times T^2 + g_3 \times T^3) \times P + (n_0 + n_1 \times T + n_2 \times T^2 + n_3 \times T^3) \times P^2 + (m_0 + m_1 \times T + m_2 \times T^2 + m_3 \times T^3) \times P^3 \quad (2)$$

where

DAC = Digitally compensated value at the input of the DAC

h_x, g_x, n_x and m_x are TC and NL compensation coefficients programmed in EEPROM

P is pressure

T is temperature

7.3.17.2.1 TC and NL Coefficients

The PGA300 device implements third-order TC and NL compensation of the bridge offset, bridge span, and bridge nonlinearity. The equation has 16 coefficients, and hence requires at least 16 different measurement points to compute a unique set of 16 coefficients. The TC-compensated DAC output equation is as follows:

$$DAC = (h_0 + h_1T + h_2T^2 + h_3T^3) + (g_0 + g_1T + g_2T^2 + g_3T^3) \times P + (n_0 + n_1T + n_2T^2 + n_3T^3) \times P^2 + (m_0 + m_1T + m_2T^2 + m_3T^3) \times P^3 \quad (3)$$

The 16 different P ADC and T ADC measurements can be made, for example, at four temperatures and at four different pressures. Note that

- P GAIN and T GAIN values must be set to a fixed value for all measurements.
- At each measurement point, the P ADC value and the T ADC value must be recorded in order to compute the 16 coefficients.
- Sometimes, it may be expensive to measure P ADC and T ADC at different temperatures and pressures. In this case, there are three approaches:
  - Use a model of the bridge to estimate P ADC and T ADC measurements instead of actually measuring.
  - Use *batch modeling*, in which a family of sense elements is characterized across temperature, and the TC coefficients of the compensation equation are determined prior to calibration. On a production line, measurements are made at a limited number of temperature and pressure set points, and coefficients are adjusted accordingly. Discuss with TI application engineers for details.
  - Reduce the number of coefficients by reducing the order of TC compensation. Discuss the procedure to use fewer coefficients with TI application engineers.

7.3.17.2.1.1 No TC and NL Coefficients

The equation for P ADC-to-DAC conversion is as follows:

$DAC = H_{0EE} + G_{0EE} \times P\ ADC$

Table 8. Coefficient Values for No TC and NL Compensation

COEFFICIENT	VALUE (HEX)
h_0	H_{0EE} (1)
h_1	0x0000
h_2	0x0000
h_3	0x0000
g_0	G_{0EE} (1)
g_1	0x0000
g_2	0x0000
g_3	0x0000
n_0	0x0000
n_1	0x0000
n_2	0x0000
n_3	0x0000
m_0	0x0000
m_1	0x0000
m_2	0x0000
m_3	0x0000

(1) H_{0EE} and G_{0EE} are the values stored in EEPROM, which are 2^{14} times the actual H_0 and G_0 coefficients.

Consider an example of scaling the positive half of the 16-bit P ADC to a 14-bit DAC value. In this case, $H_0 = 0$ and $G_0 = 0.5$. Therefore, $H_{0EE} = 0$, and $G_{0EE} = 2^{13}$.

7.3.17.2.2 TC Compensation Using the Internal Temperature Sensor

Temperature compensation can be performed using the internal temperature sensor with T GAIN = 5 V/V gain. The internal temperature ADC values at the different temperatures are:

Table 9. T ADC Value for the Internal Temperature Sensor

TEMPERATURE	T ADC VALUE (HEX VALUE)
–40°C	0x16C9
0°C	0x1ACF
150°C	0x29E5

For T ADC at intermediate temperatures, use linear interpolation.

7.3.17.3 Clamping

The output of the digital compensation is clamped. The low and high clamp values are programmable using the LOW_CLAMP and HIGH_CLAMP registers in the EEPROM. In addition, a normal operating output can be configured using the NORMAL_LOW and NORMAL_HIGH registers in the EEPROM. Figure 21 shows an example of the clamping feature for a 0-V to 5-V output operational mode. In a similar way, the output of the compensation can be configured when the 4-mA to 20-mA operational mode is used. In such case, however, the LOW_CLAMP value must be larger than the maximum current needed for normal operation of the device.

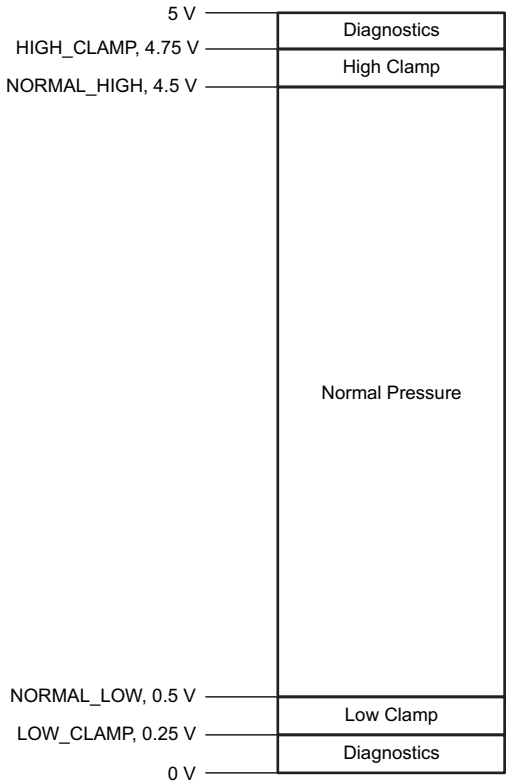


Figure 21. Example of Clamping the Digital Compensation Output

7.3.17.4 Filter

The IIR filter is as follows:

$w(n) = (a_0 \times DAC(n) + a_1 \times w(n - 1) + a_2 w(n - 2))$

$DACF(n) = (b_0 \times w(n) + b_1 \times w(n - 1) + b_2 w(n - 2)$

where a_0, a_1, a_2, b_0, b_1, and b_2 are the IIR filter coefficients, DAC(n) is the DAC output prior to the IIR filter, and DACF(n) is the output of the PGA300 device after the second-order IIR filter.

7.3.18 Filter Coefficients

7.3.18.1 No Filtering

If filtering must be disabled, set a_0 = 0x0000.

7.3.18.2 Filter Coefficients for P ADC Sampling Rate = 128 µs

Table 10. Filter Cutoff Frequency and Filter Coefficients

CUTOFF FREQUENCY (Hz)	a_0 (Hex)	a_1 (Hex)	a_2 (Hex)	b_0 (Hex)	b_1 (Hex)	b_2 (Hex)
600	4000	AAA1	2060	0B01	1602	0B01
700	4000	B169	1CEE	0E57	1CAF	0E57
800	4000	B818	19E0	11F8	23F0	11F8
900	4000	BEAE	172D	15DB	2BB7	15DB
1000	4000	C52D	14CE	19FB	33F6	19FB
1100	4000	CB95	12BC	1E52	3CA3	1E52
1200	4000	D1EA	10F2	22DC	45B8	22DC

Table 10. Filter Cutoff Frequency and Filter Coefficients (continued)

CUTOFF FREQUENCY (Hz)	a_0 (Hex)	a_1 (Hex)	a_2 (Hex)	b_0 (Hex)	b_1 (Hex)	b_2 (Hex)
1300	4000	D82D	0F6A	2798	4F2F	2798
1400	4000	DE61	0E21	2C82	5905	2C82
1500	4000	E487	0D14	319B	6336	319B
1600	4000	EAA3	0C3F	36E2	6DC4	36E2
1700	4000	F0B6	0BA1	3C56	78AD	3C56
1800	4000	F6C3	0B37	41FA	83F4	41FA
1900	4000	FCCC	0B02	47CE	8F9C	47CE
2000	4000	02D4	0B01	4DD4	9BA9	4DD4
2100	4000	08DD	0B33	540F	A81F	540F
2200	4000	0EE9	0B99	5A82	B504	5A82
2300	4000	14FC	0C33	612F	C25E	612F
2400	4000	1B17	0D05	681B	D037	681B
2500	4000	213C	0E0F	6F4B	DE96	6F4B

7.4 Device Functional Modes

There are two main functional modes for the PGA300 device: current (4-mA to 20-mA loop) and voltage modes. Depending on which mode is being used, the external components and connections are slightly different.

7.4.1 Voltage Mode

When configured in this mode, the FB– pin must be connected to the OUT pin. If the OUT pin is driving a large capacitive load, a compensation capacitor can be connected to the COMP pin and an isolation resistor can be placed between the OUT and FB– pins. The FB+ pin is not used in voltage mode.

7.4.2 Current Mode

When configured in this mode, the OUT pin is driving the base of a bipolar junction transistor (BJT) as shown in Figure 40. The COMP pin is connected to the emitter of the BJT and the FB+ pin is connected to the return terminal of the supply. The FB– pin is not used in current mode.

7.5 Register Maps

7.5.1 Register Settings

Before the PGA300 device can be used in any application, the device must be configured by setting various control registers to the desired values. Table 11 lists all the registers that must be configured and their respective default configurations. Note that the registers are configured by writing to the appropriate EEPROM addresses listed in the *Control and Status Registers* section.

Table 11. Default Register Settings

REGISTER	VALUE (HEX)	DESCRIPTION
DAC_CONFIG	0x00	DAC is set for absolute voltage output.
OP_STAGE_CTRL	0x08	Output is configured for 4-mA to 20-mA mode.
BRG_CTRL	0x00	Bridge excitation is set to 2.5 V.
P_GAIN_SELECT	0x00	P_GAIN is set to 5 V/V gain.
T_GAIN_SELECT	0x00	T_GAIN is set for 1.33 V/V gain.
TEMP_CTRL	0x40	I_{TEMP} drive is disabled and T signal chain is set for $V_{INT+} – V_{INT–}$.
TEMP_SE	0x00	T GAIN is in single-ended configuration.
NORMAL_LOW_LSB	0x67	DAC normal low output set to 0x0667. Must be updated during calibration
NORMAL_LOW_MSB	0x06	DAC normal low output set to 0x0667. Must be updated during calibration
NORMAL_HIGH_LSB	0x9A	DAC normal high output set to 0x399A. Must be updated during calibration

Register Maps (continued)

Table 11. Default Register Settings (continued)

REGISTER	VALUE (HEX)	DESCRIPTION
NORMAL_HIGH_MSB	0x39	DAC normal high output set to 0x399A. Must be updated during calibration
LOW_CLAMP_LSB	0x34	DAC clamp low output set to 0x0334. Must be updated during calibration
LOW_CLAMP_MSB	0x03	DAC clamp low output set to 0x0334. Must be updated during calibration
HIGH_CLAMP_LSB	0xCF	DAC clamp high output set to 0x3CCF. Must be updated during calibration
HIGH_CLAMP_MSB	0x3C	DAC clamp high output set to 0x3CCF. Must be updated during calibration
DIAG_ENABLE	0x00	Diagnostics are disabled.
EEPROM_LOCK	0x00	EEPROM is unlocked.
AFEDIAG_CFG	0x07	Diagnostics pulldown (1 MΩ) and pullup (1 MΩ) resistors enabled, VINP_UV threshold = 7.5% and VINP_OV threshold = 92.5%
AFEDIAG_MASK	0x33	VINP_OV and PGAIN_UV detection enabled
SERIAL_NUMBER_BYTE0-1-2-3	0x00	Serial number specified by customer
EEPROM_CRC	0xB8	Must be updated every time EEPROM is changed if diagnostics are enabled

7.5.2 Control and Status Registers

Table 12. Control and Status Registers

Register Name	DI Page Address	DI Offset Address	EEPROM Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
H0_LSB	N/A	N/A	0x40000000	RW								
H0_MSB	N/A	N/A	0x40000001	RW								
G0_LSB	N/A	N/A	0x40000002	RW								
G0_MSB	N/A	N/A	0x40000003	RW								
N0_LSB	N/A	N/A	0x40000004	RW								
N0_MSB	N/A	N/A	0x40000005	RW								
M0_LSB	N/A	N/A	0x4000003C	RW								
M0_MSB	N/A	N/A	0x4000003D	RW								
H1_LSB	N/A	N/A	0x40000006	RW								
H1_MSB	N/A	N/A	0x40000007	RW								
G1_LSB	N/A	N/A	0x40000008	RW								
G1_MSB	N/A	N/A	0x40000009	RW								
N1_LSB	N/A	N/A	0x4000000A	RW								
N1_MSB	N/A	N/A	0x4000000B	RW								
M1_MSB	N/A	N/A	0x4000003E	RW								
M1_LSB	N/A	N/A	0x4000003F	RW								
H2_LSB	N/A	N/A	0x4000000C	RW								
H2_MSB	N/A	N/A	0x4000000D	RW								
G2_LSB	N/A	N/A	0x4000000E	RW								
G2_MSB	N/A	N/A	0x4000000F	RW								
N2_LSB	N/A	N/A	0x40000010	RW								
N2_MSB	N/A	N/A	0x40000011	RW								
M2_LSB	N/A	N/A	0x40000040	RW								
M2_MSB	N/A	N/A	0x40000041	RW								
H3_LSB	N/A	N/A	0x40000036	RW								
H3_MSB	N/A	N/A	0x40000037	RW								
G3_LSB	N/A	N/A	0x40000038	RW								
G3_MSB	N/A	N/A	0x40000039	RW								
N3_LSB	N/A	N/A	0x4000003A	RW								
N3_MSB	N/A	N/A	0x4000003B	RW								
M3_LSB	N/A	N/A	0x40000042	RW								

Table 12. Control and Status Registers (continued)

Register Name	DI Page Address	DI Offset Address	EEPROM Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
M3_MSB	N/A	N/A	0x40000043	RW								
A0_LSB	N/A	N/A	0x40000012	RW								
A0_MSB	N/A	N/A	0x40000013	RW								
A1_LSB	N/A	N/A	0x40000014	RW								
A1_MSB	N/A	N/A	0x40000015	RW								
A2_LSB	N/A	N/A	0x40000016	RW								
A2_MSB	N/A	N/A	0x40000017	RW								
B0_LSB	N/A	N/A	0x40000018	RW								
B0_MSB	N/A	N/A	0x40000019	RW								
B1_LSB	N/A	N/A	0x4000001A	RW								
B1_MSB	N/A	N/A	0x4000001B	RW								
B2_LSB	N/A	N/A	0x4000001C	RW								
B2_MSB	N/A	N/A	0x4000001D	RW								
PADC_DATA1	0x2	0x20	N/A	R								
PADC_DATA2	0x2	0x21	N/A	R								
TADC_DATA1	0x2	0x24	N/A	R								
TADC_DATA2	0x2	0x25	N/A	R								
DAC_REG0_1	0x2	0x30	N/A	RW								
DAC_REG0_2	0x2	0x31	N/A	RW								
DAC_CONFIG	0x2	0x39	0x40000020	RW								DAC_RATIOMETRIC
OP_STAGE_CTRL	0x2	0x3B	0x40000021	RW				DACCAP_EN	4_20MA_EN	DAC_GAIN[2]	DAC_GAIN[1]	DAC_GAIN[0]
BRDG_CTRL	0x2	0x46	0x40000022	RW						VBRDG_CTRL[1]	VBRDG_CTRL[0]	
P_GAIN_SELECT	0x2	0x47	0x40000023	RW	P_INV			P_GAIN[4]	P_GAIN[3]	P_GAIN[2]	P_GAIN[1]	P_GAIN[0]
T_GAIN_SELECT	0x2	0x48	0x40000024	RW	T_INV						T_GAIN[1]	T_GAIN[0]
TEMP_CTRL	0x2	0x4C	0x40000025	RW		ITEMP_CTRL[2]	ITEMP_CTRL[1]	ITEMP_CTRL[0]	TEMP_MUX_CTRL[3]	TEMP_MUX_CTRL[2]	TEMP_MUX_CTRL[1]	TEMP_MUX_CTRL[0]
TEMP_SE	N/A	N/A	0x40000028	RW								TEMP_SE
NORMAL_LOW_LSB	N/A	N/A	0x4000002A	RW								

Table 12. Control and Status Registers (continued)

Register Name	DI Page Address	DI Offset Address	EEPROM Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
NORMAL_LOW_MSB	N/A	N/A	0x4000002B	RW								
NORMAL_HIGH_LSB	N/A	N/A	0x4000002C	RW								
NORMAL_HIGH_MSB	N/A	N/A	0x4000002D	RW								
LOW_CLAMP_LSB	N/A	N/A	0x4000002E	RW								
LOW_CLAMP_MSB	N/A	N/A	0x4000002F	RW								
HIGH_CLAMP_LSB	N/A	N/A	0x40000030	RW								
HIGH_CLAMP_MSB	N/A	N/A	0x40000031	RW								
PADC_GAIN_LSB	N/A	N/A	0x40000032	RW								
PADC_GAIN_MSB	N/A	N/A	0x40000033	RW								
PADC_OFFSET_BYTE0	N/A	N/A	0x40000034	RW								
PADC_OFFSET_BYTE1	N/A	N/A	0x40000035	RW								
DIAG_ENABLE	N/A	N/A	0x40000044	RW								
EEPROM_LOCK	N/A	N/A	0x40000045	RW								
AFEDIAG_CFG	N/A	N/A	0x40000046	RW	-	DIS_R_T	DIS_R_P	THRS[2]	THRS[1]	THRS[0]	PD2	PD1
AFEDIAG_MASK	N/A	N/A	0x40000047	RW	TGAIN_UV	TGAIN_OV	PGAIN_UV	PGAIN_OV	-	INT_OV	INP_UV	INP_OV
FAULT_LSB	N/A	N/A	0x4000004A	RW								
FAULT_MSB	N/A	N/A	0x4000004B	RW								
TADC_GAIN_LSB	N/A	N/A	0x4000004C	RW								
TADC_GAIN_MSB	N/A	N/A	0x4000004D	RW								
TADC_OFFSET_BYTE0	N/A	N/A	0x4000004E	RW								
TADC_OFFSET_BYTE1	N/A	N/A	0x4000004F	RW								
SERIAL_NUMBER_BYTE0	N/A	N/A	0x40000050	RW								
SERIAL_NUMBER_BYTE1	N/A	N/A	0x40000051	RW								

Table 12. Control and Status Registers (continued)

Register Name	DI Page Address	DI Offset Address	EEPROM Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
SERIAL_NUMBER_BYTE2	N/A	N/A	0x40000052	RW								
SERIAL_NUMBER_BYTE3	N/A	N/A	0x40000053	RW								
EEPROM_CRC_VALUE	0x5	0x8D	0x4000007F	R								
COMPENSATION_CONTROL	0x0	0x0C	N/A	RW							COMPENSATION_RESET	IF_SEL
EEPROM ARRAY	0x5	0x00-0x7F	N/A	RW								
EEPROM_CACHE	0x5	0x80-0x87	N/A	RW								
EEPROM_PAGE_ADDRESS	0x5	0x88	N/A	RW						ADDR[2]	ADDR[1]	ADDR[0]
EEPROM_CTRL	0x5	0x89	N/A	RW					FIXED_ERASE_PROG_TIME	ERASE_AND_PROGRAM	ERASE	PROGRAM
EEPROM_CRC	0x5	0x8A	N/A	RW								CALCULATE_CRC
EEPROM_STATUS	0x5	0x8B	N/A	R						PROGRAM_IN_PROGRESS	ERASE_IN_PROGRESS	READ_IN_PROGRESS
EEPROM_CRC_STATUS	0x5	0x8C	N/A	R							CRC_GOOD	CRC_CHECK_IN_PROG

7.5.2.1 DAC_CONFIG

DI PAGE ADDRESS: 0x2, DI PAGE OFFSET: 0x39

Figure 22. DAC_CONFIG Register (EEPROM Address = 0x40000020)

DAC_CONFIG	7	6	5	4	3	2	1	0
BIT DEFINITION	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	DAC_RATIOMETRIC
RW ACCESS								RW
RESET VALUE								0

Table 13. DAC_CONFIG Register (EEPROM Address = 0x40000020) Bit Descriptions

Register	Bits	Description
DAC_CONFIG	0: DAC_RATIOMETRIC	1: DAC is in ratiometric mode 0: DAC is in absolute mode
	1–7: UNUSED	

7.5.2.2 OP_STAGE_CTRL

DI PAGE ADDRESS: 0x2, DI PAGE OFFSET: 0x3B

Figure 23. OP_STAGE_CTRL Register (EEPROM Address = 0x40000021)

OP_STAGE_CTRL	7	6	5	4	3	2	1	0
BIT DEFINITION	UNUSED	UNUSED	PULLUP_EN	DACCAP_EN	4_20MA_EN	DAC_GAIN[2]	DAC_GAIN[1]	DAC_GAIN[0]
RW ACCESS			RW	RW	RW	RW	RW	RW
RESET VALUE			0	0	0	1	0	1

Table 14. OP_STAGE_CTRL Register (EEPROM Address = 0x40000021) Bit Descriptions

Register	Bits	Description			
OP_STAGE_CTRL	0: DAC_GAIN[0]	**DAC_GAIN[2]**	**DAC_GAIN[1]**	**DAC_GAIN[0]**	**Description**
	1: DAC_GAIN[1]	0	0	0	Voltage mode disabled
	2: DAC_GAIN[2]	0	0	1	Gain = 10V/V
		0	1	0	Gain = 4V/V
		0	1	1	Reserved
		1	0	0	Gain = 2V/V
		1	0	1	Reserved
		1	1	0	Gain = 6.67V/V
		1	1	1	Reserved
	3: 4_20MA_EN	1: Enable 4 to 20mA Current Loop (Close switch S5 in DAC Gain) 0: Disable 4 to 20mA Current Loop (Open switch S5 in DAC Gain)			
	4: DACCAP_EN	1: Enable DACCAP capacitor (Close switch S4 in DAC Gain) 0: Disable DACCAP capacitor (Open switch S4 in DAC Gain)			
	5: PULLUP_EN	1: Enable Pull up at the input of DAC Gain (Close switch S8 in DAC Gain) 0: Disable Pull up at the input of DAC Gain (Open switch S8 in DAC Gain)			
	6–7: UNUSED				

7.5.2.3 BRDG_CTRL

DI PAGE ADDRESS: 0x2, DI PAGE OFFSET: 0x46

Figure 24. BRDG_CTRL Register (EEPROM Address = 0x40000022)

BRDG_CTRL	7	6	5	4	3	2	1	0
BIT DEFINITION	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	VBRDG_CTRL[1]	VBRDG_CTRL[0]	UNUSED
RW ACCESS						RW	RW	
RESET VALUE						0	0	

Table 15. BRDG_CTRL Register (EEPROM Address = 0x40000022) Bit Descriptions

Register	Bits	Description		
BRDG_CTRL	0: UNUSED			
	1: VBRDG_CTRL[0] 2: VBRDG_CTRL[1]	**VBRDG_CTRL[1]**	**VBRDG_CTRL[0]**	**Bridge Supply Voltage**
		0	0	2.5V
		0	1	2.0V
		1	0	1.25V
		1	1	1.25V
	3–7: UNUSED			

7.5.2.4 P_GAIN_SELECT

DI PAGE ADDRESS: 0x2, DI PAGE OFFSET: 0x47

Figure 25. P_GAIN_SELECT Register (EEPROM Address = 0x40000023)

P_GAIN_SELECT	7	6	5	4	3	2	1	0
BIT DEFINITION	P_INV	UNUSED	UNUSED	P_GAIN[4]	P_GAIN[3]	P_GAIN[2]	P_GAIN[1]	P_GAIN[0]
RW ACCESS	RW			RW	RW	RW	RW	RW
RESET VALUE	0			0	0	0	0	0

Table 16. P_GAIN_SELECT Register (EEPROM Address = 0x40000023) Bit Descriptions

Register	Bits	Description
P_GAIN_SELECT	0: P_GAIN[0] 1: P_GAIN[1] 2: P_GAIN[2] 3: P_GAIN[3] 4: P_GAIN[4]	See Electrical Parameters for Gain Selections
	5–6: UNUSED	
	7: P_INV	1: Inverts the output of the PGAIN Output 0: No Inversion

7.5.2.5 T_GAIN_SELECT

DI PAGE ADDRESS: 0x2, DI PAGE OFFSET: 0x48

Figure 26. T_GAIN_SELECT Register (EEPROM Address = 0x40000024)

T_GAIN_SELECT	7	6	5	4	3	2	1	0
BIT DEFINITION	T_INV	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	T_GAIN[1]	T_GAIN[0]
RW ACCESS	RW						RW	RW
RESET VALUE	0						0	0

Table 17. T_GAIN_SELECT Register (EEPROM Address = 0x40000024) Bit Descriptions

Register	Bits	Description
T_GAIN_SELECT	0: T_GAIN[0] 1: T_GAIN[1]	See Electrical Parameters for Gain Selections
	2–6: UNUSED	
	7: T_INV	1: Inverts the output of the T GAIN Output 0: No Inversion

7.5.2.6 TEMP_CTRL

DI PAGE ADDRESS: 0x2, DI PAGE OFFSET: 0x4C

Figure 27. TEMP_CTRL Register (EEPROM Address = 0x40000025)

TEMP_CTRL	7	6	5	4	3	2	1	0
BIT DEFINITION	UNUSED	ITEMP_CTRL[2]	ITEMP_CTRL[1]	ITEMP_CTRL[0]	TEMP_MUX_CTRL[3]	TEMP_MUX_CTRL[2]	TEMP_MUX_CTRL[1]	TEMP_MUX_CTRL[0]
RW ACCESS		RW	RW	RW	RW	RW	RW	RW
RESET VALUE		1	0	0	0	0	0	0

Table 18. TEMP_CTRL Register (EEPROM Address = 0x40000025)

Register	Bits	Description				
TEMP_CTRL	0: TEMP_MUX_CTRL[0]	**TEMP_MUX_CTRL[3]**	**TEMP_MUX_CTRL[2]**	**TEMP_MUX_CTRL[1]**	**TEMP_MUX_CTRL[0]**	**Description**
	1: TEMP_MUX_CTRL[1]	0	0	0	0	INT+ and INT–
	2: TEMP_MUX_CTRL[2]	0	0	1	1	VTEMP_INT-GND (Internal Temperature Sensor)
	3: TEMP_MUX_CTRL[3]					
	4: ITEMP_CTRL[0]	**ITEMP_CTRL[2]**		**ITEMP_CTRL[1]**	**ITEMP_CTRL[0]**	**Description**
	5: ITEMP_CTRL[1]	0		0	0	25µA
	6: ITEMP_CTRL[2]	0		0	1	50µA
		0		1	0	100µA
		0		1	1	500µA
		1		X	X	OFF
	7: UNUSED					

7.5.2.7 TEMP_SE

Figure 28. TEMP_SE Register (EEPROM Address = 0x40000028)

TEMP_SE	7	6	5	4	3	2	1	0
BIT DEFINITION	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	TEMP_SE
RW ACCESS								RW
RESET VALUE								0

Table 19. TEMP_SE Register (EEPROM Address = 0x40000028) Bit Descriptions

Register	Bits	Description
TEMP_SE	0: TEMP_SE	1: Output of Temperature Mux is differential 0: Output of Temperature Mux is single-ended
	1–7: UNUSED	

7.5.2.8 DIAG_ENABLE

Figure 29. DIAG_ENABLE Register (EEPROM Address = 0x40000044)

DIAG_ENABLE	7	6	5	4	3	2	1	0
BIT DEFINITION	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	DIAG_ENABLE
RW ACCESS								RW
RESET VALUE								0

Table 20. DIAG_ENABLE Register (EEPROM Address = 0x40000044) Bit Descriptions

Register	Bits	Description
DIAG_ENABLE	0: DIAG_ENABLE	**Read:** 1: Enables Diagnostics 0: Disables Diagnostics
	1–7: UNUSED	

7.5.2.9 AFEDIAG_CFG

Figure 30. AFEDIAG_CFG Register (EEPROM Address = 0x40000046)

AFEDIAG_CFG	7	6	5	4	3	2	1	0
BIT DEFINITION	UNUSED	DIS_R_T	DIS_R_P	THRS[2]	THRS[1]	THRS[0]	PD2	PD1
RW ACCESS		RW	RW	RW	RW	RW	RW	RW
RESET VALUE		0	0	0	0	0	0	0

Table 21. AFEDIAG_CFG Register (EEPROM Address = 0x40000046) Bit Descriptions

Register	Bits	Description				
AFEDIAG_CFG		**PD2**			**PD1**	**Pull Down Resistor Value**
	0: PD1	0			0	4MΩ
	1: PD2	1			0	3MΩ
		0			1	2MΩ
		1			1	1MΩ
		THRS[2]	**THRS[1]**	**THRS[0]**	**VINP_UV Threshold**	**VINP_OV Threshold**
	2: THRS[0]	0	0	0	5% of Programmed VBRDG	95% of Programmed VBRDG
	3: THRS[1]	0	0	1	7.5% of Programmed VBRDG	92.5% if Programmed VBRDG
	4: THRS[2]	0	1	0	10% of Programmed VBRDG	90% of Programmed VBRDG
		0	1	1	12.5% of Programmed VBRDG	87.5% of Programmed VBRDG
		1	0	0	15% of Programmed VBRDG	85% of Programmed VBRDG
		1	0	1	20% of Programmed VBRDG	80% of Programmed VBRDG
		1	1	0	25% of Programmed VBRDG	75% of Programmed VBRDG
		1	1	1	30% of Programmed VBRDG	70% of Programmed VBRDG
	5: DIS_R_P	1: Disables pulldown resistors used for open/short diagnostics on the INP+ and INP– pins 0: Enables pulldown resistors used for open/short diagnostics on the INP+ and INP– pins				
	6: DIS_R_T	1: Disables pullup resistors used for open/short diagnostics on the INT+ and INT– pins 0: Enables pullup resistors used for open/short diagnostics on the INT+ and INT– pins				
	7: UNUSED					

7.5.2.10 AFEDIAG_MASK

Figure 31. AFEDIAG_MASK Register (EEPROM Address = 0x40000047)

AFEDIAG	7	6	5	4	3	2	1	0
BIT DEFINITION	TGAIN_UV	TGAIN_OV	PGAIN_UV	PGAIN_OV	UNUSED	INT_OV	INP_UV	INP_OV
RW ACCESS	RW	RW	RW	RW		RW	RW	RW
RESET VALUE	0	0	0	0		0	0	0

Table 22. AFEDIAG_MASK Register (EEPROM Address = 0x40000047) Bit Descriptions

Register	Bits	Description
AFEDIAG	0: INP_OV	1: Enable overvoltage detection at input pins of P Gain 0: Disable overvoltage detection at input pins of P Gain
	1: INP_UV	1: Enable undervoltage detection at input pins of P Gain 0: Disable undervoltage detection at input pins of P Gain
	2: INT_OV	1: Enable overvoltage detection at input pins of T Gain 0: Disable overvoltage detection at input pins of T Gain
	3: UNUSED	
	4: PGAIN_OV	1: Enable overvoltage detection at output pins of P Gain 0: Disable overvoltage detection at output pins of P Gain
	5: PGAIN_UV	1: Enable undervoltage detection at output pins of P Gain 0: Disable undervoltage detection at output pins of P Gain
	6: TGAIN_OV	1: Enable overvoltage detection at output pins of T Gain 0: Disable overvoltage detection at output pins of T Gain
	7: TGAIN_UV	1: Enable undervoltage detection at output pins of T Gain 0: Disable undervoltage detection at output pins of T Gain

7.5.2.11 COMPENSATION_CONTROL

DI PAGE ADDRESS: 0x0, DI PAGE OFFSET: 0x0C

Figure 32. COMPENSATION_CONTROL Register (EEPROM Address = N/A)

COMPENSATION_CONTROL	7	6	5	4	3	2	1	0
BIT DEFINITION	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	COMPENSATION_RESET	IF_SEL
RW ACCESS							RW	RW
RESET VALUE							0	0

Table 23. COMPENSATION_CONTROL Register (EEPROM Address = N/A) Bit Descriptions

Register	Bits	Description
COMPENSATION_CONTROL	0: IF_SEL	1: Digital Interface accesses the PGA300 resources 0: Calculation Engine accesses the PGA300 resources
	1: COMPENSATION_RESET	1: Compensation Engine is in Reset 0: Compensation Engine is Running
	2–7: UNUSED	

7.5.2.12 EEPROM_LOCK

Figure 33. EEPROM_LOCK Register (EEPROM Address = 0x40000045)

EEPROM_LOCK	7	6	5	4	3	2	1	0
BIT DEFINITION	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	EEPROM_LOCK
RW ACCESS								RW
RESET VALUE								0

Table 24. EEPROM_LOCK Register (EEPROM Address = 0x40000045) Bit Descriptions

Register	Bits	Description
EEPROM_LOCK	0: EEPROM_LOCK	1: EEPROM is locked - EEPROM is not accessible 0: EEPROM is unlocked - EEPROM is accessible
	1–7: UNUSED	

7.5.2.13 EEPROM_PAGE_ADDRESS

DI PAGE ADDRESS: 0x5, DI PAGE OFFSET: 0x88

Figure 34. EEPROM_PAGE_ADDRESS Register (EEPROM Address = N/A)

EEPROM_PAGE_ADDRESS	7	6	5	4	3	2	1	0
BIT DEFINITION	UNUSED	UNUSED	UNUSED	UNUSED	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
RW ACCESS					RW	RW	RW	RW
RESET VALUE					0	0	0	0

Table 25. EEPROM_PAGE_ADDRESS Register (EEPROM Address = N/A) Bit Descriptions

Register	Bits	Description
EEPROM_PAGE_ADDRESS	0–3: ADDR[0-3]	EEPROM page address used in the EEPROM Programming Procedure
	4–7: UNUSED	

7.5.2.14 EEPROM_CTRL

DI PAGE ADDRESS: 0x5, DI PAGE OFFSET: 0x89

Figure 35. EEPROM_CTRL Register (EEPROM Address = N/A)

EEPROM_CTRL	7	6	5	4	3	2	1	0
BIT DEFINITION	UNUSED	UNUSED	UNUSED	UNUSED	FIXED_ERASE_PROG_TIME	ERASE_AND_PROGRAM	ERASE	PROGRAM
RW ACCESS					RW	RW	RW	RW
RESET VALUE					0	0	0	0

Table 26. EEPROM_CTRL Register (EEPROM Address = N/A) Bit Descriptions

Register	Bits	Description
EEPROM_CTRL	0: PROGRAM	1: Program contents of EEPROM cache into EEPROM memory pointed to by EEPROM_PAGE_ADDRESS 0: No action
	1: ERASE	1: Erase contents of EEPROM memory pointed to by EEPROM_PAGE_ADDRESS 0: No action
	2: ERASE_AND_PROGRAM	1: Erase contents of EEPROM memory pointed to by EEPROM_PAGE_ADDRESS and program of contents of EEPROM cache 0: No action
	3: FIXED_ERASE_PROG_TIME	1: Use Fixed 8ms as the Erase/Program time 0: Use Variable time <8ms as the Erase/Program time. The EEPROM programming logic will determine the duration to program the EEPROM memory.
	4–7: UNUSED	

7.5.2.15 EEPROM_CRC

DI PAGE ADDRESS: 0x5, DI PAGE OFFSET: 0x8A

Figure 36. EEPROM_CRC Register (EEPROM Address = N/A)

EEPROM_CRC	7	6	5	4	3	2	1	0
BIT DEFINITION	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	CALCULATE_CRC
RW ACCESS								RW
RESET VALUE								0

Table 27. EEPROM_CRC Register (EEPROM Address = N/A) Bit Descriptions

Register	Bits	Description
EEPROM_CRC	0: CALCULATE_CRC	1: Calculate EEPROM CRC 0: No action
	1–7: UNUSED	

7.5.2.16 EEPROM_STATUS

DI PAGE ADDRESS: 0x5, DI PAGE OFFSET: 0x8B

Figure 37. EEPROM_STATUS Register (EEPROM Address = N/A)

EEPROM_STATUS	7	6	5	4	3	2	1	0
BIT DEFINITION	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	PROGRAM_IN_PROGRESS	ERASE_IN_PROGRESS	READ_IN_PROGRESS
RW ACCESS						R	R	R
RESET VALUE						0	0	0

Table 28. EEPROM_STATUS Register (EEPROM Address = N/A) Bit Descriptions

Register	Bits	Description
EEPROM_STATUS	0: READ_IN_PROGRESS	1: EEPROM Read in progress 0: EEPROM Read not in progress
	1: ERASE_IN_PROGRESS	1: EEPROM Erase in progress 0: EEPROM Erase not in progress
	2: PROGRAM_IN_PROGRESS	1: EEPROM Program in progress 0: EEPROM Program not in progress
	3–7: UNUSED	

7.5.2.17 EEPROM_CRC_STATUS

DI PAGE ADDRESS: 0x5, DI PAGE OFFSET: 0x8C

Figure 38. EEPROM_CRC_STATUS Register (EEPROM Address = N/A)

EEPROM_CRC_STATUS	7	6	5	4	3	2	1	0
BIT DEFINITION	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	CRC_GOOD	CRC_CHECK_IN_PROG
RW ACCESS							R	R
RESET VALUE							0	0

Table 29. EEPROM_CRC_STATUS Register (EEPROM Address = N/A) Bit Descriptions

Register	Bits	Description
EEPROM_CRC_STATUS	0: CRC_CHECK_IN_PROGRESS	1: EEPROM CRC check in progress 0: EEPROM CRC check not in progress
	1: CRC_GOOD	1: EEPROM Programmed CRC matches calculated CRC 0: EEPROM Programmed CRC does not match calculated CRC
	2–7: UNUSED	

7.5.2.18 EEPROM_CRC_VALUE

DI PAGE ADDRESS: 0x5, DI PAGE OFFSET: 0x8D

Figure 39. EEPROM_CRC_VALUE Register (EEPROM Address = 0x4000007F)

EEPROM_CRC_VALUE	7	6	5	4	3	2	1	0
BIT DEFINITION								
RW ACCESS	R	R	R	R	R	R	R	R
RESET VALUE	1	1	1	1	1	1	1	1

Table 30. EEPROM_CRC_VALUE Register (EEPROM Address = 0x4000007F) Bit Descriptions

Register	Bits	Description
EEPROM_CRC_VALUE	0–7	CRC value as calculated by the digital logic

EEPROM CRC value should be located in the last byte of the EEPROM

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The PGA 300 can be used in a variety of applications to measure pressure and temperature. Depending on the application, the device can be configured in different modes as illustrated in the following sections.

8.1.1 4-mA to 20-mA Output With Internal Sense Resistor

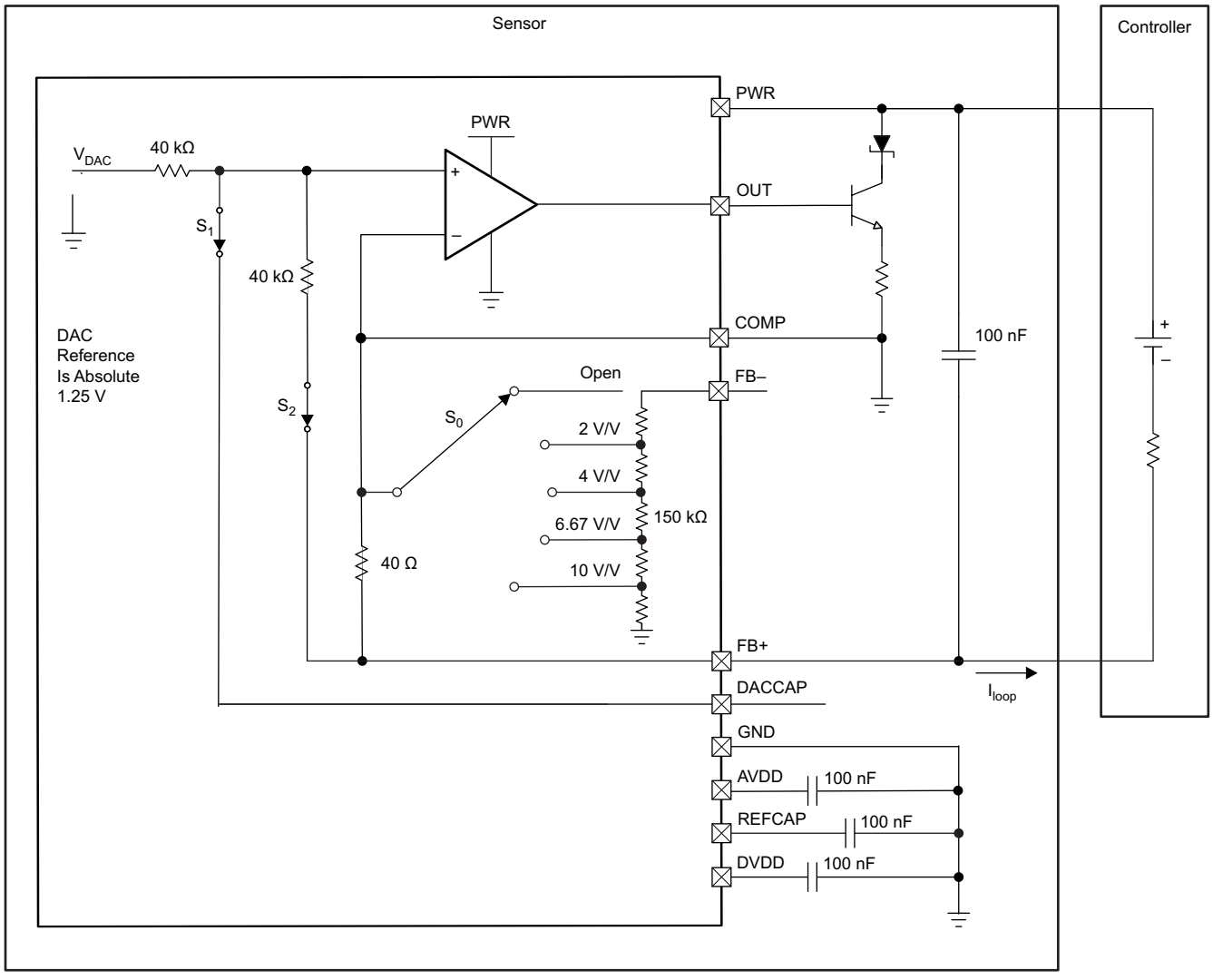


Figure 40. 4-mA to 20-mA Output With Internal Sense Resistor Diagram

8.1.1.1 Design Requirements

There are only a few requirements to take into account when using the PGA300 device in a design:

- Do not exceed the maximum slew rate of 0.5 V/µs at the PWR pin.
- Place a 100-nF capacitor from the AVDD pin to ground, as close as possible to the AVDD pin.

Application Information (continued)

- Place a 100-nF capacitor from the DVDD pin to ground, as close as possible to the DVDD pin.
- Place a capacitor between 10 nF and 1000 nF from the REFCAP pin to ground, as close as possible to the REFCAP pin.
- Place a 150-Ω resistor between the COMP pin and the emitter of the BJT for current-loop stability purposes.
- Place a 10-Ω resistor between the FB+ pin and the negative terminal of the controller for current measurement.

8.1.1.2 Detailed Design Procedure

8.1.1.2.1 Calibration Tips

8.1.1.2.1.1 Programming the EEPROM for 4-mA to 20-mA Output

The EEPROM in the PGA300 is configured by default to operate in current mode using the OP_STG_CTRL register. If not, the following sequence must be followed to change it to current mode:

1. Send an OWI activation pulse to stop the digital compensation from running.
2. Set OP_STAGE_CTRL to 0x80 for current mode and DAC_CONFIG EEPROM to 0x00 or 0x01 for No_Gain.
3. Let the digital compensation run again to read the new EEPROM values.

8.1.1.3 Application Curve

Voltage measured between the GND pin in the PGA300 device and the negative terminal of the controller. This includes the internal 40-Ω resistor and an external 10-Ω resistor, V_{PWR} = 15 V. The DAC codes used were 0x880 and 0x2760 for 4 mA and 20 mA, respectively.

Figure 41. Loop Current Step From 4 mA to 20 mA

Application Information (continued)

8.1.2 0- to 10-V Absolute Output With Internal Drive

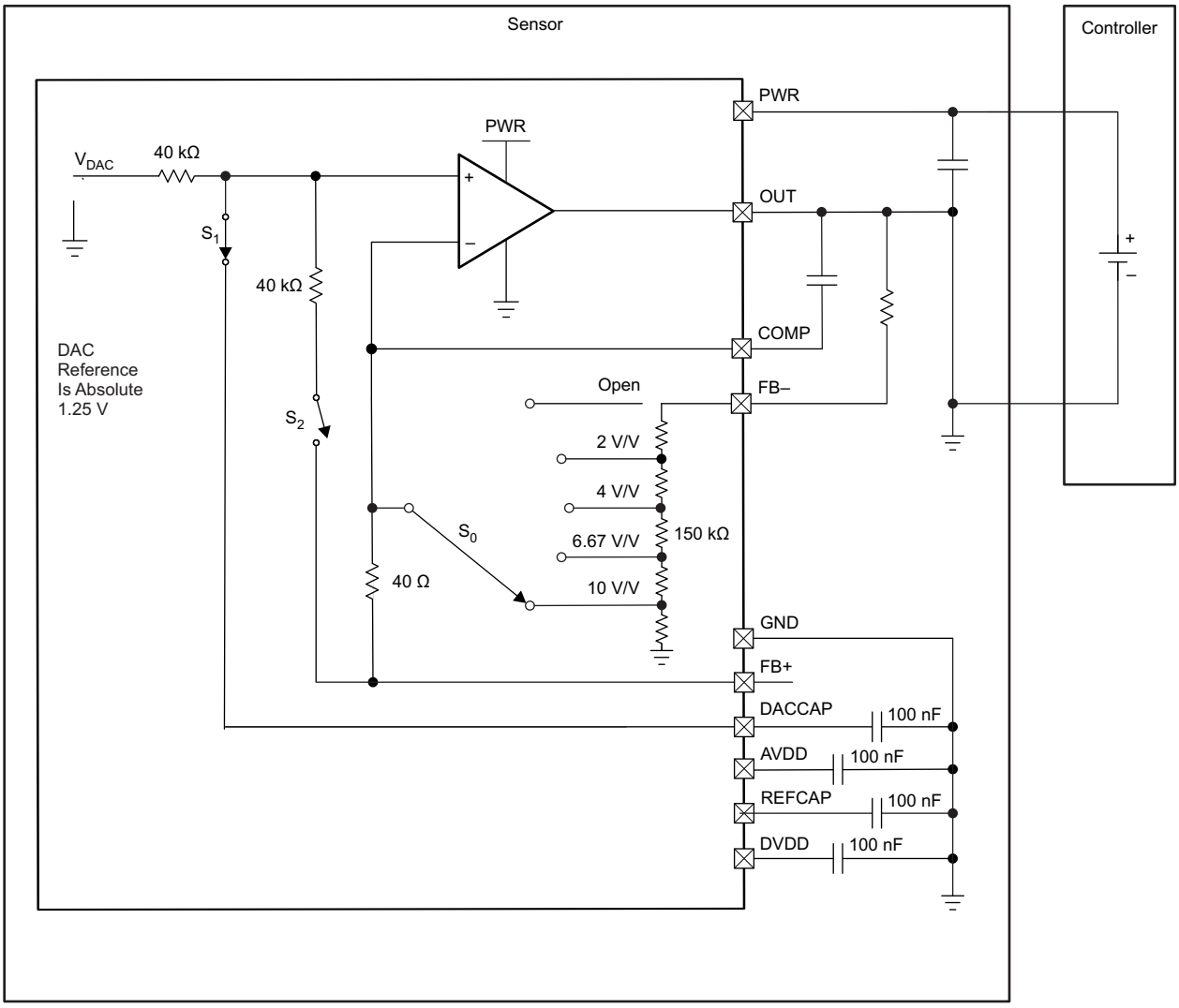


Figure 42. 0- to 10-V Absolute Output With Internal Drive Diagram

8.1.2.1 Design Requirements

There are only a few requirements to take into account when using the PGA300 in a design:

- Do not exceed the maximum slew rate of 0.5 V/µs at the VDD pin.
- Place a 100-nF capacitor from the AVDD pin to ground, as close as possible to the AVDD pin.
- Place a 100-nF capacitor from the DVDD pin to ground, as close as possible to the DVDD pin.
- Place a capacitor between 10 nF and 1000 nF from the REFCAP pin to ground, as close as possible to the REFCAP pin.
- Implement compensation, using the COMP pin and an isolation resistor, when driving large capacitive loads with the OUT pin.

Application Information (continued)

8.1.2.2 Detailed Design Procedure

8.1.2.2.1 Programmer Tips

8.1.2.2.1.1 Resetting the Microprocessor and Enable Digital Interface

The following bits must be configured to reset the M0 microprocessor and to enable digital interface:

1. Set the IF_SEL bit in the MICRO_INTERFACE_CONTROL register to 1.
2. Set the MICRO_RESET bit in the MICRO_INTERFACE_CONTROL register to 1.

8.1.2.2.1.2 Turning On the Accurate Reference Buffer (REFCAP Voltage)

The following bits must be configured to turn ON the accurate reference buffer:

1. Set the SD bit in the ALPWR register to 0.
2. Set the ADC_EN_VREF bit in the ALPWR register to 1.

By turning on the accurate reference buffer, the reference voltage can be measured on REFCAP pin. Further, the capacitor on the REFCAP pin is connected to the reference buffer.

8.1.2.2.1.3 Turning On DAC and DAC GAIN

The following bits must be configured to turn on DAC and DAC GAIN:

- Set the SD bit in the ALPWR register to 0.
- Set the ADC_EN_VREF bit in the ALPWR register to 1.
- Set the DAC_ENABLE bit in the DAC_CTRL_STATUS register to 1.
- Set the 4_20_MA_EN bit in the OP_STAGE_CTRL register for voltage output or current output mode.
- Set the DACCAP_EN bit in the OP_STAGE_CTRL register to connect or disconnect the external capacitor at the DAC output.
- Set the DAC_RATIOMETRIC bit in the DAC_CONFIG register for ratiometric or absolute-voltage output mode.
- Set the TEST_MUX_DAC_EN bit in the AMUX_CTRL register to 1.

Application Information (continued)

8.1.3 0- to 5-V Ratiometric Output With Internal Drive

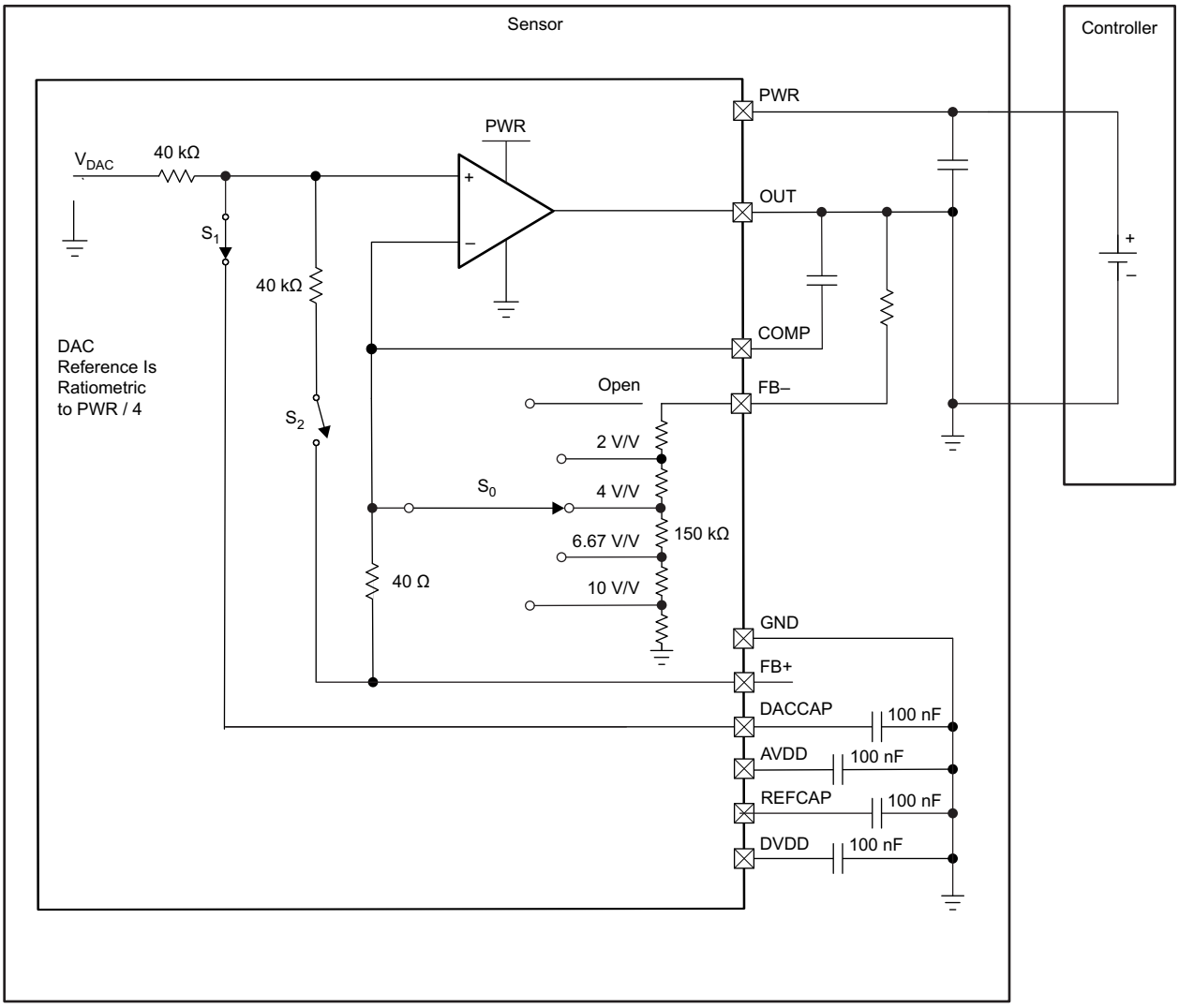


Figure 43. 0- to 5-V Ratiometric Output With Internal Drive Diagram

8.1.3.1 Design Requirements

There are only a few requirements to take into account when using the PGA300 in a design:

- Do not exceed the maximum slew rate of 0.5 V/µs at the PWR pin.
- Place a 100-nF capacitor from the AVDD pin to ground, as close as possible to the AVDD pin.
- Place a 100-nF capacitor from the DVDD pin to ground, as close as possible to the DVDD pin.
- Place a capacitor between 10 nF and 1000 nF from the REFCAP pin to ground, as close as possible to the REFCAP pin.
- Implement compensation, using the COMP pin and an isolation resistor, when driving large capacitive loads with the OUT pin.

Application Information (continued)

8.1.3.2 Detailed Design Procedure

8.1.3.2.1 Programmer Tips

8.1.3.2.1.1 Resetting the Microprocessor and Enable Digital Interface

The following bits must be configured to reset the M0 microprocessor and to enable digital interface:

1. Set the IF_SEL bit in the MICRO_INTERFACE_CONTROL register to 1.
2. Set the MICRO_RESET bit in the MICRO_INTERFACE_CONTROL register to 1.

8.1.3.2.1.2 Turning On the Accurate Reference Buffer (REFCAP Voltage)

The following bits must be configured to turn ON the accurate reference buffer:

1. Set the SD bit in the ALPWR register to 0.
2. Set the ADC_EN_VREF bit in the ALPWR register to 1.

By turning on the accurate reference buffer, the reference voltage can be measured on REFCAP pin. Further, the capacitor on the REFCAP pin is connected to the reference buffer.

8.1.3.2.1.3 Turning On DAC and DAC GAIN

The following bits must be configured to turn on DAC and DAC GAIN:

- Set the SD bit in ALPWR register to 0.
- Set the ADC_EN_VREF bit in the ALPWR register to 1.
- Set the DAC_ENABLE bit in the DAC_CTRL_STATUS register to 1.
- Set the 4_20_MA_EN bit in the OP_STAGE_CTRL register for the voltage-output or current-output mode.
- Set the DACCAP_EN bit in the OP_STAGE_CTRL register to connect or disconnect the external capacitor at the DAC output.
- Set the DAC_RATIOMETRIC bit in the DAC_CONFIG register for ratiometric or absolute-voltage output mode.
- Set the TEST_MUX_DAC_EN bit in the AMUX_CTRL register to 1.

9 Power Supply Recommendations

The PGA300 device has a single pin, PWR, for the input power supply. The maximum slew rate for the PWR pin is 0.5 V/µs as specified in the Recommended Operating Conditions. Faster slew rates might generate a POR. A decoupling capacitor for PWR should be placed as close as possible to the pin.

10 Layout

10.1 Layout Guidelines

Standard layout good practices should be used when designing a board to test the PGA300 device. Depending on the number of layers in the board, one or more GND planes should be inserted as internal layers. However, given the limited number of external components needed for an application using the PGA300 device and the number of NC pins in the device, it is very possible to design a simple two-layer board. In addition, the PWR decoupling capacitor should be placed as close as possible to the pin. In a similar way, the 100 nF recommended capacitors for the AVDD and DVDD regulators as well as the 10- to 1000-nF recommended capacitor for REFCAP should be placed as close as possible to their respective pins.

Depending on the application, the signal traces for FB–, FB+, COMP, and OUT should be routed such that they do not cross one another in order to minimize coupling.

10.2 Layout Example

Figure 44 shows the main guidelines previously discussed being implemented in a six-layer, socketed EVM of the PGA300 device. Two main GND planes (layer 2 and 5) were used to provide a nearby GND plane to each of the signal layers and the power plane (layer 3) in the EVM. This EVM supports voltage and current modes for the device, and as a result, GND separation is needed, depending on the application. As a result, layer 2 is a solid GND plane for the majority of the circuitry in the EVM (IRETURN). Because most of the circuitry is referred to this GND plane, layers 3 and 4 also contain copper pours connected to IRETURN. This GND plane is the return path for the supply used in the 4-mA to 20-mA loop. Layer 5 is a split plane for the ground references for the digital communication signals used for this EVM (USBGND) and the ground pins in the device (GND, AVSS and DVSS), referred to as ASICGND. The EVM provides jumpers to connect, or disconnect, these three planes one from another, depending on the desired configuration.

Figure 44 shows the recommended capacitors for the proper operation of the PGA300 device. These capacitors are placed as close as possible to their respective pins of the socket used for this particular EVM. The signal traces for FB–, FB+, COMP, and OUT can also be observed to be routed all in the same layer to avoid crossing each other and minimize coupling.

Layout Example (continued)

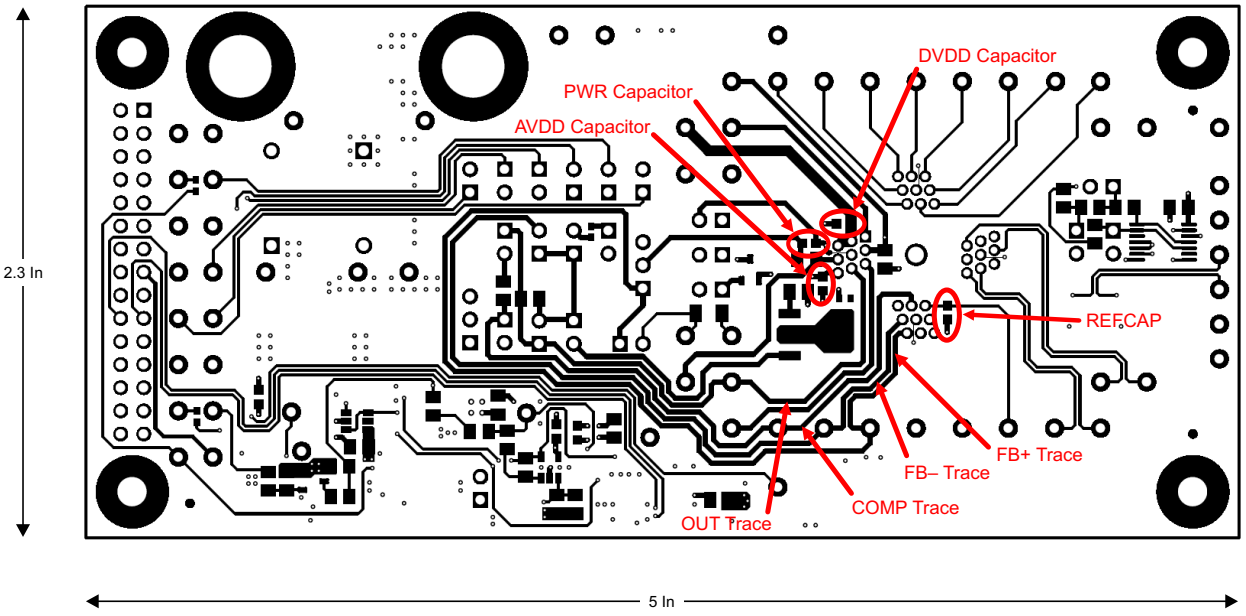


Figure 44. Layout Diagram

11 Device and Documentation Support

11.1 Trademarks

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA300ARHHR	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	PGA300A RHH	Samples
PGA300ARHHT	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	PGA300A RHH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

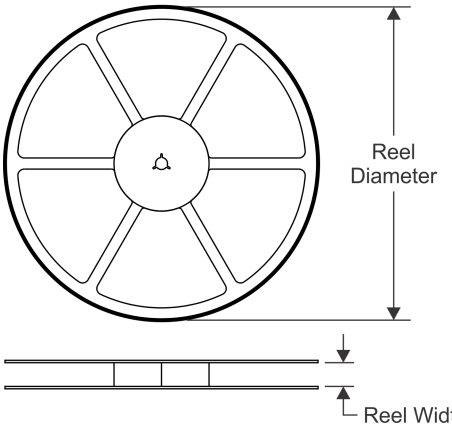
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

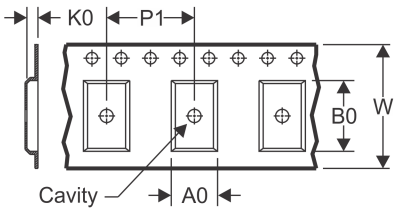
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

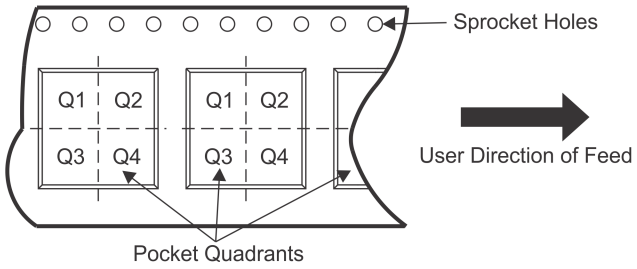


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

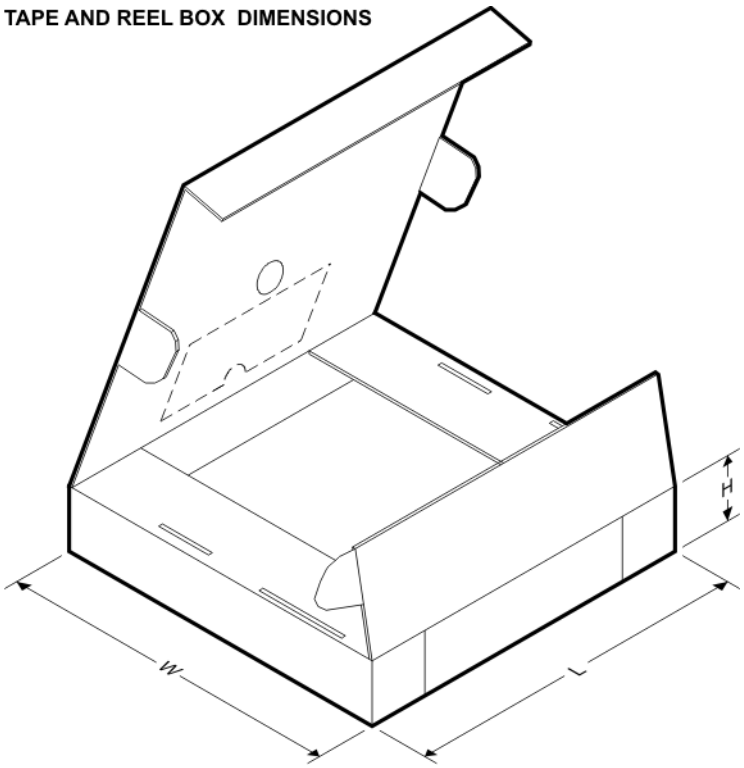
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA300ARHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
PGA300ARHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

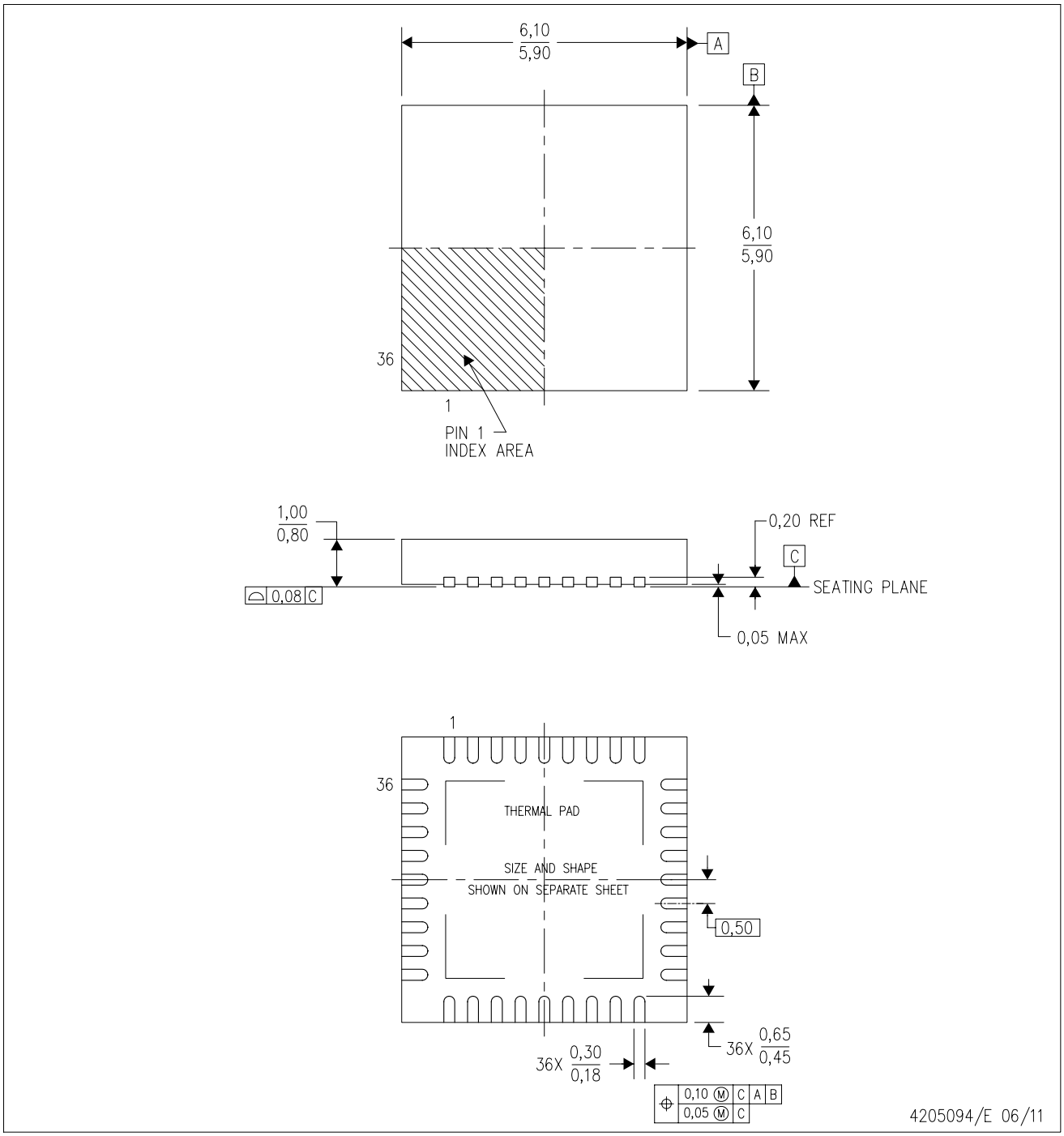
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA300ARHHR	VQFN	RHH	36	2500	367.0	367.0	38.0
PGA300ARHHT	VQFN	RHH	36	250	210.0	185.0	35.0

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

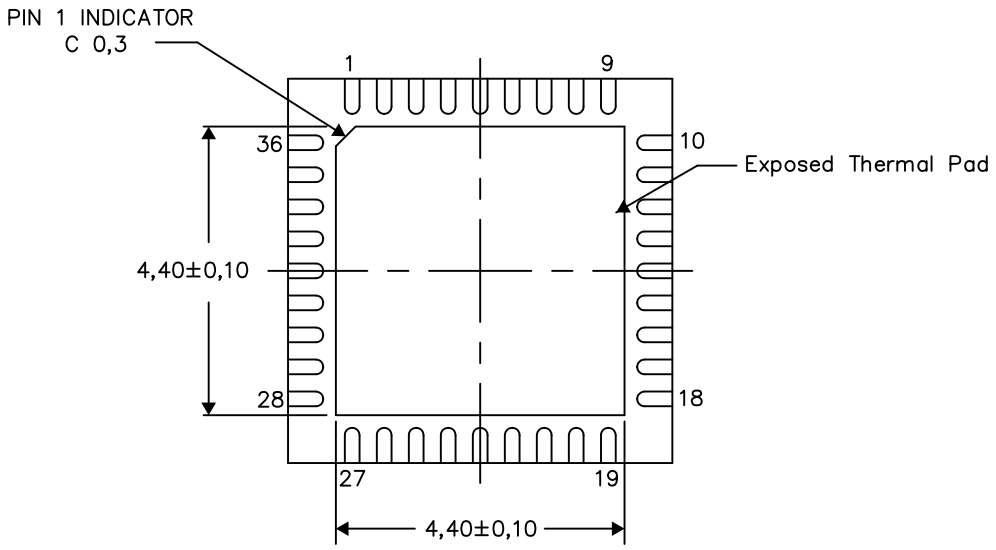
RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



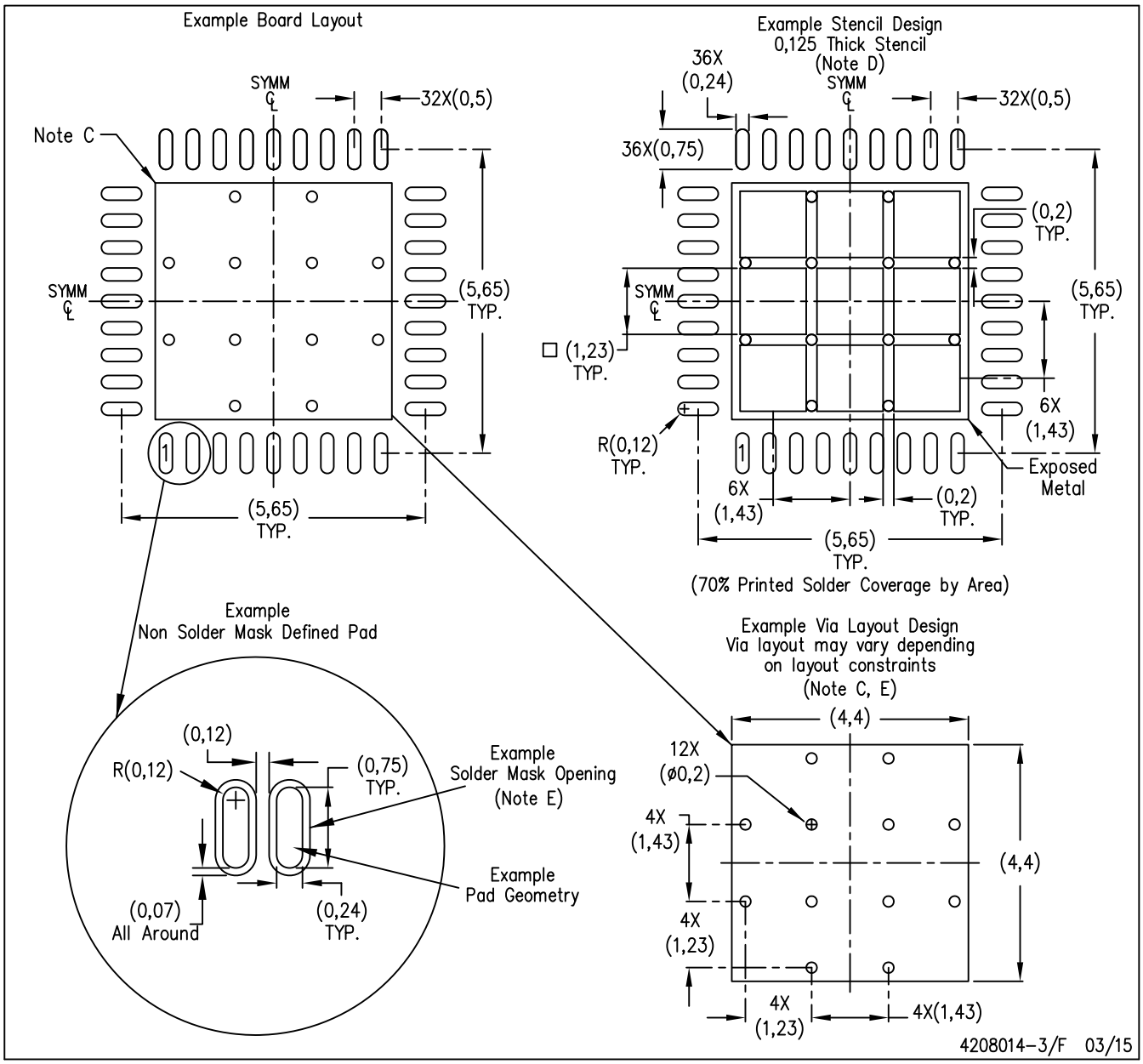
Bottom View

Exposed Thermal Pad Dimensions

4206362–5/M 11/13

NOTE: All linear dimensions are in millimeters

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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