SIEMENS

# ICs for Communications

## Signal Processing Subscriber Line Interface Codec Filter SLICOFI®

PEB 3065 Version 3.2
PEF 3065 Version 3.2

Data Sheet 01.98

DS 2

| PEB 3065<br>PEF 3065<br>Revision History: | | Current Version: 01.98 |
|---|---|---|
| Previous Version: | | 03.95 (V 1.0) |
| Page (in previous Version) | Page (in current Version) | Subjects (major changes since last revision) |
| | | |
| | | |

**Edition 01.98**

**Published by Siemens AG,**
**HL TS,**
**Balanstraße 73,**
**81541 München**



**Attention please!**

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

For questions on technology, delivery and prices please contact the Semiconductor Group Offices in Germany or the Siemens Companies and Representatives worldwide (see address list).

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Siemens Office, Semiconductor Group.

Siemens AG is an approved CECC manufacturer.

**Packing**

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.
For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

**Components used in life-support devices or systems must be expressly authorized for such purpose!**

Critical components[1] of the Semiconductor Group of Siemens AG, may only be used in life-support devices or systems[2] with the express written approval of the Semiconductor Group of Siemens AG.

1 A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or effectiveness of that device or system.

2 Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.

**Table of Contents** **Page**

**Table of Contents** **Page**

# 1 General Description

The Signal Processing Subscriber Line Interface Codec Filter SLICOFI (PEB 3065/PEF 3065) is a logic continuation of the well established family of the SIEMENS PCM-Codec-Filter-IC's with the vertical integration of all DC-feeding, Supervision and Meterpulse Injection features on chip as well. Fabricated in a standard 1 µm BiCMOS technology the SLICOFI is tailored for very flexible solutions in digital communication systems.

For the first time the SLICOFI uses the benefits of a DSP not only for the voice channel but even for line feeding and supervision which leads to a very high flexibility without the need for external components.

Based on an advanced digital filter concept, the PEB 3065/PEF 3065 provides excellent transmission performance. The new filter concept (second generation in SIEMENS-Codec-family) leads to a maximum of independence between the different filter blocks. Each filter block can be seen as a one to one representative of the corresponding network element. Together with the software package SLICOS, filter optimizing to different applications can be done in a clear and straight forward procedure. The AC frequency behavior is mainly determined by the digital filters. Using the new oversampling 1 bit-AD/DA converter, linearity is only limited by second order parasitic effects.

The new - digital - solution of line feeding offers free programmability of feeding current and voltage as well as very fast settling of the dc-operating point after transitions. A 0.3 Hz lowpass filter in the DC-loop is mainly responsible for the system stability.

Additionally teletax generation and filtering is implemented as well as free programmable (balanced) ring generation with zero-crossing injection. Offhook detection with programmable thresholds is possible in all operating modes. To reduce overall power consumption of the line card, the SLICOFI provides a special mode called Power Denial where Offhook is done via 2 high voltage inputs ($V_{LINE1}$ and $V_{LINE2}$) directly connected to the line if the HV-SLIC is switched off.

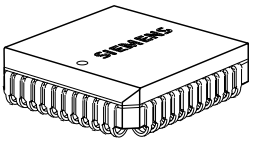
SIEMENS

**Signal Processing**
**Subscriber Line Interface Codec Filter**
**SLICOFI®**

**PEB 3065**
**PEF 3065**

**Data Sheet for the Version 3.2** **CMOS**

## 1.1 Features



**P-LCC-44**

- Single chip CODEC and FILTER including all LOW VOLTAGE SLIC functions
- Only few external components required
- No trimming or adjustments required
- Specification according to relevant CCITT, LSSGR and DBP recommendations
- Digital signal processing technique
- Advanced low power 1 µm BiCMOS[1)] technology
- PCM encoded digital voice transmission (A-Law or µ-Law)
- Four pin serial IOM-2 Interface
- Standard P-LCC-44 package
- High performance AD and DA Conversion
- Programmable digital filters for
  - Impedance matching
  - Transhybrid balancing
  - Frequency response
  - Gain
- Advanced test capabilities
  - Integrated line and circuit tests
  - Two programmable tone generators
- Optimized HV-SLIC Interface
- Fully digital programmable DC-Characteristic
  - Programmable Constant Current from 0-70 mA
  - Programmable Resistive Values from 0-2 $\times$ 500 $\Omega$
- Programmable Integrated Teletax Injection and Filtering during Conversation and Onhook
  - Programmable up to 125 mVrms (5 Vrms at ab-wire)
  - Programmable frequency 12/16 kHz

1) Abbreviations see **chapter 10.4**.

| Type | Package |
|---|---|
| PEB 3065N V3.2 | P-LCC-44 / Tube |
| PEB 3065N V3.2 | P-LCC-44 / Tape in Real |
| PEF 3065N V3.2 | P-LCC-44 / Tape in Real |

- Polarity reversal (programmable soft or hard)
- Integrated (balanced) Ringing Generation with zero crossing injection
  - Programmable frequency between 16.6 and 70 Hz (up to 300 Hz for test)
  - Programmable amplitude up to 2.125 Vrms (85 Vrms at ab-wire)
- Four operating modes: Power Denial, Power Down, Active and Ringing
- Offhook detection with programmable thresholds for all operating modes
- Integrated Ring Trip Detection with zero crossing turn off function
- Ground Start and Loop Start possible
- Integrated checksum Calculation for CRAM
- Line Card Identification

## 2 Pin Configuration

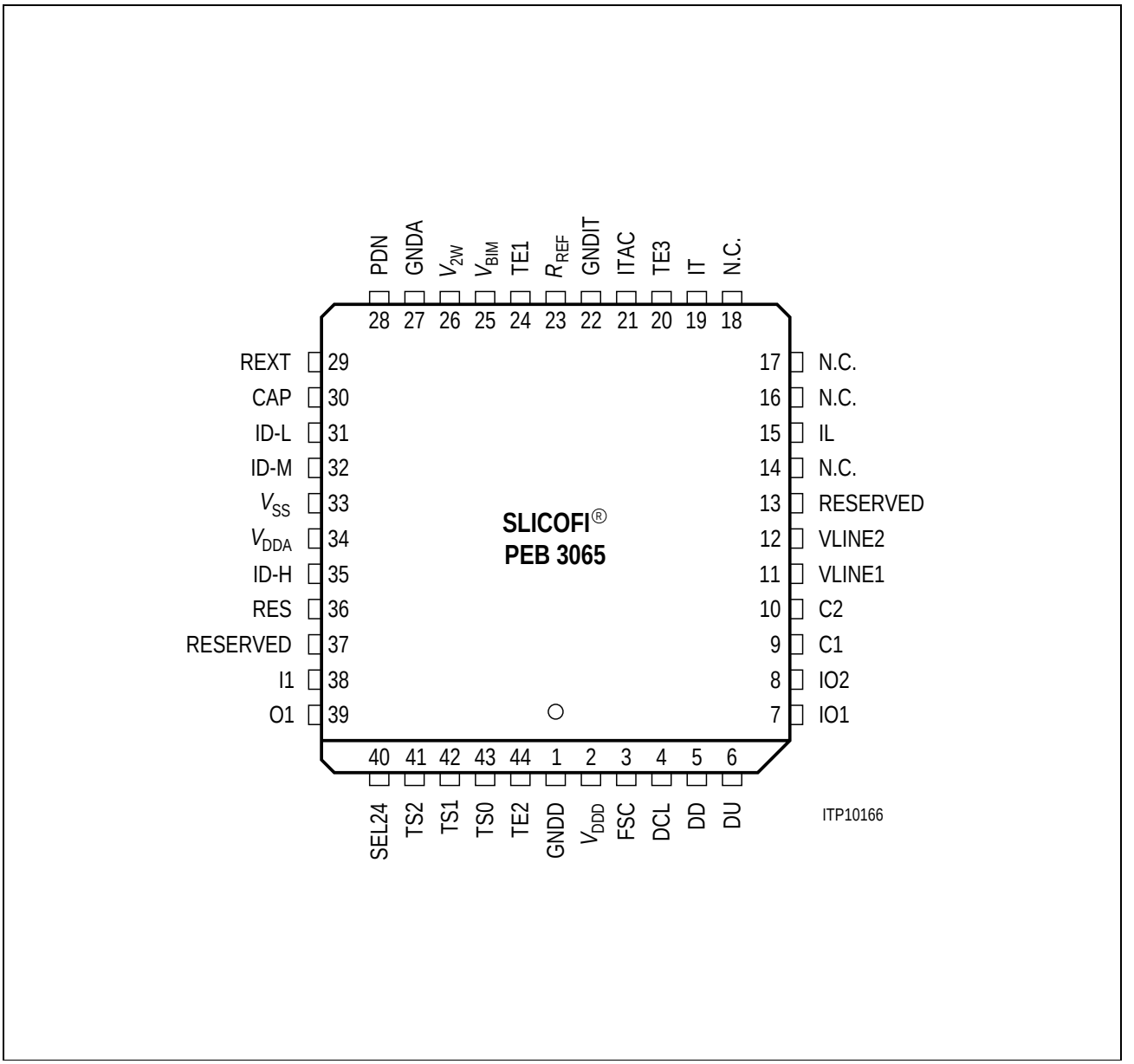



**Figure 1**

## 2.1 Pin Definition and Functions

The following tables group the pins according to their functions. They include pin number, pin name, type, a brief description of the function, and cross-references referring to the sections in which the pin functions are discussed.

**Table 1**

| Pin No. | Name | Type | Function | Reference |
|---|---|---|---|---|
| 27 | GNDA | – | Analog Ground | **chapter 9.1.1** |
| 1 | GNDD | – | Digital Ground | **chapter 9.1.1** |
| 34 | $V_{DDA}$ | – | + 5 V Analog Supply Voltage | **chapter 9.1.1** |
| 2 | $V_{DDD}$ | – | + 5 V Digital Supply Voltage | **chapter 9.1.1** |
| 33 | $V_{SS}$ | – | – 5 V Analog Supply Voltage | **chapter 9.1.1** |

**Table 2 IOM®-2 Pins**

| Pin No. | Name | Type | Function | Reference |
|---|---|---|---|---|
| 6 | DU | O | IOM-2 Data Upstream | **chapter 4** |
| 5 | DD | I | IOM-2 Data Downstream | **chapter 4** |
| 4 | DCL | I | IOM-2 Data-Clock | **chapter 4** |
| 3 | FSC | I | IOM-2 Frame-Sync. | **chapter 4** |
| 43 | TS0 | I | Time Slot selection Pin 0 | **chapter 4** |
| 42 | TS1 | I | Time Slot selection Pin 1 | **chapter 4** |
| 41 | TS2 | I | Time Slot selection Pin 2 | **chapter 4** |
| 40 | SEL24 | I | Select DCL = 2 or 4 MHz | **chapter 4** |

**Table 3 Interface to HV-SLIC**

| Pin No. | Name | Type | Function | Reference |
|---|---|---|---|---|
| 25 | $V_{BIM}$ | I | Battery Image Input | **chapter 7** |
| 28 | PDN | O | Set the HV-SLIC to Power Denial | **chapter 7** |
| 19 | IT | I | Transversal Current Input (AC + DC) | **chapter 7** |
| 21 | ITAC | I | Transversal Current Input (for AC) | **chapter 7** |
| 22 | GNDIT | I | Analog Ground | **chapter 7** |
| 15 | IL | I | Longitudinal Current Input | **chapter 7** |

**Table 3 Interface to HV-SLIC** (cont'd)

| Pin No. | Name | Type | Function | Reference |
|---|---|---|---|---|
| 26 | $V_{2W}$ | O | Two Wire Output Voltage | **chapter 7** |
| 9 | C1 | O | Ternary Interface to HV-SLIC | **chapter 7** |
| 10 | C2 | O | Ternary Interface to HV-SLIC | **chapter 7** |
| 11 | $V_{LINE\ 1}$ | I | Offhook-Detection in Power Denial Mode | **chapter 7** |
| 12 | $V_{LINE\ 2}$ | I | Offhook-Detection in Power Denial Mode | **chapter 7** |

**Table 4 IO Pins**

| Pin No. | Name | Type | Function | Reference |
|---|---|---|---|---|
| 7 | IO1 | I/O | User-Programmable I/O Pin | **chapter 5.6** |
| 8 | IO2 | I/O | User-Programmable I/O Pin | **chapter 5.6** |
| 38 | I1 | I | Fixed Input Pin | **chapter 5.6** |
| 39 | O1 | O | Fixed Output Pin | **chapter 5.6** |

**Table 5 Miscellaneous Function Pins**

| Pin No. | Name | Type | Function | Reference Values |
|---|---|---|---|---|
| 36 | RES | I | Reset | **chapter 6.1** |
| 30 | CAP | I | External Capacitor to GNDA | 68 nF 5% |
| 23 | RREF | I | External Resistor to GNDA | 30 k 1% |
| 29 | REXT | I | External Ring Sync. Input | **chapter 6.6** |
| 31 | ID-L | I | External Identification (Pin strapping) | **chapter 10.2** |
| 32 | ID-M | I | External Identification (Pin strapping) | **chapter 10.2** |
| 35 | ID-H | I | External Identification (Connect ASIC) | **chapter 10.2** |
| 20 | TE3 | O | Test Pin, mustn't be connected | – |
| 24 | TE1 | – | Test Pin (Not connected) | – |
| 44 | TE2 | O | Test Pin, mustn't be connected | – |

**Table 6 Pins not Used**

| Pin No. | Name | Type | Function | Reference |
|---|---|---|---|---|
| 13 | RESERVED | – | Reserved (not connected) | – |
| 37 | RESERVED | O | Reserved test pin, mustn’t be connected | – |
| 14 | N.C. | – | Not connected (not used) | – |
| 16 | N.C. | – | Not connected (not used) | – |
| 17 | N.C. | – | Not connected (not used) | – |
| 18 | N.C. | – | Not connected (not used) | – |

## 3 SLICOFI® Principles

Five Oversampling AD/DA converters are necessary for data conversion to gain the aspired programmability in the DSP. Generally the SLICOFI can be divided between the AC-Loop which is handling the voice and additionally teletax and the DC-Loop for line feeding, ringing injection and supervision.

### 3.1 SLICOFI® Signal Flow Graph: AC

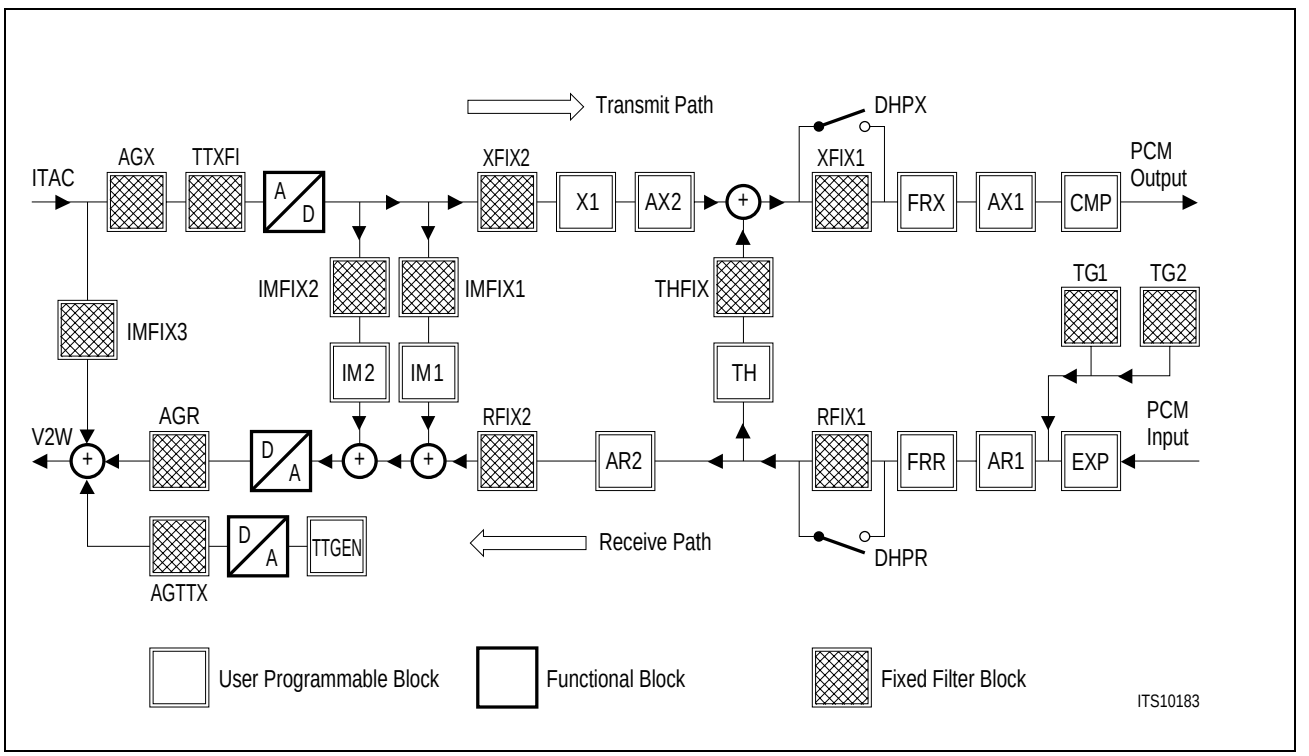



**Figure 2**

### Transmit Path

The analog input signal has to be connected to pin 21 (ITAC) by an external capacitor (680 nF - 1 µF) for AC/DC separation. After passing a simple initializing prefilter (PREFI) the voice signal is converted to a 1-bit digital data stream in the ΣΔ-converter. The first down sampling steps are done in fast running digital hardware filters. The following steps are implemented in the micro code which has to be executed by the central Digital Signal Processor. This DSP-machine is able to handle the workload for the DC-loop as well. At the end the fully processed signal (flexibly programmed in many parameters) is transferred to the IOM-2 Interface in a PCM-compressed signal representation.

### Receive Path

The digital input signal is received via the IOM-2 Interface. Expansion, PCM-lowpass-filtering, gain correction and frequency response correction are the next

steps which are done by the DSP-machine. The up sampling interpolation steps are again processed by fast hardware structures to reduce the DSP-workload. The upsampled 1-bit data stream is then converted to an analog equivalent which is smoothed by a POST-Filter (POFI). At the summing point the values of the TTX-Generator and the DC-loop are added and then transferred to the output pin 26 ($V_{2W}$).

### Loops

There are two different loops implemented: The Impedance Matching (IM) loop which is divided in 3 separate loops to guarantee very high flexibility to various impedances, and the Transhybrid Balancing (TH) loop.

## 3.2 SLICOFI® Signal Flow Graph: DC

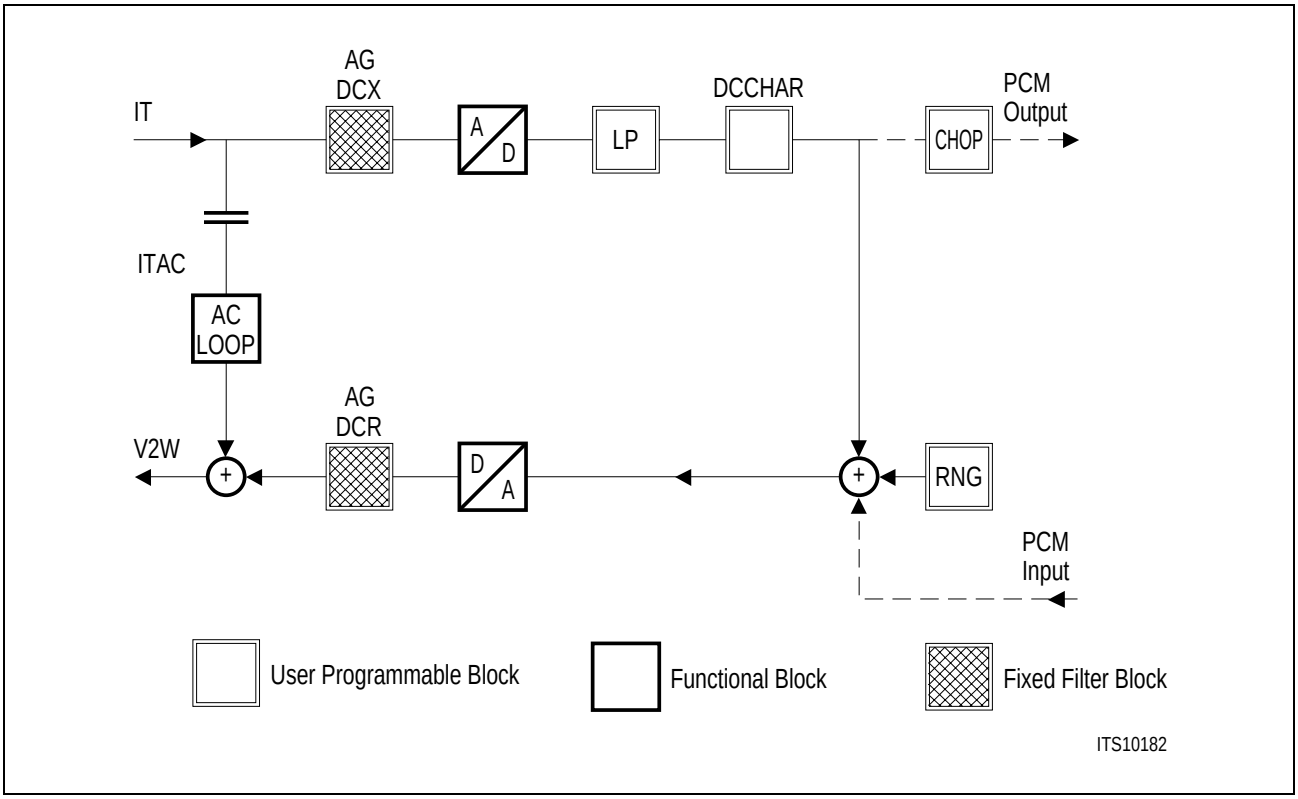



**Figure 3**

### DC Characteristic

The incoming information at pin IT (scaled transversal current (AC + DC) transferred to a voltage via a resistor) is first lowpass filtered (0.3 Hz) for stability and noise reasons and then fed into the DC-characteristic block. This consists of two branches which represents different kinds of feeding behavior. In typical applications it acts as a programmable constant current source ($R_{in}$ > 30 k). If the desired value cannot be held

feeding switches automatically and smooth to the resistive branch ($R_{in}$ > 0-1 k). For superposing voice as well as Teletax pulses the necessary drop at the line can be calculated and taken into account as well. The outgoing DC-feeding value - superposed with the AC-Loop result at the summing point is transferred to pin 26 ($V_{2W}$).

**Supervision**

The HOOK-information is the most important one and the SLICOFI provides this information via CIDU (see **chapter 5.6**), in all operating modes:

For Power Denial via 2 high voltage input pins ($V_{LINE}$) directly connected to the line.

For each other mode the line current information (from pin IT) is transferred via an ADC to the DSP where the Offhook information is extracted in the proper way:

Power Down: Offhook is detected if Constant current feeding is possible.

Active: Offhook is detected if the incoming voltage at IT exceeds a programmed value. To avoid instable information, lowpass filtering and a hystereses is provided (2 independent programmable values for Offhook and Onhook detection).

Ringing: Ring Trip occurs if the DC-value at IT exceeds the programmed Ring Trip threshold. The AC-value is filtered by the SLICOFI automatically. Ring Trip detection is reported within 2 cycles of the ring period and then the internal ring generator is switched off within 3 cycles at zero crossing of the ring voltage.

Ground key (CIDU-6: GNK) is reported if the absolute value of the voltage at pin IL exceeds 255 mV. With a programmable lowpass filter (see **chapter 5.6**) interfering frequencies (e.g. power lines with 50/60 Hz) can be filtered very effectively.

## 3.3 Test Features

The SLICOFI provides two different kinds of test features: Internal test loops for circuit testing and defined test loops to perform board and line tests. There are loops for testing AC and DC path. As a special feature it is possible to switch signals to and from the DC-path via the IOM-2 Interface. Additionally there is the possibility to cut off the AC-receive and transmit path.

(The different kinds of testmodes are described in **chapter 10.3**)

## 3.4 SLICOFI® Signal Block Diagram

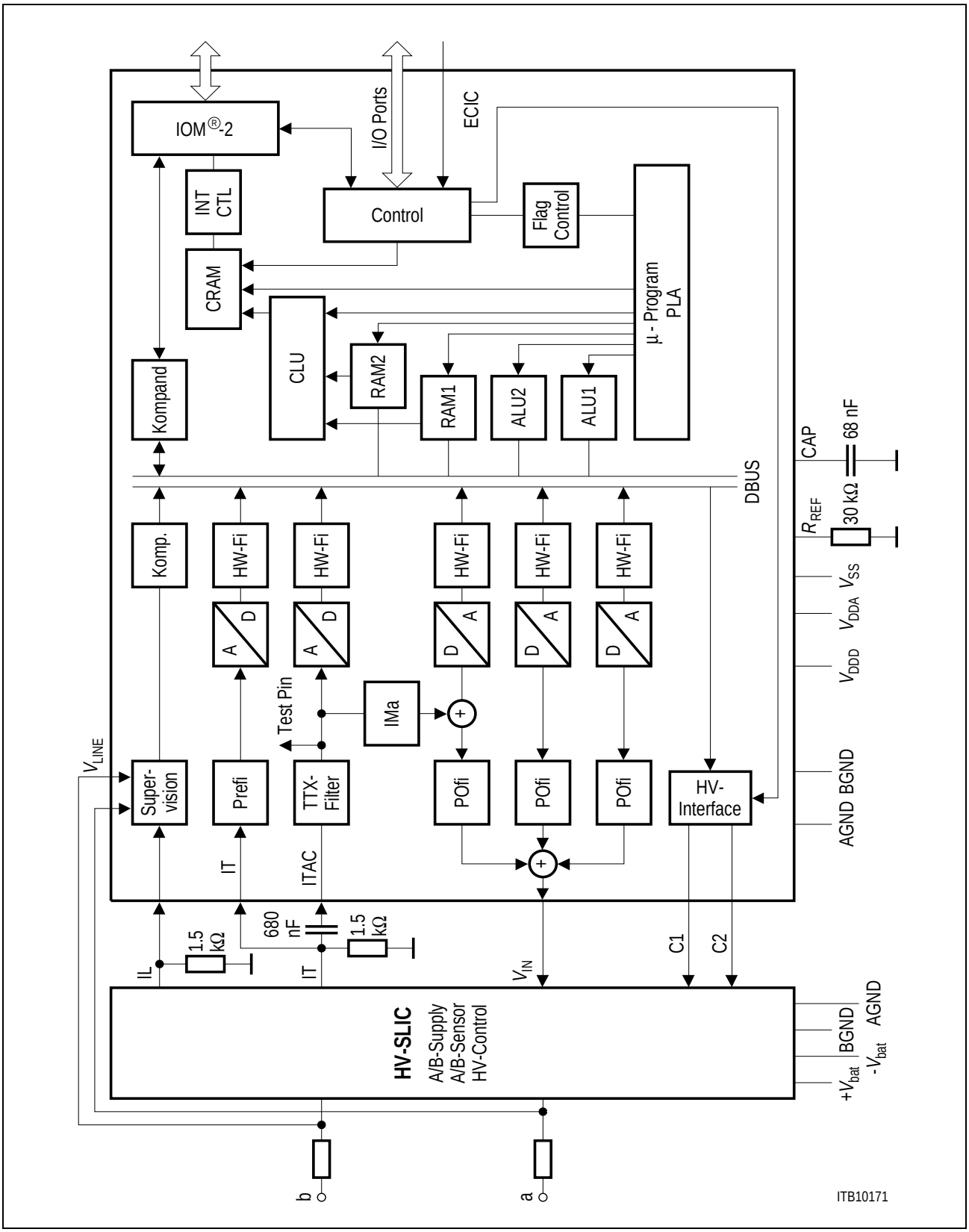



**Figure 4**

## 4 IOM®-2 Interface

The IOM-2 interface consists of two data lines and two clock lines. DU (data upstream) carries data from the SLICOFI to a master device. DD (data downstream) carries data from the master device to the SLICOF. A frame synchronization clock signal (8 kHz, FSC) as well as a data clock signal (2048 kHz or 4096 kHz, DCL) has to be supplied to the SLICOFI. The SLICOFI handles data as described in the IOM-2 specification for analog devices.

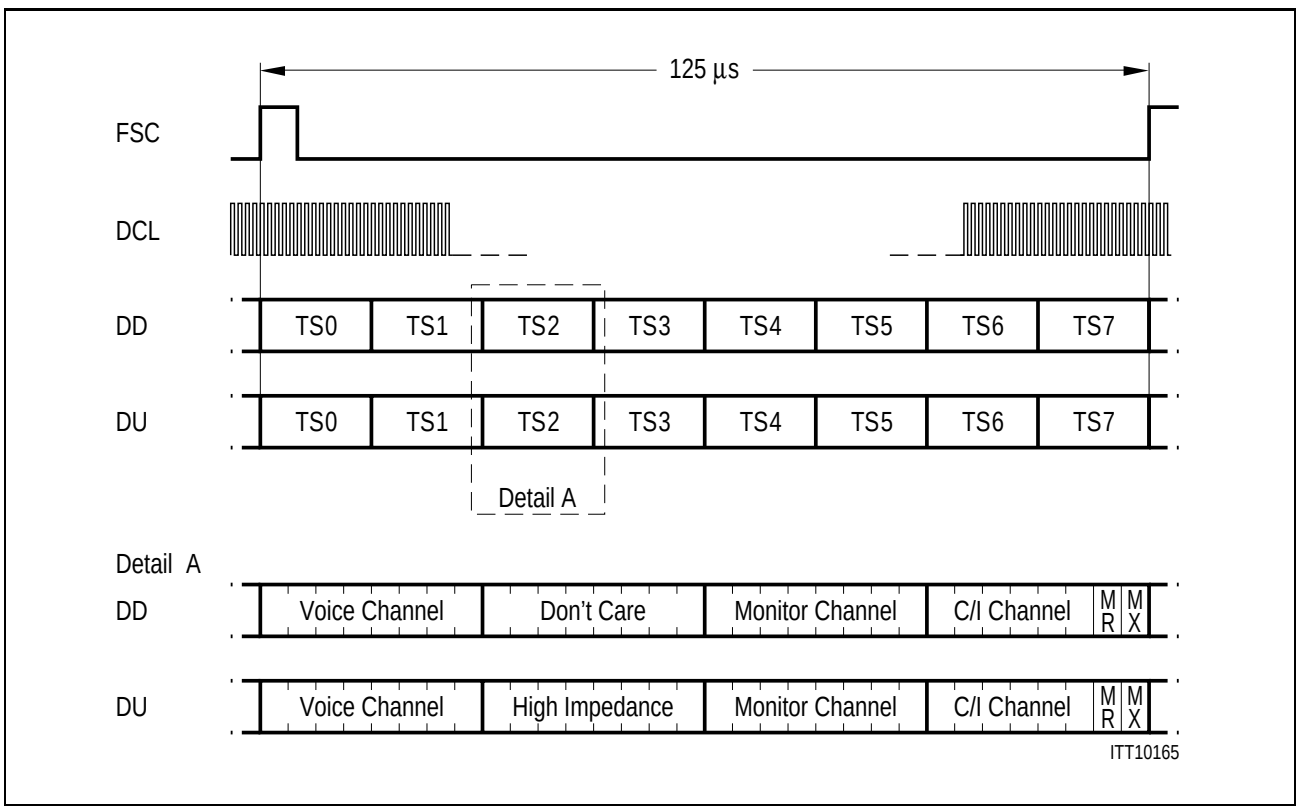



**Figure 5 IOM®-2 Interface Timing for 8 voice channels (per 8 kHz frame)**

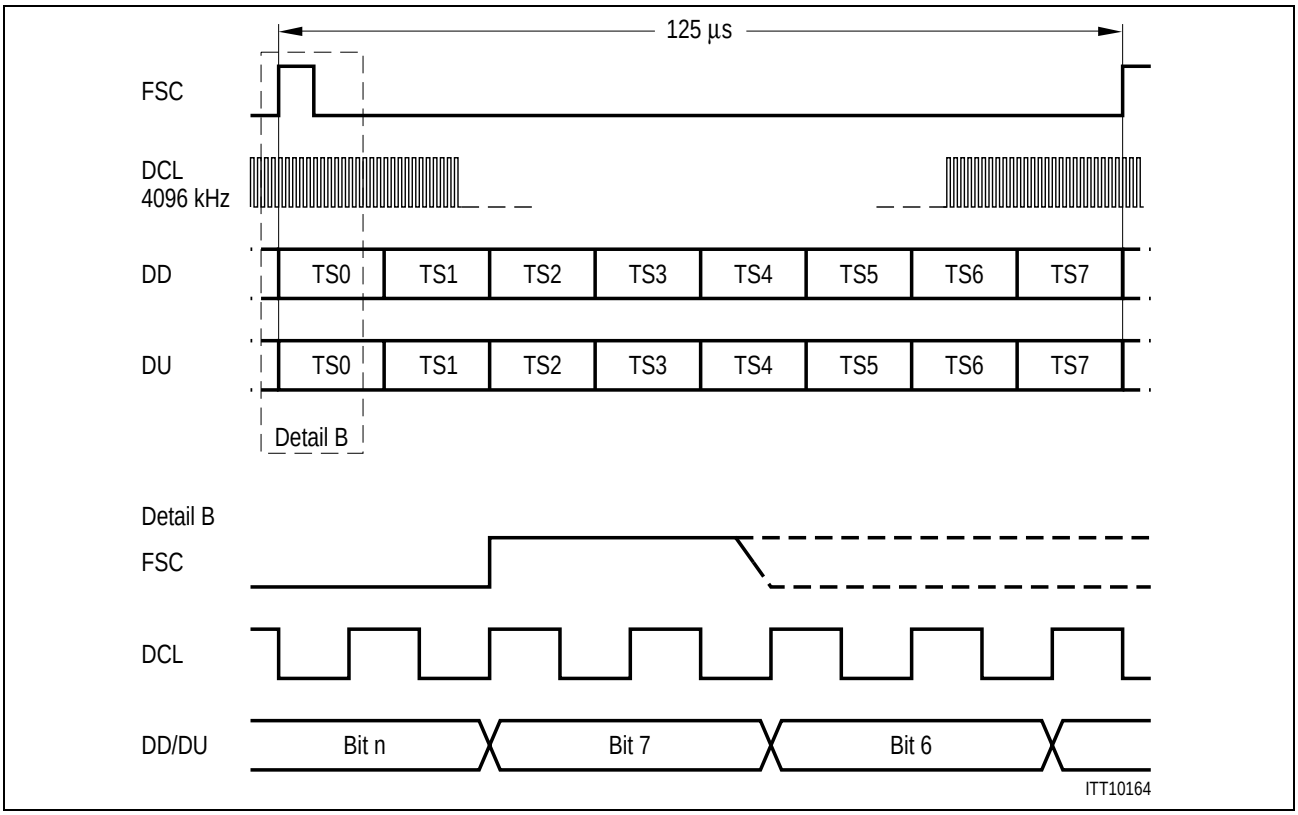



**Figure 6 IOM®-2 Interface Timing (DCL = 4096 kHz, SEL24 = 1, per 8 kHz frame)**

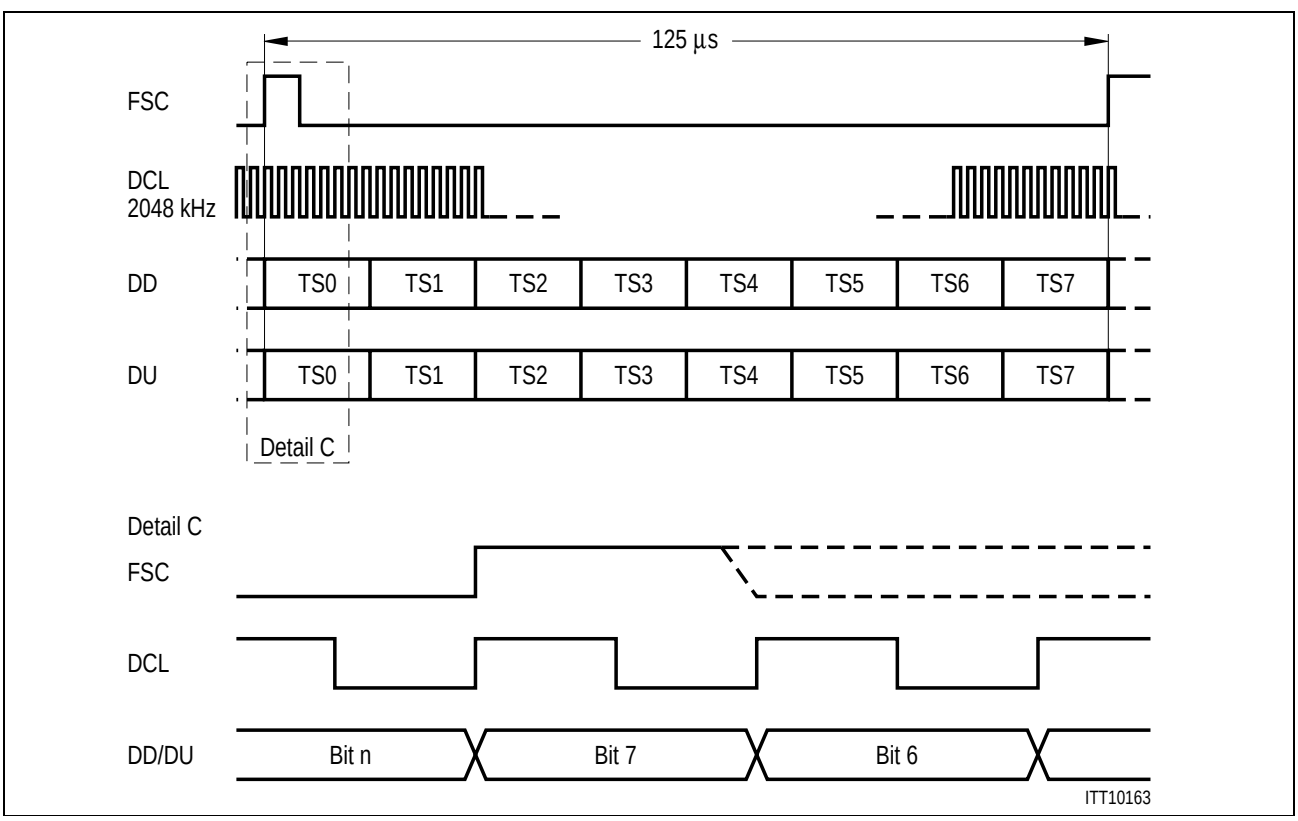



**Figure 7 IOM®-2 Interface Timing (DCL = 2048 kHz, SEL24 = 0)**

### IOM®-2 Time Slot Assignment

An assignment of 8 time slots is possible for each voice-channel. The IOM-2 operating mode and time slot selection is set completely by pin-strapping.

**Table 7**

| SEL24 | TS2 | TS1 | TS0 | IOM®-2 Operating Mode |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Time slot 0; DCL = 2048 kHz |
| ~~0~~ | ~~0~~ | ~~0~~ | ~~1~~ | ~~Time slot 1; DCL = 2048 kHz~~ [1)] |
| ~~0~~ | ~~0~~ | ~~1~~ | ~~0~~ | ~~Time slot 2; DCL = 2048 kHz~~ [1)] |
| ~~0~~ | ~~0~~ | ~~1~~ | ~~1~~ | ~~Time slot 3; DCL = 2048 kHz~~ [1)] |
| 0 | 1 | 0 | 0 | Time slot 4; DCL = 2048 kHz |
| ~~0~~ | ~~1~~ | ~~0~~ | ~~1~~ | ~~Time slot 5; DCL = 2048 kHz~~ [1)] |
| 0 | 1 | 1 | 0 | Time slot 6; DCL = 2048 kHz |
| 0 | 1 | 1 | 1 | Time slot 7; DCL = 2048 kHz |
| 1 | 0 | 0 | 0 | Time slot 0; DCL = 4096 kHz |
| 1 | 0 | 0 | 1 | Time slot 1; DCL = 4096 kHz |
| 1 | 0 | 1 | 0 | Time slot 2; DCL = 4096 kHz |
| 1 | 0 | 1 | 1 | Time slot 3; DCL = 4096 kHz |
| 1 | 1 | 0 | 0 | Time slot 4; DCL = 4096 kHz |
| 1 | 1 | 0 | 1 | Time slot 5; DCL = 4096 kHz |
| 1 | 1 | 1 | 0 | Time slot 6; DCL = 4096 kHz |
| 1 | 1 | 1 | 1 | Time slot 7; DCL = 4096 kHz |

[1)] Time slots 1, 2, 3 and 5 are not working with DCL = 2048 kHz.

For a workaround in the 2MHz mode please contact the SIEMENS HL Application group.

# 5 Programming the SLICOFI®

With the appropriate commands, the SLICOFI can be programmed and verified very flexible via the IOM-2 Interface monitor channel.

Data transfer to the SLICOFI starts with a SLICOFI-specific address byte ($81_H$).

With the second byte one of 3 different types of commands (SOP, TOP or COP) is selected. SOP and COP can be used as a write or read command, the TOP-Command is used for reading only. Due to the extended SLICOFI feature control facilities, SOP, COP and TOP commands contain additional information (e.g. number of subsequent bytes) for programming (write) and verifying (read) the SLICOFI status.

A write command is followed by up to 8 bytes of data. The SLICOFI responds to a read command with its IOM2 specific address and the requested information, that is up to 15 bytes of data (see **chapter 5.2**).

**Attention:** Each byte on the monitor channel has to be sent twice at least according to the IOM2 Monitor handshake procedure. (For more information on IOM-2 specific Monitor Channel Data Structure see **chapter 10**).

## 5.1 Types of Monitor Bytes

The 8-bit Monitor bytes have to be interpreted as either commands or status information stored in Configuration Registers or the Coefficient Ram. There are three different types of SLICOFI commands which are selected by bit 2 and 3 as shown below.

(x... don't care)

**SOP** **Status Operation:** SLICOFI status setting/monitoring

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | 0 | 1 | | |

**TOP** **Transfer Operation:** Read Certain Status Options only

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | 1 | 1 | | |

**COP** **Coefficient Operation:** filter coefficient setting/monitoring

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | x | 0 | | |

**Storage of programming information:**

8 (9) status configuration registers: (SCR0), SCR1, ... SCR8 accessed by SOP commands

| | |
|---|---|
| 8 test configuration registers: | STCR1...STCR8 accessed by SOP commands |
| 18 Transfer configuration registers: | TCR1, TCR2...TCR18 accessed by TOP commands |
| 1 Coefficient RAM: | CRAM accessed by COP commands |

## 5.2 SLICOFI® Programming Procedure

(DD... Data Downstream, DU... Data Upstream, only the Monitor Bytes are considered)

**SOP– Write Commands**

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| SOP-Write 0 Byte | | 0 | | | 0 | 1 | 0 | 0 | | Idle | | | | | | | | |

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| SOP-Write 2 Bytes | | 0 | | | 0 | 1 | 0 | 1 | | Idle | | | | | | | | |
| SCR1 | Data | | | | | | | | | Idle | | | | | | | | |
| SCR2 | Data | | | | | | | | | Idle | | | | | | | | |

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| SOP-Write 8 Bytes | | 0 | | | 0 | 1 | 1 | 0 | | Idle | | | | | | | | |
| SCR1 | Data | | | | | | | | | Idle | | | | | | | | |
| : | : | | | | | | | | | : | | | | | | | | |
| SCR8 | Data | | | | | | | | | Idle | | | | | | | | |

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| SOP-Write 8 Bytes | | 0 | | | 0 | 1 | 1 | 1 | | Idle | | | | | | | | |
| STCR1 | Data | | | | | | | | | Idle | | | | | | | | |
| : | : | | | | | | | | | : | | | | | | | | |
| STCR8 | Data | | | | | | | | | Idle | | | | | | | | |

### TOP – Write Commands

no write command possible; reading only.

### COP – Write Commands

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| COP-Write 8 Bytes | | 0 | 0 | | | 0 | | | | Idle | | | | | | | | |
| Coeff. 1 | Data | | | | | | | | | Idle | | | | | | | | |
| : | : | | | | | | | | | : | | | | | | | | |
| Coeff. 8 | Data | | | | | | | | | Idle | | | | | | | | |

### SOP – Read Commands

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| SOP-Read 1 Byte | | 1 | | | 0 | 1 | 0 | 0 | | Idle | | | | | | | | |
| | Idle | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
| | Idle | | | | | | | | | Data | | | | | | | | SCR0 |

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| SOP-Read 3 Bytes | | 1 | | | 0 | 1 | 0 | 1 | | Idle | | | | | | | | |
| | Idle | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
| | Idle | | | | | | | | | Data | | | | | | | | SCR0 |
| | Idle | | | | | | | | | Data | | | | | | | | SCR1 |
| | Idle | | | | | | | | | Data | | | | | | | | SCR2 |

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| SOP-Read 9 Bytes | | 1 | | | | 1 | 1 | 0 | | Idle | | | | | | | | |
| | Idle | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
| | Idle | | | | | | | | | Data | | | | | | | | SCR0 |
| | : | | | | | | | | | : | | | | | | | | : |
| | Idle | | | | | | | | | Data | | | | | | | | SCR8 |

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| SOP-Read 8 Bytes | | 1 | | | | 1 | 1 | 1 | | Idle | | | | | | | | |
| | Idle | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
| | Idle | | | | | | | | | Data | | | | | | | | STCR1 |
| | : | | | | | | | | | : | | | | | | | | : |
| | Idle | | | | | | | | | Data | | | | | | | | STCR8 |

**TOP – Read Commands**

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| TOP-Read 1 Byte | | 1 | | | 1 | 1 | 0 | 0 | | Idle | | | | | | | | |
| | Idle | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
| | Idle | | | | | | | | | Data | | | | | | | | TCR1 |

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| TOP-Read 3 Bytes | | 1 | | | 1 | 1 | 0 | 1 | | Idle | | | | | | | | |
| | Idle | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
| | Idle | | | | | | | | | Data | | | | | | | | TCR1 |
| | Idle | | | | | | | | | Data | | | | | | | | TCR2 |
| | Idle | | | | | | | | | Data | | | | | | | | TCR3 |

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| TOP-Read 15 Bytes | | 1 | | | 1 | 1 | 1 | 0 | | Idle | | | | | | | | |
| | Idle | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
| | Idle | | | | | | | | | Data | | | | | | | | TCR4 |
| | : | | | | | | | | | : | | | | | | | | : |
| | Idle | | | | | | | | | Data | | | | | | | | TCR18 |

### COP – Read Commands

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| COP-Read 8 Bytes | | 1 | 0 | | | 0 | | | | Idle | | | | | | | | |
| | Idle | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
| | Idle | | | | | | | | | Data | | | | | | | | Coeff. 1 |
| | : | | | | | | | | | : | | | | | | | | : |
| | Idle | | | | | | | | | Data | | | | | | | | Coeff. 8 |

### Example for a Mixed Command

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| SOP-Write 2 Bytes | | 0 | | | 0 | 1 | 0 | 1 | | Idle | | | | | | | | |
| SCR1 | Data | | | | | | | | | Idle | | | | | | | | |
| SCR2 | Data | | | | | | | | | Idle | | | | | | | | |
| COP-Write 8 Bytes | | 0 | 0 | | | 0 | | | | Idle | | | | | | | | |
| Coeff. 1 | Data | | | | | | | | | Idle | | | | | | | | |
| Coeff. 2 | Data | | | | | | | | | Idle | | | | | | | | |
| Coeff. 3 | Data | | | | | | | | | Idle | | | | | | | | |
| Coeff. 4 | Data | | | | | | | | | Idle | | | | | | | | |
| Coeff. 5 | Data | | | | | | | | | Idle | | | | | | | | |
| Coeff. 6 | Data | | | | | | | | | Idle | | | | | | | | |
| Coeff. 7 | Data | | | | | | | | | Idle | | | | | | | | |
| Coeff. 8 | Data | | | | | | | | | Idle | | | | | | | | |
| SOP-Read 3 Bytes | | 1 | | | 0 | 1 | 0 | 1 | | Idle | | | | | | | | |
| | Idle | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
| | Idle | | | | | | | | | Data | | | | | | | | SCR0 |
| | Idle | | | | | | | | | Data | | | | | | | | SCR1 |
| | Idle | | | | | | | | | Data | | | | | | | | SCR2 |
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| COP-Read 8 Bytes | | 1 | 0 | | | 0 | | | | Idle | | | | | | | | |
| | Idle | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |

| DD | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Idle | | | | | | | | | Data | | | | | | | | Coeff. 1 |
| | Idle | | | | | | | | | Data | | | | | | | | Coeff. 2 |
| | Idle | | | | | | | | | Data | | | | | | | | Coeff. 3 |
| | Idle | | | | | | | | | Data | | | | | | | | Coeff. 4 |
| | Idle | | | | | | | | | Data | | | | | | | | Coeff. 5 |
| | Idle | | | | | | | | | Data | | | | | | | | Coeff. 6 |
| | Idle | | | | | | | | | Data | | | | | | | | Coeff. 7 |
| | Idle | | | | | | | | | Data | | | | | | | | Coeff. 8 |
| Address | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Idle | | | | | | | | |
| TOP-Read 1 Byte | | 1 | | | 1 | 1 | 0 | 0 | | Idle | | | | | | | | |
| | Idle | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
| | Idle | | | | | | | | | Data | | | | | | | | TCR1 |

## 5.3 SOP Command

To modify or evaluate the SLICOFI status, the contents of up to 8 configuration registers SCR1, ... SCR8 may be transferred to, or up to 9 (incl. SCR0) from the SLICOFI. This is done by a SOP-Command (status operation command).

With LSEL = 11 some test registers can be set/read (for internal use only!).

The two commands POLNR and RST are only valid if RW = 0 (write); they are ignored for RW = 1 (read)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | RW | POLNR | RST | 0 | 1 | LSEL1 | LSEL0 |

**RW** Read/Write Information: Enables reading from the SLICOFI or writing information to the SLICOFI
RW = 0 Write to SLICOFI
RW = 1 Read from SLICOFI

**POLNR** General DC feeding Information: Normal or Reverse Polarity
POLNR = 0 sets the SLICOFI to Normal Polarity feeding
POLNR = 1 sets the SLICOFI to Reverse Polarity feeding

**RST** Software Reset
RST = 0 Normal Operation
RST = 1 Reset SLICOFI (same as Reset pin 36 (RES)): sets the SLICOFI to the basic setting mode (see **chapter 6.1**).

**LSEL** Length select information (also see programming procedure, **chapter 5.2**).
This field identifies the number of subsequent data bytes
If RW = 0 Write to SLICOFI
LSEL = 00 no byte of data is following
LSEL = 01 2 bytes of data are following (SCR1, SCR2)
LSEL = 10 8 bytes of data are following (SCR1,... SCR8)
LSEL = 11 Accesses Test Registers (see Appendix)

If RW = 1 Read from SLICOFI
LSEL = 00 1 byte of data is following (SCR0)
LSEL = 01 3 bytes of data are following (SCR0, SCR1, SCR2)
LSEL = 10 9 bytes of data are following (SCR0, ... SCR8)
LSEL = 11 Accesses Test Registers (see Appendix, **chapter 10.3**)

### SCR0 Configuration Register 0

Configuration Register SCR0 can be read only. It gives a mirror of the SOP-Command itself to control its contents and represents the reset value as defined below.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | POLNR | RSTST | 0 | 1 | LSEL1 | LSEL0 |

Reset value: $54_H$ (if only SCR0 is read. It depends on LSEL1 and LSEL0.)

**POLNR** General DC feeding Information: Normal or Reverse Polarity
- POLNR = 0 indicates, that the SLICOFI was set to Normal Polarity feeding
- POLNR = 1 indicates, that the SLICOFI was set to Reverse Polarity feeding[1)]

**RSTST** Status of Reset
Indicates the occurrence of a reset:
- RSTST = 1 if there has been a Reset by any of the following three reasons:
  – via the Reset-pin (RES)
  – via the Power on Reset
  – via the Software Reset (SOP–Command)
  the RSTST-bit is set to ‘1’.
- RSTST = 0 no Reset has occurred since the last SOP-Read (with LSEL = 00b).

This bit is cleared only by a SOP-read with LSEL = 00b at the end of the data transmission.

**LSEL** is the mirror of the SOP-Read LSEL contents.

1) The internal manipulation with “Reverse meterpulses” is not indicated by that bit.

### SCR1 Configuration Register 1

Configuration register SCR1 defines the basic feeding modes of the SLICOFI and enables/disables test features:

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | PD | N/BB | LB | ETG1 | HI-b | HI-a | DHP-X | COR |

Reset value: $00_H$

**PD** SLICOFI is set either in Power Down or Power Denial mode together with CIDD-bits CIDD6,7 (see **chapter 6**).
- PD = 0 SLICOFI set to Power Denial mode; line supervision via $V_{LINE1, 2}$
- PD = 1 SLICOFI set to Power Down mode

**N/BB** SLICOFI is in normal or Boosted Battery mode (see **chapter 6.5**).
- N/BB = 0 Normal feeding
- N/BB = 1 Changes ternary interface to HV-SLIC which sets the HV-SLIC to Boosted Battery mode

**LB** Handling of Loop Back functions for on chip test loops
- LB = 0 normal function
- LB = 1 the desired Loop Back function (analog or digital) is enabled (selected by SCR6, together with the TM-bit (SCR2-3))

**ETG1** Enables programmable Test Tone Generator 1
- ETG1 = 0 Test Tone Generator 1 is disabled
- ETG1 = 1 Test Tone Generator 1 is enabled

**HI-b** For HV-SLIC test function
- HI-b = 0 normal operation
- HI-b = 1 changes ternary Interface to HV-SLIC which sets the b-leg of the line into high impedance state

**HI-a** For HV-SLIC test function
- HI-a = 0 normal operation
- HI-a = 1 changes ternary Interface to HV-SLIC which sets the a-leg of the line into high impedance state

**DHP-X** Disable Transmit Highpass for test reasons (see **chapter 10.3**)
- DHP-X = 0 Transmit Highpass Filter is enabled
- DHP-X = 1 Transmit Highpass Filter is disabled

**COR** Cut Off Receive Path for test reasons (see **chapter 10.3**)
- COR = 0 Receive Path transmission is available
- COR = 1 Receive Path is disabled

### SCR2 Configuration Register 2

Configuration register SCR2 defines some testmode output results, some special SLMA-mode requirements and the possibility to program 2 I/O-ports.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | MVA | OKTON | OKTTX | OKRNG | TM | NOSL | IO1 | IO2 |

Reset value: $00_H$ (then as measured)

**MVA** Internal measurement results shown in the following 3 bits are valid or not valid (read only) (see **chapter 10.3**)
MVA = 0 the following 3 ok-bit results are not valid
MVA = 1 the following 3 ok-bit results are valid

**OKTON** Test Tone measurement information (read only) - programmed via COP-command (Testloop: DLB_4M and TG1 enabled, see **chapter 10.3**)
OKTON = 0 Test tone value out of defined range
OKTON = 1 Test tone value in defined range

**OKTTX** Test teletax metering information (read only) - programmed via COP-command (see **chapter 10.3**)
OKTTX = 0 Test teletax metering value smaller than defined value
OKTTX = 1 Test teletax metering value larger than defined value

**OKRNG** Test Ring tone information (read only) – programmed via COP-command (see **chapter 10.3**)
OKRNG = 0 Ring tone value smaller than defined value
OKRNG = 1 Ring tone value larger than defined value

**TM** enables or disables the SLICOFI Testmodes (see **chapter 10.3**)
TM = 0 resets the assigned tests (normal mode)
TM = 1 sets the assigned tests (selected by SCR6, together with the LB-bit (SCR1-5))

**NOSL** No slope: means that the ramping of teletax (TTX) signal is switched off
NOSL = 0 Slope of TTX-Signal is smooth
NOSL = 1 Hard switch of TTX-Signal

**IO1** Selection for programmable IO - Pin IO1
IO1 = 0 sets the pin IO1 as an input
IO2 = 1 sets the pin IO1 as an output

**IO2** Selection for programmable IO - Pin IO2
IO1 = 0 sets the pin IO2 as an input
IO2 = 1 sets the pin IO2 as an output

### SCR3 Configuration Register 3

Configuration register SCR3 defines the meterpulse settings and the Data Upstream Persistency Counter.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TTXNO | TTX12 | SOREV | PDADIS | DUP3 | DUP2 | DUP1 | DUP0 |

Reset value: $8A_H$

**TTXNO** Meterpulses are represented by teletax (TTX) with 12 or 16 kHz or with Reverse Polarity
TTXNO = 0 Meterpulses are represented with 12 kHz or 16 kHz
TTXNO = 1 Meterpulses are represented with Reverse Polarity

**TTX12** Teletax-signal with 12 kHz or 16 kHz
TTX12 = 0 16 kHz teletax-signal
TTX12 = 1 12 kHz teletax-signal

**SOREV** The reversal pulse is either soft or hard
SOREV = 0 hard reversal
SOREV = 1 soft reversal

*Note: For proper function special coefficients generated by SLICOS should be used.*

To realize this function following settings must be done:

1. Enable the testregisters (Configuration Register 5: SCR5-1 (ENTR)=1), (**page 32**)
2. The testregisterblock must be load with STCR3-0 (SOFTVER) = 1, (see **chapter 10.3**)

### STCR3 Test Configuration Register 3

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

3. SCR3-5 (SOREV) = 1

**PDADIS** The automatic HV-SLIC Power Down - Active switching (see **chapter 6.4**) can be switched off
PDADIS = 0 use automatic Power Down-Active switching
PDADIS = 1 disables automatic Power Down-Active switching

**DUP** To restrict the rate of upstream C/I-bit changes, deglitching (persistence checking) of the status information from the SLICOFI may be applied. New status information will be transmitted upstream, after it has been stable for N milliseconds. N is binary programmable in the range of 1 to 15 ms in steps of 1 ms; with DUP = $0_H$ the deglitching is disabled.
Reset value is 10 ms.
The HOOK, SLCX and the I(O)-bits are influenced (different counters but same programming).
Detailed info see **chapter 5.4**.

### SCR4 Configuration Register 4

Configuration register SCR4 defines the basic SLICOFI settings which enable / disable the programmable digital filters and the second tone generator.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TH | IM | FRX | FRR | AX | AR | ETG2 | PTG |

Reset value: $00_H$

**TH** Set transhybrid Balancing Filter – together with the bit FIXC (SCR5-5).
For FIXC = 1 the TH-Filter is set to $H_{TH}$ = for $Z_{BRD}$;
for FIXC = 0:
TH = 0 TH-filter is disabled
TH = 1 TH-filter is enabled (use programmed values)

**IM** Set DSP-implemented Impedance Matching Filter - together with the bit FIXC (SCR5-5).
For FIXC = 1 the IM-Filter is set to $H_{IM}$ = for 900;
for FIXC = 0:
IM = 0 IM-filter is disabled
IM = 1 IM-filter is enabled (use programmed values)

**FRX** Enable FRX- (Frequency Response Transmit) Filter
FRX = 0 FRX-filter is disabled ($H_{FRX}$ = 1)
FRX = 1 FRX-filter is enabled (use programmed values)

**FRR** Enable FRR- (Frequency Response Receive) Filter
FRR = 0 FRR-filter is disabled ($H_{FRR}$ = 1)
FRR = 1 FRR-filter is enabled (use programmed values)

**AX** Set AX- (Amplification/Attenuation Transmit) Filter
AX = 0 AX-filter is set to default value ($H_{AX}$= 10 dB)
AX = 1 AX-filter is enabled (use programmed values)

**AR** Set AR- (Amplification/Attenuation Receive) Filter
AR = 0 AR-filter is set to default value ($H_{AR}$= – 15.11 dB)
AR = 1 AR-filter is enabled (use programmed values)

**ETG2** Enable programmable Test Tone Generator 2
ETG2 = 0 Test Tone Generator 2 is disabled
ETG2 = 1 Test Tone generator 2 is enabled

**PTG** User programmable frequency or fixed frequency is selected
PTG = 0 fixed frequency for both Test Tone Generators
TG1 = 1008 Hz, TG2 = 2 kHz
PTG = 1 programmed frequency for both Test Tone Generators

### SCR5 Configuration Register 5

Configuration register SCR5 defines various different features.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | DHP-R | LAW | FIXC | LIN | IDR | REXTEN | ENTR | 0 |

Reset value: $20_H$

**DHP-R** Disable Receive Highpass for test reasons (see **chapter 10.3**)
DHP-R = 0 Receive Highpass Filter is enabled
DHP-R = 1 Receive Highpass Filter is disabled

**LAW** PCM - law selection
LAW = 0 A-Law is selected
LAW = 1 µ-Law (µ255 PCM) is selected

**FIXC** The SLICOFI uses either fixed coefficients or the programmed ones.
FIXC = 0 programmed coefficients used
FIXC = 1 fixed coefficients used
fixed coefficients: (see **chapter 6.2**)

**LIN** Linear mode selection (16 bit linear information in voice channel A (upper byte) and B (lower byte).
LIN = 0 PCM-mode is selected
LIN = 1 linear mode is selected

**IDR** Initialize Data RAM
IDR = 0 normal operation is selected
IDR = 1 contents of Data RAM is set to 0 (for test purposes)

**REXTEN** Ringing External
REXTEN = 0 normal operation
REXTEN = 1 used for external (unbalanced) ringing

**ENTR** Enable Test Mode Register
ENTR = 0 normal operation: the contents of the Test Registers are permanently set to the default values
ENTR = 1 the contents of the Test Registers can be changed

### SCR6 Configuration Register 6

Configuration register SCR6 defines various test features and test loops.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | COT8 | COT16 | OPIMAN | OPIM4M | TEST LOOPS | | | |

Reset value: $00_H$

**COT8** Cut Off Transmit Path at 8 kHz for test reasons (Input of Compression)
COT8 = 0 transmit path transmission is enabled
COT8 = 1 transmit path is disabled (output is zero for μ-law and linear mode, + 1 (= LSB) for A-law)

**COT16** Cut Off Transmit Path at 16 kHz for test reasons (Input of TH-Filter)
COT16 = 0 transmit path transmission is enabled
COT16 = 1 transmit path is disabled

**OPIMAN** Open analog Impedance Matching Loop (IMAN)
OPIMAN = 0 normal operation
OPIMAN = 1 opens analog IM-Loop ($H_{IMAN} = 0$)

**OPIM4M** Open fast digital Impedance Matching Loop (IM4M)
OPIM4M = 0 normal operation
OPIM4M = 1 opens fast digital IM-Loop ($H_{IM4M} = 0$)

**TEST LOOPS** 4 bit field for various analog and digital test loops can be set together with LB and TM (see **chapter 10.3**, for detailed information).

### SCR7 Configuration Register 7

Configuration register SCR7 is the Mask register. With it each bit of TCR1 (Signalling register) can be masked; that means changes of such a “masked bit” are not causing a change of the SLCX - bit (Data Upstream C/I-channel byte).

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | HOOKM | GNKM | VB/2M | ICONM | TEMPM | CFAILM | 1 | 1 |

Reset value: $FF_H$

**HOOKM** Mask bit for Offhook information
- HOOKM = 0 each change of the HOOK bit leads to an interrupt (SLCX-bit)
- HOOKM = 1 changes of HOOK bit are neglected

**GNKM** Mask bit for ground key information
- GNKM = 0 each change of the GNK bit leads to an interrupt (SLCX-bit)
- GNKM = 1 changes of GNK bit are neglected

**VB/2M** Mask bit for half battery information
- VB/2M = 0 each change of the VB/2 bit leads to an interrupt (SLCX-bit)
- VB/2M = 1 changes of VB/2 bit are neglected

**ICONM** Mask bit for constant current information
- ICONM = 0 each change of the ICON bit leads to an interrupt (SLCX-bit)
- ICONM = 1 changes of ICON bit are neglected

**TEMPM** Mask bit for over temperature information
- TEMPM = 0 each change of the TEMPA bit leads to an interrupt (SLCX-bit)
- TEMPM = 1 changes of TEMPA bit are neglected

**CFAILM** Mask bit for clock fail information
- CFAILM = 0 each change of the CFAIL bit leads to an interrupt (SLCX-bit)
- CFAILM = 1 changes of CFAIL bit are neglected

Information about changing half battery- and constant current- information will be neglected on both of the Power Denial and the Ringing state, and information about changing ground key information will be neglected in the Power Denial state.

### SCR8 Configuration Register 8

Configuration register SCR8 defines some Test Mode Settings and the Ground Key/External Indication Data Upstream Persistency Counter.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | DCANAL | CHOPACT | DCHOLD | EXT_MCLK 1 | DUPGNK3 | DUPGNK2 | DUPGNK1 | DUPGNK0 |

Reset value: $05_H$

**DCANAL** Test bit to shorten internally the IT with the $V_{2W}$ pin
DCANAL = 0 normal operation
DCANAL = 1 the DC Analog Loop is closed

**CHOPACT** Transforms DC-Test values to 500 Hz rectangular values at the PCM interface
CHOPACT = 0 normal operation
CHOPACT = 1 chopping function is activated

**DCHOLD** Holds the actual DC-value at the $V_{2W}$ output
DCHOLD = 0 normal operation
DCHOLD = 1 hold DC-value at V2W

**EXT_MCLK1** External Masterclock (16 MHz)
EXT_MCLK1 = 0 internal masterclock is used
EXT_MCLK1 = 1 external masterclock is used

To use an external masterclock of 16 MHz following steps must be done:
1. IO1 must be set to input and becomes the input-pin of the masterclock (**page 42**)
2. Connect the internal clockline to IO1 and disable the PLL by setting the bit EXT_MCLK1 = 1

**DUPGNK** To restrict the rate of upstream C/I-bit changes, deglitching (persistence checking) of the status information from the SLICOFI may be applied. New status information will be transmitted upstream, after it has been stable for N milliseconds. N is binary programmable in the range of 4 to 60 ms in steps of 4 ms, with DUPGNK = 0h the deglitching is disabled. Reset value is 20 ms.
The HOOK bit (for external Indication) and the GNK bit are influenced. Detailed info see **chapter 5.6**.

## 5.4 TOP Command

If no status modification of the SLICOFI is required (there is no TOP-write operation) a transfer operation byte TOP may be transferred.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | RW | 0 | 0 | 1 | 1 | LSEL1 | LSEL0 |

**RW** Read Information: Enables reading from the SLICOFI
RW = 0 No operation
RW = 1 Read from SLICOFI

**LSEL** Length select information (also see programming procedure, **chapter 5.2**). This field identifies the number of subsequent data bytes.
LSEL = 00 Read TCR1 (Signalling Register) only
LSEL = 01 Read 3 bytes of data (TCR1, TCR2, TCR3)
LSEL = 10 Read extended line card design and configuration information only (TCR4, ... TCR18).
Details see **chapter 10.2**
LSEL = 11 future reserved

### TCR1 Configuration Register 1

TCR1 is the Signalling register. It indicates status information. If there is any change of one or more bit, it is indicated via the SLCX bit in the C/I-channel. Each bit can be masked by SCR7 Register.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | HOOK | GNK | VB/2 | ICON | TEMPA | CFAIL | x | x |

Reset value: $00_H$

**HOOK** Loop information On/Offhook (same as in C/I-channel)
HOOK = 0 Onhook
HOOK = 1 Offhook

**GNK** Ground key or Ground start information via IL-pin (same as in C/I-channel)
interrupt masked in Power Denial State
GNK = 0 no longitudinal current detected
GNK = 1 longitudinal current detected

**VB/2** Half battery voltage across the HV-SLIC is detected ($V_{2W}$ compared to $V_{BIM}/2$)
interrupt masked in Power Denial and Ringing State
VB/2 = 0 line voltage smaller than half battery (| $V_{2W}$ | > | $V_{BIM}/2$ |)
VB/2 = 1 line voltage larger than half battery (| $V_{2W}$ | < | $V_{BIM}/2$ |)

**ICON** Current limitation information
interrupt masked in Power Denial and Ringing State
ICON = 0 Resistive Feeding
ICON = 1 Constant Current Feeding

**TEMPA** Temperature alarm of the HV-SLIC which is signalled through the HV-SLIC Interface (see **chapter 7**).
TEMPA = 0 normal temperature
TEMPA = 1 Temperature alarm from HV-SLIC detected

**CFAIL** Clock Fail: Not the right count of clock cycles between two frame syncs
CFAIL = 0 no clock fails detected
CFAIL = 1 clock fails detected
The CFAIL bit is not influenced by the DUP-counter (each failure is reported).

**x** undefined

Any change of these bits is signalled via the interrupt-bit (SLCX) in the C/I-DU-channel. There are two types of generating an interrupt:

– Each toggling of a non-masked TCR1-bit combined with a DUP-counter
– Toggling of the non-masked CFAIL-bit (no filtering by the DUP-counter)

The status information is stored in the TCR1-register by an interrupt or - if there is no interrupt - before reading this register only.

The HOOK- and the GNK-input are directly filtered by an own DUP-/DUPGNK-counter too and they are also directly included in the C/I-DU-channel.

Reading the TCR1-register is possible in two ways:

– Reading only TCR1 (TOP-command with LSEL = 0b)
– Reading TCR1 with other TCR-registers (TOP-command with LSEL = 0b)

The first way gives the actual status of all TCR1-inputs if the internal interrupt is not active and actualizes the TCR1-register.

Is the interrupt active the content of TCR1-register is read and the interrupt is cleared.

The second way gives the content of TCR1-register and nothing will be changed.

The following figure shows the flow diagram of the interrupt logic.

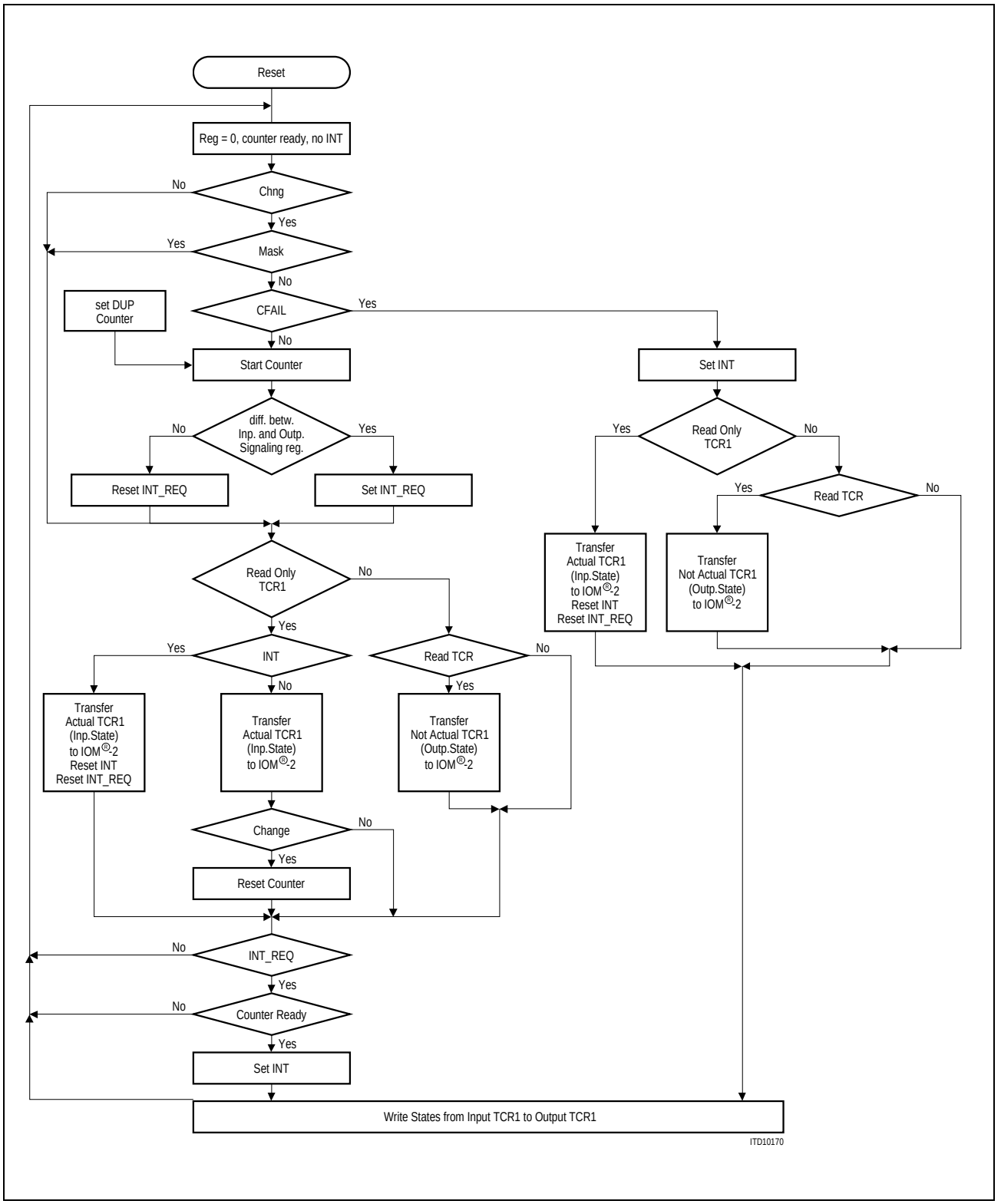



**Figure 8 Flow Diagram of the Interrupt Logic**

### TCR2 and TCR3 Configuration Registers 2 and 3

TCR2 and TCR3 are the checksum of all the Coefficient bytes written into the Coefficient RAM (CRAM) of the SLICOFI by the COP-Command.

**TCR2**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | LOW Byte of CRAM-checksum | | | | | | | |

**TCR3**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | OKCS | HIGH Byte of CRAM-checksum | | | | | | |

**OKCS** shows, if the checksum is valid or the internal checksum calculation is not yet finished [1)]

OKCS = 0 checksum is not valid
OKCS = 1 checksum is valid

Algorithm of defining the checksum: $x^{16}\ x^{10}\ x^{7}\ x\ 1$

With that algorithm you can reach a fault coverage of: $(1 - 2^{-15})$

1) After each change of the CRAM contents (COP-write or COP-read) the checksum has to be recalculated. During calculation time OKCS = 0.

### TCR4 to TCR18: Configuration Register 4 to 18

These 15 bytes are the possible design information bytes which are described in **chapter 10.2** more detailed for the extended I0M-2 Channel Identification Command using an external ASIC.

**TCR4**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | Byte 0 | | | | | | | |

**TCR5**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | Byte 1 | | | | | | | |

**TCR18**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | Byte 14 | | | | | | | |

TCR4 - TCR18 show the contents of the serial input of the ASIC via IDH-pin.

## 5.5 COP Command

With a COP Command coefficients for the programmable filters can be written to the SLICOFI Coefficient RAM or read from the Coefficient RAM via the IOM-2 interface for verification. (Filter optimizing to different applications is supported by the software package SLICOS.)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | RW | CODE 4 | CODE 3 | CODE 2 | 0 | CODE 1 | CODE 0 |

**RW** Read / Write
RW = 0 Subsequent data is written to the SLICOFI
RW = 1 Read data from the SLICOFI

**CODE** includes number of following bytes and filter-addresses[1)]

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | TH-Filter coefficients (part 1) | (followed by 8 bytes of data) |
| 0 | 0 | 0 | 0 | 0 | 1 | TH-Filter coefficients (part 2) | (followed by 8 bytes of data) |
| 0 | 0 | 0 | 0 | 1 | 0 | TH-Filter coefficients (part 3) | (followed by 8 bytes of data) |
| 0 | 0 | 0 | 0 | 1 | 1 | IM-Filter coefficients (part 1) | (followed by 8 bytes of data) |
| 0 | 0 | 1 | 0 | 0 | 0 | IM-Filter coefficients (part 2) | (followed by 8 bytes of data) |
| 0 | 0 | 1 | 0 | 0 | 1 | FRX-Filter coefficients | (followed by 8 bytes of data) |
| 0 | 0 | 1 | 0 | 1 | 0 | FRR-Filter coefficients | (followed by 8 bytes of data) |
| 0 | 0 | 1 | 0 | 1 | 1 | DC-Loop coefficient (part 1) | (followed by 8 bytes of data) |
| 0 | 1 | 0 | 0 | 0 | 0 | DC-Loop coefficient (part 2) | (followed by 8 bytes of data) |
| 0 | 1 | 0 | 0 | 0 | 1 | DC-Loop coefficient (part 3) | (followed by 8 bytes of data) |
| 0 | 1 | 0 | 0 | 1 | 0 | TTX and DC-Loop coefficient | (followed by 8 bytes of data) |
| 0 | 1 | 0 | 0 | 1 | 1 | AX-Filter coefficients | (followed by 8 bytes of data) |
| 0 | 1 | 1 | 0 | 0 | 0 | AR-Filter coefficients | (followed by 8 bytes of data) |
| 0 | 1 | 1 | 0 | 0 | 1 | TG1-Filter+BP1+LM-BP coefficients | (followed by 8 bytes of data) |
| 0 | 1 | 1 | 0 | 1 | 0 | TG2-Filter+BP2 coefficients | (followed by 8 bytes of data) |
| 0 | 1 | 1 | 0 | 1 | 1 | Testing (levelmeter) coefficients | (followed by 8 bytes of data) |

[1)] For generating a correct checksum all not used bits must be set to ‘0’.

## 5.6 IOM®-2 Interface Command / Indication Byte

The Command/Indication (C/I) channel is used to communicate real time status information and for fast controlling of the SLICOFI. Data on the C/I channel is continuously transmitted in each frame until new data is to be sent.

### Data Downstream C/I - Channel Byte (receive) - CIDD

Note that there is no address DD direction because there is only one SLICOFI per IOM2-channel. This byte is used for fast controlling of the SLICOFI. Each transfer to the SLICOFI has to last for at least 2 consecutive frames (FSC-cycles) so that it is accepted internally. Changes (spikes) of less than 2 FSC cycles are neglected.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 |
|---|---|---|---|---|---|---|
| | RING | CONV | TIM | IO1 | IO2 | O1 |

**RING** see table below (for details see **chapter 6**).

**CONV** see table below (for details see **chapter 6**).

**Table 8**

| RING | CONV | Description |
|---|---|---|
| 0 | 0 | Power Denial or Power Down State (depending on PD-bit (SCR1-7) |
| 0 | 1 | Active State |
| 1 | 0 | Power Down or (automatic) Power Down Ring Pause |
| 1 | 1 | (normal) Ringing State |

**TIM** Timing bit to control the timing of ringing or meterpulses (for details see **chapter 6**).

TIM = 0 SLICOFI is in the ringing pause or no meterpulse is on.

TIM = 1 SLICOFI is in the ringing phase or output of a meterpulse is running.

**IO1** Value for the programmable Input/Output Pin IO1 (Pin 7) if programmed as an output pin. If the bit REXTEN (SCR5-2) is set to 1 (external ringing) the internally created Ring Burst On Signal (for an external relay driver) is switched to the IO1 pin instead of the IO1-bit (for more details see **chapter 6** , **page 51**).

IO1 = 0 The corresponding pin at the digital interface of the SLICOFI is set to a logic 0.

IO1 = 1 The corresponding pin at the digital interface of the SLICOFI is set to a logic 1.

**IO2** Value for the programmable Input/Output Pin IO2 (Pin 8) if programmed as an output pin.

IO2 = 0 The corresponding pin at the digital interface of the SLICOFI is set to a logic 0.

IO2 = 1 The corresponding pin at the digital interface of the SLICOFI is set to a logic 1.

**O1** Value for the fixed Output Pin O1 (Pin 39).

O1 = 0 The corresponding pin at the digital interface of the SLICOFI is set to a logic 0.

O1 = 1 The corresponding pin at the digital interface of the SLICOFI is set to a logic 1.

### Data Upstream C/I - Channel Byte (transmit) - CIDU

Note that there is no address in DU direction too. This byte is used for fast transfer of the most important and time critical informations from the SLICOFI.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 |
|---|---|---|---|---|---|---|
| | HOOK | GNK | SLCX | IO1 | IO2 | I1 |

**HOOK** Indication of the loop condition (filtered via the DUP-counter or the DUPGNK-counter in Power Denial State).

HOOK = 0 Subscriber is Onhook.

HOOK = 1 Subscriber is Offhook.

**GNK** Indication if a ground connection is detected (filtered via the DUPGNK-counter). The function is disabled in Power Denial State (GNK is set to 0).

GNK = 0 No ground connection detected.

GNK = 1 Ground connection detected.

**SLCX** Interrupt bit: Summary output of the whole signalling register (TCR1) if they are not masked - filtered via the DUP counter (see SCR7; the interrupt logic is described in detail in **chapter 5.4**, **page 36**).

SLCX = 0 No unmasked bit in the signalling register has toggled.

SLCX = 1 Any unmasked bit in the signalling register has toggled.

**IO1** Logical state of the programmable Input/Output Pin IO1 (Pin 7) - even if not programmed as an input pin.[1)]

IO1 = 0 The corresponding pin at the digital interface of the SLICOFI is receiving a logic 0.

IO1 = 1 The corresponding pin at the digital interface of the SLICOFI is receiving a logic 1.

**IO2** Logical state of the programmable Input/Output Pin IO2 (Pin 8) - even if not programmed as an input pin.[1)]

- IO2 = 0 The corresponding pin at the digital interface of the SLICOFI is receiving a logic 0.
- IO2 = 1 The corresponding pin at the digital interface of the SLICOFI is receiving a logic 1.

**I1** Logical state of the programmable Input Pin I1 (Pin 38).

- I1 = 0 The corresponding pin at the digital interface of the SLICOFI is receiving a logic 0.
- I1 = 1 The corresponding pin at the digital interface of the SLICOFI is receiving a logic 1.

The DUP- (DUPGNK) - counters filter the status-information and the input-pin I1 respectively. The counters count down and generate enable-signals for the registers if they are zero. Then they start counting again at the programmed value. If a status-information or an input-signal changes the proper counter is set and continues counting down. There are three different DUP-counters for HOOK, SLCX and the input-pin and one DUPGNK-counter for HOOK in PDen-mode or GNK in all other modes. Changing the mode freezes the actual status of HOOK and sets the actual HOOK-counter.

1) If the Input/Output Pin is programmed as an output the corresponding bit in the CIDU is '1'

## 6 Operating Modes

The SLICOFI supports 4 different Operating Modes: Power Denial (PDen), Power Down (PDown), Active and Ringing which are controlled via the upper 3 bits of the Data Downstream C/I channel byte (CIDD).

**Table 9**

| RiING-(CIDD7) | CONV-(CIDD6) | TIM-(CIDD5) | Mode |
|---|---|---|---|
| 0 | 0 | x | PDen: PD (SCR1-7) = 0 |
| 0 | 0 | x | PDown: PD (SCR1-7) = 1 |
| 1 | 0 | 0 | PDown (Ring Pause) |
| 0 | 1 | 0 | Active |
| 0 | 1 | 1 | Active with Meterpulse on |
| 1 | x | 1 | Ringing: Ring Burst On |
| 1 | 1 | 0 | Ringing: Ring Pause |

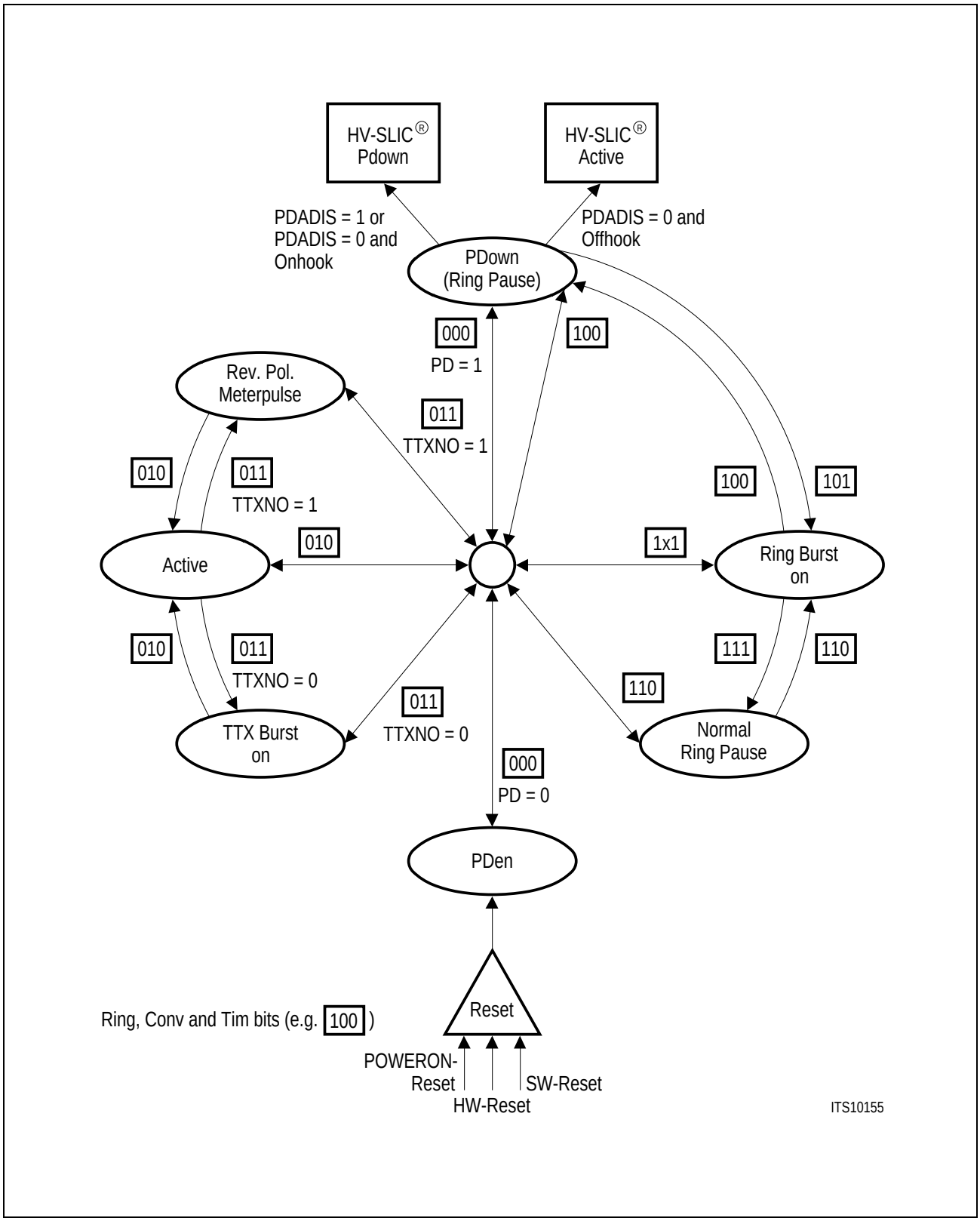

HV-SLIC® Pdown
HV-SLIC® Active
PDADIS = 1 or PDADIS = 0 and Onhook
PDADIS = 0 and Offhook
PDown (Ring Pause)
000
PD = 1
100
Rev. Pol. Meterpulse
011
TTXNO = 1
010
011
TTXNO = 1
100
101
Active
010
1x1
Ring Burst on
010
011
TTXNO = 0
111
110
110
011
TTXNO = 0
TTX Burst on
Normal Ring Pause
000
PD = 0
PDen
Reset
Ring, Conv and Tim bits (e.g. 100 )
POWERON-Reset
SW-Reset
HW-Reset
ITS10155

**Figure 9**

## 6.1 Reset Behavior

The SLICOFI has 3 different reset sources that are all internally connected.

**The Reset pin RES** (pin 36), which works totally asynchronous to the external clocks.

**The Reset bit** (Within SOP - command, bit 4). The reset is valid for SOP-write only.

**Power On Reset.** If internal $V_{DDD}$ gets above 1.5 Volts the SLICOFI is Reset by Power On Reset.

All 3 different sources set the SLICOFI to the basic setting modes (see below).

After a reset caused by any of the sources mentioned above, the reset bit (SCR0-4 = RSTST) in read direction is set to one. This bit is cleared (RSTST = 0) after it has been read by a SOP-read operation with the LSEL bits set to 00b (means: read only SCR0 byte). A SOP-read with other LSEL bits reads the actual RSTST value, but does not clear it.

The Reset pin RES has a Schmitt-Trigger input to reduce the sensitivity for spikes. In addition the pin RES has a spike rejection. All spikes smaller than typ. 70 ns are neglected. The pin RES can be set to 1 for an unlimited time but at least 125 µs is recommended; during that, the DU pin is set to high impedance.

The SLICOFI leaves this mode automatically with the beginning of the next 8 kHz-frame (or after pin RES is released).

## 6.2 Basic Setting Modes

After RESET, the SLICOFI automatically is switched to its basic settings in which it uses internal default values for all filters and settings (AC and DC), so that the SLMA still works in a kind of “emergency mode” and can be handled by C/I-Interface commands only.

This means that for an (un-)determined reset (e.g. Power On Reset) the SLICOFI is reset, but can be switched to or return automatically to any operating mode presented to the C/I-channel after 2 FSC cycles. In all modes the SLMA stays stable, supervision and DC-feeding are still working and conversation can go on in a proper way until all filters and settings have been reloaded by SOP and COP-commands.

So what happens internally after reset?

– all configuration registers are set to their default values (note that the Coefficient RAM is **not** reset)
– the RSTST-bit (SCR0-4) is set to 1 to indicate that a reset has taken place
– The IOM-2 interface is reset. Running communication is stopped
– DU is in high impedance state
– AC- and DC-loop use the default values and not the programmed ones (see below)

**Table 10 DC**

| Parameter | Values | Unit | Test Condition/Result |
|---|---|---|---|
| Const I | 26 | mA | limit for Constant Current (for Active and Power Down) |
| RFS | $2 \times 150$ | | Feeding Resistance (for Active and Power Down - excluding the external Fuse resistors) |
| $V_{drop}$ | 10 | V | Overall voltage drop (to reach maximum length and there is no Teletax) |
| $f_{Ring}$ | 25 | Hz | Ring Frequency |
| ARing | 1.7 | V | Ring rms-value at $V_{2W}$ |
| PDen | 1.45 | Vrms | Power Denial Voltage for Offhook |
| Offhook | 8 | mA | Offhook Detection (for Power Down, Ringing and Active without hysteresis) |
| DC-Lowpass | 0.3/5 | Hz | DC- Lowpass set to 0.3 and 5 Hz respectively |
| Levelmeter | | | undefined (parameters stored in CRAM) |
| DUP | 10 | ms | Data Upstream Persistency Counter is set to 10 ms |
| DUPGNK | 20 | ms | Data Upstream Persistency Counter for GNK is set to 20 ms |

Boosted Battery is reset to normal feeding

Reverse Polarity is reset to Normal Polarity

all bits of the Signalling Register are masked and reset to 0

the Data Upstream C/I channel byte is reset to 0 (and IO's are set to Input pins)

C1 and C2 are set to PDNR and PDN is set high

A-Law is chosen

**Table 11 AC**

| Parameter | Values | Unit | Test Condition/Result |
|---|---|---|---|
| IM-Filter | 900 | | Approximately 900 Real Input Impedance |
| TH-Filter | $TH_{BRD}$ | | Approximately BRD-Impedance for Balanced Network |
| AX | 10 | dB | Attenuation Transmit (this means about 0 dB for SLMA) |
| AR | – 15.11 | dB | Attenuation Receive (this means about – 7 dB for SLMA) |
| ATTX | 190 | mV | Teletax Generator Amplitude at $V_{2W}$; but note that the SLICOFI is set to TTXNO = 1 with reset |

**Table 11 AC** (cont'd)

| Parameter | Values | Unit | Test Condition/Result |
|---|---|---|---|
| $f_{TTX}$ SOREV | 16 | kHz | Teletax Generator frequency; but note that the SLICOFI is set to TTXNO = 1 with reset for Metering with Polarity Reversal: Hard Reversal is used. |
| TG1 | 1008 | Hz | Tone Generator 1 and AC-levelmeter Bandpass |
| TG2 | 2000 | Hz | Tone Generator 2 (+ 2 dB compared to TG1) |

### 6.3 Power Denial (PDen)

After a Reset (including the Power On Reset) the SLICOFI is set to Power Denial State. In Power Denial all functions that are not necessary are disabled to minimize power consumption. Via the two pins $V_{LINE1}$ and $V_{LINE2}$ the SLICOFI is directly connected to the a - and b - wire, while the PDN-Pin is set high (which turns off the HV-SLIC). While the interface is fully working - including programmability of the registers with SOP- or TOP commands and the Coefficient RAM (COP commands) the rest of the SLICOFI is turned off except the supervision of the line. The change of the line state is reported via the HOOK-bit in the IOM-2 Data upstream channel. To avoid spurious Offhook - informations caused by longitudinal induction the HOOK - bit is low pass filtered (programmable with the DUPGNK - counter in PDen state only). The HV-interface pins C1, C2 are switched off. The voice channel Data Downstream is directly fed into the voice channel Data Upstream. The HOOK-indication in PDen is optimized for longitudinal suppression up to 65 Vrms for the Offhook transition.

### 6.4 Power Down (PDown)

In Power Down Mode the DC-Loop of the SLICOFI is fully working; the AC-Loop is still turned off. The output voltage at the V2W pin is controlled via the IT input in such a way that it behaves like a programmable constant current source. Current limitation is used for detecting Offhook, too. The change of the line state is reported via the HOOK-bit in the IOM-2 Data upstream channel. To avoid spurious Offhook-informations the HOOK-bit is lowpass filtered (programmable with DUP-counter).

The ternary HV-interface (C1, C2) is set to Power Down mode. If Offhook is detected the HV-interface is set to one of the active modes. This can be avoided by setting PDADIS = 1 (SCR3-4). Then the HV-SLIC interface is set to Power Down anyway.

The longitudinal current supervision via the IL pin is activated in this mode.

The voice channel Data Downstream is directly fed into the voice channel Data Upstream.

Together with the bits Hi-a and Hi-b of the configuration register 1 (SCR1-2 and SCR1-3) simple handling of Ground Start function is possible.

**Table 12**

| | Pin No./Pin Name | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | **CIDD7** | **CIDD6** | **CIDD5** | **SCR1-7** | **SCR1-3** | **SCRI1-2** | **PIN 28** | **PIN 9** | **PIN 10** |
| | **RING** | **CONV** | **TIM** | **PD** | **HI-b** | **HI-a** | **PDN** | **C1** | **C2** |
| PDNH - Loop open (Iab < 30 µA) | 0 | 0 | 1 | x | x | x | 1 | $V_{OL}$ | $V_{OL}$ |
| PDNR | 0 | 0 | 0 | 0 | not (11) | | 1 | $V_{OZ}$ | $V_{OZ}$ |
| PDown | 0 | 0 | 0 | 1 | 0 | 0 | 0 | $V_{OH}$ | $V_{OH}$ |
| PDown (with Hi-a) | 0 | 0 | 0 | 1 | 0 | 1 | 0 | $V_{OL}$ | $V_{OH}$ |
| PDown (with Hi-b) | 0 | 0 | 0 | 1 | 1 | 0 | 0 | $V_{OZ}$ | $V_{OH}$ |
| b-line high impedance (Ground Start) | 0 | 0 | 0 | x | 1 | 1 | 0 | $V_{OZ}$ | $V_{OH}$ |

## 6.5 Active Mode (Act)

In Active Mode (“Conversation State”) both AC-and DC-Loop are fully working. The output voltage at the $V_{2W}$ pin is controlled via the IT input pin in such way, that it behaves like a constant current source which turns automatically into a programmable resistive feeding source due to the DC-Characteristic values (see **chapter 3.2**, **page 13** for more details).

The ternary HV-interface is set to one of the active modes.

### Polarity

The SLICOFI supports either normal or reverse Polarity which is set by the POLNR-bit (SOP-5). The information is transferred to the HV-Interface and simultaneously a 180 degree phase shift of the AC- and DC-Loop is done. The performance and the functionality is not influenced by that.

### Boosted Battery

To feed subscriber lines with enhanced loop resistance the SLICOFI supports the Boosted Battery mode. The HV-Interface pins are set to Boosted Battery (BB) mode and the maximum $V_{2W}$ output voltage is extended to – 3.2 V.

### Meterpulses

The SLICOFI supports two different kinds of meterpulses: Meterpulses with 12/16 kHz (Teletax Metering) and with polarity reversal. In the Active Mode the Timing bit (TIM) controls the meterpulse which might be 12/16 kHz **or** reversal. The decision between

these two ways is made by the bit TTXNO (SCR3-7). If bit TTXNO is set to 1, then the meterpulse is reversal. In this case the Timing bit is linked to POLNR (SOP-5) by an EXOR gate. If bit TTXNO is set to 0, then the Timing bit and POLNR are completely independent from another and Teletax Metering is used.

**Metering with Polarity Reversal**

Hard or Soft (SOREV, SCR 3-5)

As long as the TIM bit of the C/I-channel is set to 1, the SLICOFI is changing the actual polarity of the HV-Interface and performs an immediate 180 degree phase shift of the AC- and DC-Loop.

**Teletax Metering Injection**

For countries with Teletax Metering, the SLICOFI provides either a 12 or 16 kHz Signal (switchable with the bit TTX12 (SCR3-6))[1] which amplitude is free programmable up to 250 mVrms at $V_{2W}$. The SLICOFI filters the Teletax pulses in transmit direction, too. The slope of the pulses are internally shaped, so that the noise during switching and transmission is less than 50 mV at $V_{2W}$ and 1 mV at the IOM-2 interface (psophometrically weighted). With the bit NOSL (SCR2-2) the slope can be switched off. In that case the switching noise is not defined (for signalling only).

## 6.6 Ringing Mode

The SLICOFI generally supports balanced ringing.

If the SLICOFI is set to Ringing Mode, the HV-Interface is set to Ringing Mode, the AC-loop is turned off and the DC-Loop is automatically opened.

The voice channel Data Downstream is directly fed into the voice channel Data Upstream.

**Balanced Ringing**

The sine wave of the ringing is generated in the SLICOFI. The frequency and the amplitude are free programmable between 16 and 70 Hz and up to 2.125 Vrms at $V_{2W}$, respectively[2]. In Ring Pause 0 V is provided at $V_{2W}$. If the Ring Burst On (RBO) command is sent to the SLICOFI via the C/I-channel (RING and TIM = 1) the begin and end (TIM = 0) of the ring burst is automatically synchronized at the voltage zero crossing. If the DC-current at the IT-pin exceeds the programmed value, Offhook is detected within 2 periods of the ringing frequency and the Ring Burst at $V_{2W}$ is switched off within 3 periods. During Offhook the Ring Burst On command is neglected.

1) Note, that the right Teletax Coefficient Set (via COP-command) must be provided, too.
2) Note that the DC-value is 0. So DC injection has to be performed by the HV-SLIC.

### Unbalanced (external) Ringing

The sine wave for ringing is generated by an external ring generator. To coordinate with the SLICOFI following settings must be done:

1. IO1 set as an output
2. SCR5-2 (REXTEN) = 1
3. RING-(CIDD7) = 1 (PDown: Ring Pause)
4. TIM-(CIDD5) = 1 (Ringing: Ring Burst On)

Pin REXT: a positive puls according to zerocrossing of the ringer voltage

RINGING:

5. signal for relays on IO1
6. HV-SLIC in PDen Mode
7. SLICOFI in PDown Mode, Offhook-detection via $V_{LINE1,2}$

RING PAUSE:

8. TIM-(CIDD5) = 0 (PDown: Ring Pause), Offhook-detection via IT (in the same way as balanced ringing)

# 7 SLIC Interface

### 2 Wire Output Voltage ($V_{2W}$)

The $V_{2W}$ output voltage pin (26) represents the sum for AC- and DC-loop together with Teletax info or Ring Burst at the receive path. The buffer is designed for a load of $R_L$ > 600 and $C_L$ < 10 pF and directly connected to the HV-SLIC in typical applications.

### Transversal Current Sense AC - Input (ITAC)

The pin ITAC (21) is the input voltage pin for the AC transversal current information from the HV-SLIC in the transmit path. AC/DC separation is done by an external highpass filter (capacitor range between 680 nF - 1 µF). The input resistance is larger than 20 k. Current/voltage conversion is done via an external resistor (same for pin IT).

### Transversal Current Sense DC - Input (IT)

The pin IT (19) is the input voltage pin for the DC transversal current information from the HV-SLIC in the transmit path. The signal is internally filtered via a 0.3 Hz lowpass. The input resistance is larger than 20 k. Current/voltage conversion is done via an external resistor (same for pin ITAC).

### Longitudinal Current Sense - Input (IL)

The scaled longitudinal current information transferred from the HV-SLIC – the current-voltage conversion is done by an external resistor – is lowpass filtered (time programmable using DUPGNK-counter) and is reported via the Data Upstream C/I-channel (CIDU-6). In Power Denial, the GNK-bit is set to ‘0’ and the setting of the Interrupt bit (CIDU-5) caused by GNK is prohibited. Changing from PDen to any other mode, the DUPGNK-counter is set to the programmed value; so the change of the GNK information (CIDU-6) is lowpass filtered anyway.

### Battery Image Input ($V_{BIM}$)

The information about the actually used battery voltage ($V_{BAT}$) of the SLMA is transferred from the HV-SLIC via the $V_{BIM}$ pin to the SLICOFI· In order to give some information about the operating point of the SLMA there is a comparison of the actual battery voltage and the output voltage $V_{2W}$ of the SLICOFI· This information is transferred via the Signalling register (TCR1-5: VB/2).

If | $V_{2W}$ | < | $V_{BIM}$ / 2 | the VB/2-bit is set to 1, else to 0.

### Ternary Interface (C1, C2) and HV-SLIC Switch Off Output (PDN)

In order to set the HV-SLIC to the different operating states, the information of the SLMA-controller is passed through from the IOM-2-channel to the ternary HV-SLIC-Interface pins C1 and C2.

**Table 13**

| | | C2 (PIN 10) | | |
|---|---|---|---|---|
| | | **VOL** | **VOZ** | **VOH** |
| **C1 (PIN 9)** | **VOL** | RING RP/PDNH | RING NP | HI-a |
| | **VOZ** | BB RP | BB NP/PDNR | HI-b |
| | **VOH** | Active RP | Active NP | PDown |

BB - Boosted battery

RP - Reverse Polarity

NP - Normal Polarity

HI-b - High Impedance b-leg

HI-a - High Impedance a-leg

PDNH - Power Denial High Impedance

PDNR - Power Denial Resistive

For signalling “Over temperature” the HV-SLIC drains a current ($I_{OT}$) from pin 9. The message is transferred via the Signalling register (TCR1-3). This is possible in any operating states of the HV-Interface except for Power Denial.

The HV-SLIC (PEB 4065) has two different Power Denial Modes:

1. PDNR, the resistive mode which provides a connection of 15 kΩ from TIP and RING to BGND and $V_{BAT}$, respectively
2. PDNH, offers high impedance at TIP and RING

In this mode (PDN = 1) the HV-SLIC is completely turned off. Line supervision is done via the $V_{LINE1,2}$ pins. In all other modes, PDN is set to GND ($R_{ON}$ < 250 Ω).

### Line Sense Pins ($V_{LINE1,2}$)

In Power Denial state the line supervision is done via the $V_{LINE1,2}$ pins. If the voltage $V_{LINE}$ between the two pins exceeds the programmed value, Offhook is reported via the Data Upstream C/I-channel (CIDU-7)[1)]. To reach the longitudinal voltage suppression, the incoming signal is low pass filtered using the values that are programmed by the DUPGNK counter (no longitudinal current information present in PDen, but the same interferences).

1) Note: $V_{LINE} = V_{LINE1} - V_{LINE2}$; so the voltage of $V_{LINE1}$ has to be higher than $V_{LINE2}$ for correct external indication

## 8 Transmission Characteristics

The target figures in this specification are based on the subscriber-line board requirements. The proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) needs a complete knowledge of the SLICOFI's analog environment. Unless otherwise stated, the transmission characteristics are guaranteed within the test conditions.

### Test Conditions

$T_A$ = 0 °C to 70 °C;

$V_{DDD} = V_{DDA}$ = 5 V ± 5%; $V_{SS}$ = – 5 V ± 5%; GNDA = GNDD = 0 V
$R_L$ > 600 Ω; $C_L$ < 10 pF (at $V_{2W}$); $H_{IM} = H_{TH} = 0$; $H_{FRX} = H_{FRR} = 1$
AR = 0 dB
AX = 0 dB
$f$ = 1004 Hz; 0 dBm0; A-Law or µ-Law;

In Transmit direction for µ-law an additional gain of 1.94 dB is implemented.

The 0 dBm0 definitions for Receive and Transmit are different.

A 0 dBm0 signal in Transmit direction is equivalent to 206 mVrms [165 mVrms].

(A -Law, [µ-Law]).

A 0 dBm0 signal in Receive direction is equivalent to 118 mVrms.

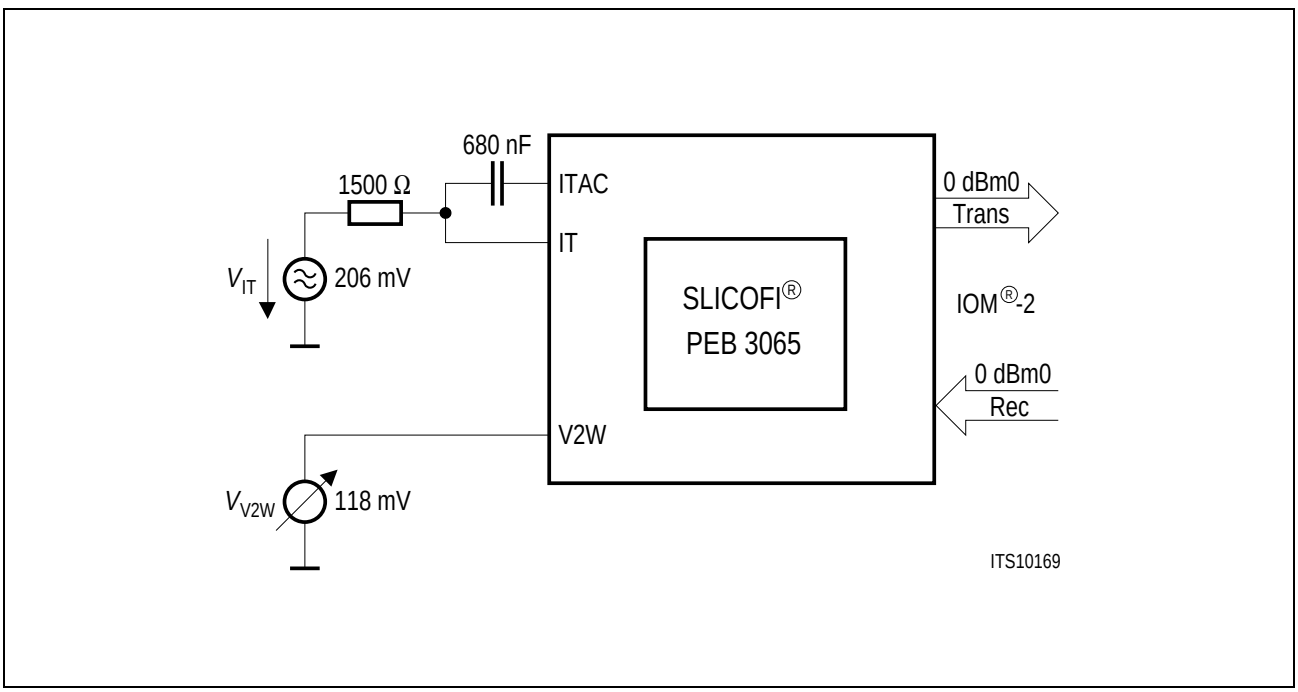



**Figure 10**

With $V_{IT}$ = 0 dBm0|$_{SLICOFI}$ = – 11.51 dBm0|$_{600}$ = 206 mV for transmit
With $V_{V2W}$ = 0 dBm0|$_{SLICOFI}$ = – 16.34 dBm0|$_{600}$ = 118 mV for receive

**Table 14**

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Gain absolute | | | | | | |
| transmit | $G_X$ | – 0.20 | ± 0.05 | 0.20 | dB | |
| receive | $G_R$ | – 0.20 | ± 0.05 | 0.20 | dB | |
| IMAN-Loop | $G_{IMAN}$ | – 0.5 | ± 0.1 | 0.5 | dB | adding to – 7.2 dB Loop gain |
| TTX-injection | $G_{TTX}$ | – 0.7 | ± 0.3 | 0.7 | dB | |
| Total Harmonic distortion | | | | | | |
| transmit | $THD_T$ | | – 56 | – 48 | dB | at 0 dBm0; $f$ = 1 kHz; 2nd, 3rd order |
| receive | $THD_R$ | | – 56 | – 48 | dB | at 0 dBm0; $f$ = 1 kHz; 2nd, 3rd order |
| Ringing injection | $THD_{Rng}$ | | – 35 | – 34 | dB | $f$ = 16.3-70 Hz |
| TTX injection | $THD_{TTX}$ | | – 60 | – 40 | dB | $f$ = 12 kHz and 16 kHz |
| Idle channel noise | | | | | | |
| transmit | $N_{TP}$ | | – 69 | – 67 | dBm0p | Teletax countries, burst off A-law, psophometric: $V_{IN}$ = 0 V |
| | $N_{TTX\_TP}$ | | – 65 | – 60 | dBm0p | Teletax burst on A-law, psophometric: $V_{IN}$ = 0 V |
| | $N_{G\_TP}$ | | – 58 | – 53 | dBm0p | AX = 30 dB Teletax countries, burst off A-law, psophometric: $V_{IN}$ = 0 V |
| receive | $N_{RP}$ | | – 88 | – 81 | dBm0p | Teletax countries, burst off A-law, psophometric idle code +0 |
| | $N_{TTX\_RP}$ | | – 87 | – 80 | dBm0p | Teletax burst on A-law, psophometric idle code +0 |

## 8.1 Frequency Response

**Receive:** reference frequency 1 kHz, signal level 0 dBm0, $H_{FRR}$ = 1

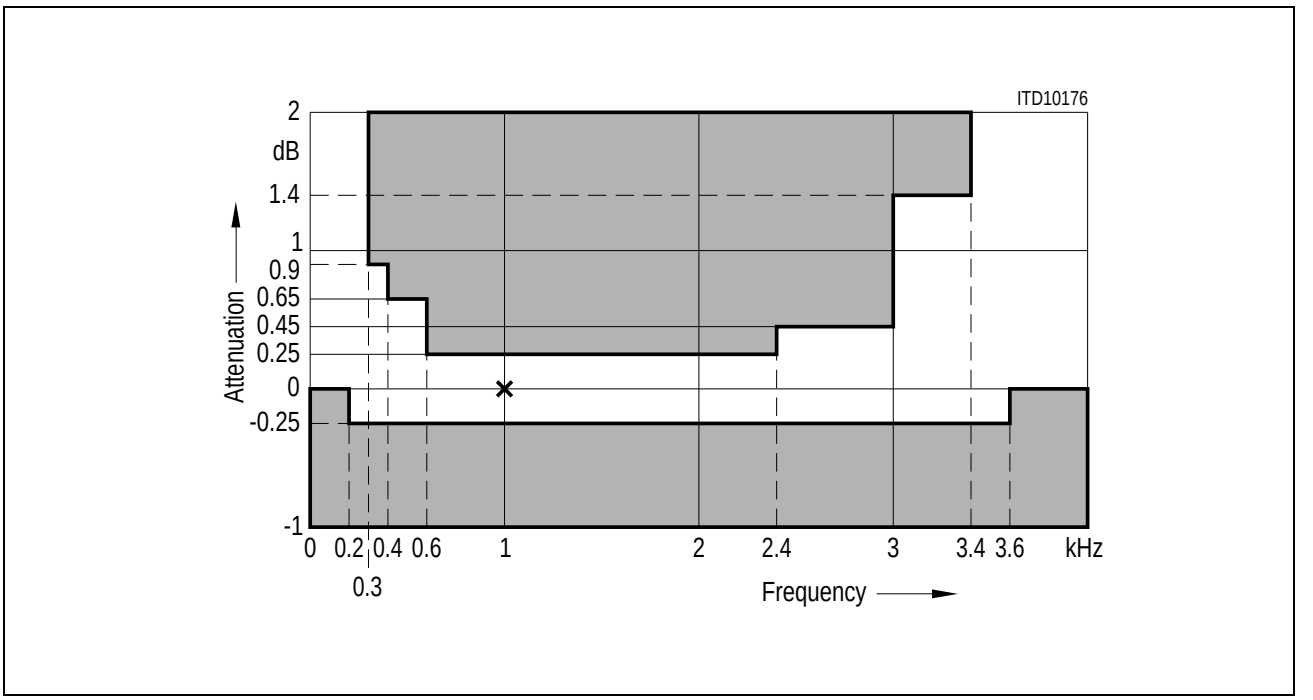



**Figure 11**

**Transmit:** reference frequency 1 kHz, signal level 0 dBm0, $H_{FRX}$ = 1

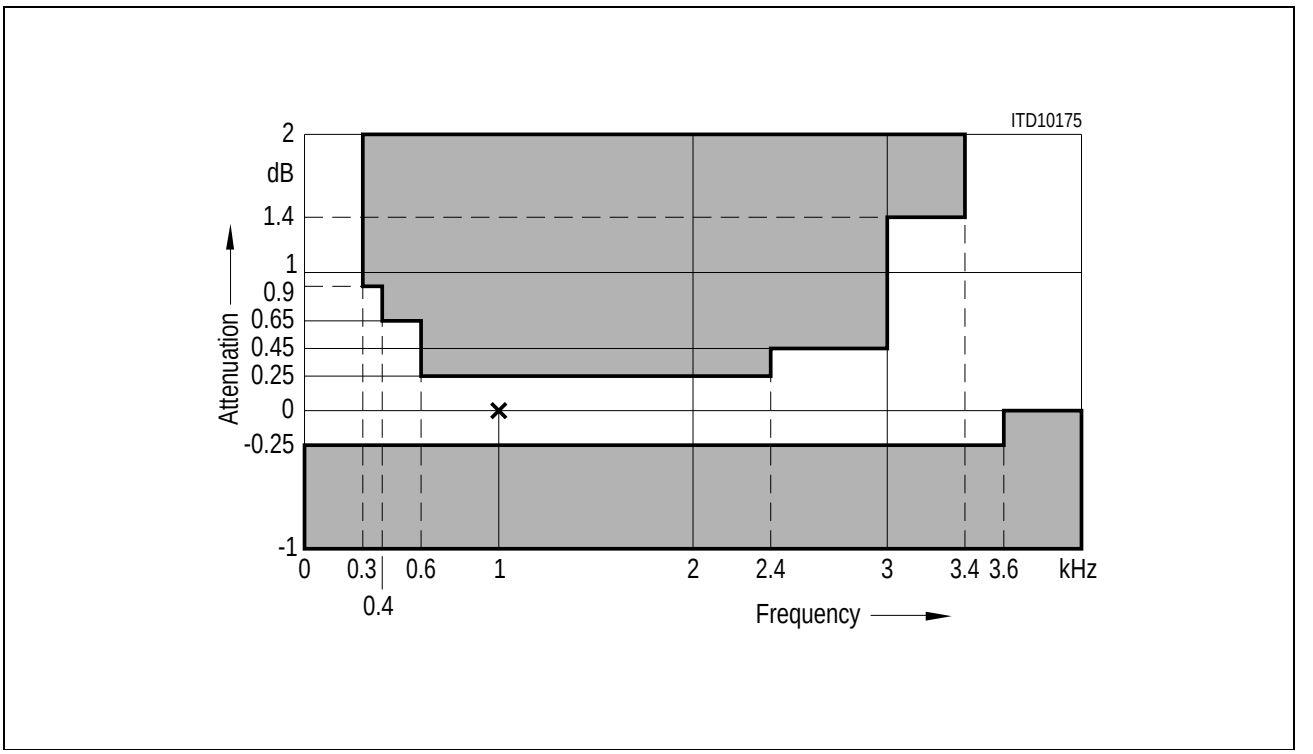



**Figure 12**

## 8.2 Group Delay

Maximum delays when the SLICOFI is operating with $H_{TH} = H_{IM} = 0$ and $H_{FRR} = H_{FRX} = 1$ including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

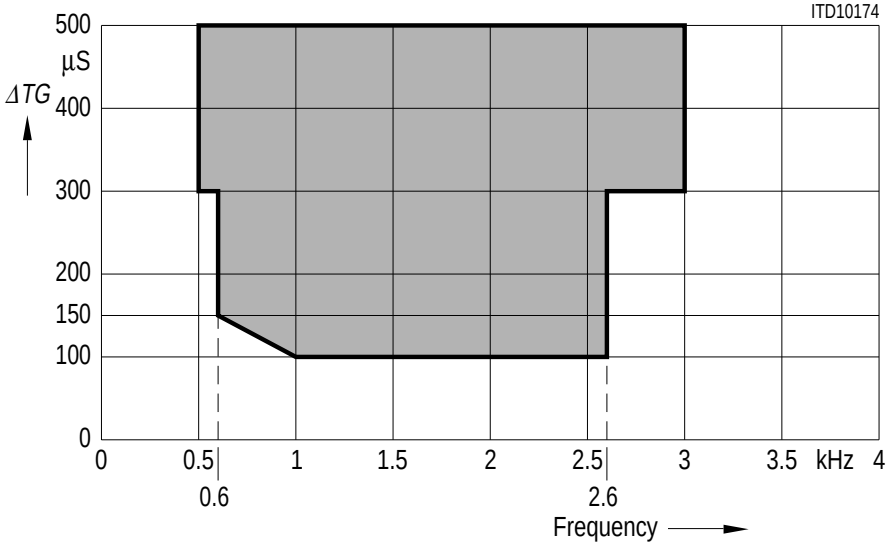
Group Delay deviations stay within the limits in the figures below.

**Group Delay absolute values:** Signal level 0 dBm0

**Table 15**

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Transmit delay | $D_{XA}$ | 250 | 312 | 375 | µs | $f_{Test}$ @ $T_{Gmin}$ |
| Receive delay | $D_{RA}$ | 250 | 312 | 375 | µs | $f_{Test}$ @ $T_{Gmin}$ |
| Digital loop back | $D_{RX}$ | | | 630 | µs | $f_{Test}$ @ $T_{Gmin}$ |

**Group Delay Distortion receive and transmit:** Signal level 0 dBm0, $f_{Test}$ @ $T_{Gmin}$



## 8.3 Out-of-Band Signals at Analog Output (receive)

With a 0 dBm0 sine wave with frequency *f* (300 Hz to 3.4 kHz) applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output

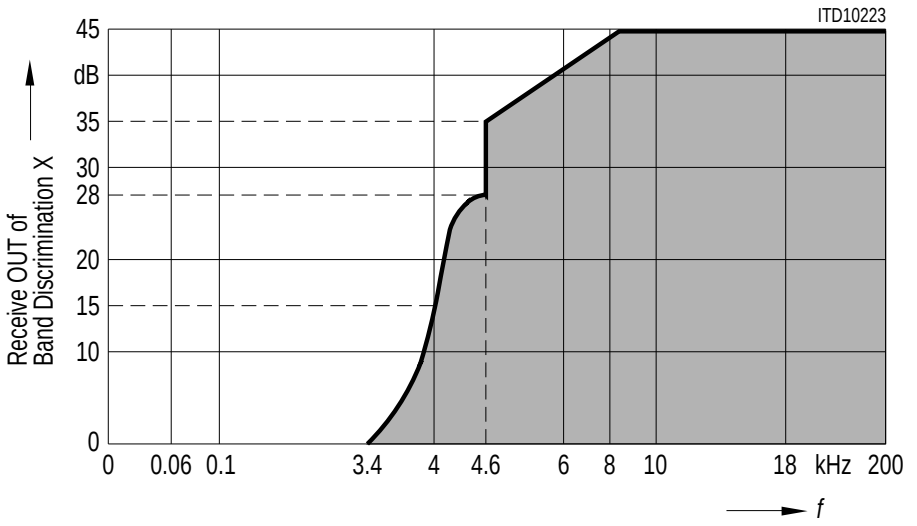



**Figure 13**

$$3.4\ldots4.6\ \text{kHz: } X = -14\left(\sin\left(\left(\pi\frac{4000-f}{1200}\right)-1\right)\right.$$

## 8.4 Out-of-Band Signals at Analog Input (transmit)

With a 0 dBm0 out-of-band sine wave signal with frequency $f$ (< 100 Hz or 3.4 kHz to 100 kHz) applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog input.[1)]

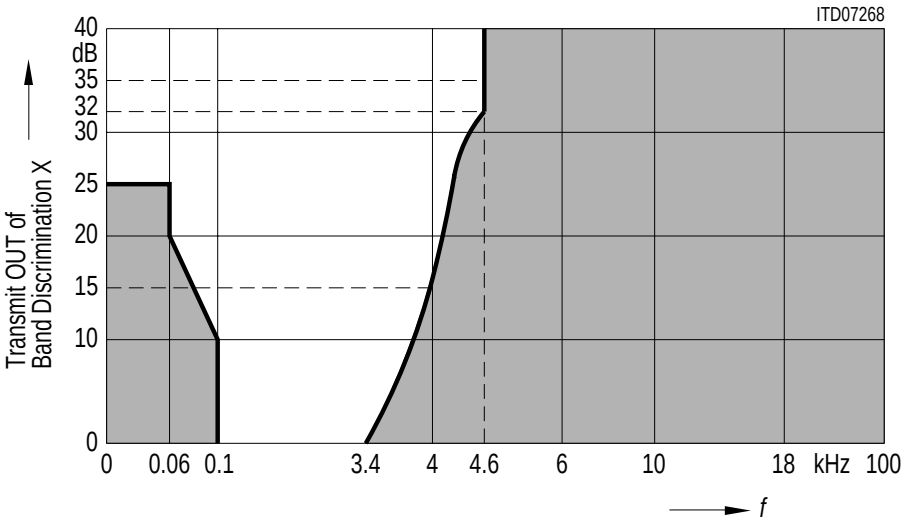



**Figure 14**

$$3.4\ldots4.0\ \text{kHz: } X = -14\left(\sin\left(\pi\frac{4000-f}{1200}\right)-1\right)$$

$$4.0\ldots4.6\ \text{kHz: } X = -18\left(\sin\left(\pi\frac{4000-f}{1200}\right)-\frac{7}{9}\right)$$

1) Poles at 12 kHz ± 150 Hz respectively 16 kHz ± 150 Hz and harmonics will be provided.

## 8.5 Overload Compression

**Transmit:** measured with sine wave $f$ = 1004 Hz.

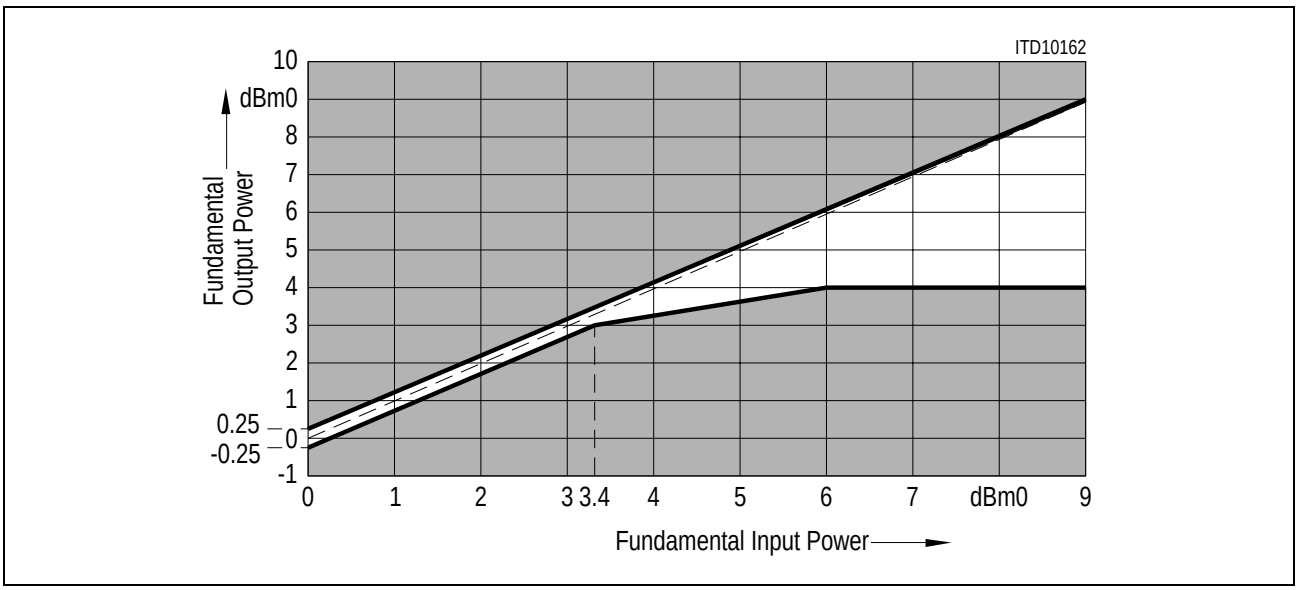



**Figure 15**

## 8.6 Gain Tracking (receive or transmit)

The gain deviations stay within the limits in the figures below.

**Receive:** measured with sine wave $f$ = 1004 Hz
reference level is – 10 dBm0.
**$A_R$ = 6 dB**

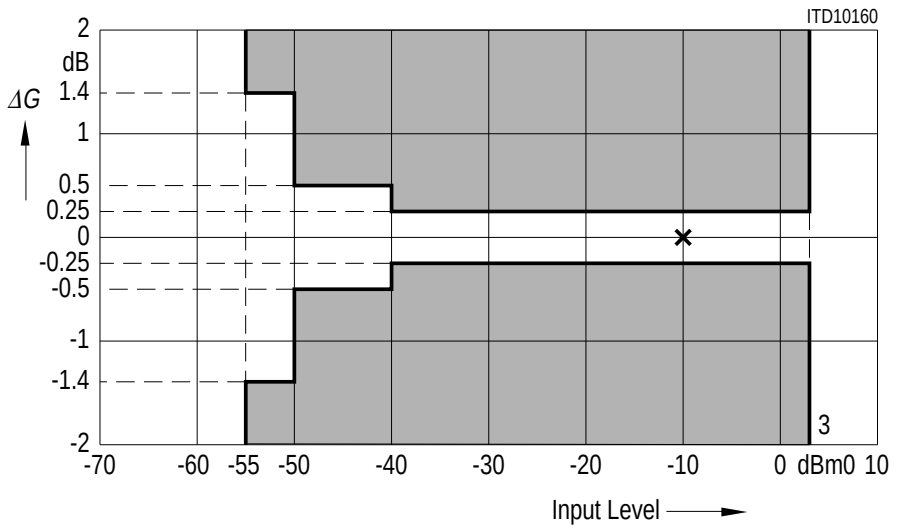



**Figure 16**

**Transmit:** measured with sine wave $f$ = 1004 Hz
reference level is – 10 dBm0.
**$A_X$ = 0 dB**

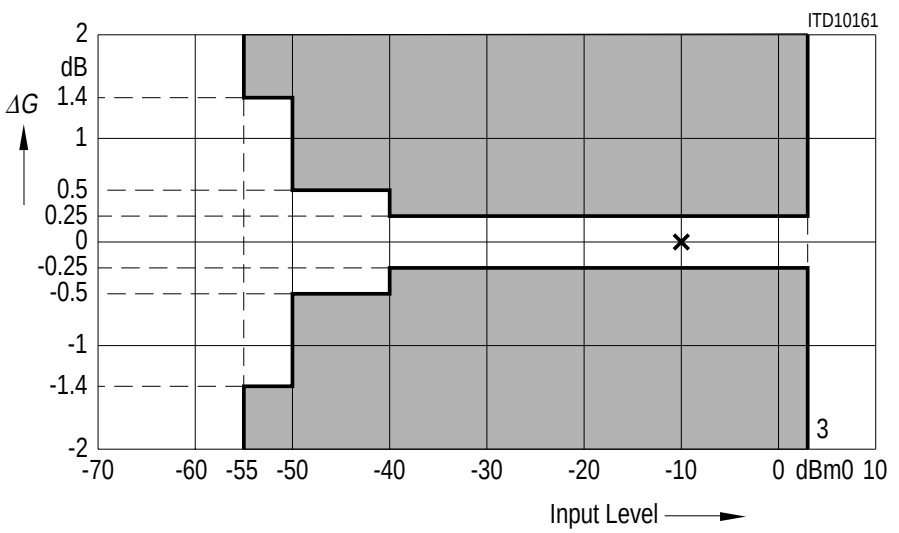



**Figure 17**

## 8.7 Total Distortion

The signal to distortion ratio exceeds the limits in the following figure:

**Receive:** measured with sine wave $f$ = 1004 Hz (C-message weighted for µ-law, psophometrically weighted for A-law).

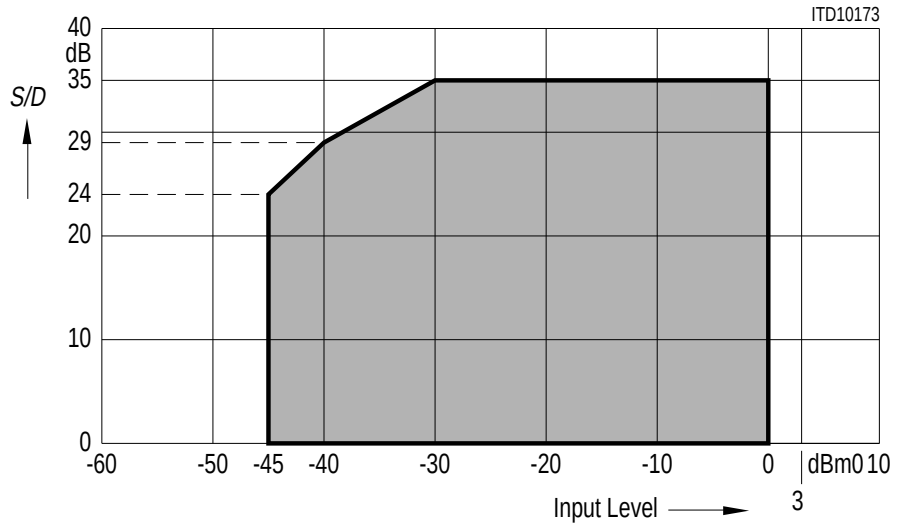



**Figure 18**

$\Sigma(A_{R1} + A_{R2})$ = 7 dB

**Table 16**

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Signal to Distortion at full attenuation | $SD_{att\_R}$ | | – 13 | – 7 | dB | Signal S = – 40 dB<br>$A_R$ = 30 dB |

**Transmit:** measured with sine wave $f$ = 1004 Hz (C-message weighted for µ-law, psophometrically weighted for A-law).

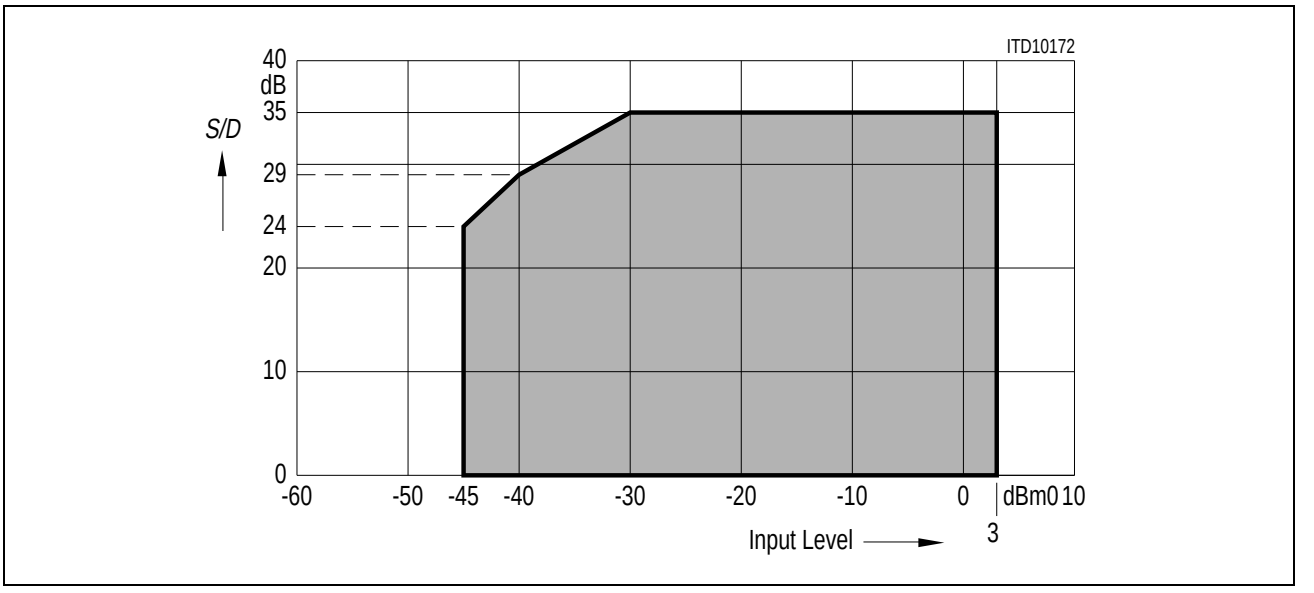



**Figure 19**

$A_X$ = – 7 dB

**Table 17**

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Signal to Distortion at full gain | $SD_{att\_T}$ | | – 17 | – 12 | dB | Signal S = – 40 dB<br>$A_X$ = – 30 dB |
| Signal to Distortion in IMAN Loop | $SD_{IMAN}$ | | – 39 | – 30 | dB | Signal S = – 45 dB |

## 8.8 Transhybrid Loss

The quality of Transhybrid-Balancing is very sensitive to deviations in gain and group delay – deviations inherent to the SLICOFI A/D- and D/A-converters as well as to all external components used on a line card (HV-SLIC).

Measurement of SLICOFI Transhybrid-Loss: A 0 dBm0 sine wave signal with a frequency in the range between 300-3400 Hz is applied to the digital input. The resulting analog output signal at pin $V_{2W}$ is connected to the pin ITAC via a 1 le filters FRR, $A_R$, FRX, $A_X$ and IM are disabled, the balancing filter TH is enabled with coefficients optimized for this configuration ($V_{2W}$ = ITAC).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the table below

**Table 18**

| | **COP-write** | **Coefficients** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| TH-Filter Part 1 | $00_H$ | 00 | 80 | 80 | 18 | 00 | 08 | 00 | 88 |
| TH-Filter Part 2 | $01_H$ | 08 | 00 | AF | 84 | 04 | AC | 2B | 90 |
| TH-Filter Part 3 | $02_H$ | DA | AB | B3 | 22 | DB | 37 | 88 | 00 |

**Table 19**

| **Parameter** | **Symbol** | **Limit Values** | | **Unit** | **Test Condition** |
|---|---|---|---|---|---|
| | | **min.** | **typ.** | | |
| Transhybrid Loss at 500 Hz | $THL_{500}$ | 33 | 50 | dB | |
| Transhybrid Loss at 2500 Hz | $THL_{2500}$ | 29 | 44 | dB | |
| Transhybrid Loss at 3000 Hz | $THL_{3000}$ | 27 | 42 | dB | |

# 9 Electrical Characteristics

## 9.1 Absolute Maximum Ratings

**Table 20**

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|
| | | min. | max. | | |
| $V_{DDA}$ referred to GNDA<br>$V_{DDD}$ referred to GNDD<br>$V_{SS}$ referred to GNDA<br>GNDA with respect to GNDD<br>$V_{DDA}$ with respect to $V_{DDD}$<br>$V_{LINE1,2}$ referred to GND | | – 0.3<br>– 0.3<br>– 5.5<br>– 0.3<br>– 0.3<br>– 75 | 7.0<br>7.0<br>0.3<br>0.3<br>0.3<br>75 | V<br>V<br>V<br>V<br>V<br>V | |
| Analog input and output voltage referred to<br>$V_{DDA}$ = 5 V; ($V_{SS}$ = –5 V)<br>referred to<br>$V_{SS}$ = – 5 V; ($V_{DDA}$ = 5 V) | | – 10.3<br><br>– 0.3 | 0.3<br><br>10.3 | V<br><br>V | |
| All digital input voltages referred to GNDD = 0 V;<br>($V_{DDD}$ = 5 V)<br>referred to $V_{DDD}$ = 5 V;<br>(GNDD = 0 V) | | – 0.3<br><br>– 5.3 | 5.3<br><br>0.3 | V<br><br>V | |
| DC input and output current at any input or output pin (free from latch -up) | | | 100 | mA | |
| Storage temperature<br>Ambient temperature under bias | $T_{STG}$<br>$T_A$ | – 65<br>– 10 | 125<br>80 | °C<br>°C | |
| Power dissipation | $P_D$ | | 1 | W | |
| ESD-integrity (according MIL-Std 883D, method 3015.7) [1] | $V_{ESD}$ | 1000 | | V | |

[1] All Pins except $V_{LINE1}$ and $V_{LINE2}$ (11, 12); for these Pins $V_{ESD}$ < 500 V due to process limitation

*Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.*
*Functional operation under these conditions is not implied.*
*Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may effect device reliability.*

### 9.1.1 Operating Range

$T_A$ = – 40 to 85 °C; $V_{DD}$ = $V_{DDD}$ = $V_{DDA}$ = 5 V ± 5%;
$V_{SS}$ = – 5 V ± 5%; GNDD = GNDA = 0 V

**Table 21**

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| $V_{DD}$ supply current[1)] | | | | | | |
| Power Denial | $IDD_{PDen}$ | | 4 | 6 | mA | |
| Power Down | $IDD_{PDown}$ | | 11 | 15 | mA | |
| Active | $IDD_{Act}$ | | 21 | 30 | mA | |
| Active with TTX | $IDD_{TTX}$ | | 25 | 34 | mA | |
| Ringing | $IDD_{Rng}$ | | 11 | 15 | mA | |
| $V_{SS}$ supply current[1)] | | | | | | |
| Power Denial | $ISS_{PDen}$ | | 1 | 2 | mA | |
| Power Down | $ISS_{PDown}$ | | 3,5 | 6 | mA | |
| Active | $ISS_{Act}$ | | 4,5 | 7 | mA | |
| Active with TTX | $ISS_{TTX}$ | | 7 | 10 | mA | |
| Ringing | $ISS_{Rng}$ | | 3.5 | 6 | mA | |
| Power supply rejection-ratio | PSRR | | | | | ripple: 1 kHz, 70 mVrms |
| receive $V_{DD}$ | | 56 | 70 | | dB | at $V_{2W}$ |
| receive $V_{SS}$ | | 56 | 65 | | dB | at $V_{2W}$ |
| transmit $V_{DD}$ | | 40 | 70 | | dB | at IOM-2 |
| transmit $V_{SS}$ | | 40 | 50 | | dB | at IOM-2 |
| Power dissipation[1)] | | | | | | |
| Power Denial | PDen | | 25 | 42 | mW | |
| Power Down | PDown | | 73 | 110 | mW | |
| Active | Act | | 128 | 195 | mW | |
| Active with TTX | TTX | | 160 | 231 | mW | |
| Ringing | Rng | | 73 | 110 | mW | |

1) Power dissipation and supply currents are target values.

## 9.2 Digital Interface

$T_A$ = – 40 to 85 °C; $V_{DD} = V_{DDD} = V_{DDA}$ = 5 V ± 5%;
$V_{SS}$ = – 5 V ± 5%; GNDD = GNDA = 0 V

**Table 22**

| Parameter | Symbol | Limit Values | | Unit | Test condition |
|---|---|---|---|---|---|
| | | min | max. | | |
| For all input pins (including IO-Pins): | | | | | |
| Low-input pos.-going | $V_{T+}$ | – 0,3 | 3.15 | V | see figure below |
| Low-input neg.-going | $V_{T-}$ | 1.35 | $V_{DD}$ + 0,3 | V | see figure below |
| Low-input Hysteresis | $V_H$ | 0.5 | | V | $V_H = V_{T+} - V_{T-}$ |
| Input leakage current | $I_{IL}$ | – 1 | 1 | µA | $-0.3 \le V_{in} \le V_{DD}$ |
| Spike rejection for RESET (pin 36) | $t_{rej}$ | 50 | 200 | ns | |
| Ternary Inputs: ID-L, ID-M (pins 31, 32) | | | | | |
| High level | $V_{IHID}$ | 2.0 | | V | |
| Zero level | $V_{IMID}$ | – 0.8 | 0.8 | V | |
| Low level | $V_{ILID}$ | | – 2.0 | V | |
| For all output pins except DU (Pin 6; including IO-Pins): | | | | | |
| Low-output voltage | $V_{OL}$ | | 0.45 | V | $I_O$ = – 2 mA (typ. at $I_O$ = – 3.5 mA) |
| High-output voltage | $V_{OH}$ | 3.5 | | V | $I_O$ = 400 µA |
| for DU-pin (Pin 6) | | | | | |
| Low-output voltage | $V_{OLDU}$ | | 0.45 | V | $I_O$ = – 4 mA (typ. at $I_O$ = – 7 mA) |
| High-output voltage | $V_{OHDU}$ | 3.5 | | V | $I_O$ = 400 µA |

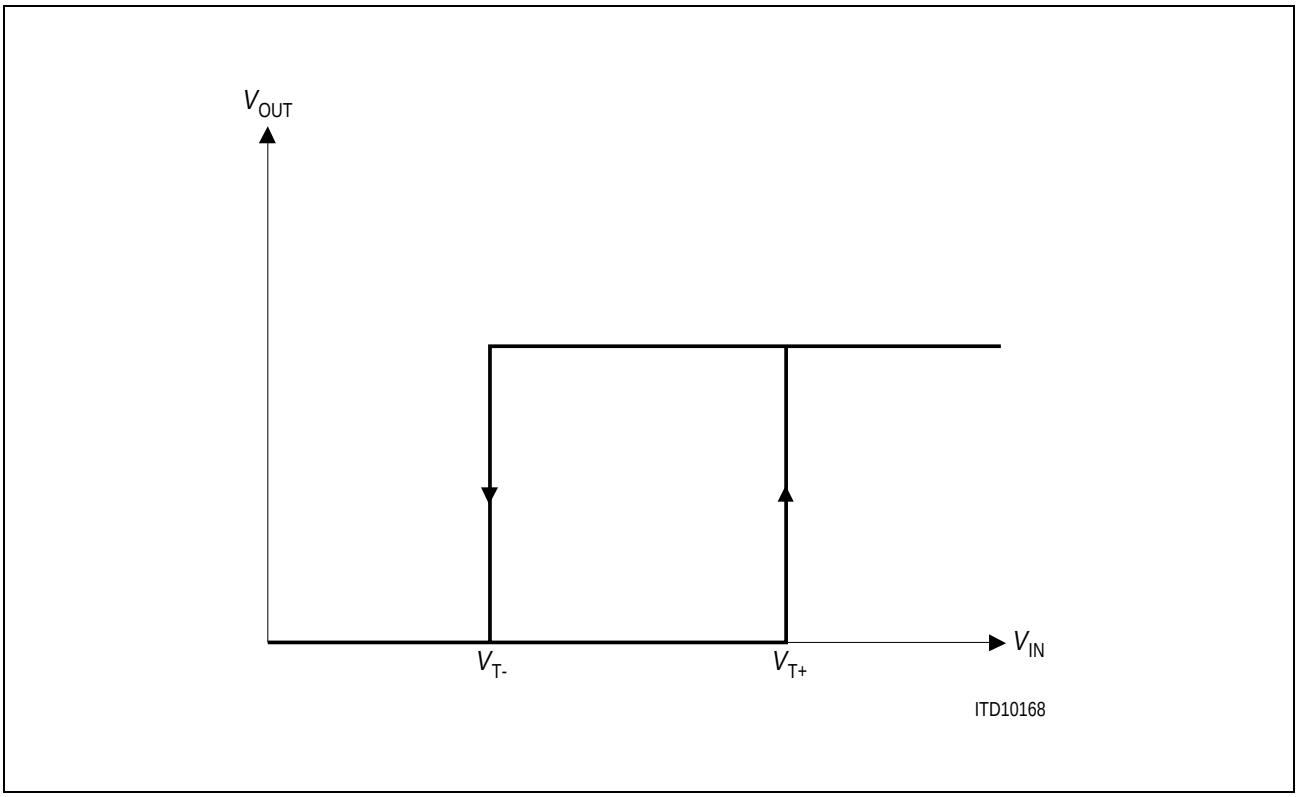



**Figure 20**

## 9.3 DC-Feeding

### 9.3.1 DC-Feeding ($T_A$ = 0 to 70 °C)

$T_A$ = – 0 to 70 °C; $V_{DD}$ = $V_{DDD}$ = $V_{DDA}$ = 5 V ± 5%;
$V_{SS}$ = – 5 V ± 5%; GNDD = GNDA = 0 V

**Table 23**

| Parameter | Symbol | Limit Values | | | Unit | Test condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| "Line Current" Measurement: | | | | | | |
| Transmit | $V_{IT\ offset}$ | – 25 | | 25 | mV | direct/reverse polarity |
| | $V_{IT\ gain}$ | 0.94 | | 1.06 | | $f$ < 50 Hz, direct polarity |
| | $V_{IT\ gain}$ | – 1.06 | | – 0.94 | | $f$ < 50 Hz, reverse polarity |
| | $V_{IT\ THD}$ | 40 | 50 | | dB | direct/reverse polarity |
| "Line Voltage" Feeding: | | | | | | |
| Receive | $V_{2W\ offset}$ | – 25 | | 25 | mV | normal battery, $f$ = 300 Hz |
| | $V_{2W\ gain}$ | 0.94 | | 1.06 | | normal battery, $f$ = 300 Hz |
| | $V_{2W\ THD}$ | 40 | 50 | | dB | normal battery |
| Receive Boosted | $V_{2W\ offset}$ | – 40 | | 40 | mV | boosted battery, $f$ = 300 Hz |
| | $V_{2W\ gain}$ | 1.5 | 1.6 | 1.7 | | boosted battery, $f$ = 300 Hz |
| | $V_{2W\ THD}$ | 40 | 50 | | dB | boosted battery |

### 9.3.2 DC-Feeding ($T_A$ = – 40 to 85 °C)

$T_A$ = – 40 to 85 °C; $V_{DD}$ = $V_{DDD}$ = $V_{DDA}$ = 5 V ± 5%;
$V_{SS}$ = – 5 V ± 5%; GNDD = GNDA = 0 V

**Table 24**

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| "Line Current" Measurement: | | | | | | |
| Transmit | $V_{IT\ offset}$ | – 30 | | 30 | mV | direct/reverse polarity |
| | $V_{IT\ gain}$ | 0.94 | | 1.06 | | $f$ < 50 Hz, direct polarity |
| | $V_{IT\ gain}$ | – 1.06 | | – 0.94 | | $f$ < 50 Hz, reverse polarity |
| | $V_{IT\ THD}$ | 40 | 50 | | dB | direct/reverse polarity |

**Table 24** (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| "Line Voltage" Feeding: | | | | | | |
| Receive | $V_{2W\ offset}$ | –30 | | 30 | mV | normal battery, $f$ = 300 Hz |
| | $V_{2W\ gain}$ | 0.927 | | 1.073 | | normal battery, $f$ = 300 Hz |
| | $V_{2W\ THD}$ | 40 | 50 | | dB | normal battery |
| Receive Boosted | $V_{2W\ offset}$ | –48 | | 48 | mV | boosted battery, $f$ = 300 Hz |
| | $V_{2W\ gain}$ | 1.48 | 1.6 | 1.72 | | boosted battery, $f$ = 300 Hz |
| | $V_{2W\ THD}$ | 40 | 50 | | dB | boosted battery |

## 9.4 HV-SLIC Interface

$T_A$ = – 40 to 85 °C; $V_{DD}$ = $V_{DDD}$ = $V_{DDA}$ = 5 V ± 5%;
$V_{SS}$ = – 5 V ± 5%; GNDD = GNDA = 0 V

**Table 25**

| Parameter | Symbol | Limit Values | | | Unit | Test Condition/Result |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Ground Key Detection at Pin IL | $V_{ILLo}$ | – 217 | | 217 | mV | GNK = 0 |
| | $V_{ILHi}$ | 293 | | – 293 | mV | GNK = 1 |
| Half Battery Information at Pin $V_{2W}$ | | | | | | $V_{BIM}$ = – 3 V |
| | $V_{V2WLo}$ | | | – 1.65 | V | VB/2 = 0 |
| | $V_{V2WHi}$ | – 1.35 | | | V | VB/2 = 1 |
| PDN-Pin max. $R_{on}$ | $R_{on}$ | | 90 | 250 | | in Active-Mode to GND |

**Table 25** (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition/Result |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Output voltage:<br>HV-SLIC-Interface<br>Pins 9, 10 (C1, C2) | | | | | | |
| High level | $V_{OHHV}$ | 2.5 | | | V | $I_{out}$ < 10 |
| Zero level | $V_{OMHV}$ | – 0.8 | | 0.8 | V | $I_{out}$ < 10 |
| Low level | $V_{OLHV}$ | | | – 2.5 | V | $I_{out}$ < 10 |
| Current drained | $I_{OTLo}$ | | | 320 | µA | TEMPA = 0 |
| from pin 9 (C1) | $I_{OTHi}$ | 480 | | | µA | TEMPA = 1 |
| in all 3 states | | | | | | |
| External Indication | | | | | | measured at IOM-2 |
| | $V_{EXT\_off}$ | – 200 | | 200 | mV | without DC $V_{LINE}$ = 0 V |
| | $V_{EXT\_0}$ | 0.5 | | 1.3 | V | without DC $V_{LINE}$ = 6 V |
| | $V_{EXT\_6}$ | 0.3 | | 1.5 | V | with DC = 30 V<br>$V_{LINE}$ [1)] = 6 V |

1) $V_{LINE} = V_{LINE1} - V_{LINE2}$

## 9.5 IOM®-2 Interface Timing

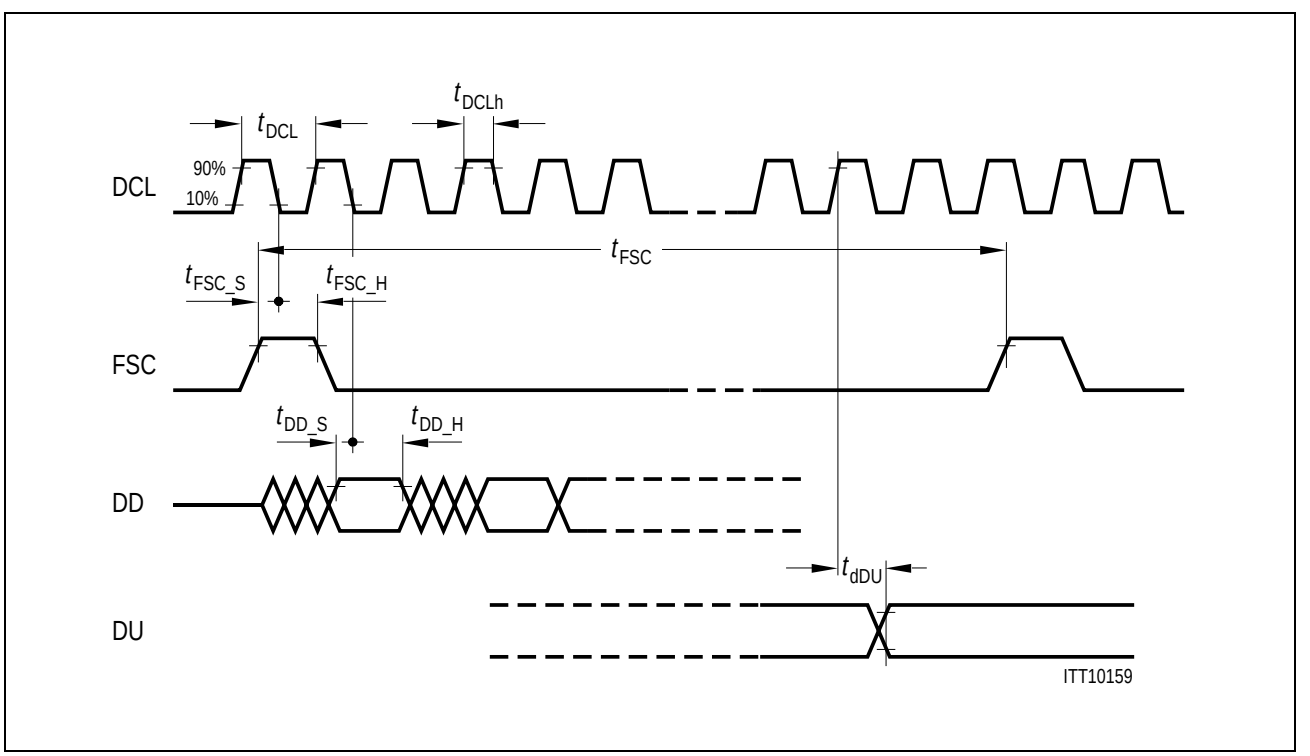



**Figure 21**

**Table 26 Switching Characteristics**

| Parameter | Symbol | Limit Values | | | Unit |
|---|---|---|---|---|---|
| | | min. | typ. | max. | |
| Period DCL “slow” mode[1] | $t_{DCL}$ | | 1/2048 | | kHz |
| Period DCL “fast” mode[2] | $t_{DCL}$ | | 1/4096 | | kHz |
| DCL Duty Cycle | $t_{DCLh}$ | 40 | | 60 | % |
| Period FSC | $t_{FSC}$ | | 125 | | µs |
| FSC set-up time | $t_{FSC\_S}$ | 70 | $t_{DCLh}$ | | ns |
| FSC hold time | $t_{FSC\_H}$ | 40 | | | ns |
| DD data in set-up time | $t_{DD\_S}$ | 20 | | | ns |
| DD data in hold time | $t_{DD\_H}$ | 50 | | | ns |
| DU data out delay (intrinsic) | $t_{dDUintr.}$ | | 40 | 70 | ns |
| DU data out delay | $t_{dDU}$ | | 150[3] | 250 | ns |

1) DCL = 2048 kHz: $t_{FSC} = 256 \times t_{DCL}$

2) DCL = 4096 kHz: $t_{FSC} = 512 \times t_{DCL}$

3) Depending on Pull up resistor (typical 1…10 k)

## 9.6 IOM®-2 Command/Indication Interface Timing (DCL = 4096 kHz)

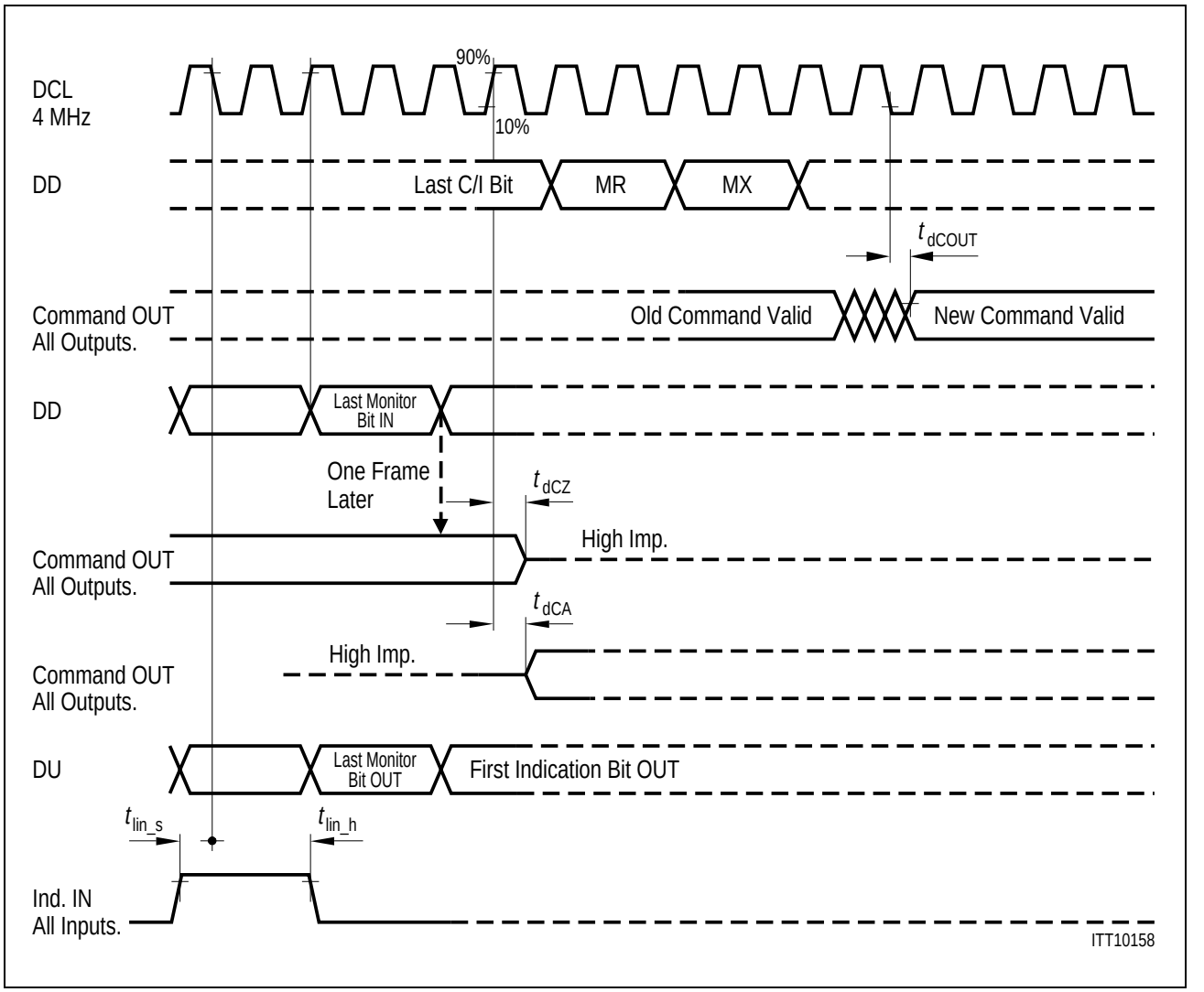



**Figure 22**

### Table 27 Switching Characteristics

| Parameter | Symbol | Limit Values | | | Unit |
|---|---|---|---|---|---|
| | | min. | typ. | max. | |
| Command out delay | $t_{dCout}$ | | | 0 | ns |
| Command out high impedance<br>Command out active | $t_{dCZ}$<br>$t_{dCA}$ | | 150<br>150 | 200<br>200 | ns<br>ns |
| Indication in set-up time<br>Indication in hold time | $t_{lin\_s}$<br>$t_{lin\_h}$ | 50<br>200 | | | ns<br>ns |

## 9.7 IOM®-2 Command/Indication Interface Timing (DCL = 2048 kHz)

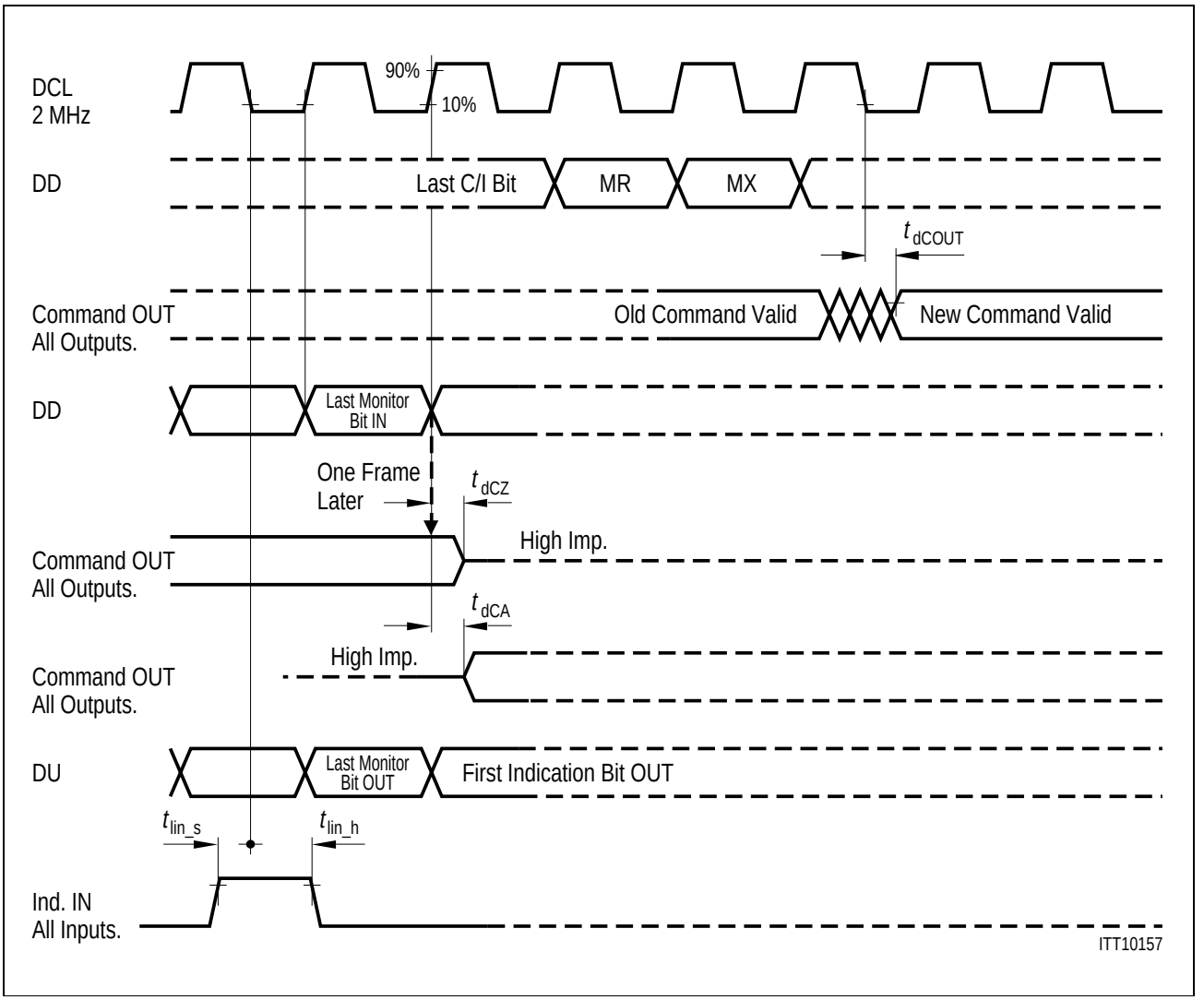



**Figure 23**

**Table 28 Switching Characteristics**

| Parameter | Symbol | Limit Values | | | Unit |
|---|---|---|---|---|---|
| | | min. | typ. | max. | |
| Command out delay | $t_{dCout}$ | | | 0 | ns |
| Command out high impedance<br>Command out active | $t_{dCZ}$<br>$t_{dCA}$ | | 150<br>150 | 200<br>200 | ns<br>ns |
| Indication in set-up time<br>Indication in hold time | $t_{lin\_s}$<br>$t_{lin\_h}$ | 50<br>200 | | | ns<br>ns |

## 9.8 External Masterclock

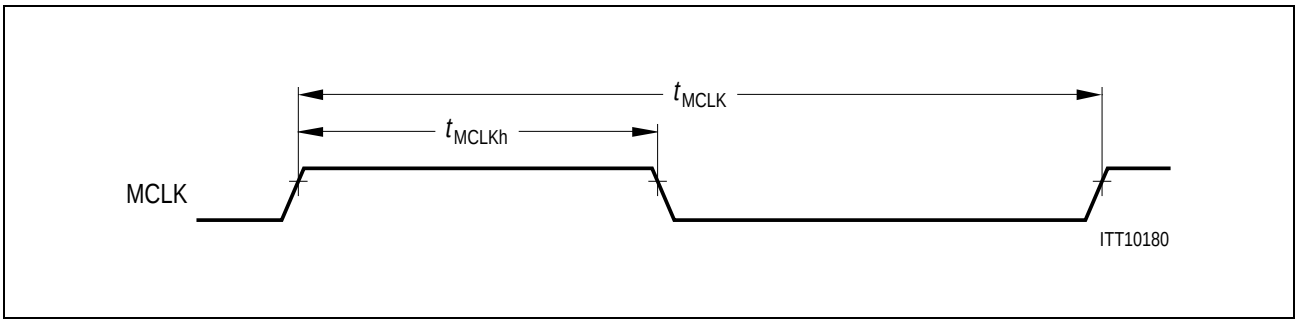



**Figure 24**

**Table 29 Switching Characteristics**

| Parameter | Symbol | Limit Values | | | Unit |
|---|---|---|---|---|---|
| | | min. | typ. | max. | |
| Period MCLK | $t_{MCLK}$ | | 1/16.384 | | MHz |
| MCLK Duty Cycle | $t_{MCLKh}$ | 40 | | 60 | % |

# 10 Appendix

## 10.1 IOM®-2 Interface Monitor Transfer Protocol

### Monitor Channel Operation

The monitor channel is used for the transfer of maintenance information between two functional blocks. Using two monitor control bits (MR and MX) per direction, the data are transferred in a complete handshake procedure. The MR and MX bits in the fourth octet (C/I channel) of the IOM2 frame are used for the handshake procedure of the monitor channel

The monitor channel transmission operates on a pseudo-asynchronous basis:

– Data transfer (bits) on the bus is synchronized to Frame Sync FSC
– Data flow (bytes) are asynchronously controlled by the handshake procedure.

For example: Data is placed onto the DD-Monitor-Channel by the Monitor-transmitter of the master device (DD-MX-Bit is activated i.e. set to ‘0’). This data transfer will be repeated within each frame (125 µs rate) until it is acknowledged by the SLICOFI Monitor-receiver by setting the DU-MR-bit to ‘0’, which is checked by the Monitor-transmitter of the master device. Thus, the data rate is not 8-Kbytes/s.

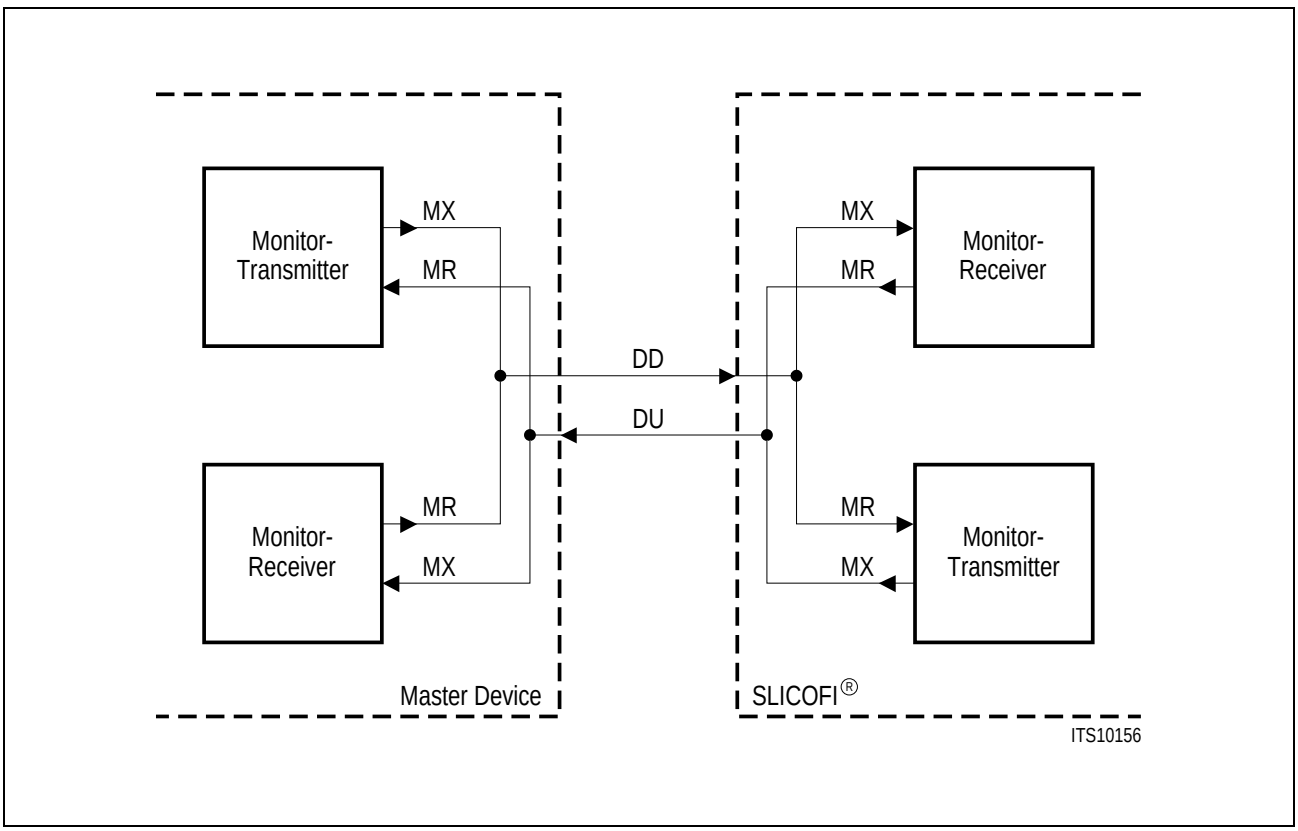



**Figure 25**

### Monitor Handshake Procedure

The monitor channel works in 3 states

**Idle state** A pair of inactive (set to ‘1’) MR- and MX-bits during two or more consecutive frames: End of Message (EOM)

**Sending state** MX-bit is activated (set to ‘0’) by the Monitor-transmitter, together with data-bytes (can be changed) on the Monitor-channel

**Acknowledging** MR-bit is set to active (set to ‘0’) by the Monitor-receiver, together with a data-byte remaining in the Monitor-channel.

A start of transmission is initiated by a Monitor-transmitter in sending out an active MX-bit together with the first byte of data (the address of the receiver) to be transmitted in the Monitor-channel.

This state remains until the addressed Monitor-Receiver acknowledges the received data by sending out an active MR-bit, which means that the data-transmission is repeated each 125 µs frame (minimum is one repetition). During this time the Monitor-transmitter evaluates the MR-bit.

Flow control, means in the form of transmission delay, can only take place when the transmitters MX and the receivers MR bit are in active state.

Since the receiver is able to receive the monitor data at least twice (in two consecutive frames), it is able to check for data errors. If two different bytes are received the receiver will wait for the receipt of two identical successive bytes (last look function)

A collision resolution mechanism (check if another device is trying to send data during the same time) is implemented in the transmitter. This is done by looking for the inactive (‘1’) phase of the MX-bit and making a per bit collision check on the transmitted monitor data (check if transmitted ‘1’s are on DU/DD-line; DU/DD-line are open-drain lines).

Any abort leads to a reset of the SLICOFI command stack, the device is ready to receive new commands.

To obtain a maximum speed data transfer, the transmitter anticipates the falling edge of the receivers acknowledgment.

Due to the inherent programming structure, duplex operation is not possible. It is not **allowed** to send any data to the SLICOFI, while transmission is active.

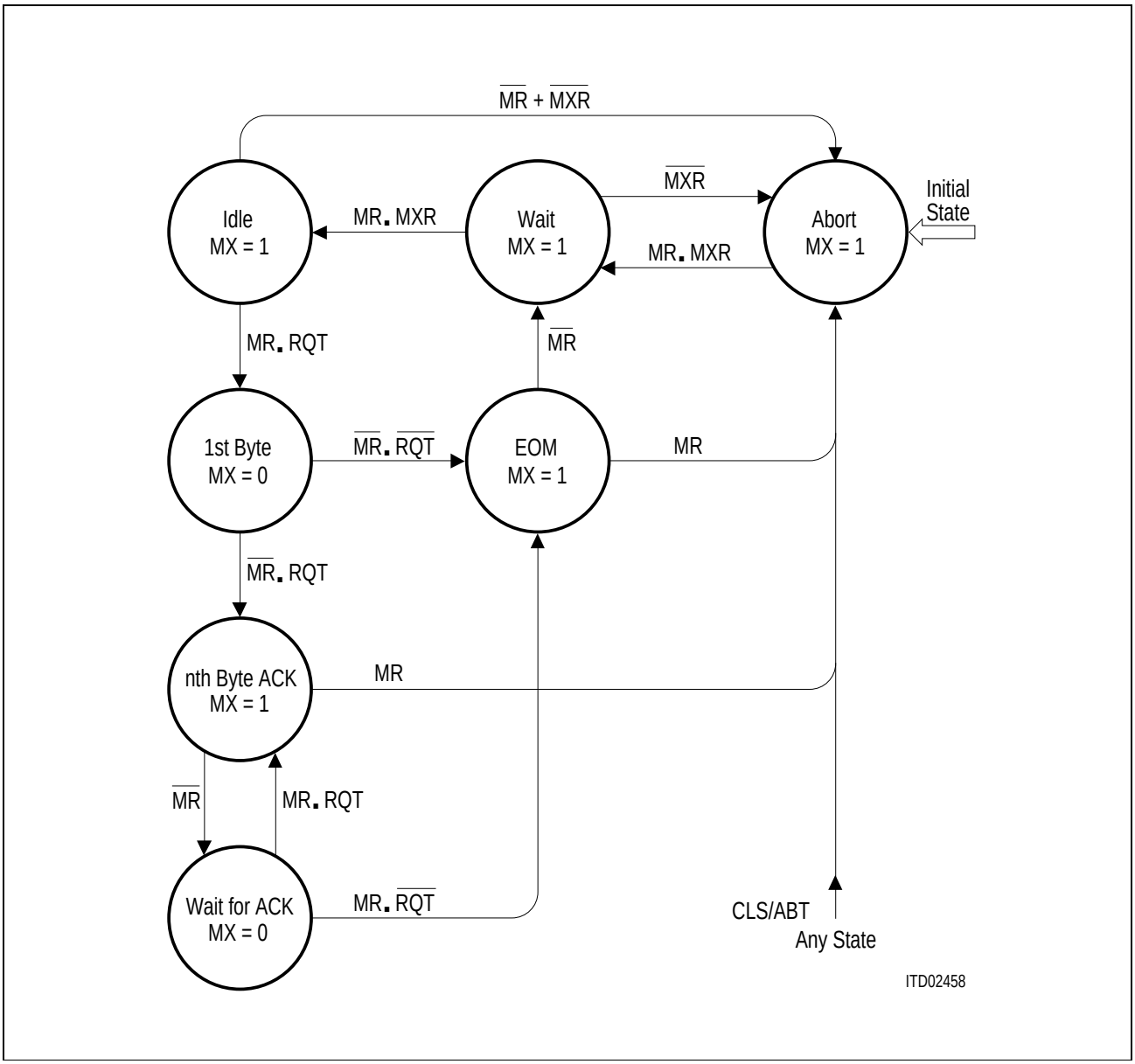



**Figure 26 State Diagram of the SLICOFI Monitor Transmitter**

MR ... MR - bit received on DD - line
MX ... MX - bit calculated and expected on DU - line
MXR ... MX - bit sampled on DU - line
CLS ... Collision within the monitor data byte on DU - line
RQT ... Request for transmission form internal source
ABT ... Abort request/indication

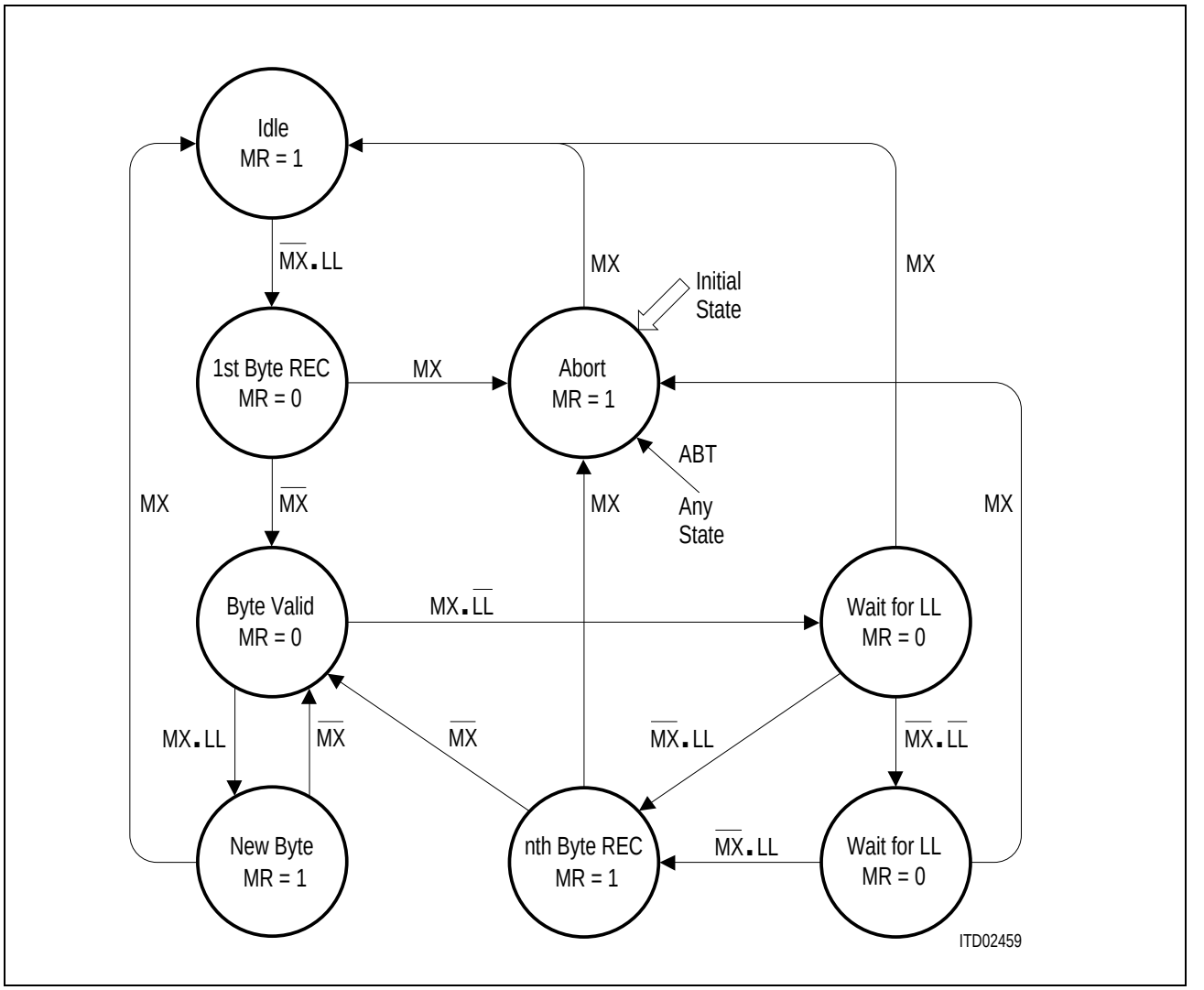



**Figure 27 State Diagram of the SLICOFI Monitor Receiver**

MR ... MR - bit calculated and transmitted on DU - line
MX ... MX - bit received data downstream (DD - line)
LL ... Last lock of monitor byte received on DD - line
ABT ... Abort indication to internal source

### Monitor Channel Data Structure

The monitor channel is used for the transfer of maintenance information between two functional blocks. By use of two monitor control bits (MR and MX) per direction, the data are transferred in a complete handshake procedure.

**Address Byte**

Messages to and from the SLICOFI are started with the following byte:

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Thus providing information for only one analog line, the SLICOFI is one device on one IOM-2 time slot. Monitor data for the analog channel is selected by the SLICOFI specific command (SOP, TOP or COP) following.

## 10.2 Channel Identification Command (CIC)

In order to unambiguously identify different devices by software, a two Byte identification command is defined for analog lines IOM-2 devices. A device requesting the identification of the SLICOFI will send the following 2 byte code:

| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|

Each device will then respond with its specific identification code. For the SLICOFI this two byte identification code is:

| 1 | 0 | 0 | 0 | CONF |
|---|---|---|---|---|

| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|

**CONF** an optional 4-bit code indicating the specific hardware environment. A typical application of the CONF code is the differentiation of various types of line circuits that use the same SLICOFI/SLIC hardware within the same system.

For the realization of the Channel Identification Commands on the line card, it needs 3 pins at the SLICOFI. There are two inputs that can handle a ternary code (ID-L and ID-M). One pin is a binary input (ID-H) which is switchable as a digital serial interface of a shift register, to transfer special line card design informations up to 15 bytes into the monitor channel of the IOM-2 interface.

There are two different solutions of the CIC for the SLICOFI to identify the version of the line card.

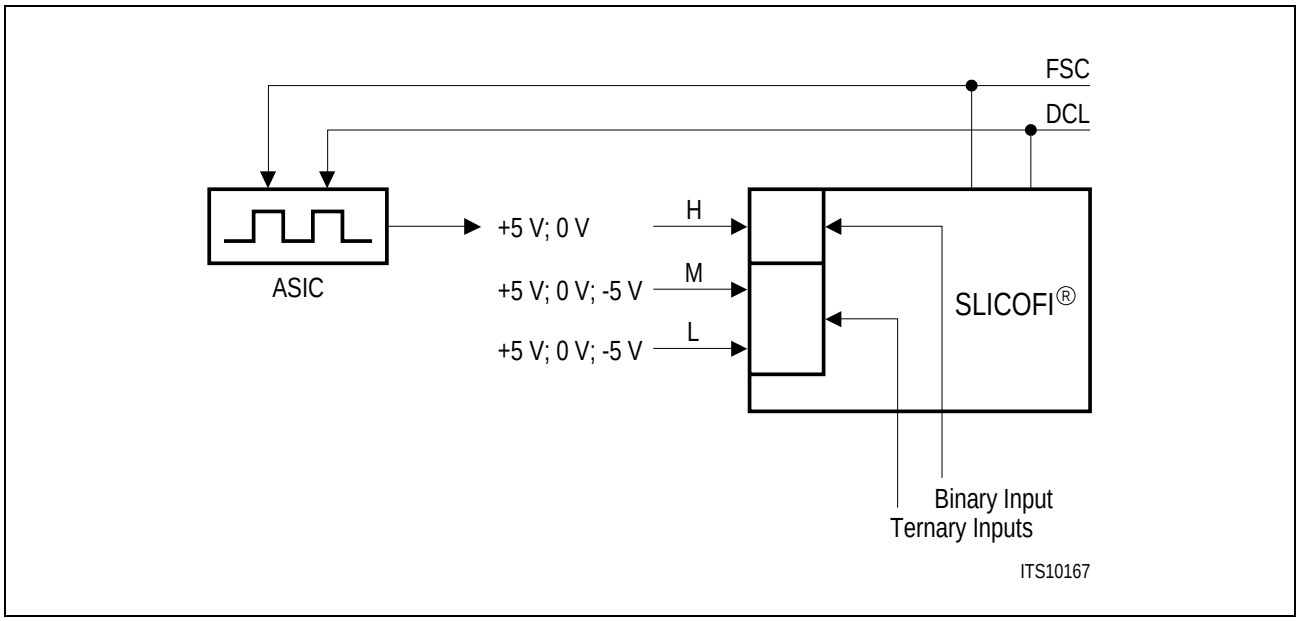



**Figure 28**

**Solution 1 ("Normal" Channel Identification Command):**

The input of the 3 pin interface (ID-H, ID-L, ID-M) is transferred to the 4 bit CONF information using the following truth-table:

**Table 30**

| SLICOFI Ports | | | CONF-inf. |
|---|---|---|---|
| **ID-H** | **ID-M** | **ID-L** | **(4 bits)** |
| + 5 V | − 5 V | − 5 V | 0 0 0 0 |
| + 5 V | − 5 V | 0 V | 0 0 0 1 |
| + 5 V | − 5 V | + 5 V | 0 0 1 0 |
| + 5 V | 0 V | − 5 V | 0 0 1 1 |
| + 5 V | 0 V | 0 V | 0 1 0 0 |
| + 5 V | 0 V | + 5 V | 0 1 0 1 |
| + 5 V | + 5 V | − 5 V | 0 1 1 0 |
| + 5 V | + 5 V | 0 V | 0 1 1 1 |
| 0 V | + 5 V | 0 V | 1 0 0 0 |
| 0 V | + 5 V | − 5 V | 1 0 0 1 |
| 0 V | 0 V | + 5 V | 1 0 1 0 |
| 0 V | 0 V | 0 V | 1 0 1 1 |
| 0 V | 0 V | − 5 V | 1 1 0 0 |
| 0 V | − 5 V | + 5 V | 1 1 0 1 |
| 0 V | − 5 V | 0 V | 1 1 1 0 |
| 0 V | − 5 V | − 5 V | 1 1 1 1 |

This is a 16 possible individual line card design information or an address pointer for the system to get more basic information.

The information is read through the IOM-2 monitor channel with the CIC command.

**Solution 2 (Extended Channel Identification Command):**

The second realization step is that the combination of ports (M + L) = + 5 V changes the input port ID-H to a shift register input.

**Table 31**

| SLICOFI Ports | | | CONF-inf. |
|---|---|---|---|
| **ID-H** | **ID-M** | **ID-L** | **(4 bits)** |
| X | + 5 V | + 5 V | 1 1 1 1 |

An external shift register on the line card transmits up to 15 bytes of special HW + FW line card design information (TCR4 - TCR18).

The information is read through the IOM2 monitor channel with the TOP Command. The LSEL bits TOP Command's register must be ‘10’ - code for reading extended line card design and configuration information from TCR4 - TCR18 registers, which are sequential reading using two shift register. The CONF code is ‘1111’ by this extended identification.

The first schematic gives an overview of the different timings for the extended channel identification.

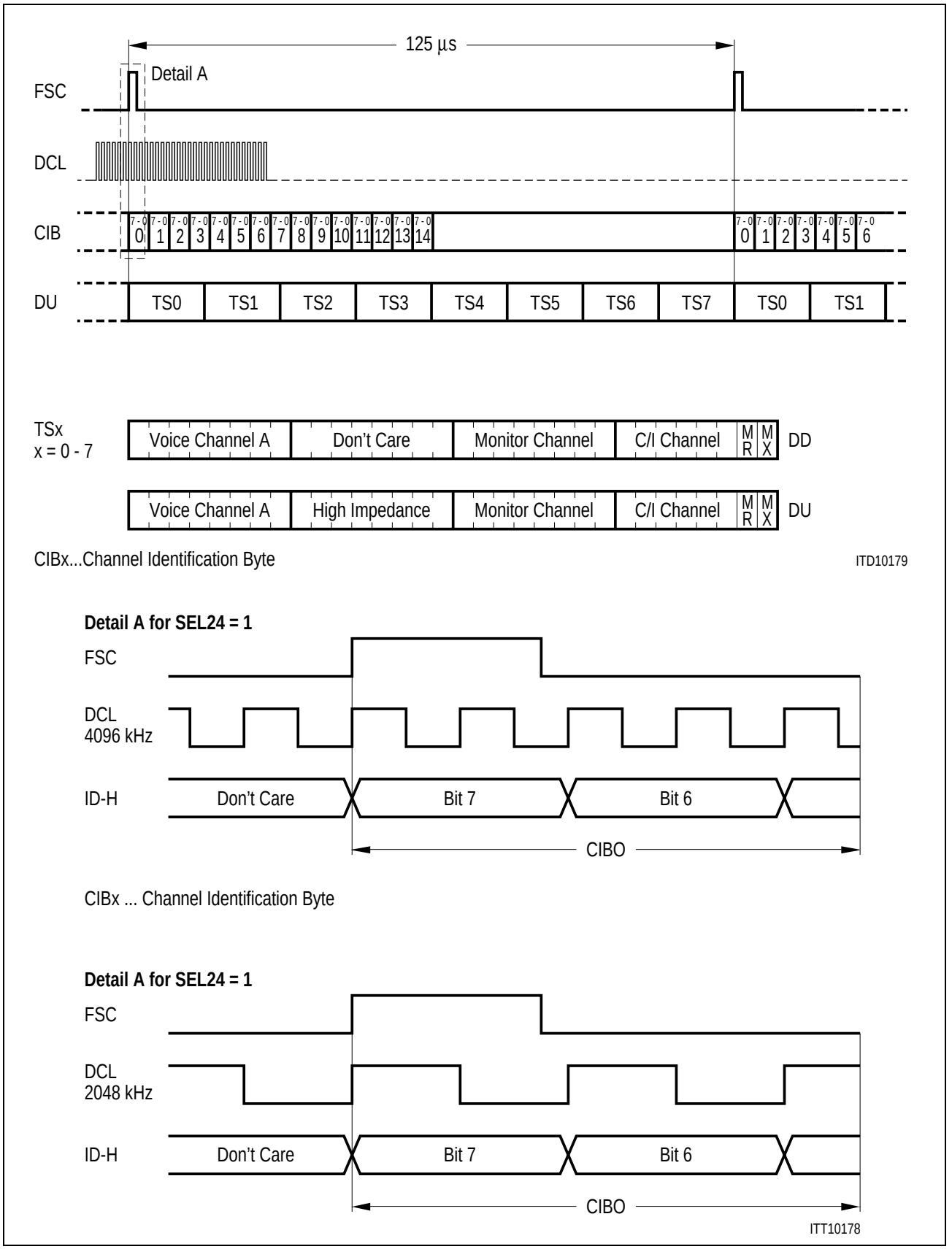



**Figure 29 General Timing**

**Expected Input of the ASIC (via ID - H; ID - L = ID - M 0 = + 5 V)**

If - for example - the SLICOFI has the time slot 6 (TSx = 110, see **chapter 4**, **page 16**, too), the Monitor Channel of TS6 looks like the following (for all other time slots equivalent).

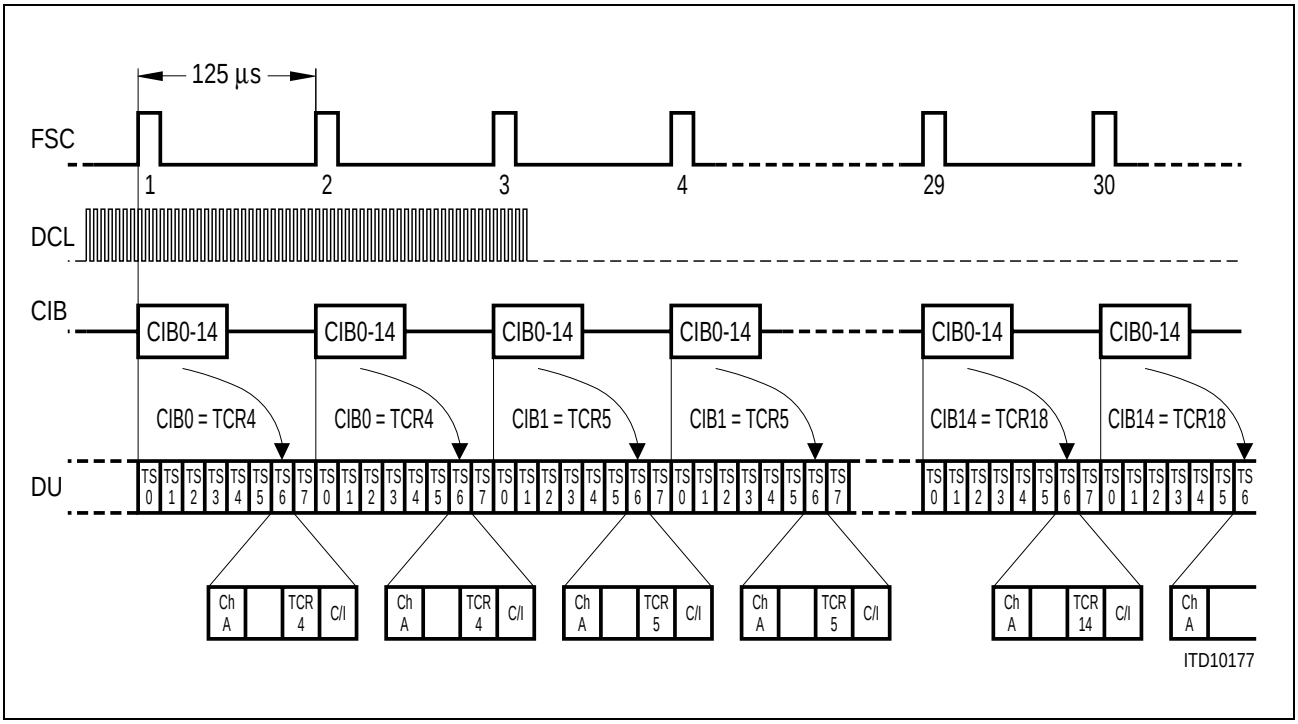



**Figure 30**

Expected Input Timing and IOM-2 Interface Timing and Switching characteristic: To be defined.

## 10.3 Test Modes

Various loops and tests (to cut off at different points or disable some filters) for testing either the chip or the board and the line are implemented in the SLICOFI.

**Table 32**

| LB | TM | T3 | T2 | T1 | T0 | Testloop |
|---|---|---|---|---|---|---|
| SCR1-5 | SCR2-3 | SCR6-3 | SCR6-2 | SCR6-1 | SCR6-0 | |
| 1 | 0 | 0 | 0 | 0 | 1 | ALB_ADC |
| 1 | 0 | 0 | 1 | 0 | 1 | DLB_4M |
| 1 | 0 | 1 | 0 | 0 | 0 | DLB_PCM |
| 1 | 0 | 1 | 1 | 0 | 0 | DC_ALB |
| 1 | 0 | all other combinations of T3: T0 | | | | don't use |
| 1 | 1 | 0 | 0 | 0 | 1 | RVP |
| 1 | 1 | 0 | 0 | 1 | 0 | TVP |

**Table 32** (cont'd)

| LB | TM | T3 | T2 | T1 | T0 | Testloop |
|---|---|---|---|---|---|---|
| SCR1-5 | SCR2-3 | SCR6-3 | SCR6-2 | SCR6-1 | SCR6-0 | |
| 1 | 1 | 0 | 0 | 1 | 1 | LC |
| 1 | 1 | 0 | 1 | 0 | 0 | RC |
| 1 | 1 | 0 | 1 | 0 | 1 | ILT |
| 1 | 1 | 0 | 1 | 1 | 0 | DC-THRU |
| 1 | 1 | all other combinations of T3: T0 | | | | don't use |
| 0 | X | X | X | X | X | all loops off |

### Testregister (STCR1 to 8) - Summary

The Testregisters (accessed by the SOP-command with LSEL = 11b) are for internal use only. The 8 Testregisters can only be read or written en bloc. They are enabled/disabled by the Enable Testregister bit ENTR (SCR5-1). For ENTR = 0 the STCRs are set to the basic settings - so no refresh is necessary.

**But note there are complex internal connections; so do use only the following two commands: ACDACDIS and EXT_MCLK. All other bits MUST be set as described below.**

### STCR1 Test Configuration Register 1

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset value: $00_H$

### STCR2 Test Configuration Register 2

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | EXT_MCLK | 0 | 0 | ACDACDIS | 0 | 0 |

Reset value: $00_H$

**general remark** All bits of STCR1 are set if necessary automatically by regular testloops. So setting STCR1-bits to '1', together with a testloop, the certain action is inverted.

**EXT_MCLK** Possibility to provide the SLICOFI with external clock (see also **page 35**, EXT_MCLK, SCR8-4; There are no functional differences between these two settings!)

EXT_MCLK = 0 Internal masterclock is used
EXT_MCLK = 1 External masterclock is used

To use an external masterclock of 16 MHz following steps must be done:

1) IO1 must be set to input and becomes the input-pin of the masterclock
2) Enable the testregisters (Configuration Register 5: SCR5-1 (ENTR) =1)
3) The testregisterblock must be programmed (Test Configuration Register 2: STCR2-5 (EXT_MCLK) = 1)

**ACDACDIS** Disables AC-DAC
ACDACDIS = 0 normal operation
ACDACDIS = 1 disables AC-DAC

### STCR3 Test Configuration Register 3

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset value: $00_H$

### STCR4 Test Configuration Register 4

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |

Reset value: $5F_H$

### STCR5 Test Configuration Register 5

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset value: $00_H$

### STCR6 to STCR8 Test Configuration Register 6 to 8

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset value: $00_H$

**ALB_ADC**

(Analog loop with ADC and DAC)

This testloop feasibles the test of AC analog parts including ADC and DAC.

Initializing the testloop:

Reset

Active Mode

Disable Impedance matching filter
(OPIMAN (SCR6_5) = 1, OPIM4M (SCR6_4) = 1, IM (SCR4_6) = 0)

Testloop

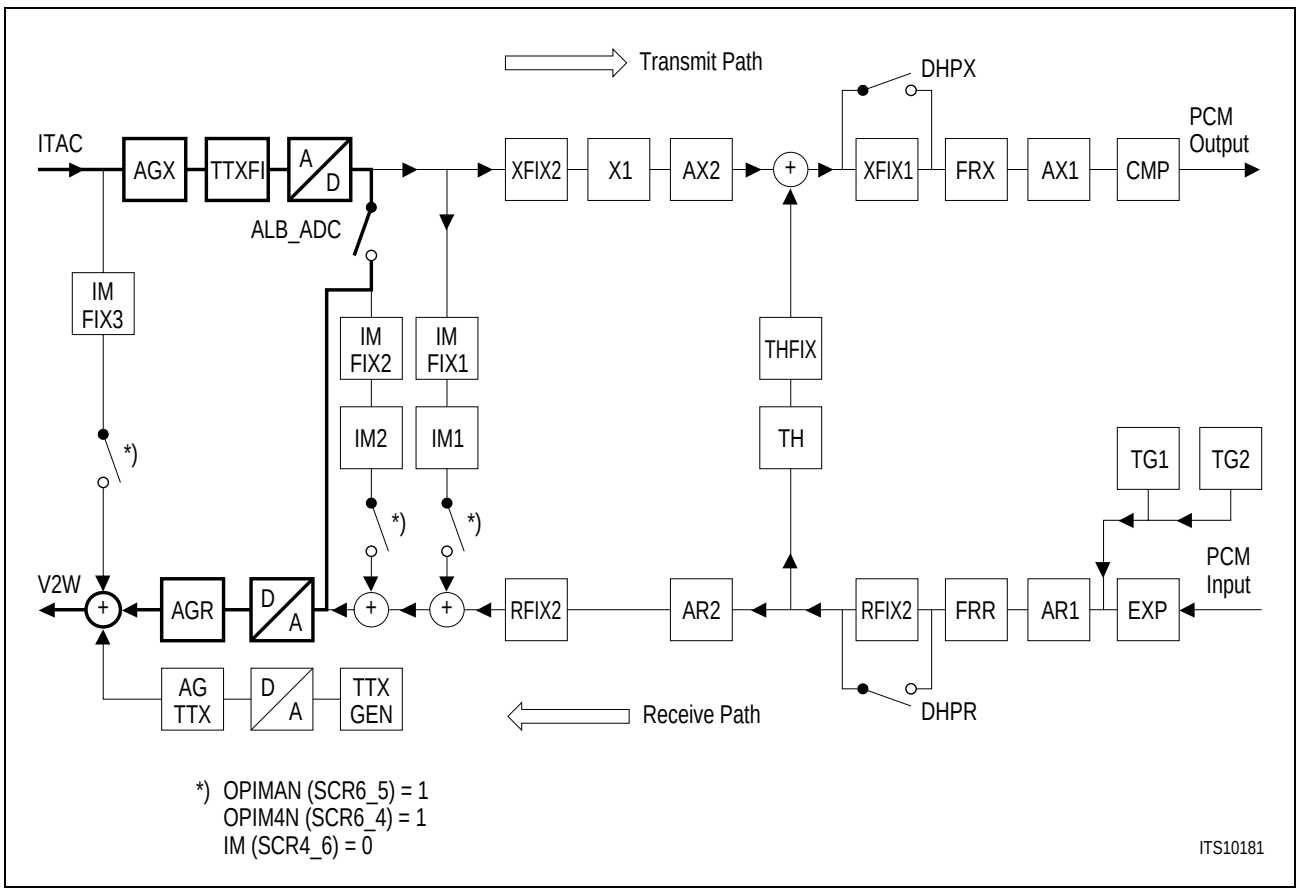



**Figure 31**

**DLB_4M**

(Digital loop up to 4 MHz)

This testloop feasibles the test of AC digital parts including DSP.

Initializing the testloop:

Reset

Store owns coefficients (generated by SLICOS)

Active Mode

Select programmed coefficients (FIXC (SCR5_5) = 0)

Open Impedance matching and Transhybrid loop
(OPIM4M (SCR6_4) = 1, IM (SCR4_6) = 0, TH (SCR4_7) = 0)

Testloop

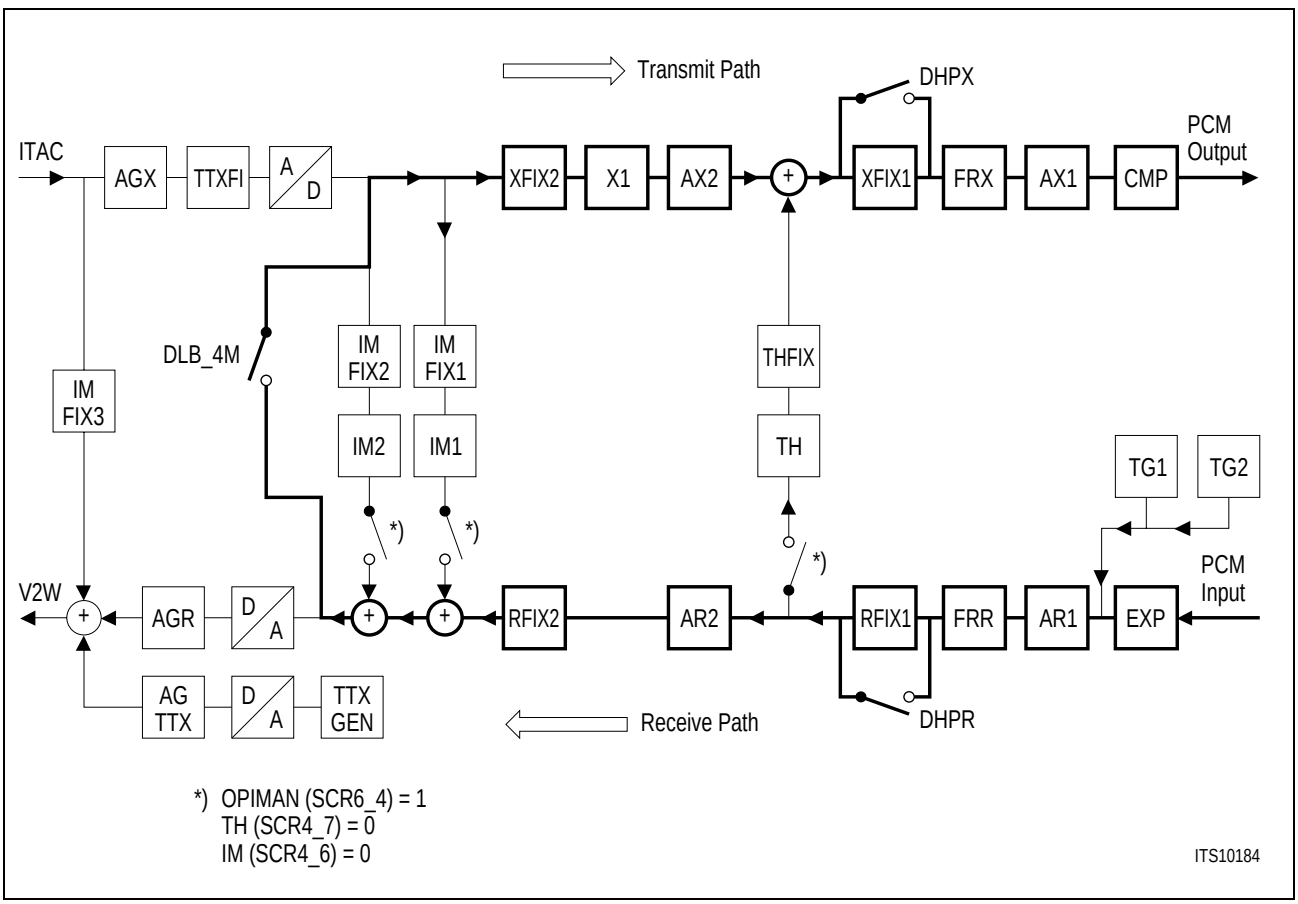



**Figure 32**

**DLB_PCM**

(Digital loop only PCM-interface)

This testloop is the basic setting after Reset and the NOT Active Mode.

It releases a shortcut between DD and DU. In Active Mode this loop can be programmed.

Initializing the testloop:

Reset

or in Active Mode:

Testloop

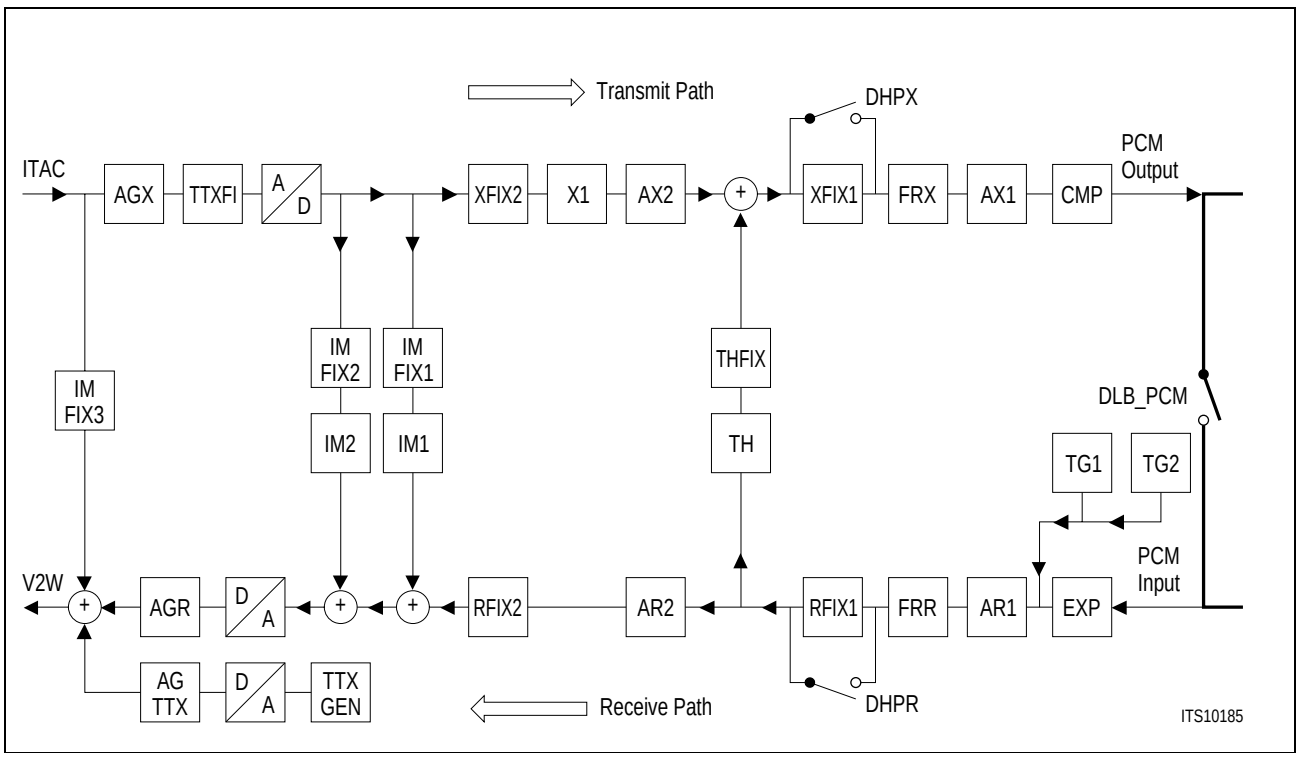



**Figure 33**

**DC_ALB**

(DC analog loop)

This testloop feasibles the test of the analog DC parts (max. frequency of the testsignal 4 kHz).

Initializing the testloop:

Reset

Active Mode

Open analog loop (OPIMAN (SCR6_5) = 1, ACDACDIS (STCR2_2) = 1)

Testloop

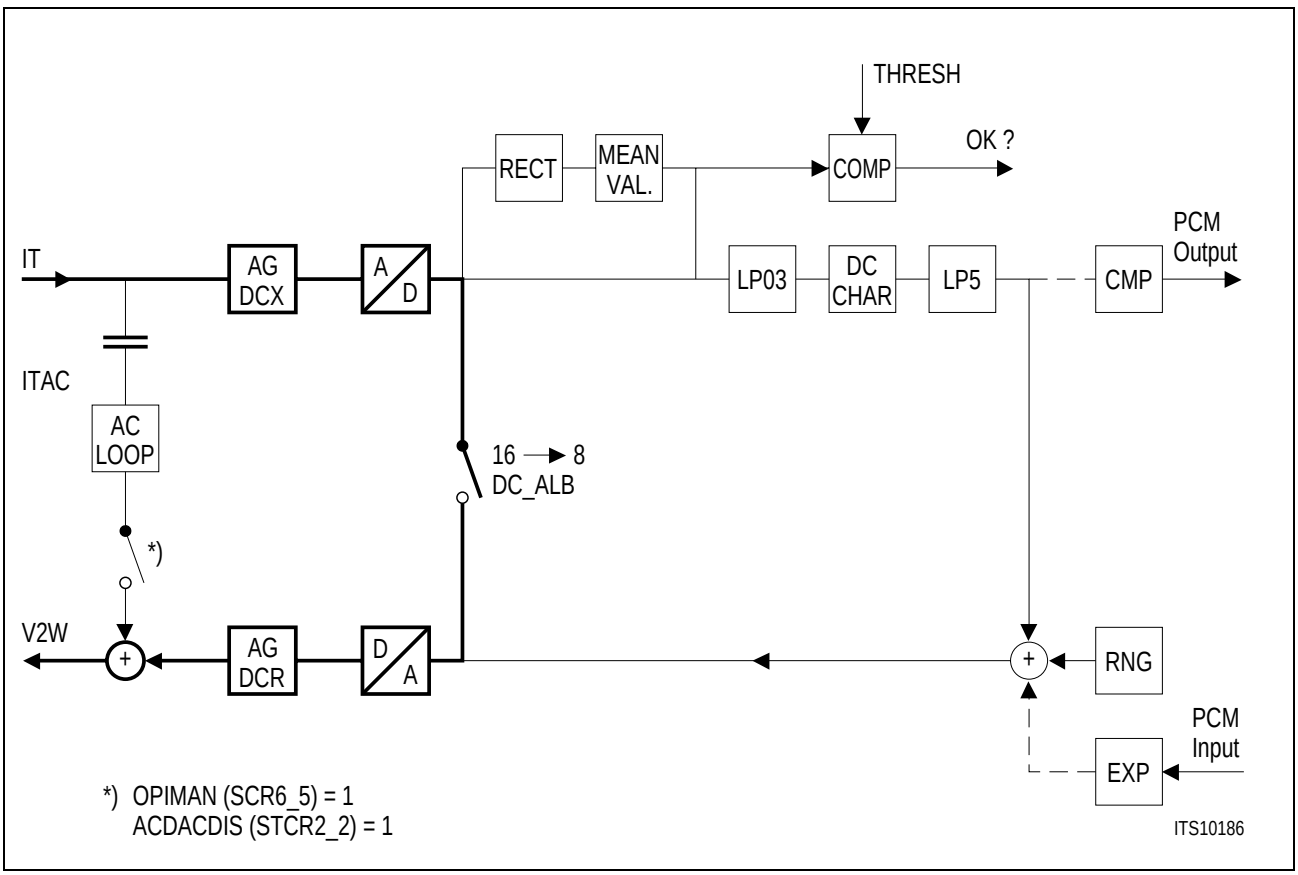



**Figure 34**

**RVP**

(Ringer voltage present)

This testloop feasibles the test of the ringer burst level.

Initializing the testloop:

Reset

Store owns coefficients and voltage level for measurement

(generated by SLICOS)

Select programmed coefficients (FIXC (SCR5_5) = 0)

Open analog loop (OPIMAN (SCR6_5) = 1, ACDACDIS (STCR2_2) = 1)

Ringing Mode, Ring Burst On (RBO) command

Testloop

Test condition is indicated in MVA (SCR2_7) and result of the comparison is stored in OKRNG (SCR2_4). The mean value can get at PCM Output, too.

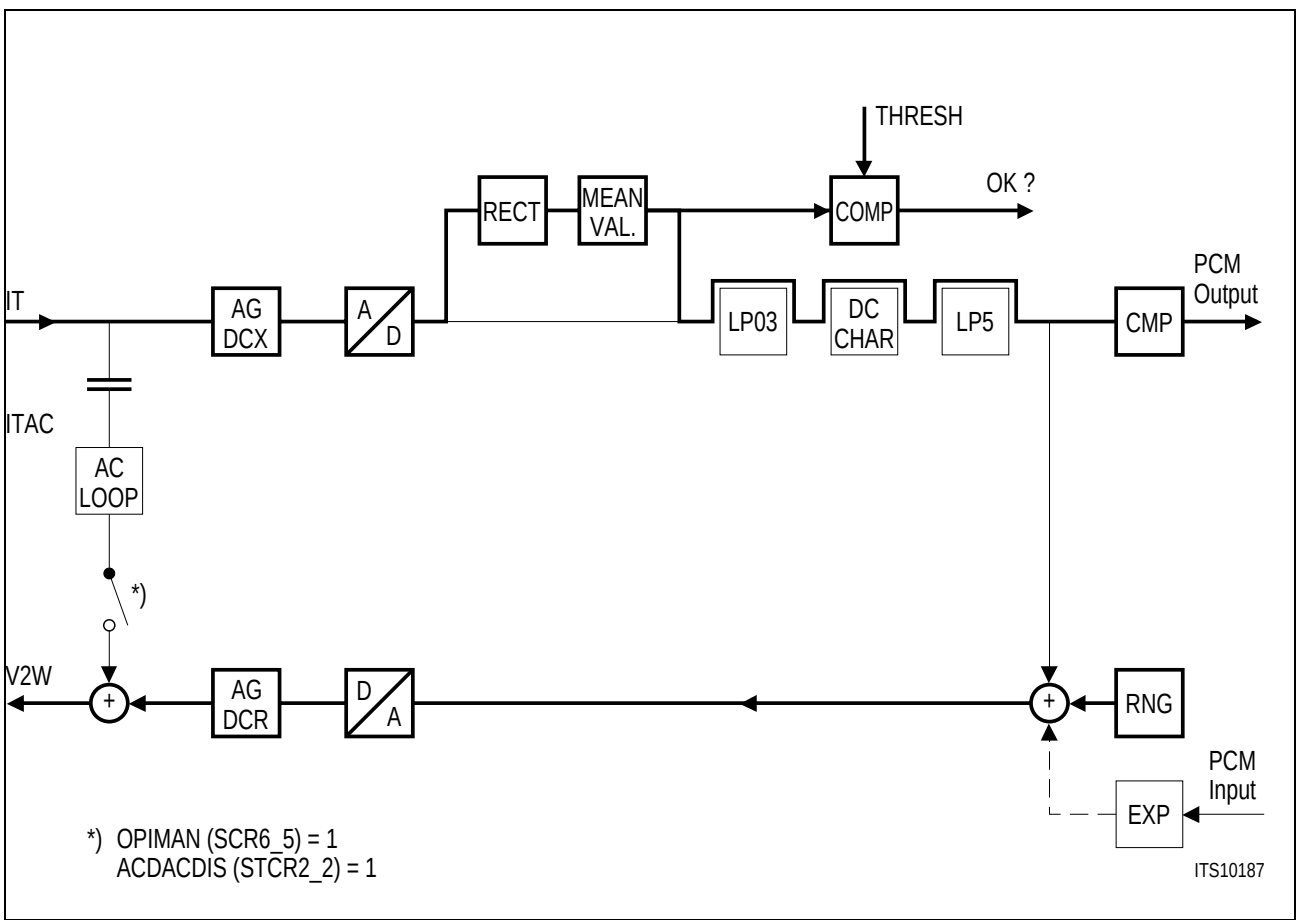



**Figure 35**

**TVP**

(Teletax voltage present)

This testloop feasibles the test of the teletax burst level which includes the test of TTX adaptation and basic functions of HV-SLIC.

Initializing the testloop:

Reset

Store owns coefficients and voltage level for measurement (generated by SLICOS)

Select programmed coefficients (FIXC (SCR5_5) = 0)

Active Mode, Teletax Burst On: TTXNO (SCR3_7) = 0

Testloop

Test condition is indicated in MVA (SCR2_7) and result of the comparison is stored in OKTTX (SCR2_5). The rectified value can get at PCM Output, too. (During the testloop the last DC value is hold.)

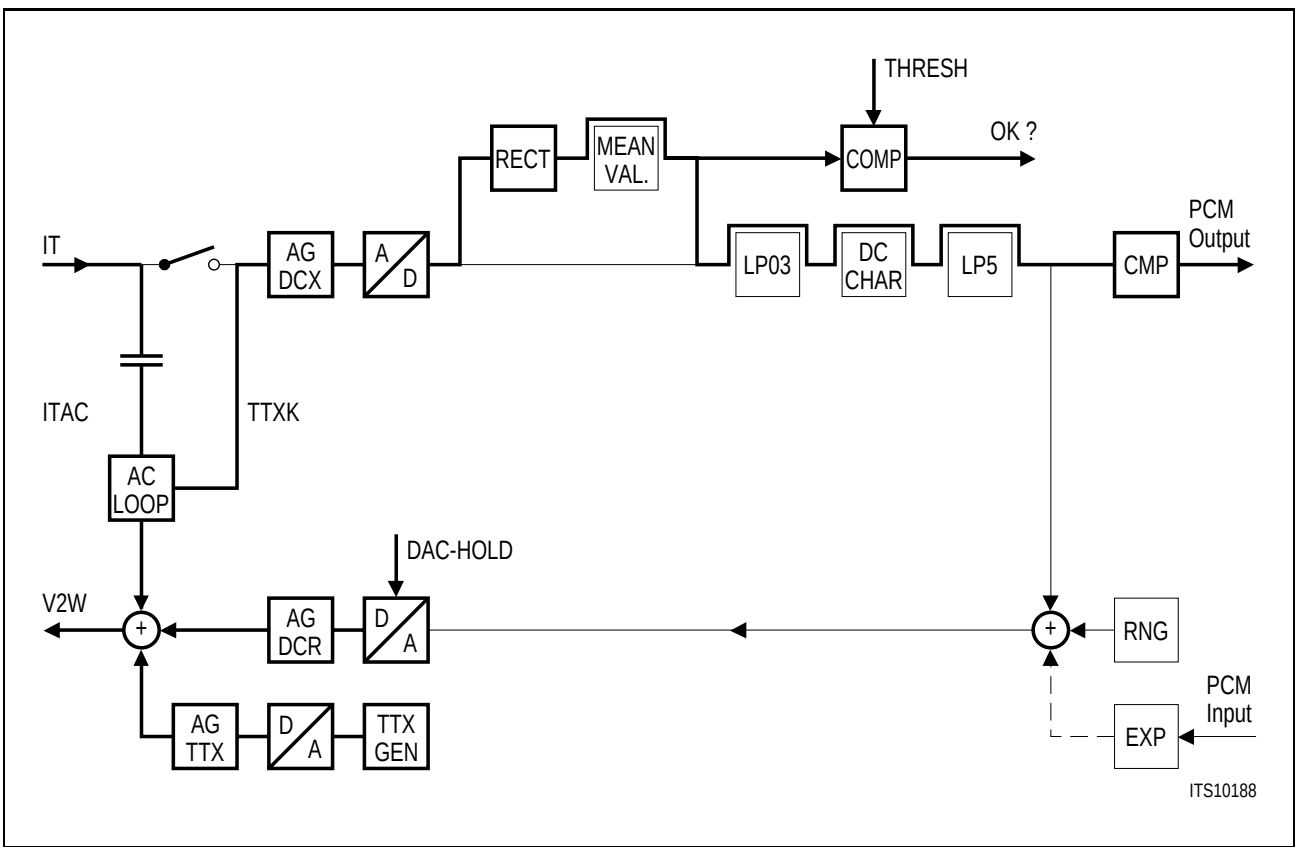



**Figure 36**

**LC**

(Loop current measurement)

This testloop feasibles a DC test of the line (shortcut, resistance, operating point) and basic function of the HV-SLIC.

Initializing the testloop:

Reset

Store owns coefficients (generated by SLICOS)

Select programmed coefficients (FIXC (SCR5_5) = 0)

Open analog loop (OPIMAN (SCR6_5) = 1, ACDACDIS (STCR2_2) = 1)

Active Mode

Testloop

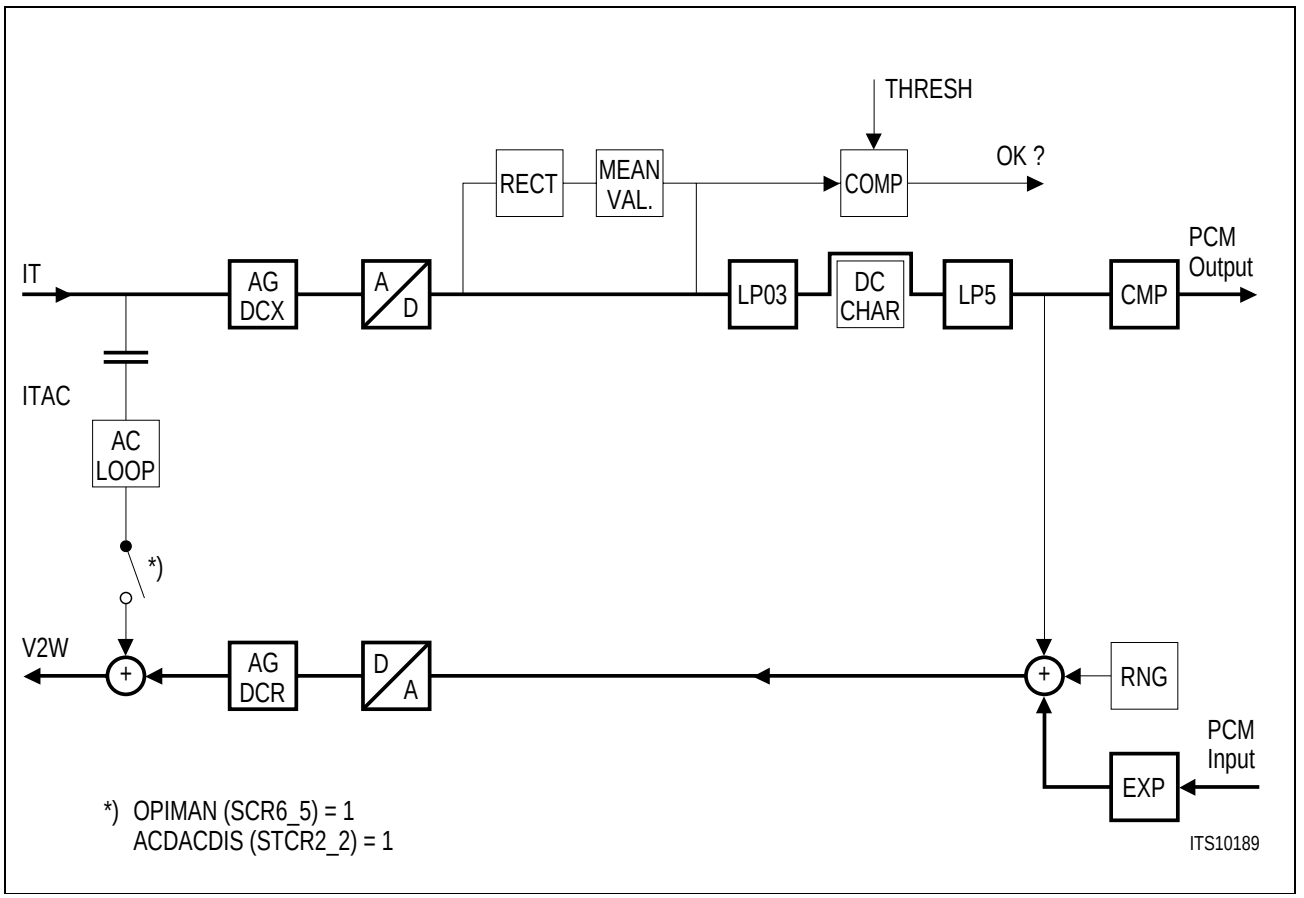



**Figure 37**

**RC**

(Ringer capacitance measurement)

This testloop feasibles the test of the line concerning the ringer.

Initializing the testloop:

Reset

Store owns coefficients (generated by SLICOS)

Select programmed coefficients (FIXC (SCR5_5) = 0)

Open analog loop (OPIMAN (SCR6_5) = 1, ACDACDIS (STCR2_2) = 1)

Ringing Mode, Ring Burst On (RBO) command

Testloop

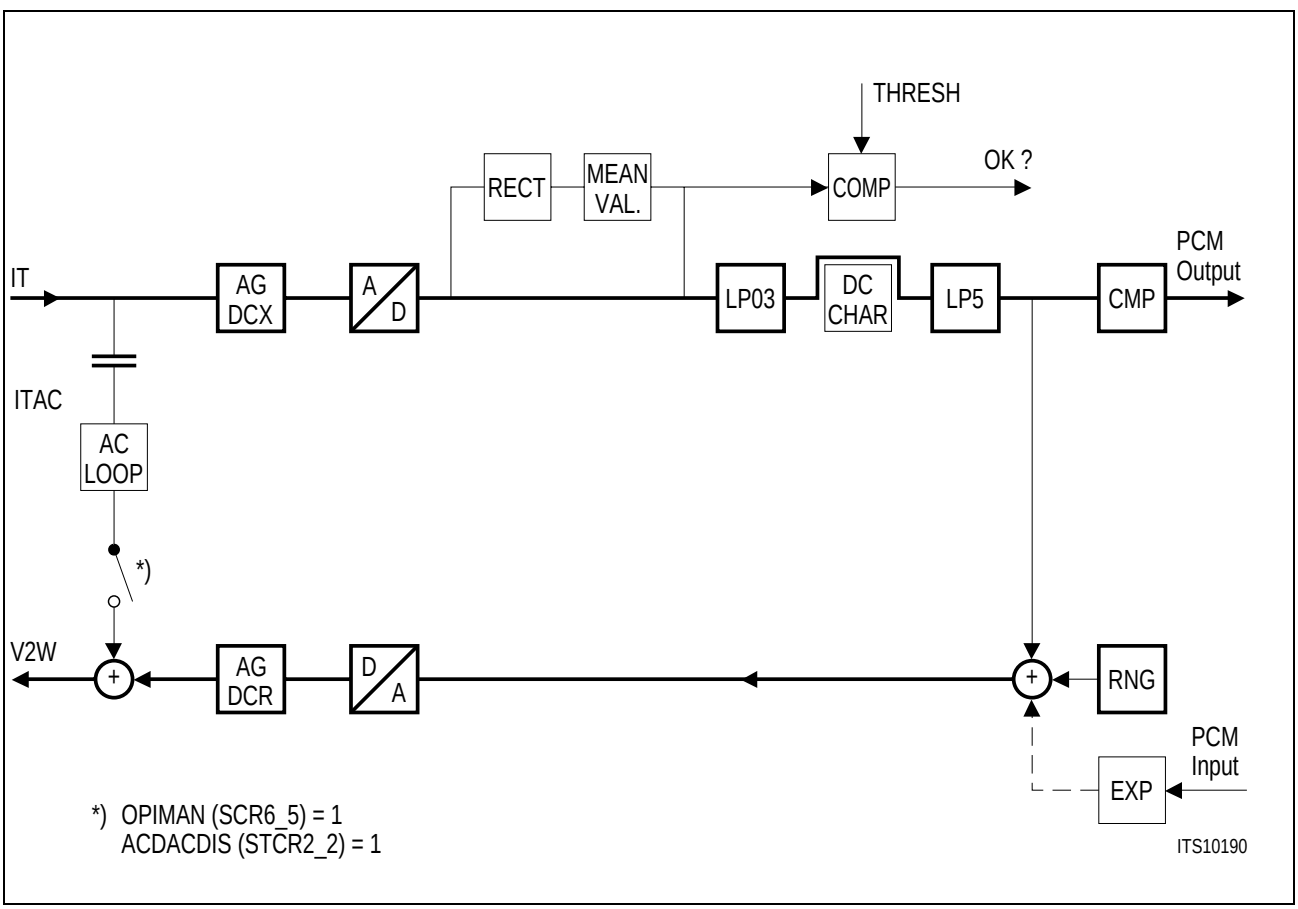



**Figure 38**

**ILT**

(Longitudinal current measurement)

This testloop feasibles the test of the line.

Initializing the testloop:

Reset

Store owns coefficients (generated by SLICOS)

Select programmed coefficients (FIXC (SCR5_5) = 0)

Open analog loop (OPIMAN (SCR6_5) = 1, ACDACDIS (STCR2_2) = 1)

Active Mode

Testloop

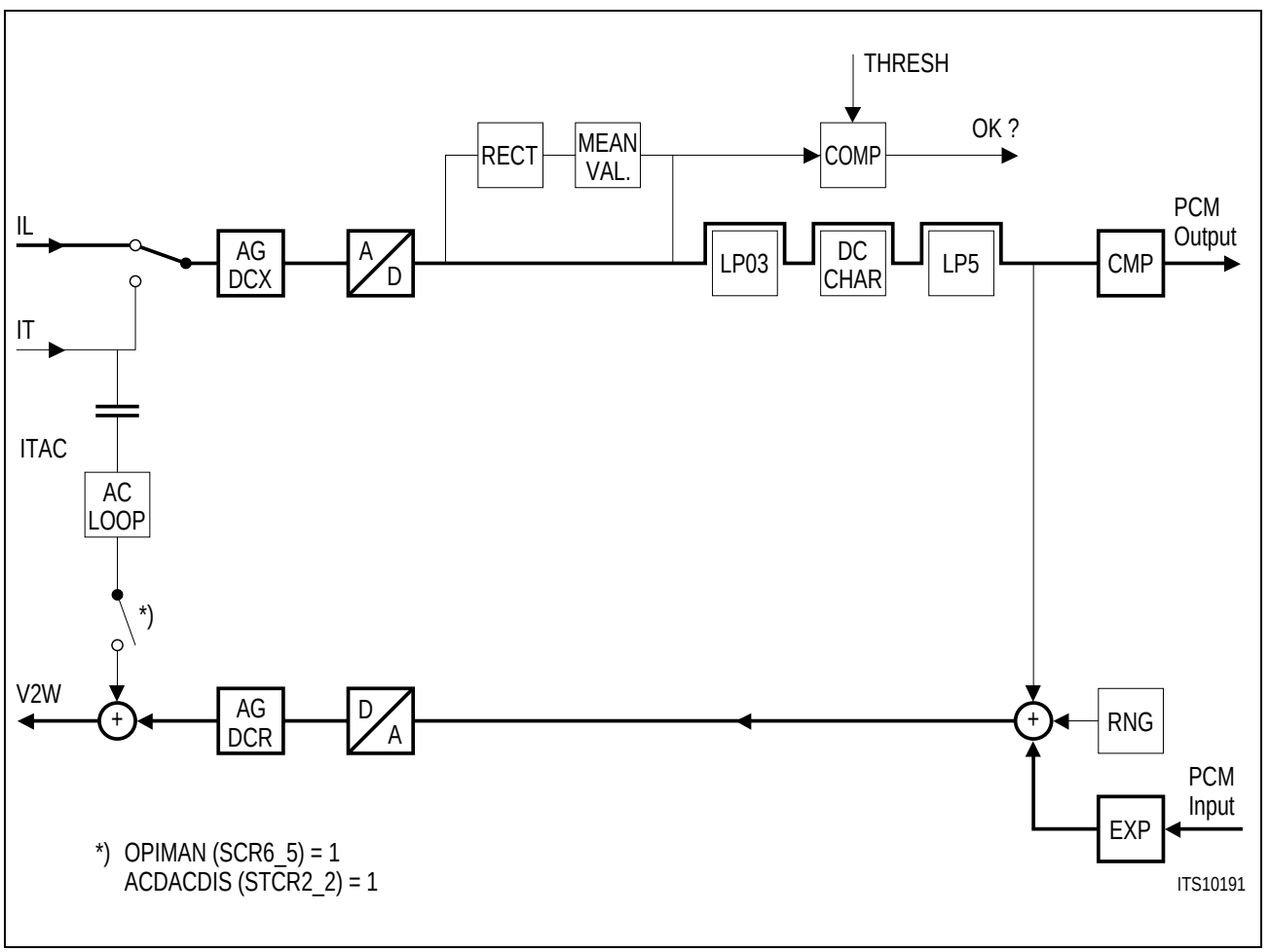



**Figure 39**

### DC_THRU (DC loop)

This testloop feasibles the test of the DC parts.

Initializing the testloop:

Reset

PDown Mode (AC-Loop disactivated)

Testloop

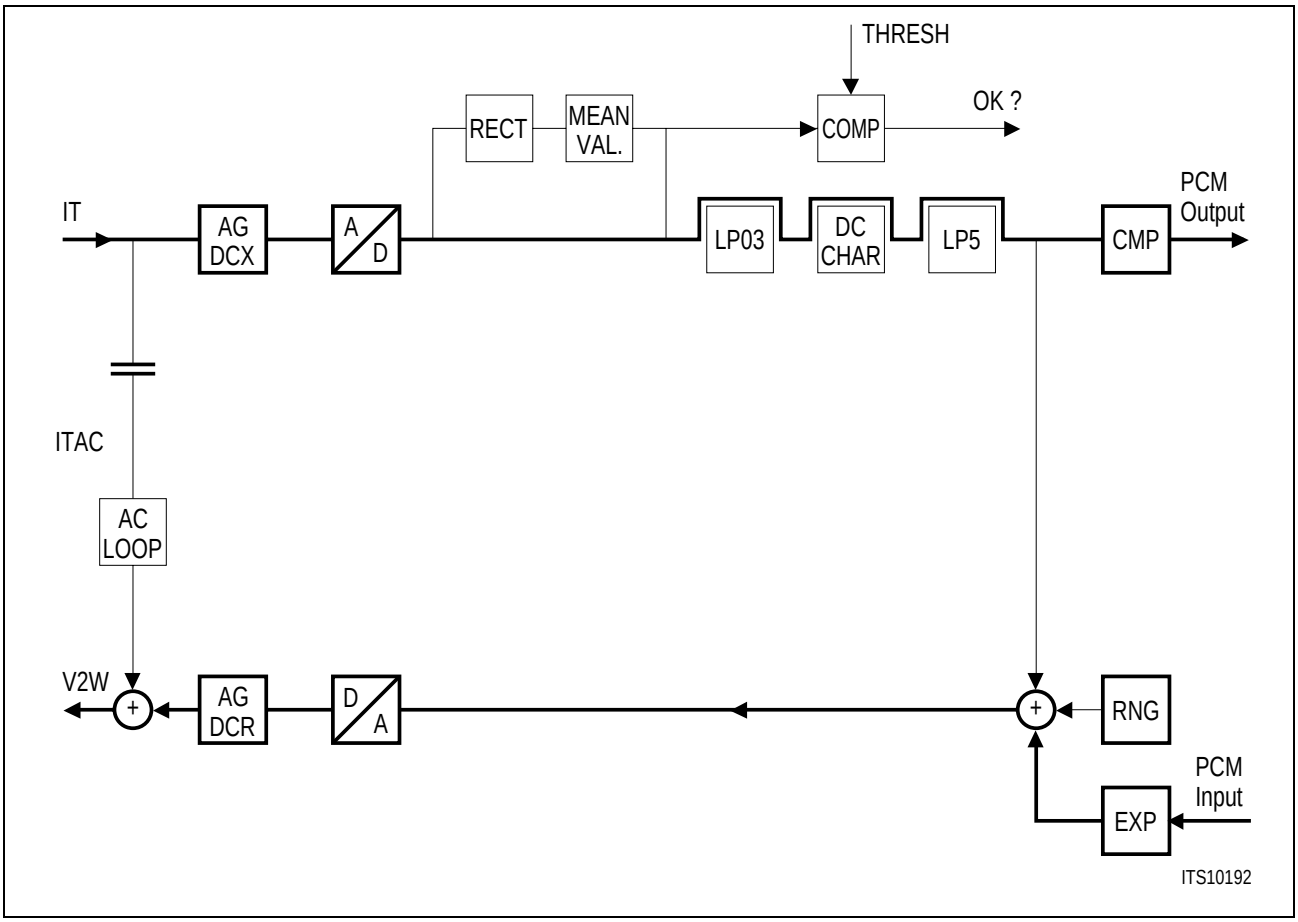



**Figure 40**

## 10.4 List of Abbreviations

| | |
|---|---|
| Act | Active Mode |
| ADC | Analog Digital Converter |
| AGDCR | Attenuation DC Receive |
| AGDCX | Attenuation DC Transmit |
| AGR | Attenuation Receive |
| AGX | Attenuation Transmit |
| AGTTX | Attenuation Teletax |
| AR | Attenuation Receive |
| ASIC | Application Specific Integrated Circuit |
| AX | Attenuation Transmit |
| | |
| BB | Boosted Battery |
| BiCMOS | Bipolar Complementary Metal Oxid Semiconductor |
| BP | Band Pass |
| | |
| C/I-DD | Channel Identification-Data Downstream |
| C/I-DU | Channel Identification-Data Upstream |
| C1, 2 | Digital Interface to HV-SLIC |
| CAP | External Capacitor to GNDA |
| CCITT | Commité Consultatif International de Telephone et Telegraph |
| CHOP | Chopper (see SCR8_6) |
| CMP | Compander |
| CODEC | Coder Decoder |
| COMP | Comparator (Testloops, Levelmetering) |
| COP | Coefficient Operation |
| CRAM | Coefficient RAM |
| | |
| DAC | Digital Analog Converter |
| DAC-HOLD | DC DAC Hold (Testloop TVP) |
| DBP | Deutsche Bundes Post |
| DCCHAR | DC Characteristic block |
| DCL | Data Clock |
| DD | Data Downstream |

| | |
|---|---|
| DHP_R | Disable Receive Highpass (SCR5_7) |
| DHP_X | Disable Transmit Highpass (SCR1_1) |
| DSP | Digital Signal Processor |
| DU | Data Upstream |
| DUP | Data Upstream Persistency Counter |
| DUPGNK | Data Upstream Persistency Counter for GNK |
| EXP | Expander |
| FRR | Frequency Response Receive Filter |
| FRX | Frequency Response Transmit Filter |
| FSC | Frame Sync. |
| GNDIT | Analog Ground |
| GNK | Ground Key |
| HV-SLIC | High Voltage Subscriber Line Interface Circuit |
| I1 | Fixed Input Pin |
| ID-L | External Identification |
| ID-M | External Identification |
| IH-H | External Identification |
| IL | Longitudinal Current Input |
| IM | Impedance Matching Filter (programmable) |
| IMFIX | Impedance Matching Filter (fixed) |
| IO | User Programmable I/O Pin |
| IOM-2-Interface | ISDN Oriented Modular Interface |
| ISDN | Integrated Service Digital Network |
| IT | Transversal Current Input (for AC and DC) |
| ITAC | Transversal Current Input (for AC) |

| | |
|---|---|
| LP03 | Low Pass 0.3 Hz |
| LP5 | Low Pass 5 Hz |
| LSSGR | Local area transport access Switching System Generic Requirements |
| MEAN VAL. | Mean Value (Testloops, Levelmetering) |
| MR | Monitor Receive |
| MX | Monitor Transmit |
| O1 | Fixed Output Pin |
| PCM | Pulse Code Modulation |
| PDen | Power Denial |
| PDN | Power Down |
| PDN | PDN Pin (Sets the HV SLIC to Power Denial) |
| POFI | Post Filter |
| PREFI | Antialiasing Pre Filter |
| RB | Ring Burst |
| RECT | Rectifier (Testloops, Levelmetering) |
| RES | Reset |
| REXT | External Ring Sync. Input |
| RFIX | Receive Filter (fixed) |
| RNG | Ring Generator |
| RREF | External Resistor to GNDA |
| SCR | Status Configuration Register |
| SEL24 | Select Data Clock 2 or 4 MHz |
| SLIC | Subscriber Line Interface Circuit |
| SLICOS | SLICOFI Oriented Software |
| SLMA | Subscriber Loop Marging |
| SLXC | Summary Line Card Outputs |
| SOP | Status Operation |
| STCR | Status Test Configuration Register |

| | |
|---|---|
| TCR | Transfer Configuration Register |
| TE 1-3 | Test Pin |
| TG | Tone Generator |
| TH | Transhybrid Balancing |
| THFIX | Transhybrid Balancing Filter (fixed) |
| THRESH | Threshhold (Testloops, Levelmetering) |
| TOP | Transfer Operation |
| TS | Time Slot |
| TS 0-2 | Time Slot selection Pin |
| TTX | Teletax |
| TTXFI | Teletax Adaptation |
| TTXGEN | Teletax Generator |

| | |
|---|---|
| $V_{2W}$ | Two Wire Output Voltage |
| $V_{BIM}$ | Battery Image Input |
| $V_{LINE1, 2}$ | Offhook-Detection in Power Denial Mode |

| | |
|---|---|
| X | Transmit Filter (programmable) |
| XFIX | Transmit Filter (fixed) |

## 11 Package Outlines

**P-LCC-44 (SMD)**
(**P**lastic **L**eaded **C**hip **C**arrier)

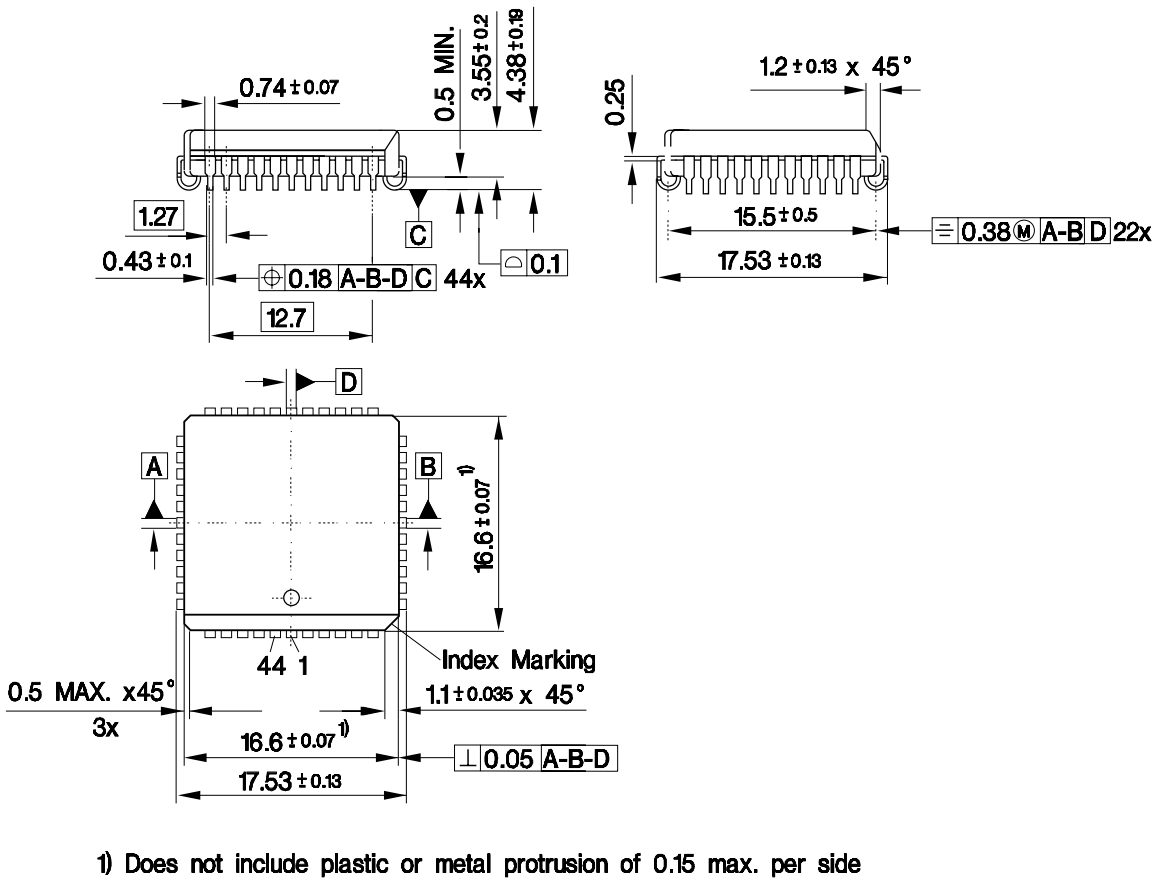



**Figure 41**

**Sorts of Packing**
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm