PCA9518A

Expandable 5-channel I²C-bus hub

Rev. 03 — 3 December 2008 Product data sheet

1. General description

The PCA9518A is a CMOS integrated circuit intended for application in I²C-bus and SMBus systems.

While retaining all the operating modes and features of the I²C-bus system, it permits extension of the I²C-bus by buffering both the data (SDA) and the clock (SCL) lines, thus enabling virtually an unlimited number of buses of 400 pF.

The I²C-bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9518A enables the system designer to divide the bus into an unlimited number of segments off of a hub where any segment to segment transition sees only one repeater delay and is multiple master capable on each segment.

Using multiple PCA9518A parts, any width hub (in multiples of five)[1] can be implemented using the expansion pins.

The PCA9518A is a wider voltage range (2.3 V to 3.6 V) version of the PCA9518 and also improves partial power-down performance, keeping I²C-bus I/O pins in high-impedance state when V_{DD} is below 2.0 V.

A PCA9518 cluster cannot be put in series with a PCA9515/16 or with another PCA9518 cluster. Multiple PCA9518 devices can be grouped with other PCA9518 devices into any size cluster thanks to the EXPxxxn pins that allow the I²C-bus signals to be sent/received from/to one PCA9518 to/from another PCA9518 within the cluster. Since there is no direction pin, slightly different ‘legal’ low voltage levels are used to avoid lock-up conditions between the input and the output of individual repeaters in the cluster. A ‘regular LOW’ applied at the input of any of the PCA9518 devices will then be propagated as a ‘buffered LOW’ with a slightly higher LOW value to all enabled outputs in the PCA9518 cluster. When this ‘buffered LOW’ is applied to a PCA9515 and PCA9516 or separate PCA9518 cluster (not connected via the EXPxxxn pins) in series, the second PCA9515 and PCA9516 or PCA9518 cluster will not recognize it as a ‘regular LOW’ and will not propagate it as a ‘buffered LOW’ again. The PCA9510/9511/9513/9514 and PCA9512 cannot be used in series with the PCA9515 and PCA9516 or PCA9518 either, but can be used in series with themselves since they use shifting instead of static offsets to avoid lock-up conditions. This note is applicable to the ‘A’ versions of these devices also.

1. Only four ports per device are available if individual Enable is required.

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2. Features

- Expandable 5 channel, bidirectional buffer
- I²C-bus and SMBus compatible
- Active HIGH individual repeater enable inputs
- Open-drain input/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode and Fast-mode I²C-bus devices and multiple masters
- Powered-off high-impedance I²C-bus pins
- Operating supply voltage range of 2.3 V to 3.6 V
- 5 V tolerant I²C-bus and enable pins
- 0 Hz to 400 kHz clock frequency[2]
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Package offerings: SO20 and TSSOP20

3. Ordering information

Table 1. Ordering information

T_{amb} = −40 °C to +85 °C

Type number	Topside mark	Package		
		Name	Description	Version
PCA9518AD	PCA9518AD	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
PCA9518APW	PA9518A	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

2. The maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.

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4. Block diagram

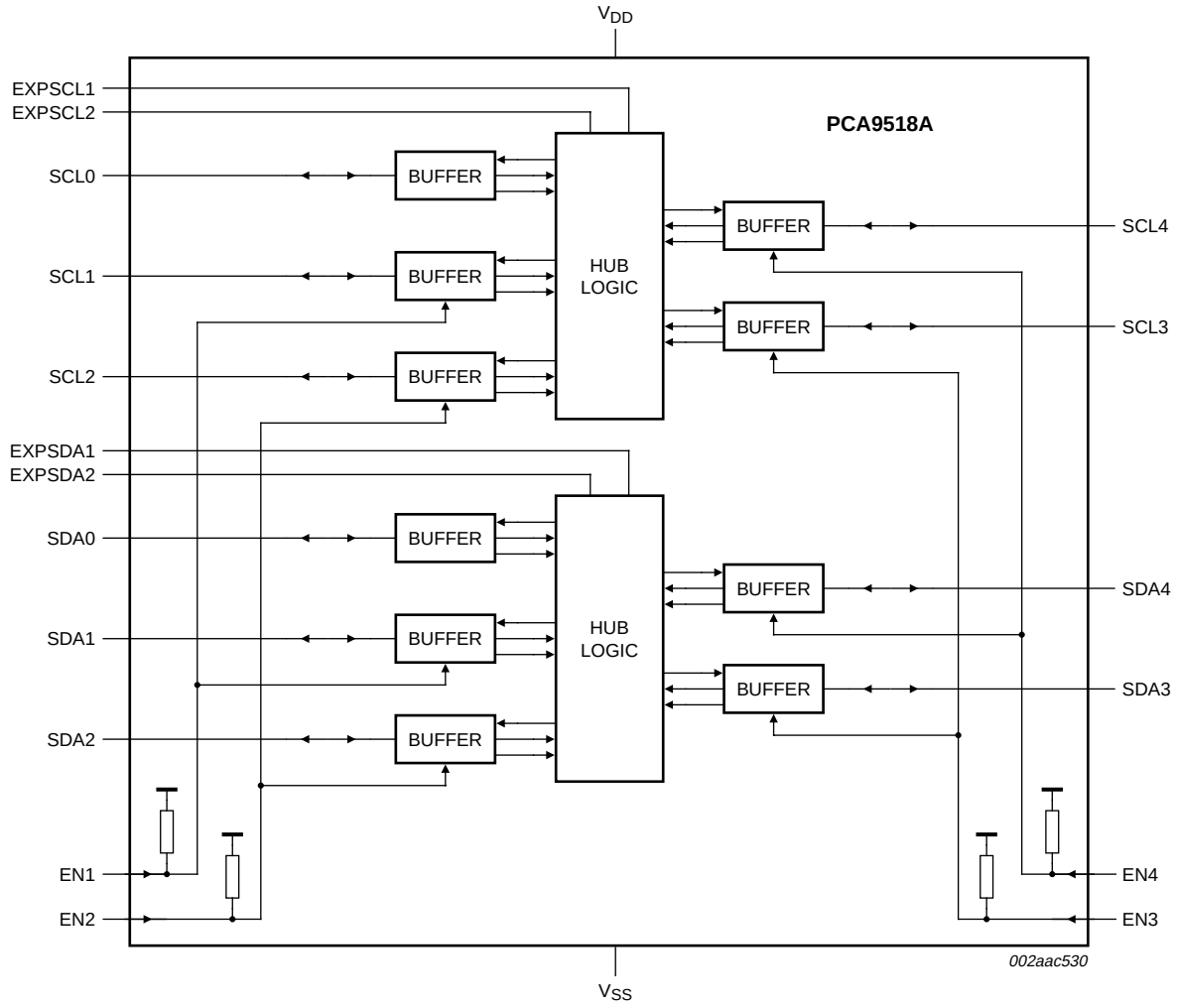

Fig 1. Block diagram of PCA9518A

A more detailed view of Figure 1 buffer is shown in Figure 2.

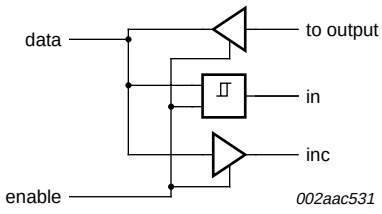

Fig 2. Buffer detail

The output pull-down voltage of each internal buffer is set for approximately 0.5 V, while the input threshold of each internal buffer is set about 0.07 V lower, when the output is internally driven LOW. This prevents a lock-up condition from occurring.

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5. Pinning information

5.1 Pinning

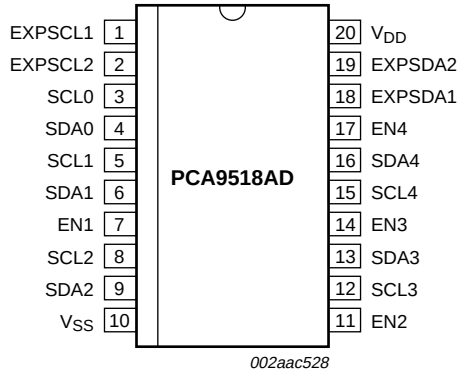

Fig 3. Pin configuration for SO20

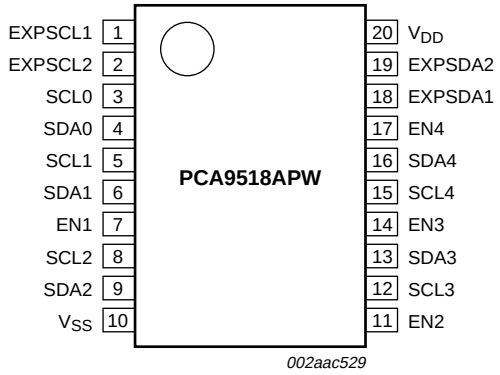

Fig 4. Pin configuration for TSSOP20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
EXPSCL1	1	expandable serial clock pin 1
EXPSCL2	2	expandable serial clock pin 2
SCL0	3	serial clock bus 0
SDA0	4	serial data bus 0
SCL1	5	serial clock bus 1
SDA1	6	serial data bus 1
EN1	7	active HIGH bus 1 enable input
SCL2	8	serial clock bus 2
SDA2	9	serial data bus 2
V_{SS}	10	supply ground
EN2	11	active HIGH bus 2 enable input
SCL3	12	serial clock bus 3
SDA3	13	serial data bus 3
EN3	14	active HIGH bus 3 enable input
SCL4	15	serial clock bus 4
SDA4	16	serial data bus 4
EN4	17	active HIGH bus 4 enable input
EXPSDA1	18	expandable serial data pin 1
EXPSDA2	19	expandable serial data pin 2
V_{DD}	20	supply voltage

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6. Functional description

The PCA9518A CMOS integrated circuit is a five-way hub repeater, which enables I²C-bus and similar bus systems to be expanded in increments of five with only one repeater delay and no functional degradation of system performance.

The PCA9518A CMOS integrated circuit contains five multi-directional, open-drain buffers specifically designed to support the standard low-level contention arbitration of the I²C-bus. Except during arbitration or clock stretching, the PCA9518A acts like a pair of non-inverting, open-drain buffers, one for SDA and one for SCL.

Refer to Figure 1 “Block diagram of PCA9518A”.

6.1 Enable

The enable pins EN1 through EN4 are active HIGH and have internal pull-up resistors. Each enable pin ENn controls its associated SDAn and SCLn ports. When LOW, the ENn pin blocks the inputs from SDAn and SCLn, as well as disabling the output drivers on the SDAn and SCLn pins. The enable pins should only change state when both the global bus and the local port are in an idle state to prevent system failures.

The active HIGH enable pins allow the use of open-drain drivers which can be wire-ORed to create a distributed enable where either centralized control signal (master) or spoke signal (sub-master) can enable the channel when it is idle.

Unused channels must have pull-up resistors unless their enable pin (ENn) is **always** LOW. Port 0 must always have pull-up resistors since it is always present in the bus and cannot be disabled.

6.2 Expansion

The PCA9518A includes 4 open-drain I/O pins used for expansion. Two expansion pins, EXPSDA1 and EXPSDA2 are used to communicate the internal state of the serial data within each hub to the other hubs. The EXPSDA1 pins of all hubs are connected together to form an open-drain bus. Similarly, all EXPSDA2 pins, EXPSCL1 pins, and all EXPSCL2 pins are connected together forming a 4-wire bus between hubs.

When it is necessary to be able to deselect every port, each expansion device only contributes 4 ports which can be enabled or disables because the fifth does not have an enable pin.

Pull-up resistors are required on the EXPxxxn[3] pins even if only one PCA9518A is used.

6.3 I²C-bus systems

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus. (Standard open-collector or open-drain configuration of the I²C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part is designed to work with Standard-mode (0 Hz to 100 kHz) and Fast-mode (0 Hz to 400 kHz) I²C-bus devices in addition to SMBus devices. Standard-mode I²C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I²C-bus system where

3. ‘xxxn’ is SDA1, SDA2, SCL1 or SCL2. ‘xxx’ is SDA or SCL.

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Standard-mode devices and multiple masters are possible. Please see application note *AN255, I²C/SMBus Repeaters, Hubs and Expanders* for additional information on sizing resistors.

7. Application design-in information

A typical application is shown in Figure 5. In this example, the system master is running on a 3.3 V I²C-bus while the slaves are connected to a 3.3 V or 5 V bus. All buses run at 100 kHz unless slave 3, slave 4 and slave 5 are isolated from the bus. Then the master bus and slave 1, slave 2 and slave 6 can run at 400 kHz.

Any segment of the hub can talk to any other segment of the hub. Bus masters and slaves can be located on any segment with 400 pF load allowed on each segment.

The PCA9518A is 5 V tolerant, so it does not require any additional circuitry to translate between the different bus voltages.

When one port of the PCA9518A is pulled LOW by a device on the I²C-bus, a CMOS hysteresis type input detects the falling edge and drives the EXPxxx1 line LOW, when the EXPxxx1 voltage is less than $0.5V_{DD}$, the other ports are pulled down to the V_{OL} of the PCA9518A which is typically 0.5 V.

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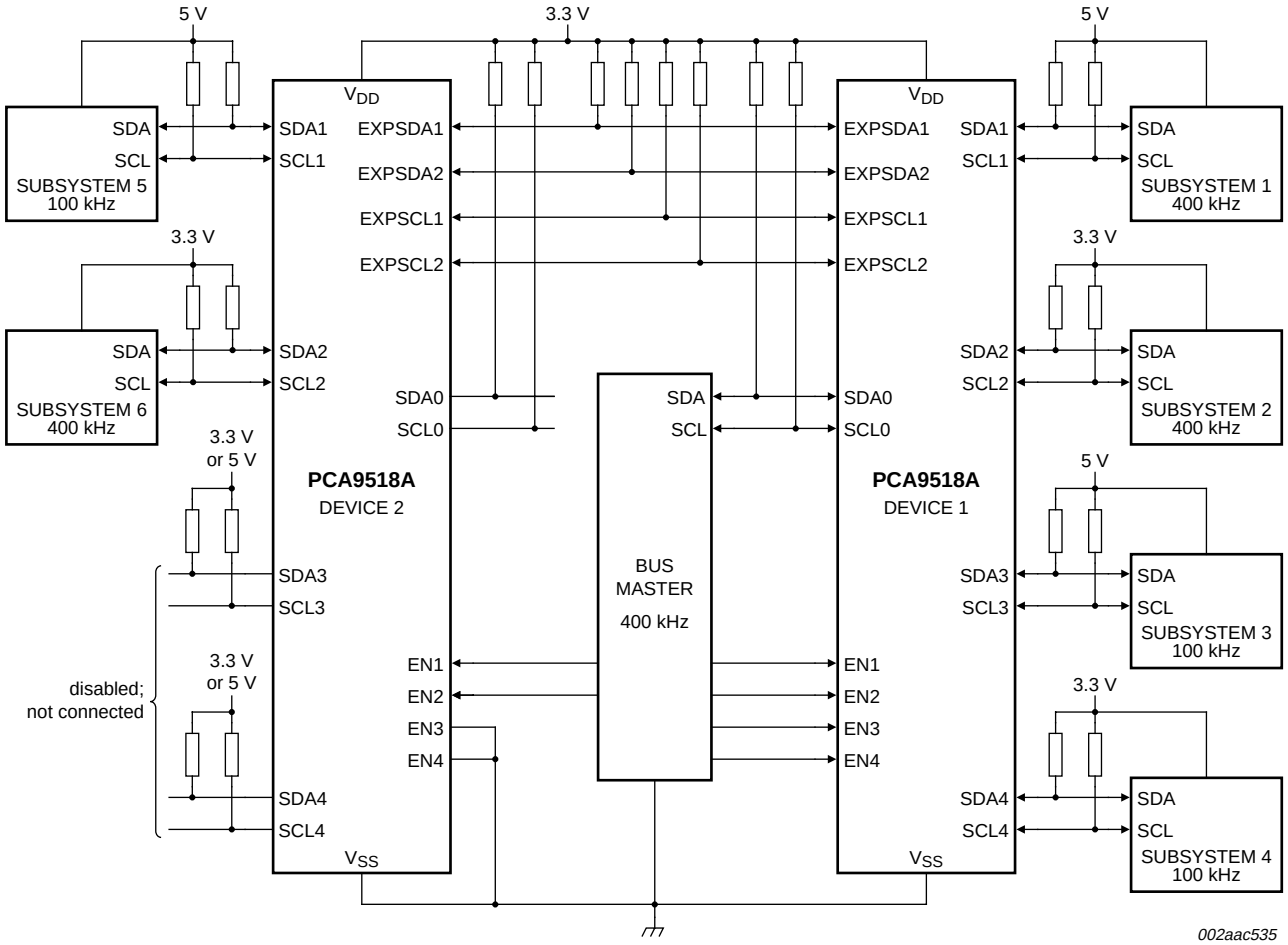

Only two of the five channels on the PCA9518A Device 2 are being used. EN3 and EN4 are connected to V_{SS} to disable channels 3 and 4 and/or SDA3/SCL3 and SDA4/SCL4 are pulled up to V_{DD}. SDA0 and SCL0 can be used as a normal I²C-bus port, but if unused then it must be pulled up to V_{DD} since there is no enable pin.

The pull-ups shown on Device 2 channels 3 and 4 are not required if their enable pins (ENn) are permanently held LOW.

Fig 5. Typical application: multiple expandable 5-channel I²C-bus hubs

In order to illustrate what would be seen in a typical application, refer to Figure 6. If the bus master in Figure 5 were to write to the slave through the PCA9518A, we would see the waveform shown in Figure 6. This looks like a normal I²C-bus transmission except for the small foot preceding each clock LOW-to-HIGH transition and proceeding each data LOW-to-HIGH transition for the master. The foot height is the difference between the LOW level driven by the master and the higher voltage LOW level driven by the PCA9518A repeater. Its width corresponds to an effective clock stretching coming from the PCA9518A that delays the rising edge of the clock. That same magnitude of delay is seen on the rising edge of the data. The foot on the rising edge of the data is extended through the 9th clock pulse as the PCA9518A repeats the acknowledge from the slave to the master. The clock of the slave looks normal except the V_{OL} is the ~0.5 V level generated by the PCA9518A. The SDA at the slave has a particularly interesting shape during the 9th clock cycle where the slave pulls the line below the value driven by the PCA9518A during

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the acknowledge and then returns to the PCA9518A level creating a foot before it completes the LOW-to-HIGH transition. SDA lines other than the one with the master and the one with the slave have a uniform LOW level driven by the PCA9518A repeater.

The other four waveforms are the expansion bus signals and are included primarily for timing reference points. All timing on the expansion bus is with respect to $0.5V_{DD}$. EXPSDA1 is the expansion bus that is driven LOW whenever any SDA pin falls below $0.3V_{DD}$. EXPSDA2 is the expansion bus that is driven LOW whenever any pin is ≤0.4 V. EXPSCL1 is the expansion bus that is driven LOW whenever any SCL pin falls below $0.3V_{DD}$. EXPSCL2 is the expansion bus that is driven LOW whenever any SCL pin is ≤0.4 V. The EXPSDA2 returns HIGH after the SDA pin that was the last one being held below 0.4 V by an external driver starts to rise. The last SDA to rise above 0.4 V is held down by the PCA9518A to ~0.5 V until after the delay of the circuit which determines that it was the last to rise, then it is allowed to rise above the ~0.5 V level driven by the PCA9518A. Considering the bus 0 SDA to be the last one to go above 0.4 V, then the EXPSDA1 returns to HIGH after the EXPSDA2 is HIGH and either the bus 0 SDA rise time is 1 µs or, when the bus 0 SDA reaches $0.7V_{DD}$, whichever occurs first. After both EXPSDA2 and EXPSDA1 are HIGH the rest of the SDA lines are allowed to rise. The same description applies for the EXPSCL1, EXPSCL2, and SCL pins.

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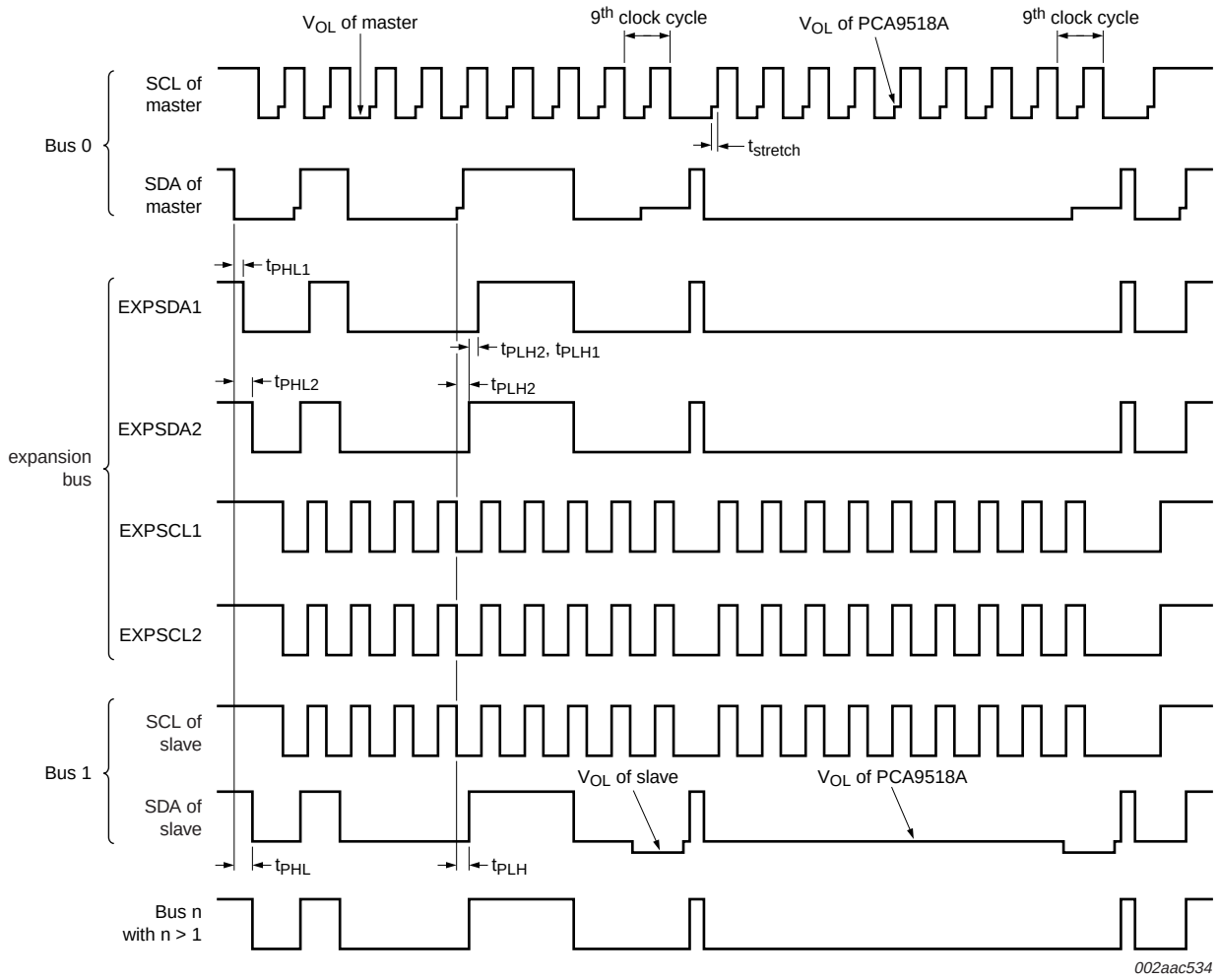

Fig 6. Bus waveforms

It is important to note that any arbitration or clock stretching events on Bus 1 require that the V_{OL} of the devices on Bus 1 be 70 mV below the V_{OL} of the PCA9518A (see V_{OL}–V_{ILc} in the Section 9 “Static characteristics”) to be recognized by the PCA9518A and then transmitted to Bus 0.

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8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage	V_{DD} to V_{SS}	[1]	–0.5	+6	V
$V_{I2C\text{-}bus}$	I²C-bus voltage	SCL or SDA	[1]	–0.5	+6	V
I_I	input current	any pin		-	50	mA
P_{tot}	total power dissipation			-	300	mW
T_{stg}	storage temperature			–55	+125	°C
T_{amb}	ambient temperature	operating		–40	+85	°C

[1] Voltages with respect to pin V_{SS}.

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9. Static characteristics

Table 4. Static characteristics

V_{DD} = 3.0 V to 3.6 V[1]; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			3.0	3.3	3.6	V
I_{CCH}	HIGH-level supply current	both channels HIGH V_{DD} = 3.6 V; SDAn = SCLn = V_{DD}		-	7.5	10	mA
I_{CCL}	LOW-level supply current	both channels LOW V_{DD} = 3.6 V; one SDA and one SCL = V_{SS}; other SDA and SCL open		-	9	11	mA
I_{CCLc}	contention LOW-level supply current	V_{DD} = 3.6 V; SDAn = SCLn = V_{SS}		-	9	11	mA
Input SCL; input/output SDA							
V_{IH}	HIGH-level input voltage	SCL, SDA		0.7V_{DD}	-	5.5	V
V_{IL}	LOW-level input voltage	SCL, SDA	[2]	−0.5	-	+0.25V_{DD}	V
V_{ILc}	contention LOW-level input voltage	SCL, SDA	[3]	−0.5	-	+0.4	V
V_{IK}	input clamping voltage	I_I = −18 mA		-	-	−1.2	V
I_{LI}	input leakage current	V_I = 3.6 V		-	-	±1	µA
I_{IL}	LOW-level input current	SCL, SDA; V_I = 0.2 V		-	-	20	µA
V_{OL}	LOW-level output voltage	I_{OL} = 20 µA or 6 mA		0.45	0.52	0.6	V
V_{OL}−V_{ILc}	difference between LOW-level output and LOW-level input voltage contention	guaranteed by design		-	-	70	mV
C_i	input capacitance	V_I = 3 V or 0 V		-	6	8	pF
Enable 1 to Enable 4 (EN1 to EN4)							
V_{IH}	HIGH-level input voltage			2.0	-	5.5	V
V_{IL}	LOW-level input voltage			−0.5	-	+0.8	V
I_{IL}	LOW-level input current	V_I = 0.2 V; EN1 to EN4		-	10	30	µA
I_{LI}	input leakage current			−1	-	+1	µA
C_i	input capacitance	V_I = 3.0 V or 0 V		-	3	7	pF
Expansion pins (EXPSCL1, EXPSCL2, EXPSDA1, EXPSDA2)							
V_{IH}	HIGH-level input voltage	EXPxxxn		0.6V_{DD}	-	5.5	V
V_{IL}	LOW-level input voltage	EXPxxxn		−0.5	-	+0.4V_{DD}	V
I_{IL}	LOW-level input current	V_I = 0.2 V; EXPxxxn		-	-	5	µA
V_{OL}	LOW-level output voltage	I_{OL} = 12 mA		-	-	0.5	V
C_i	input capacitance	V_I = 3.0 V or 0 V		-	6	8	pF

[1] For operation between published voltage ranges, refer to worst-case parameter in both ranges.

[2] V_{IL} specification is for the first LOW level seen by the SDAn/SCLn lines.

[3] V_{ILc} is for the second and subsequent LOW levels seen by the SDAn/SCLn lines.

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Table 5. Static characteristics

V_{DD} = 2.3 V to 2.7 V[1]; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			2.3	2.5	2.7	V
I_{CCH}	HIGH-level supply current	both channels HIGH V_{DD} = 2.7 V; SDAn = SCLn = V_{DD}		-	7.5	10	mA
I_{CCL}	LOW-level supply current	both channels LOW V_{DD} = 2.7 V; one SDA and one SCL = V_{SS}; other SDA and SCL open		-	9	11	mA
I_{CCLc}	contention LOW-level supply current	V_{DD} = 2.7 V; SDAn = SCLn = V_{SS}		-	9	11	mA
Input SCL; input/output SDA							
V_{IH}	HIGH-level input voltage	SCL, SDA		0.7V_{DD}	-	5.5	V
V_{IL}	LOW-level input voltage	SCL, SDA	[2]	−0.5	-	+0.25V_{DD}	V
V_{ILc}	contention LOW-level input voltage	SCL, SDA	[3]	−0.5	-	+0.4	V
V_{IK}	input clamping voltage	I_I = −18 mA		-	-	−1.2	V
I_{LI}	input leakage current	V_I = 2.7 V		-	-	±1	µA
I_{IL}	LOW-level input current	SCL, SDA; V_I = 0.2 V		-	-	20	µA
V_{OL}	LOW-level output voltage	I_{OL} = 20 µA or 6 mA		0.45	0.52	0.6	V
V_{OL}−V_{ILc}	difference between LOW-level output and LOW-level input voltage contention	guaranteed by design		-	-	70	mV
C_i	input capacitance	V_I = 3 V or 0 V		-	6	8	pF
Enable 1 to Enable 4 (EN1 to EN4)							
V_{IH}	HIGH-level input voltage			2.0	-	5.5	V
V_{IL}	LOW-level input voltage			−0.5	-	+0.8	V
I_{IL}	LOW-level input current	V_I = 0.2 V; EN1 to EN4		-	10	30	µA
I_{LI}	input leakage current			−1	-	+1	µA
C_i	input capacitance	V_I = 2.3 V or 0 V		-	3	7	pF
Expansion pins (EXPSCL1, EXPSCL2, EXPSDA1, EXPSDA2)							
V_{IH}	HIGH-level input voltage	EXPxxxn		0.6V_{DD}	-	5.5	V
V_{IL}	LOW-level input voltage	EXPxxxn		−0.5	-	+0.4V_{DD}	V
I_{IL}	LOW-level input current	V_I = 0.2 V; EXPxxxn		-	-	5	µA
V_{OL}	LOW-level output voltage	I_{OL} = 12 mA		-	-	0.5	V
C_i	input capacitance	V_I = 2.3 V or 0 V		-	6	8	pF

[1] For operation between published voltage ranges, refer to worst-case parameter in both ranges.

[2] V_{IL} specification is for the first LOW level seen by the SDAn/SCLn lines.

[3] V_{ILc} is for the second and subsequent LOW levels seen by the SDAn/SCLn lines.

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10. Dynamic characteristics

Table 6. Dynamic characteristics

V_{DD} = 3.0 V to 3.6 V[1]; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	SDA to SDAn, or SCL to SCLn; Figure 7	[2][3]	105	202	389	ns
t_{PLH}	LOW to HIGH propagation delay	SDA to SDAn, or SCL to SCLn; Figure 7	[2][4]	110	259	265	ns
t_{PHL1}	HIGH to LOW propagation delay 1	EXPSDA1 to SDA, or EXPSCL1 to SCL; Figure 7		109	193	327	ns
t_{PLH1}	LOW to HIGH propagation delay 1	EXPSDA1 to SDA, or EXPSCL1 to SCL; Figure 7		130	153	179	ns
t_{PLH2}	LOW to HIGH propagation delay 2	EXPSDA2 to SDA, or EXPSCL2 to SCL; Figure 7		160	234	279	ns
t_{THL}	HIGH to LOW output transition time	SDA, SCL; Figure 7		58	110	187	ns
t_{TLH}	LOW to HIGH output transition time	SDA, SCL; Figure 7		-	0.85 RC	-	ns
t_{su}	set-up time	enable to START condition		300	-	-	ns
t_h	hold time	enable after STOP condition		300	-	-	ns

[1] For operation between published voltage ranges, refer to worst-case parameter in both ranges.

[2] The SDA and SCL propagation delays are dominated by rise times or fall times. The fall times are mostly internally controlled and are only sensitive to load capacitance. The rise times are RC time constant controlled and therefor a specific numerical value can only be given for fixed RC time constants.

[3] The SDA HIGH to LOW propagation delay includes the fall time from V_{DD} to $0.5V_{DD}$ of the EXPSDA1 or EXPSCL1 pins and the SDA or SCL fall time from the quiescent HIGH (usually V_{DD}) to below $0.3V_{DD}$. The SDA and SCL outputs have edge rate control circuits included which make the fall time almost independent of load capacitance.

[4] The SDA or SCL LOW to HIGH propagation delay includes the rise time constant from the quiescent LOW to $0.5V_{DD}$ for the EXPSDA1 or EXPSCL2, the rise time constant for the quiescent LOW to $0.5V_{DD}$ for the EXPSDA1 or EXPSCL1, and the rise time constant from the quiescent external driven LOW to $0.7V_{DD}$ for the SDA or SCL output. All of these rise times are RC time constants determined by the external resistance and total capacitance for the various nodes.

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Table 7. Dynamic characteristics

V_{DD} = 2.3 V to 2.7 V[1]; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	SDA to SDAn, or SCL to SCLn; Figure 7	[2][3]	105	202	389	ns
t_{PLH}	LOW to HIGH propagation delay	SDA to SDAn, or SCL to SCLn; Figure 7	[2][4]	110	259	265	ns
t_{PHL1}	HIGH to LOW propagation delay 1	EXPSDA1 to SDA, or EXPSCL1 to SCL; Figure 7		109	193	327	ns
t_{PLH1}	LOW to HIGH propagation delay 1	EXPSDA1 to SDA, or EXPSCL1 to SCL; Figure 7		130	153	179	ns
t_{PLH2}	LOW to HIGH propagation delay 2	EXPSDA2 to SDA, or EXPSCL2 to SCL; Figure 7		160	234	279	ns
t_{THL}	HIGH to LOW output transition time	SDA, SCL; Figure 7		58	110	187	ns
t_{TLH}	LOW to HIGH output transition time	SDA, SCL; Figure 7		-	0.85 RC	-	ns
t_{su}	set-up time	enable to START condition		300	-	-	ns
t_h	hold time	enable after STOP condition		300	-	-	ns

[1] For operation between published voltage ranges, refer to worst-case parameter in both ranges.

[2] The SDA and SCL propagation delays are dominated by rise times or fall times. The fall times are mostly internally controlled and are only sensitive to load capacitance. The rise times are RC time constant controlled and therefor a specific numerical value can only be given for fixed RC time constants.

[3] The SDA HIGH to LOW propagation delay includes the fall time from V_{DD} to $0.5V_{DD}$ of the EXPSDA1 or EXPSCL1 pins and the SDA or SCL fall time from the quiescent HIGH (usually V_{DD}) to below $0.3V_{DD}$. The SDA and SCL outputs have edge rate control circuits included which make the fall time almost independent of load capacitance.

[4] The SDA or SCL LOW to HIGH propagation delay includes the rise time constant from the quiescent LOW to $0.5V_{DD}$ for the EXPSDA1 or EXPSCL2, the rise time constant for the quiescent LOW to $0.5V_{DD}$ for the EXPSDA1 or EXPSCL1, and the rise time constant from the quiescent external driven LOW to $0.7V_{DD}$ for the SDA or SCL output. All of these rise times are RC time constants determined by the external resistance and total capacitance for the various nodes.

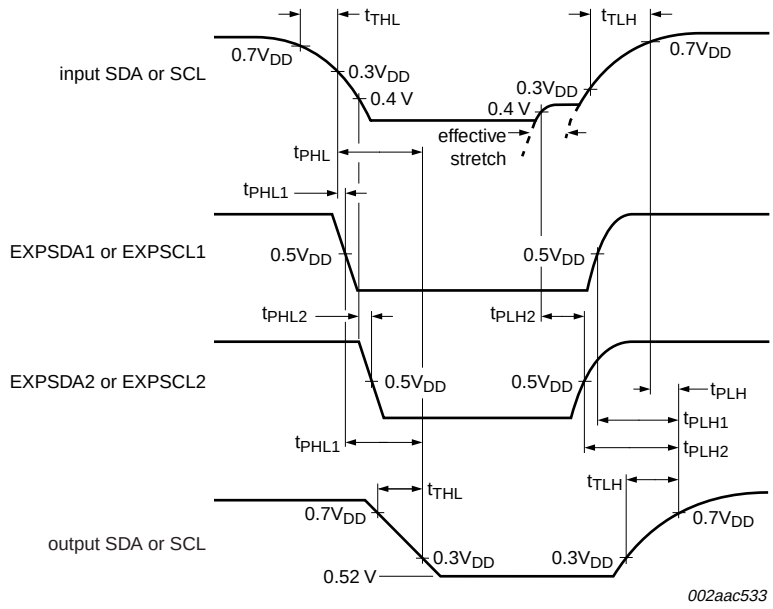

Fig 7. AC waveforms

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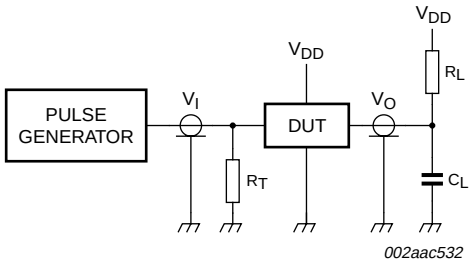
11. Test information



R_L = load resistor; 1.1 kΩ for I²C-bus, and 500 Ω for EXPxxxn.

C_L = load capacitance includes jig and probe capacitance; 100 pF for I²C-bus, and 100 pF for EXPxxxn.

R_T = termination resistance should be equal to Z_o of the pulse generators.

Fig 8. Test circuit for open-drain outputs

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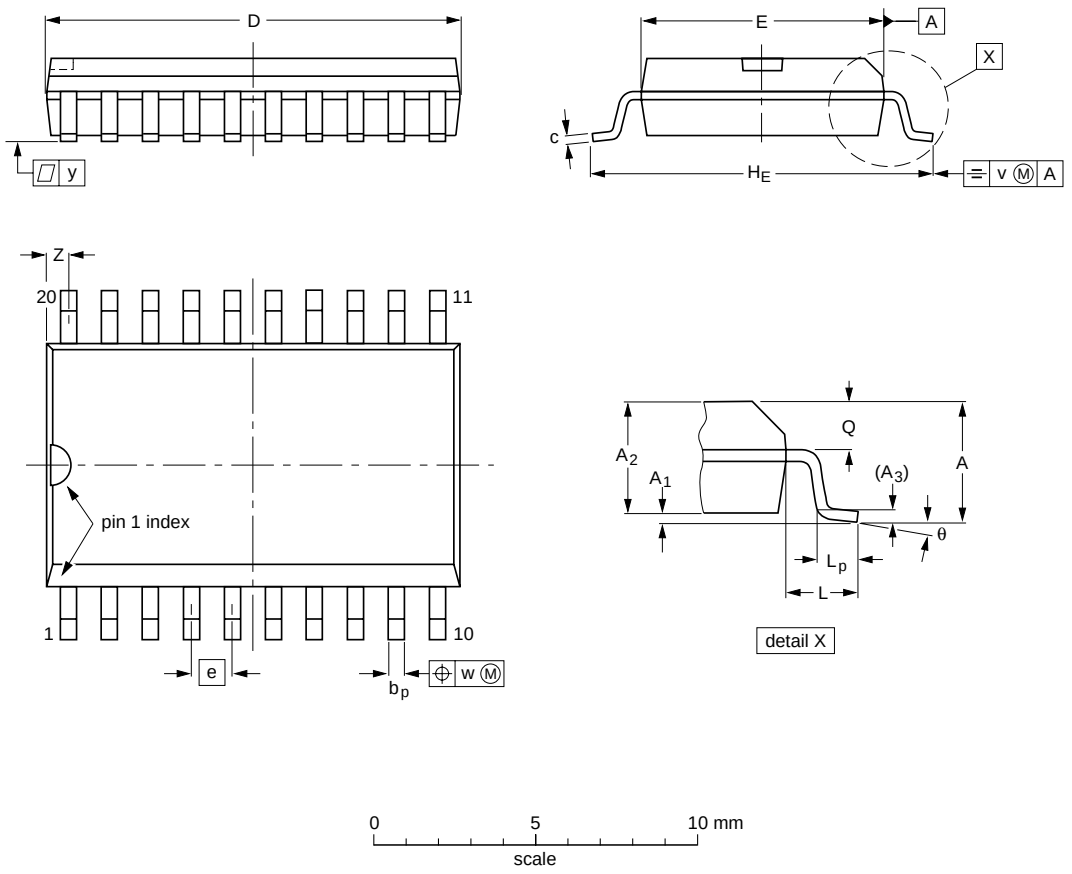
12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT163-1 (SO20)

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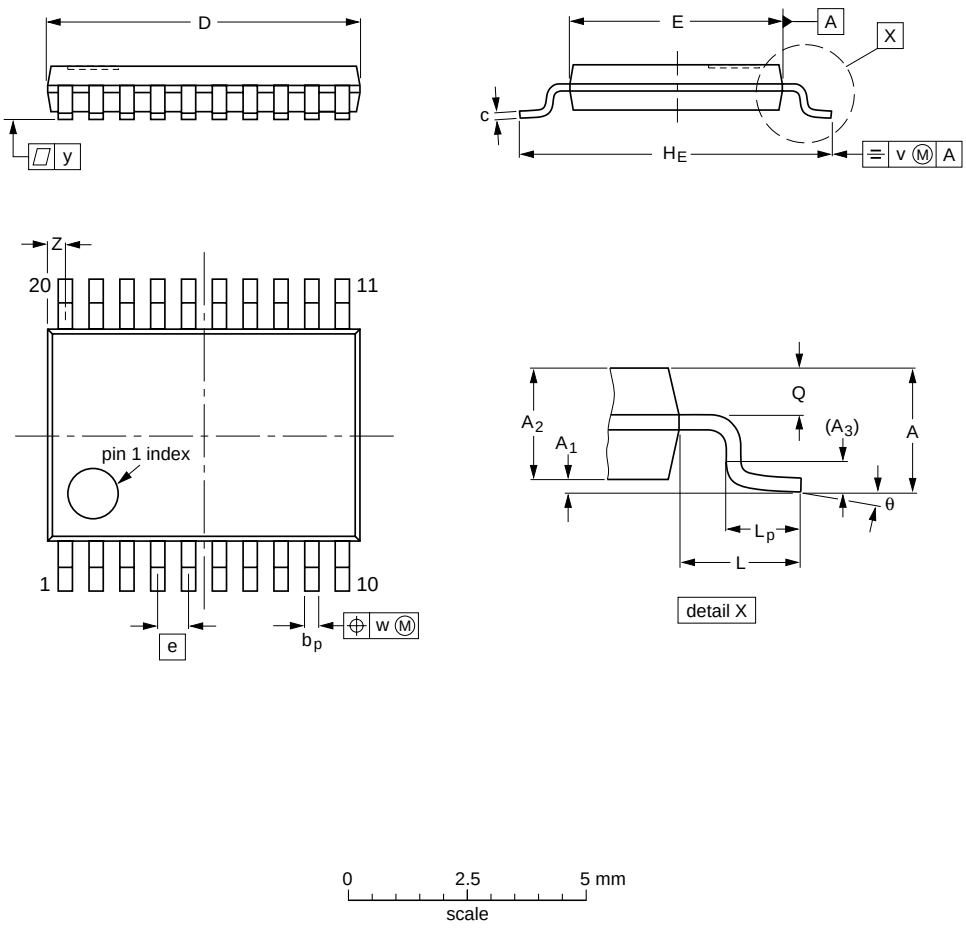
TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT360-1 (TSSOP20)

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13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8 and 9

Table 8. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.

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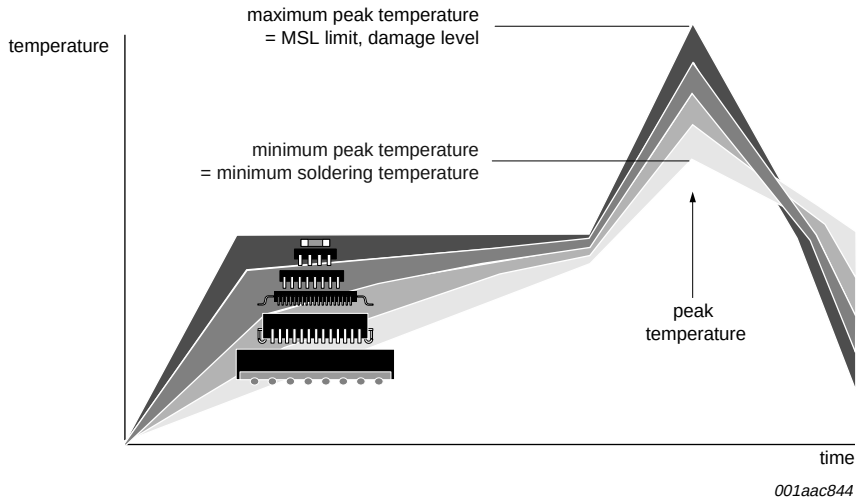

MSL: Moisture Sensitivity Level

Fig 11. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
I/O	Input/Output
I²C-bus	Inter-Integrated Circuit bus
MM	Machine Model
RC	Resistor Capacitor network
SMBus	System Management Bus

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15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9518A_3	20081203	Product data sheet	-	PCA9518A_2
Modifications:	• Section 6.1 “Enable”: added new 3rd paragraph • Figure 5 “Typical application: multiple expandable 5-channel I²C-bus hubs”: added 2nd paragraph below drawing.			
PCA9518A_2	20081001	Product data sheet	-	PCA9518A_1
PCA9518A_1	20070606	Product data sheet	-	-

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16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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