OPA858 5.5-GHz Gain Bandwidth Product Decompensated, FET Input Amplifier

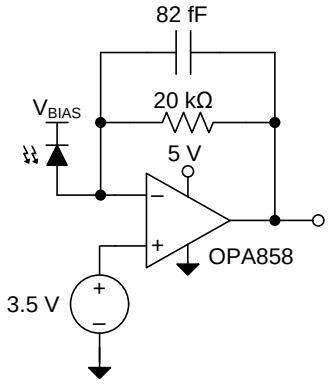
1 Features

- High Gain Bandwidth Product: 5.5 GHz
- Decompensated, Gain of 7 V/V (Stable)
- Ultra-Low Bias Current MOSFET Inputs: 10 pA
- Low Input Voltage Noise: 2.5 nV/√Hz
- Wide Input Common-Mode Range:
  - 1.4 V to Positive Supply
  - Includes Negative Supply
- Wide Input Common-Mode Range:
  - 0.4 V to Positive Supply
  - 1.1 V to Negative Supply
- Supply Voltage Range: 3.3 V to 5.25 V
- Quiescent Current: 20 mA
- Available in 8-Pin WSON Package
- Temperature Range: –40 to +125°C

2 Applications

- High-Speed Transimpedance Amplifier
- Laser Scanning Equipment
- LiDAR Receivers
- Displacement Transmitter
- Optical Time Domain Reflectometry (OTDR)
- Distributed Temperature Sensing
- 3D Scanner
- Time-of-Flight (ToF) Systems
- Autonomous Driving Systems

20-kΩ, 140-MHz Transimpedance Amplifier



3 Description

The OPA858 is an ultra-fast, wideband, low-noise, operational amplifier with CMOS inputs, designed for wideband transimpedance and general-purpose voltage amplifier applications. The extremely high 5.5-GHz gain bandwidth product enables applications requiring high transimpedance gains, and the low 2.5 nV/√Hz voltage noise maximizes SNR.

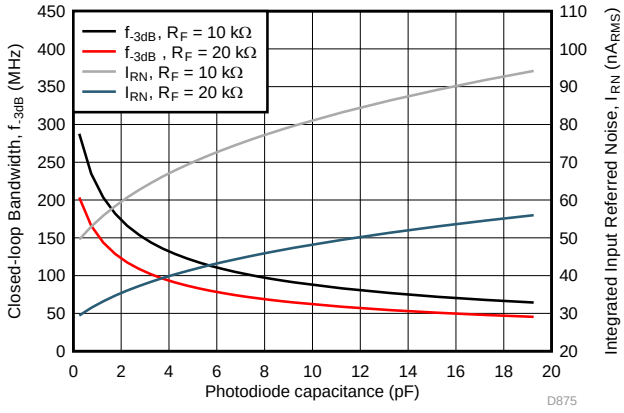
The OPA858 device is offered in a 2-mm × 2-mm, 8-pin, WSON package that features a feedback (FB) pin, which simplifies the feedback network connection to the device. The pinout features an isolation pin between the feedback and input connection to reduce parasitic coupling for applications sensitive to feedback capacitance.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA858	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Photodiode Capacitance vs. Bandwidth and Noise



ADVANCE INFORMATION

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Thermal Information ... 4
6.2 Electrical Characteristics: OPA858 ... 5
7 Detailed Description ... 7
7.1 Overview ... 7
7.2 Functional Block Diagram ... 7
7.3 Feature Description ... 8
7.4 Device Functional Modes ... 11
8 Application and Implementation ... 13
8.1 Application Information ... 13
8.2 Typical Application ... 15
9 Power Supply Recommendations ... 18
10 Layout ... 19
10.1 Layout Guidelines ... 19
10.2 Layout Example ... 20
11 Device and Documentation Support ... 21
11.1 Receiving Notification of Documentation Updates 21
11.2 Community Resources ... 21
11.3 Trademarks ... 21
11.4 Electrostatic Discharge Caution ... 21
11.5 Glossary ... 21
12 Mechanical, Packaging, and Orderable Information ... 22

ADVANCE INFORMATION

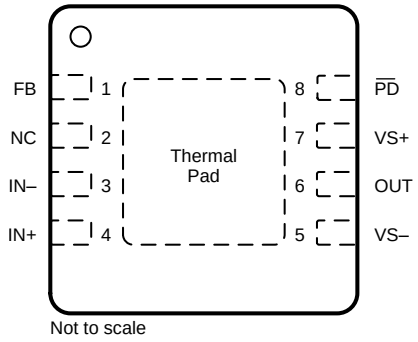
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2018	*	Initial release.

5 Pin Configuration and Functions

DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



Not to scale

NC - no internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
FB	1	I	Feedback connection to output of amplifier
IN–	3	I	Inverting input
IN+	4	I	Noninverting input
NC	2	—	Do not connect
OUT	6	O	Amplifier output
$\overline{PD}$	8	I	Power down connection. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation
VS+	7	—	Positive voltage supply
VS–	5	—	Negative voltage supply
Thermal pad	—	—	Connect the thermal pad to VS–

ADVANCE INFORMATION

6 Specifications

6.1 Thermal Information

THERMAL METRIC(1)		OPA858 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	100	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	22.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

ADVANCE INFORMATION

6.2 Electrical Characteristics: OPA858

V_{S+} = 5 V, $V_{S–}$ = 0 V, G = 7 V/V, R_F = 453 Ω, noninverting configuration, input common-mode at midsupply, R_L = 200 Ω, output load is referenced to midsupply, and T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_{OUT} = 200 mV_{PP}		1.2		GHz	C
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		600		MHz	C
GBP	Gain-bandwidth product			5.5		GHz	C
	Bandwidth for 0.1-dB flatness			130		MHz	C
SR	Slew rate (10% - 90%)	V_{OUT} = 2-V step		2000		V/µs	C
t_r	Rise time	V_{OUT} = 200-mV step		0.3		ns	C
t_f	Fall time	V_{OUT} = 200-mV step		0.3		ns	C
	Settling time to 0.1%	V_{OUT} = 2-V step		8		ns	C
	Settling time to 0.001%	V_{OUT} = 2-V step		3000		ns	C
	Overshoot or undershoot	V_{OUT} = 2-V step		7%			C
	Overdrive recovery	2x output overdrive		200		ns	C
HD2	Second-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}		80		dBc	C
		f = 50 MHz, V_{OUT} = 2 V_{PP}		68			
		f = 100 MHz, V_{OUT} = 2 V_{PP}		59			
		f = 200 MHz, V_{OUT} = 2 V_{PP}		47			
		f = 300 MHz, V_{OUT} = 2 V_{PP}		45			
HD3	Third-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}		86		dBc	C
		f = 50 MHz, V_{OUT} = 2 V_{PP}		75			
		f = 100 MHz, V_{OUT} = 2 V_{PP}		63			
		f = 200 MHz, V_{OUT} = 2 V_{PP}		35			
		f = 300 MHz, V_{OUT} = 2 V_{PP}		30			
e_n	Input-referred voltage noise	f = 1 MHz		2.5		nV/√Hz	C
Z_{OUT}	Closed-loop output impedance	f = 100 kHz		0.05		Ω	C
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain		72	75		dB	A
V_{OS}	Input offset voltage	T_A = 25°C	–4	±0.05	4	mV	A
		T_A = –40°C to +85°C		±0.15	3.25		B
$\Delta V_{OS}/\Delta T$	Input offset voltage drift	T_A = –40°C to +85°C		±1.5		µV/°C	B
I_{BN}, I_{BI}	Input bias current	T_A = 25°C		±0.1	5	pA	A
		T_A = –40°C to +85°C		±5			B
I_{BOS}	Input offset current	T_A = 25°C		±0.01	5	pA	A
		T_A = –40°C to +85°C		±0.05			B
CMRR	Common-mode rejection ratio	V_{CM} = ±0.5 V, referenced to midsupply	70	90		dB	A
INPUT							
	Common-mode input resistance			1		GΩ	C
C_{CM}	Common-mode input capacitance			0.62		pF	C
	Differential input resistance			1		GΩ	C
C_{DIFF}	Differential input capacitance			0.2		pF	C
V_{IH}	Common-mode input range (high)	CMRR > 66 dB, V_{S+} = 3.3 V	1.7	1.9		V	A
V_{IL}	Common-mode input range (low)	CMRR > 66 dB, V_{S+} = 3.3 V		0	0.4	V	A
V_{IH}	Common-mode input range (high)	CMRR > 66 dB	3.4	3.6		V	A
		T_A = –40°C to +85°C, CMRR > 66 dB		3.5			B

ADVANCE INFORMATION

Electrical Characteristics: OPA858 (continued)

V_{S+} = 5 V, $V_{S–}$ = 0 V, G = 7 V/V, R_F = 453 Ω, noninverting configuration, input common-mode at midsupply, R_L = 200 Ω, output load is referenced to midsupply, and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
V_{IL}	Common-mode input range low)	CMRR > 66 dB		0	0.4	V	A
		T_A = –40°C to +85°C, CMRR > 66 dB		0.2			B
OUTPUT							
V_{OH}	Output voltage (high)	T_A = 25°C, V_{S+} = 3.3 V	2.35	2.4		V	A
V_{OH}	Output voltage (high)	T_A = 25°C	3.95	4.1		V	A
		T_A = –40°C to +85°C		4.0			B
V_{OL}	Output voltage (low)	T_A = 25°C, V_{S+} = 3.3 V		1.05	1.15	V	A
V_{OL}	Output voltage (low)	T_A = 25°C		1.05	1.15	V	A
		T_A = –40°C to +85°C		1.1			B
	Linear output drive (sink and source)	R_L = 10 Ω, A_{OL} > 60 dB	65	80		mA	A
		T_A = –40°C to +85°C, R_L = 10 Ω, A_{OL} > 60 dB		74			B
I_{SC}	Output short-circuit current		85	105		mA	A
C_{LOAD}	Capacitive load drive	30% overshoot		40		pF	C
POWER SUPPLY							
V_S	Operating voltage		3.3		5.25	V	A
I_Q	Quiescent current	V_{S+} = 5 V	18	20.5	24	mA	A
		V_{S+} = 3.3 V	17.5	20	23.5		D
		V_{S+} = 5.25 V	18.5	21	24.5		D
I_Q	Quiescent current	T_A = –40°C to +85°C		22		mA	B
		T_A = –40°C to +125°C		24			
PSRR+	Positive power-supply rejection ratio		80	90		dB	A
PSRR–	Negative power-supply rejection ratio		70	78			
POWER DOWN							
	Disable voltage threshold	Amplifier OFF below this voltage	0.8	1		V	A
	Enable voltage threshold	Amplifier ON above this voltage		1.5	1.8	V	A
	Power-down quiescent current			.07	0.14	mA	A
	$\overline{PD}$ bias current			.07	0.2	mA	A
	Turnon time delay	Time to V_{OUT} = 90% of final value		13		ns	C
	Turnoff time delay	Time to V_{OUT} = 10% of original value		120		ns	C

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The ultra-wide, 5.5-GHz gain bandwidth product (GBP) of the OPA858, combined with the broadband voltage noise of 2.5 nV/√Hz, produces a viable amplifier for wideband transimpedance applications, high-speed data acquisition systems, and applications with weak signal inputs that require low-noise and high-gain front ends. The OPA858 combines multiple features to optimize dynamic performance. In addition to the wide, small-signal bandwidth, the OPA858 has 600 MHz of large signal bandwidth (2 V_{PP}) and a slew rate of 2000 V/µs, making the device a viable option for high-speed pulsed applications.

The OPA858 is offered in a 2-mm × 2-mm, 8-pin, WSON package that features a feedback (FB) pin for a simple feedback network connection to the amplifier. The pinout features an isolation pin between the feedback and input connection to reduce parasitic coupling for applications that are sensitive to feedback capacitance.

7.2 Functional Block Diagram

The OPA858 is a classic, voltage feedback operational amplifier (op amp) with two high-impedance inputs and a low-impedance output. Standard application circuits are supported, like the two basic options shown in Figure 1 and Figure 2. The DC operating point for each configuration is level-shifted by the reference voltage (V_{REF}), which is typically set to midsupply in single-supply operation. V_{REF} is typically connected to ground in split-supply applications.

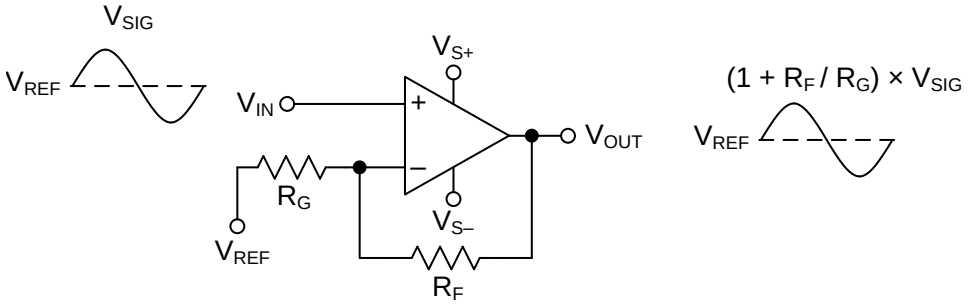


Figure 1. Noninverting Amplifier

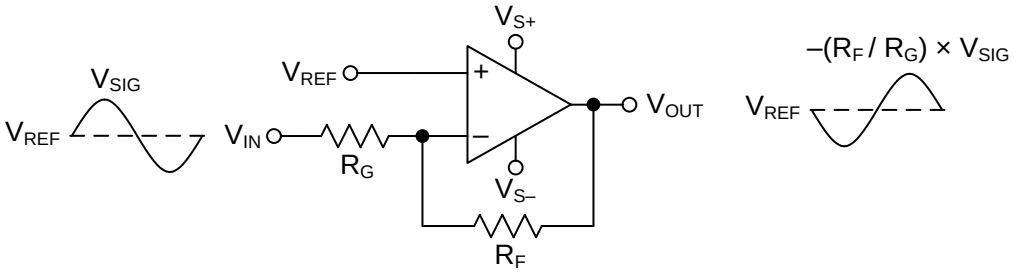


Figure 2. Inverting Amplifier

7.3 Feature Description

7.3.1 Input and ESD Protection

The OPA858 is fabricated on a low-voltage, high-speed, BiCMOS process. The internal, junction breakdown voltages are low for these small geometry devices, and as a result, all device pins are protected with internal ESD protection diodes to the power supplies, as Figure 3 shows. In addition to the diode to the power supplies, there are two anti-parallel diodes between the inputs of the amplifier that clamp the inputs during an overrange or fault condition.

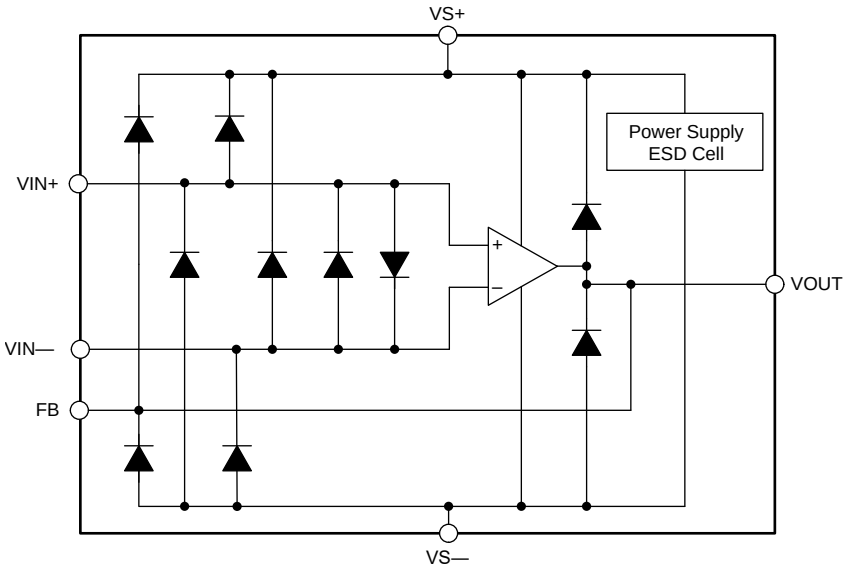


Figure 3. Internal ESD Structure

7.3.2 Feedback Pin

The OPA858 pin layout is optimized to minimize parasitic inductance and capacitance, which is critical in high-speed analog design. The FB pin (pin 1) is internally connected to the output of the amplifier. The FB pin is separated from the inverting input of the amplifier (pin 3) by a no connect (NC) pin (pin 2). The NC pin must be left floating. There are two advantages to this pin layout:

1. A feedback resistor (R_F) can connect between the FB and IN– pin on the same side of the package (see Figure 4) rather than going around the package.
2. The isolation created by the NC pin minimizes the capacitive coupling between the FB and IN– pins.

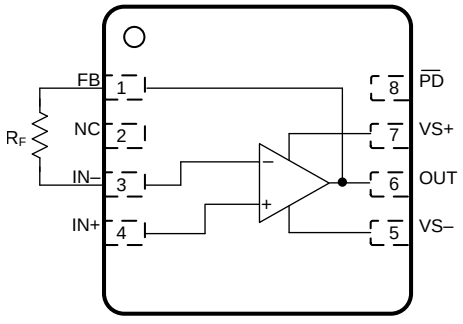


Figure 4. R_F Connection Between FB and IN– Pins

Feature Description (continued)

7.3.3 Wide Gain-Bandwidth Product

Figure 5 shows the open-loop magnitude and phase response of the OPA858. Calculate the gain bandwidth product of an op amp by determining the frequency at which the A_{OL} is 60 dB and multiplying that frequency by a factor of 1000. The second pole in the A_{OL} response occurs before the magnitude crosses 0 dB, and the resultant phase margin is less than 0°. This indicates instability at a gain of 0 dB. Amplifiers that are not unity-gain stable are known as decompensated amplifiers. Decompensated amplifiers typically show higher gain-bandwidth product and slew rate, and lower voltage noise, compared to a unity-gain stable amplifier for the same amount of quiescent power consumption.

One of the primary applications for the OPA858 is as a high-speed transimpedance amplifier (TIA), as Figure 14 shows. The low-frequency noise gain of a TIA is 1-V/V, as *What You Need To Know About Transimpedance Amplifiers – Part 1* and *What You Need To Know About Transimpedance Amplifiers – Part 2* show. The ratio of the total input capacitance and the feedback capacitance set the high-frequency gain. To maximize the TIA closed-loop bandwidth, the feedback capacitance is typically smaller than the input capacitance, which implies that the high-frequency noise gain is greater than 0 dB. As a result, op amps that are used in TIA applications are not required to be unity-gain stable, which makes a decompensated amplifier a viable option for such applications.

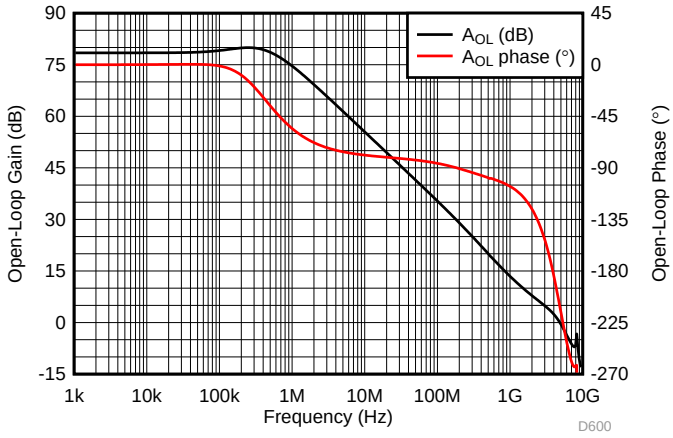


Figure 5. A_{OL} (No Load) Versus Frequency

7.3.4 Slew Rate and Output Stage

In addition to wide bandwidth, the OPA858 features a high slew rate in excess of 2000 V/µs. The slew rate is a critical parameter in high-speed pulse applications with narrow sub 10-ns pulses such as Optical Time-Domain Reflectometry (OTDR). The high-slew rate of the OPA858 implies that the device can accurately reproduce a 2-V, 1-ns pulse edge. The wide bandwidth and slew rate of the OPA858 are designed for high-speed, signal-chain front ends.

ADVANCE INFORMATION

Feature Description (continued)

Figure 6 shows the open-loop output impedance of the OPA858 as a function of frequency. To achieve high slew rates and low output impedance across frequency, the output swing of the OPA858 is limited to 3 V. The OPA858 is typically used in conjunction with high-speed pipeline ADCs and flash ADCs that have limited input ranges. Therefore, the OPA858 output swing range coupled with the class-leading voltage noise specification for a CMOS amplifier maximizes the overall dynamic range of the signal chain.

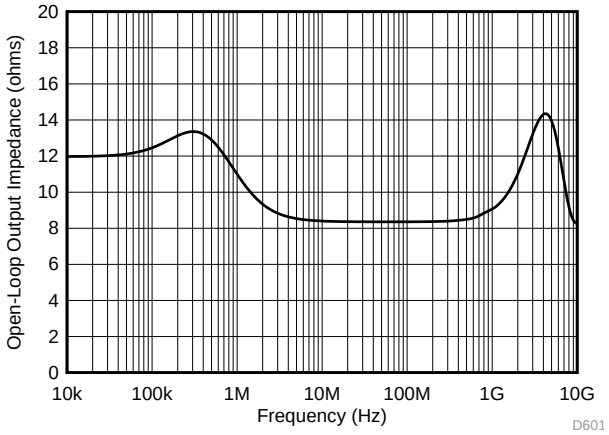


Figure 6. Open-Loop Output Impedance (Z_{OL}) Versus Frequency

7.3.5 Current Noise

The input impedance of CMOS and JFET input amplifiers at low frequencies exceed several GΩs. However, at higher frequencies, the transistors parasitic capacitance to the drain, source, and substrate reduces the impedance. The high impedance at low frequencies eliminates any bias current and the associated shot noise. At higher frequencies, the input current noise increases (see Figure 7) as a result of capacitive coupling between the CMOS gate oxide and the underlying transistor channel. This phenomenon is a natural artifact of the construction of the transistor and is unavoidable.

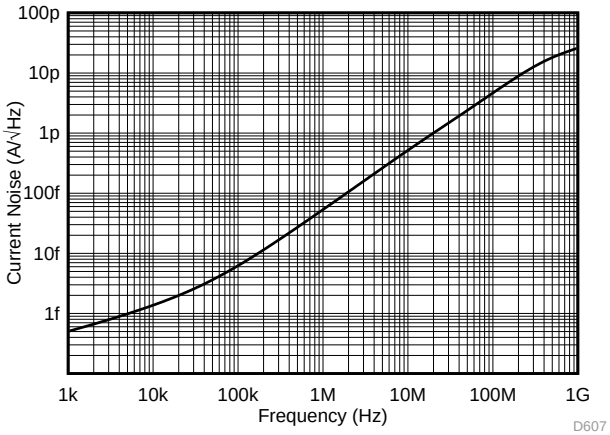


Figure 7. Input Current Noise (I_{BN} and I_{BI}) Versus Frequency

ADVANCE INFORMATION

7.4 Device Functional Modes

7.4.1 Split-Supply and Single-Supply Operation

The OPA858, like any standard, voltage feedback, operational amplifier, may be configured with single-sided supplies or split-supplies. Split-supply operation using balanced supplies with the input common-mode set to ground eases lab testing because most signal generators, network analyzers, spectrum analyzers, and other lab equipment typically reference inputs and outputs to ground. Split-supply operation is preferred in systems where the signals swing around ground. However, the system requires two supply rails. In split-supply operation, the thermal pad must be connected to the negative supply.

Newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA858 can be used with a single positive supply (negative supply at ground) with no change in performance if the input common-mode and output swing are biased within the linear operation of the device. To change the circuit from a split-supply to a single-supply configuration, level shift all the voltages by half the difference between the power supply rails. In this case, the thermal pad must be connected to ground.

7.4.2 Power-Down Mode

The OPA858 features a power-down mode to reduce the quiescent current, which conserves power. Driving the $\overline{PD}$ pin LOW (less than 0.8 V) disables the amplifier, consuming a standby current of less than 200 µA. Raise the $\overline{PD}$ pin HIGH (greater than 1.2 V) to enable the amplifier. Figure 9 shows the response of the OPA858 as the $\overline{PD}$ pin toggles between the disabled and enabled states of the amplifier. Figure 8 shows the circuit that tests the $\overline{PD}$ response. When the amplifier is turned on, the output settles to 3 V. When the amplifier is turned off, the output enters a high-impedance state and the 200-Ω resistor pulls the output node down to 2.5 V. The supply current includes the 20-mA quiescent current and the load current through the output resistor and the feedback network.

The $\overline{PD}$ disable and enable threshold voltages are with reference to the negative supply. If the amplifier is configured with the positive supply at 3.3 V and the negative supply at ground, then the disable and enable threshold voltages are 0.8 V and 1.2 V, respectively. If the amplifier is configured with ±2.5-V supplies, then the threshold voltages are at –1.7 V and –1.3 V, respectively.

Connecting the $\overline{PD}$ pin low disables the amplifier and places the output in a high-impedance state. When the amplifier is configured as a noninverting amplifier, the feedback (R_F) and gain (R_G) resistor network form a parallel load to the output of the amplifier. To protect the input stage of the amplifier, the OPA858 uses internal, back-to-back protection diodes between the inverting and noninverting input pins as Figure 3 shows. When the differential voltage between the input pins of the amplifier exceeds a diode voltage drop, an additional low-impedance path is created between the inputs. The low impedance between the inputs will be parallel to R_G.

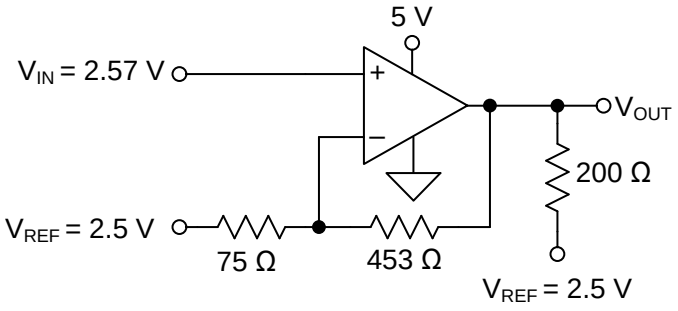


Figure 8. Power-Down Test Circuit

ADVANCE INFORMATION

Device Functional Modes (continued)

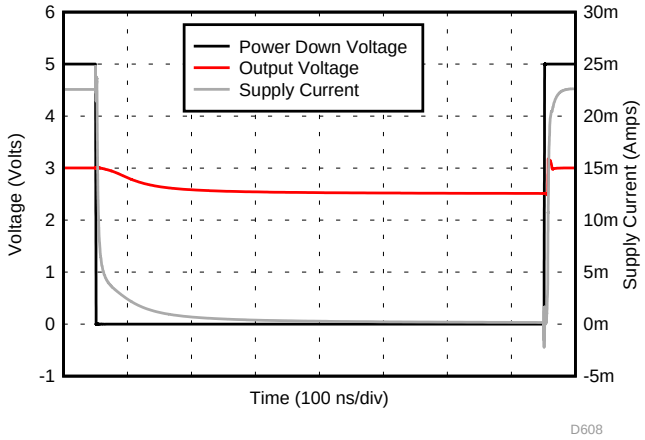


Figure 9. Power-Down Response

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Using the OPA858 in Low Gain Configurations

The OPA858 is compensated to have less than 1 dB of peaking in a gain of 7 V/V. Using the device in lower gains results in increased peaking and potential instability. The stability of the amplifier at lower gains is increased by adding an input capacitor and a feedback capacitor to increase the high-frequency noise gain (1/β). The stability and phase margin of the amplifier depends on the loop-gain of the amplifier, which is the product of the A_{OL} and 1/β of the amplifier. If done carefully, increasing 1/β increases the loop gain, which improves the phase margin. The modified network with the added capacitors alters the high-frequency noise gain, but does not alter the signal gain.

Figure 10 shows the OPA858 circuit configured in a signal gain of 7 V/V. Figure 11 shows the OPA858 circuit configured in a signal gain of 3 V/V, with the noise gain shaped by the 1-pF input capacitor and the 0.4-pF feedback capacitor.

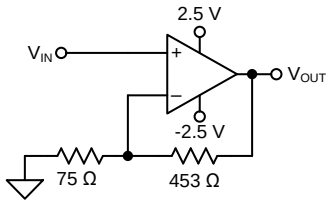


Figure 10. OPA858 Configured in a Gain of 7 V/V

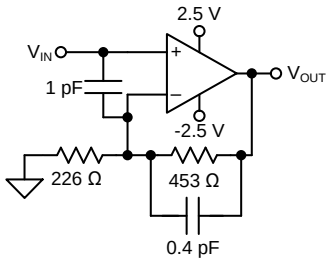


Figure 11. OPA858 Configured in a Gain of 3 V/V

Figure 12 shows the simulated frequency response. Without the added noise gain shaping components, the OPA858 shows approximately 12 dB of peaking in a gain of 3 V/V. The noise gain shaping elements reduce the peaking to less than 2 dB. The 1-pF input capacitor, the input capacitance of the amplifier, and the feedback network create a zero in the noise gain at a frequency *f*, as Equation 1 shows.

$$f = \frac{1}{2\pi\left(R_F \,||\, R_G\right)C_{IN}} \quad (1)$$

where

- R_F is the feedback resistor
- R_G is the input or gain resistor
- C_{IN} is the total input capacitance, which includes the external 1-pF capacitor, the amplifier input capacitance, and any parasitic PCB capacitance.

To counteract the effects of the noise-gain zero, add a pole by inserting the 0.4-pF feedback capacitor. The pole occurs at a frequency shown in Equation 2. The noise-gain pole and zero locations must be selected so that the rate-of-closure between the A_{OL} and 1/β curves is approximately 20 dB. To ensure this occurs, the noise-gain pole must occur before the loop-gain crossover frequency, which is defined as the frequency where the A_{OL} and 1/β curves intersect.

$$f = \frac{1}{2\pi R_F C_F} \quad (2)$$

where

- C_F is the feedback capacitor

ADVANCE INFORMATION

Application Information (continued)

Adding the noise-gain shaping elements increases the total output noise. Figure 13 shows a comparison of the output noise spectrum of the three configurations. The peaking shown in the closed-loop frequency response is shown in the output noise spectrum. The low-frequency output noise in a gain of 7 V/V is higher than the other two configurations, but the output noise is in a larger gain configuration. Table 1 lists a comparison of the three different configurations, assuming a 2-GHz brickwall filter is used. The results show that the noise-shaped gain of 3 V/V degrades the input-referred noise performance compared to the configuration with a gain of 7 V/V. However, it is possible to compensate a decompensated amplifier in a gain lower than the recommended minimum specification without stability issues.

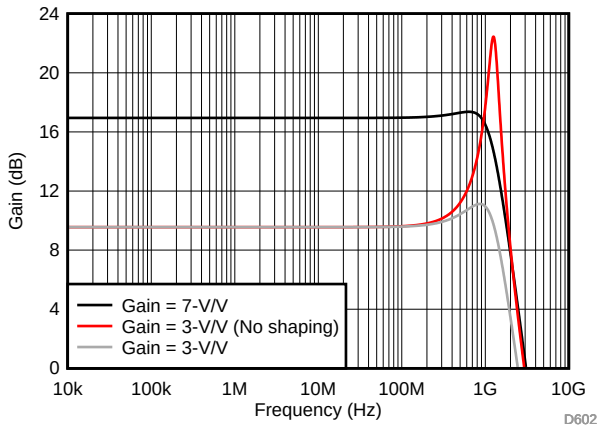


Figure 12. Frequency Response

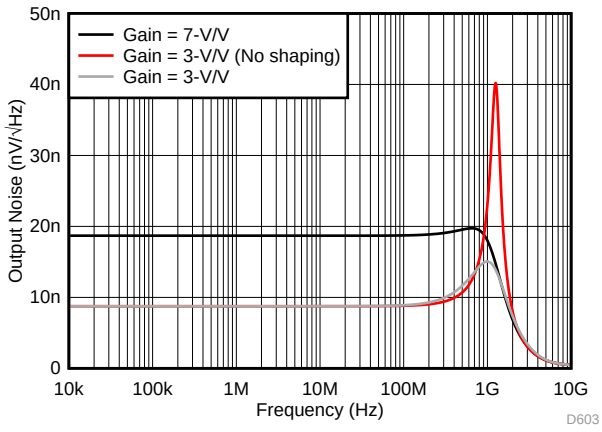


Figure 13. Output Noise Spectral Response

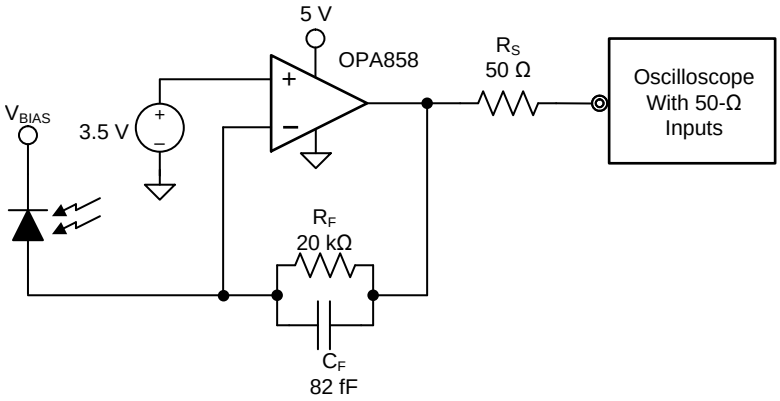
Table 1. OPA858 Noise Comparison

AMPLIFIER CONFIGURATION	$f_{-3\ dB}$ BANDWIDTH (GHz)	TOTAL OUTPUT INTEGRATED NOISE (2-GHz BANDWIDTH)	INPUT REFERRED NOISE (2-GHz BANDWIDTH)
Gain = 7-V/V	1.34	720 μV_{RMS}	102.86 μV_{RMS}
Gain = 3-V/V (no shaping)	2.14	890 μV_{RMS}	296.67 μV_{RMS}
Gain = 3-V/V	1.64	530 μV_{RMS}	176.67 μV_{RMS}

ADVANCE INFORMATION

8.2 Typical Application

The high GBP, low input voltage, and current noise of the OPA858 make the device a viable, wideband, transimpedance amplifier for moderate to high transimpedance gains.



(1) Supply decoupling not shown

Figure 14. TIA Circuit (Gain = 20 kΩ)

8.2.1 Design Requirements

Design a high-bandwidth, high-gain, transimpedance amplifier with the design requirements listed in Table 2.

Table 2. Design Requirements

TARGET BANDWIDTH (MHz)	TRANSIMPEDANCE GAIN (kΩ)	PHOTODIODE CAPACITANCE (pF)	FREQUENCY PEAKING (dB)
> 120	20	1.5	< 0.5

8.2.2 Detailed Design Procedure

The *Transimpedance Considerations for High-Speed Amplifiers* application report discusses theories and equations that show how to compensate a transimpedance amplifier for a particular transimpedance gain and input capacitance. The equations presented in the*Transimpedance Considerations for High-Speed Amplifiers* application report contain links to Microsoft® Excel® calculators that simplify the design process. What You Need To Know About Transimpedance Amplifiers – Part 1 provides a link to the calculator. Set the calculator parameters as listed in Table 3.

Table 3. Inputs to the TIA Calculator

INPUT PARAMETER	INPUT VALUE	UNITS
Op Amp Gain Bandwidth Product (GBP)	5.5	GHz
Total Input Capacitance (C_{IN})	2.3	pF
Transimpedance Gain (R_F)	20	kΩ

The total input capacitance includes the diode capacitance (1.5 pF), the OPA858 common-mode capacitance (0.6 pF), and the differential capacitance (0.2 pF). Table 4 lists the calculated outputs.

Table 4. TIA Calculator Outputs

OUTPUT PARAMETER	OUTPUT VALUE	UNITS
Feedback capacitor (C_F)	0.082	pF
Closed-loop bandwidth	138	MHz

ADVANCE INFORMATION

Equation 3 shows the high-frequency noise gain, and in this case, is equal to Equation 4, which is greater than the recommended gain of 7 V/V that ensures sufficient phase-margin. A feedback capacitor of 0.082 pF is difficult to implement in an actual circuit, because the capacitor is highly susceptible to parasitic capacitance from the PCB and the feedback resistor. Figure 15 shows the small-signal frequency response of the TIA circuit in Figure 14. The figures compare the frequency response in two cases:

- C_F = 0.082 pF
- C_F = 0.123 pF (50% larger)

With a feedback capacitance of 0.082 pF, the closed-loop bandwidth is equal to 140 MHz, which is close to the calculated value shown in Table 4. A feedback capacitance of 0.123 pF results in a closed-loop bandwidth of 81.5 MHz. Take care to minimize parasitic capacitance during layout. Use two 10-kΩ resistors in series to reduce the parasitic capacitance that is associated with the 20-kΩ feedback resistor. This results in a theoretical 50% reduction in parasitic capacitance.

$$\left(1+\frac{C_{IN}}{C_F}\right) \tag{3}$$

$$\left(1+\frac{2.3\text{ pF}}{0.082\text{ pF}}\right)=29\text{ V/V} \tag{4}$$

The common-mode is set close to the positive limit of the amplifier and the photodiode is biased to source current. This combination of amplifier common-mode and photodiode bias configuration results in a negative swing when light is incident on the photodiode and as a result maximizes the output swing of the amplifier. Figure 16 shows a comparison of the transient response to a 50-µA, 20-ns, input current pulse from the photodiode. The resulting amplifier output is a 1-V_{PP} negative pulse on a 3.5-V common-mode. Figure 17 shows a comparison of the output noise spectrum of the two cases. A 0.123-pF feedback capacitor results in lower overall noise as a result of the reduced noise gain peaking.

8.2.3 Application Curves

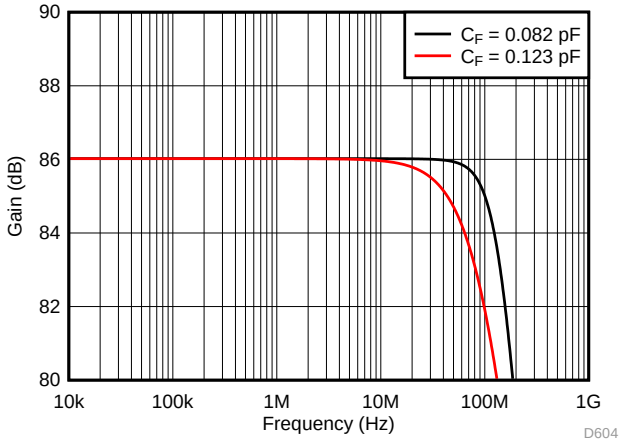
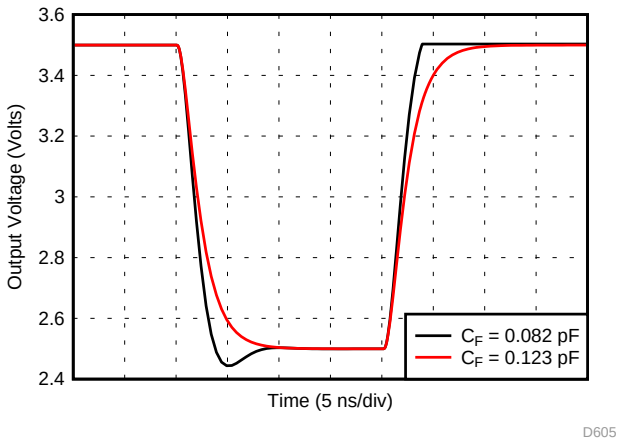


Figure 15. TIA Frequency Response



Pulse width = 10 ns Input common-mode = 3.5 V
Input = 50 µApp

Figure 16. TIA 1-V_{PP} Pulse Response

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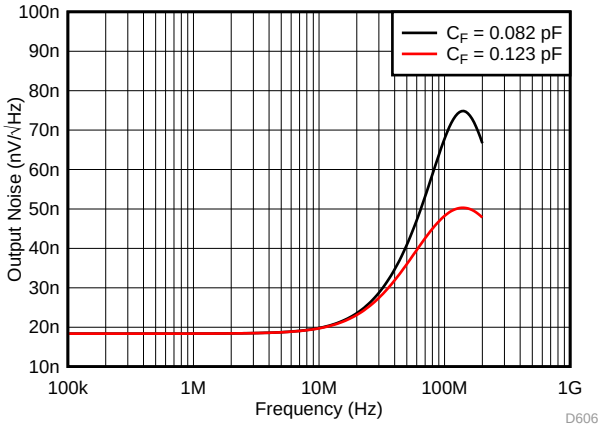


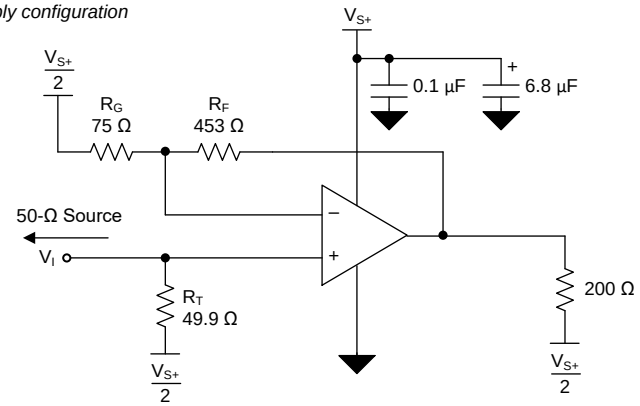
Figure 17. TIA Output Noise Spectral Response

ADVANCE INFORMATION

9 Power Supply Recommendations

The OPA858 operates on supplies from 3.3 V to 5.25 V. The OPA858 operates on single-sided supplies, split and balanced bipolar supplies, and unbalanced bipolar supplies. Because the OPA858 does not feature rail-to-rail inputs or outputs, the input common-mode and output swing ranges are limited at 3.3-V supplies.

a) Single supply configuration



b) Split supply configuration

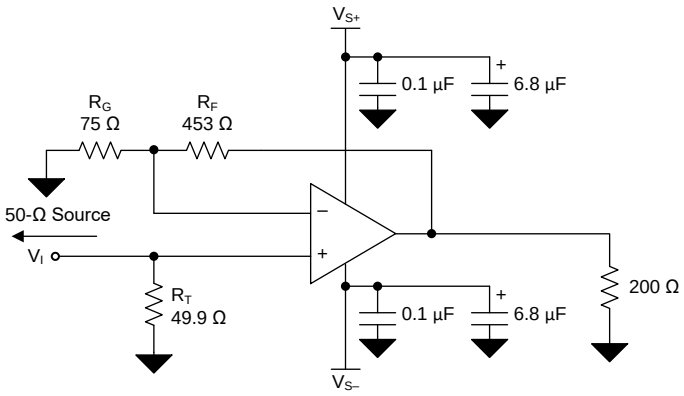


Figure 18. Split and Single Supply Circuit Configuration

ADVANCE INFORMATION

10 Layout

10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA858 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

1. Minimize parasitic capacitance from the signal I/O pins to AC ground. Parasitic capacitance on the output and inverting input pins can cause instability. To reduce unwanted capacitance, TI recommends cutting out the power and ground traces underneath the signal input and output pins. Otherwise, ground and power planes must be unbroken elsewhere on the board. When configuring the amplifier as a TIA, if the required feedback capacitor is under 0.15 pF, consider using two series resistors, each of half the value of a single resistor in the feedback loop to minimize the parasitic capacitance from the resistor.
2. Minimize the distance (less than 0.25") from the power-supply pins to high-frequency bypass capacitors. Use high quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies to ensure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, must be used on the supply pins. These are placed further from the device and are shared among several devices in the same area of the PC board.
3. **Using the OPA858 with a photodiode.** When using the OPA858 with a photodiode, ensure that the photodiode is placed as close to the inverting pin of the amplifier as possible and on the same side of the PCB as the amplifier. Excess capacitance leads to increased noise and excess inductance affects the high-frequency noise-gain response that causes instability.
4. **Careful selection and placement of external components preserves the high-frequency performance of the OPA858 .** Use low-reactance resistors. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon-composition axially-leaded resistors provide good high-frequency performance. Keep leads and PCB trace length as short as possible. Never use wirewound resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close to the output pin as possible. Place other network components (such as noninverting input termination resistors) close to the package. Even with a low parasitic capacitance shunting the external resistors, high resistor values create significant time constants that can degrade performance. Good axial metal film or surface mount resistors have approximately 0.2 pF in shunt with the resistor. When configuring the OPA858 as a voltage amplifier, keep resistor values as low as possible and consistent with load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because R_F and R_G become part of the output load network of the amplifier.
5. **TI does not recommend socketing a high-speed device such as the OPA858.** The socket introduces additional lead length and pin-to-pin capacitance that creates a troublesome parasitic network. This can make achieving a smooth, stable, frequency response almost impossible. Solder the op amp onto the board for optimal results.

ADVANCE INFORMATION

10.2 Layout Example

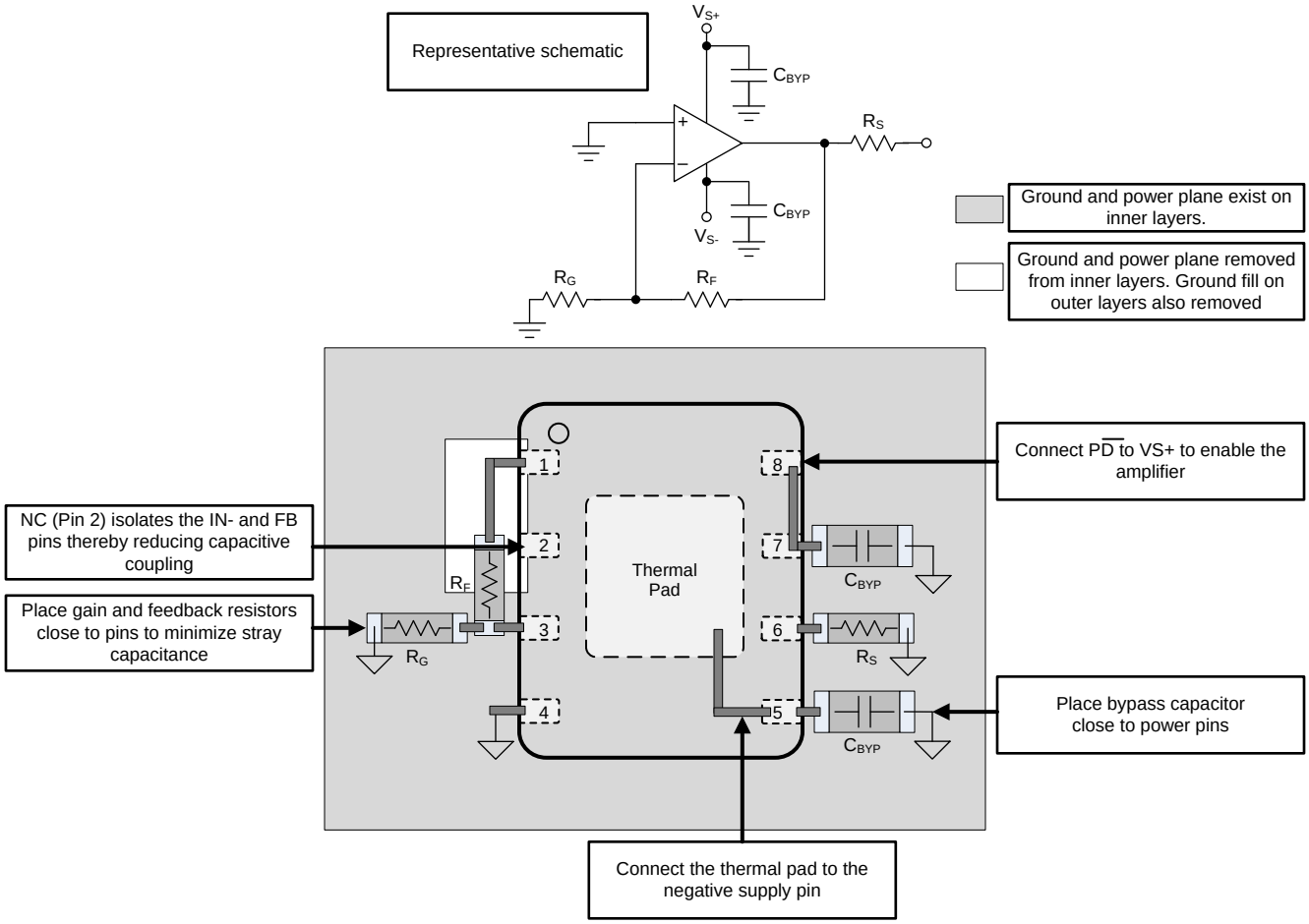


Figure 19. Layout Recommendation

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA858IDSGR	PREVIEW	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	X858	
OPA858IDSGT	PREVIEW	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	X858	
XOPA858IDSGT	ACTIVE	WSON	DSG	8	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

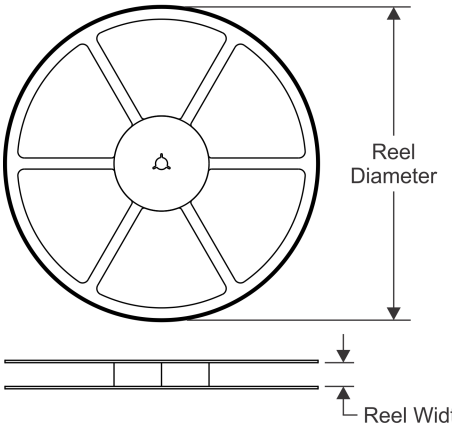
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

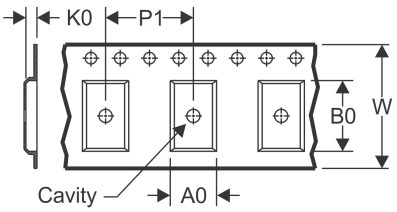
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

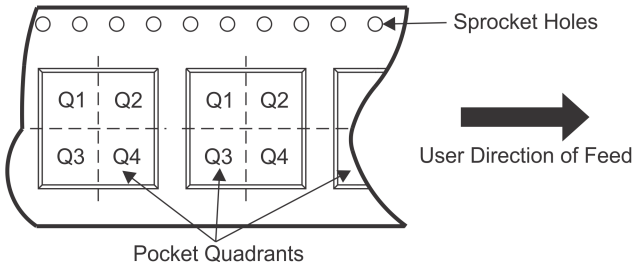


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

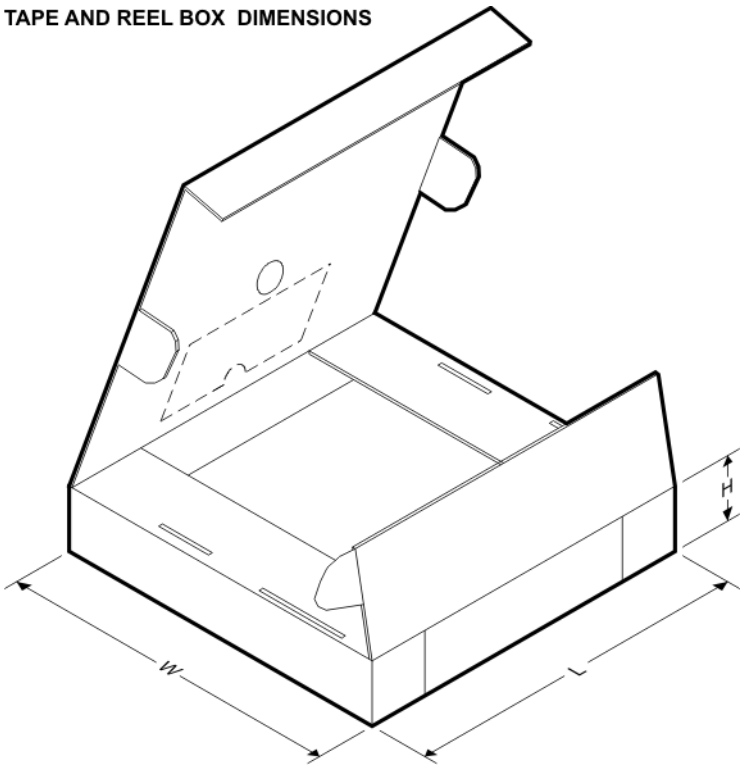
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA858IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA858IDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

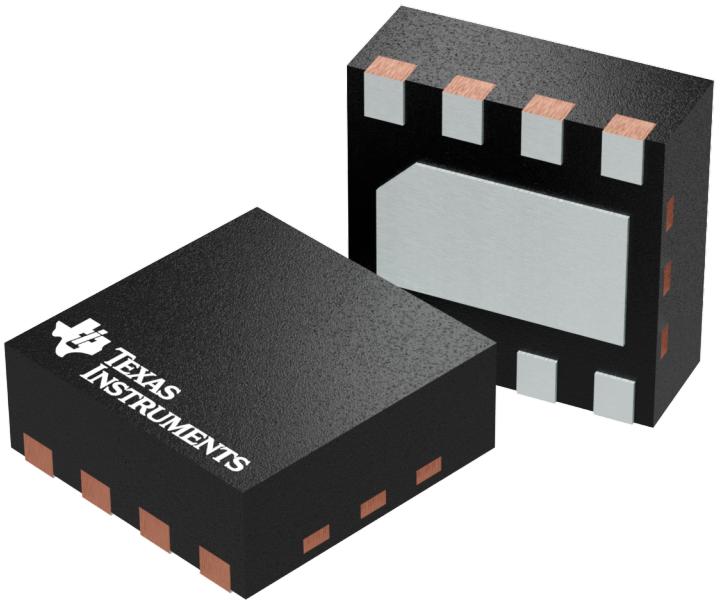


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA858IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
OPA858IDSGT	WSON	DSG	8	250	210.0	185.0	35.0

DSG 8 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



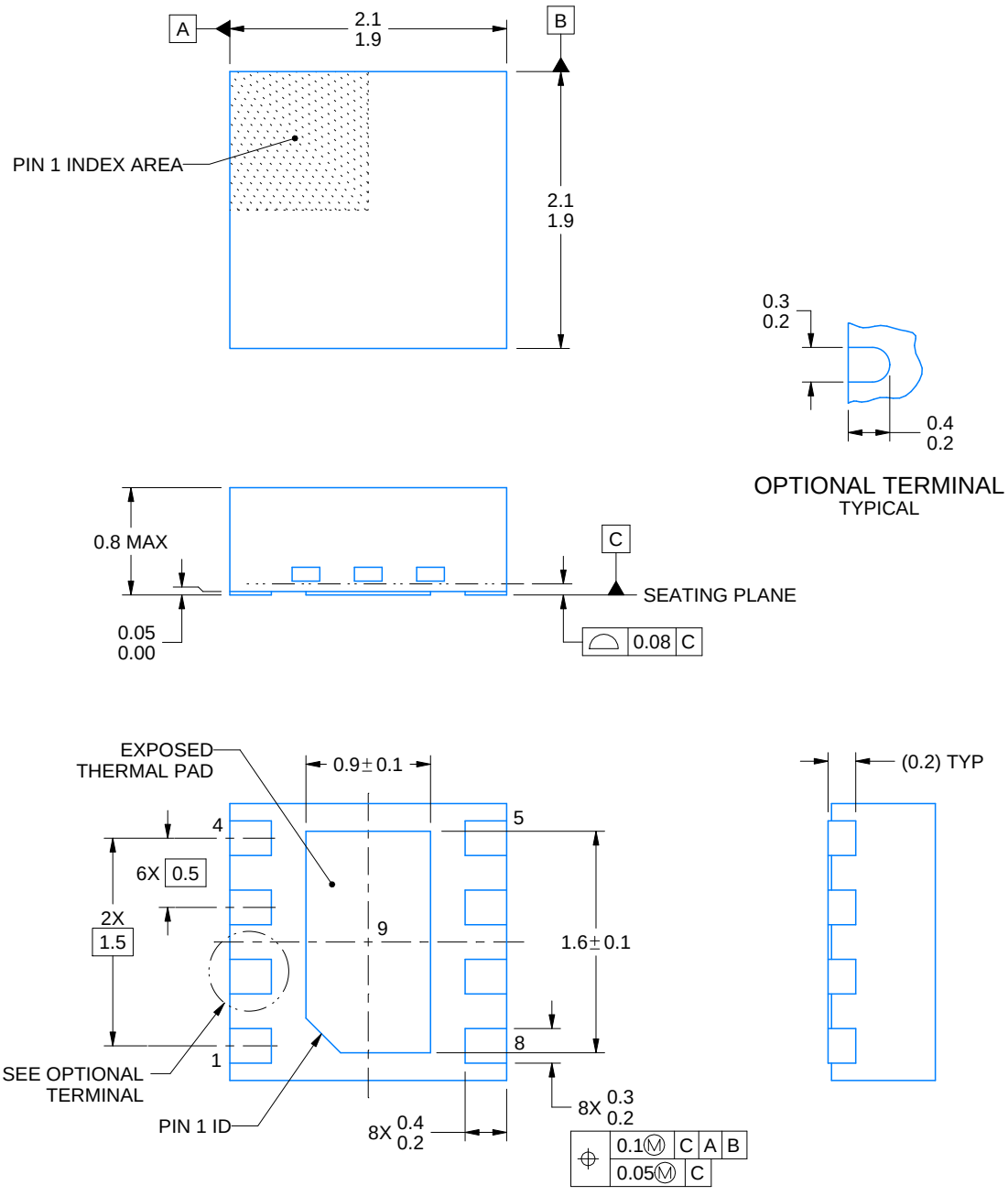
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DSG0008A

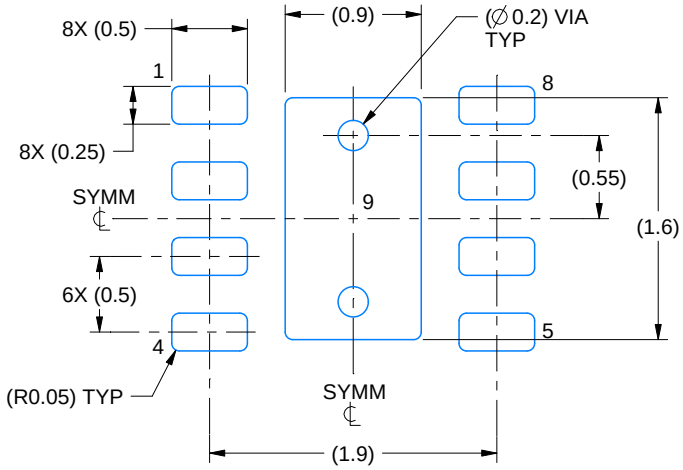
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

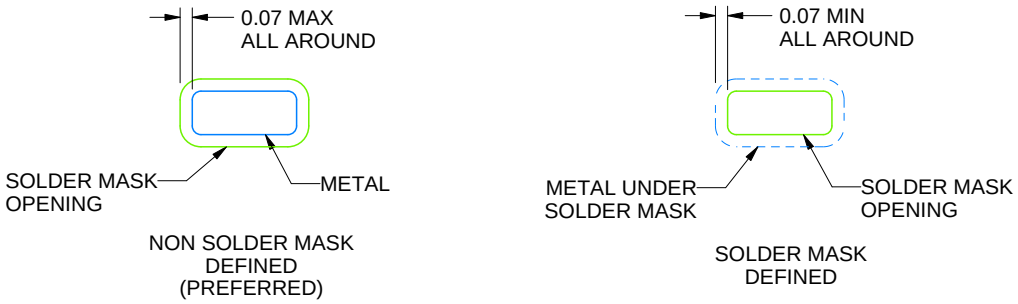


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

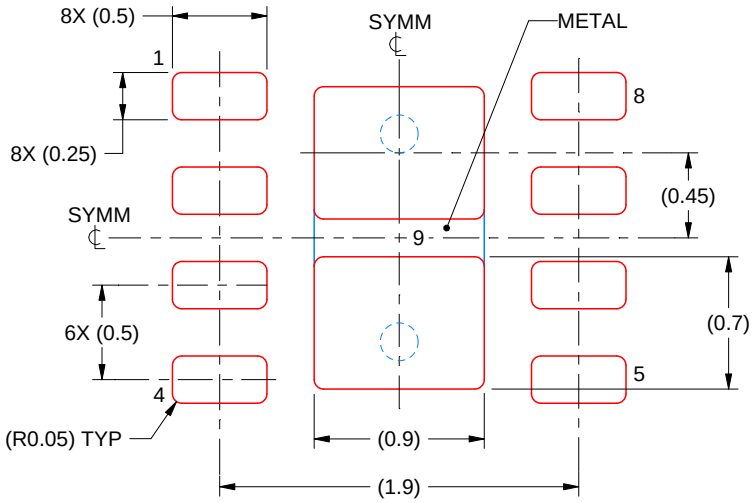


SOLDER MASK DETAILS

4218900/B 09/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

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