

OPA602

High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.5MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: $\pm 250\mu\text{V}$ max
- LOW BIAS CURRENT: $\pm 1\text{pA}$ max
- FAST SETTLING TIME: 1μs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DATA CONVERSION

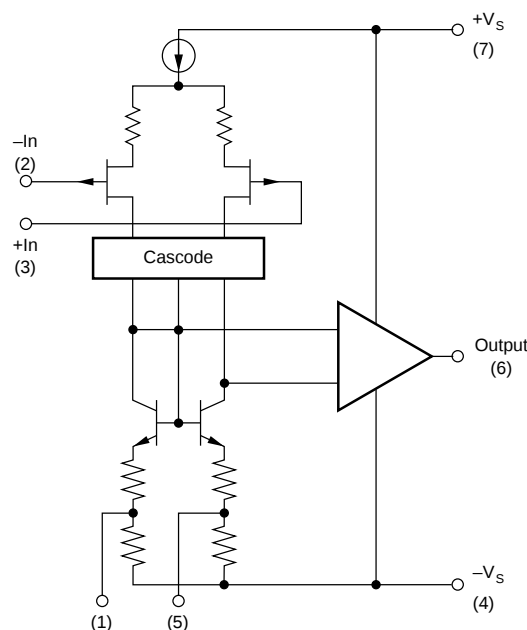
DESCRIPTION

The OPA602 is a precision, wide bandwidth FET operational amplifier. Monolithic *Difet* (dielectrically isolated FET) construction provides an unusual combination of high speed and accuracy.

Its wide-bandwidth design minimizes dynamic errors. High slew rate and fast settling time allow accurate signal processing in pulse and data conversion applications. Wide bandwidth and low distortion minimize AC errors. All specifications are rated with a 1kΩ resistor in parallel with 500pF load. The OPA602 is unity-gain stable and easily drives capacitive loads up to 1500pF.

Laser-trimmed input circuitry provides offset voltage and drift performance normally associated with precision bipolar op amps. *Difet* construction achieves extremely low input bias currents (1pA max) without compromising input voltage noise.

The OPA602's unique input cascode circuitry maintains low input bias current and precise input characteristics over its full input common-mode voltage range.



Difet® Burr-Brown Corp.

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SPECIFICATIONS

ELECTRICAL

At $V_S = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA602AM/API/AU			OPA602BM/SM/BP			OPA602CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE Voltage: $f_O = 10\text{Hz}$ $f_O = 100\text{Hz}$ $f_O = 1\text{kHz}$ $f_O = 10\text{kHz}$ $f_B = 10\text{Hz}$ to 10kHz $f_B = 0.1\text{Hz}$ to 10Hz Current: $f_B = 0.1\text{Hz}$ to 10Hz $f_O = 0.1\text{Hz}$ to 20kHz			*			23			*		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ μVrms $\mu\text{Vp-p}$ $\text{fA}/\sqrt{\text{Hz}}$
OFFSET VOLTAGE Input Offset Voltage: M Package P Package U Package Over Specified Temperature M Package P, U Packages Average Drift Supply Rejection	$V_{CM} = 0\text{VDC}$ $T_A = T_{MIN}$ to T_{MAX} $\pm V_S = 12\text{V}$ to 18V		± 300 1 1 ± 550 ± 1.5 * *	± 1000 2 3 ± 15		± 150 0.5 ± 250 ± 0.75 ± 3 100	± 500 1 ± 1000 ± 1.5 ± 5		± 100 ± 200 * *	± 250 ± 500 ± 2	μV mV mV μV mV $\mu\text{V}/^\circ\text{C}$ dB
BIAS CURRENT Input Bias Current Over Specified Temperature SM Grade	$V_{CM} = 0\text{VDC}$		± 2 ± 20	± 10 ± 500		± 1 ± 20 ± 200	± 2 ± 200 ± 2000		± 0.5 ± 10	± 1 ± 100	pA pA pA
OFFSET CURRENT Input Offset Current Over Specified Temperature SM Grade	$V_{CM} = 0\text{VDC}$		1 20	10 500		0.5 20 200	2 200 1000		0.5 10	1 100	pA pA pA
INPUT IMPEDANCE Differential Common-Mode			* *			$10^{13} \parallel 1$ $10^{14} \parallel 3$			* *		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	* 75	* *		± 10.2 88	$+13$, -11 100		* 92	* *		V dB
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 1\text{k}\Omega$	75	*		88	100		92	*		dB
FREQUENCY RESPONSE Gain Bandwidth Full Power Response Slew Rate Settling Time: 0.1% 0.01%	Gain = 100 20Vp-p, $R_L = 1\text{k}\Omega$ $V_O = \pm 10\text{V}$, $R_L = 1\text{k}\Omega$ Gain = -1, $R_L = 1\text{k}\Omega$ $C_L = 500\text{pF}$, 10V Step	3.5 20	* * * * *		4 24	6.5 570 35 0.6 1.0		5 28	* * * * *		MHz kHz V/ μs μs μs
RATED OUTPUT Voltage Output Current Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 1\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ 1MHz, Open Loop Gain = +1	± 11 * ± 25	* * * * *		± 11.5 ± 15 ± 30	$+12.9$, -13.8 ± 20 80 1500 ± 50		* * *	* * * * *		V mA Ω pF mA
POWER SUPPLY Rated Voltage Voltage Range, Derated Performance Current, Quiescent Over Specified Temperature	$I_O = 0\text{mA}$		* * * *		± 5	± 15 3 3.5	± 18 4 4.5		* * * *		VDC VDC mA mA
TEMPERATURE RANGE Specification SM Grade Operating: M Package P, U Packages Storage: M Package P, U Packages θ_{JA}	Ambient Temperature Ambient Temperature Ambient Temperature	* * -25 * -40		* * +85 * +125	-25 -55 -55 -25 -65 -40		+85 +125 +125 +85 +150 +125			* * * * *	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C/W}$

* Same specifications as OPA602BM.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18VDC
Internal Power Dissipation ($T_J \leq +175^\circ\text{C}$)	1000mW
Differential Input Voltage	Total V_S
Input Voltage Range	$\pm V_S$
Storage Temperature Range	
M Package	-65°C to +150°C
P and U Packages	-40°C to +125°C
Operating Temperature Range	
M Package	-55°C to +125°C
P and U Packages	-25°C to +85°C
Lead Temperature	
M and P Packages (soldering, 10s)	+300°C
U Package, SOIC (3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous
Junction Temperature	+175°C

PACKAGE INFORMATION

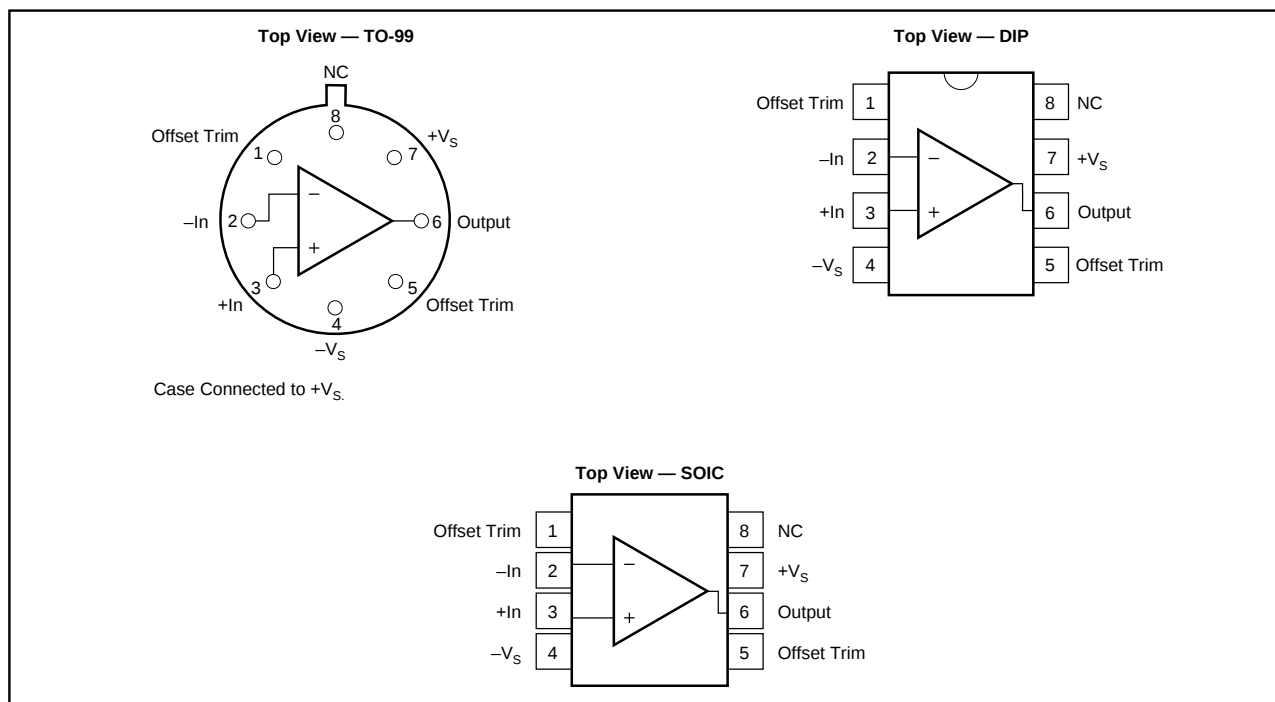
MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
OPA602AM	TO-99	001
OPA602BM	TO-99	001
OPA602CM	TO-99	001
OPA602SM	TO-99	001
OPA602AP	Plastic DIP	006
OPA602BP	Plastic DIP	006
OPA602AU	Plastic SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

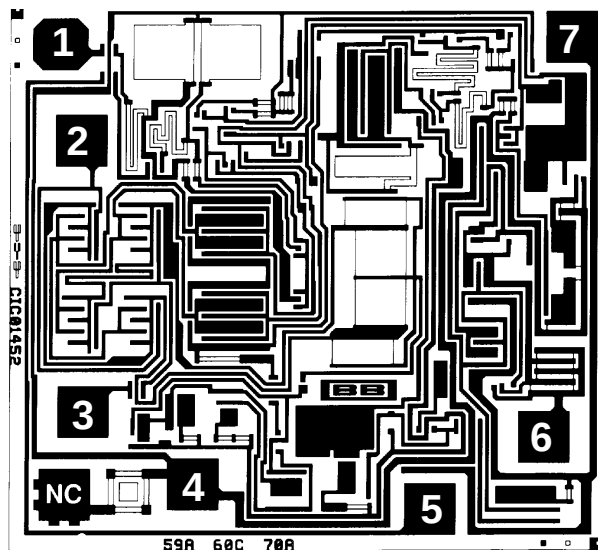
MODEL	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE MAX (μV) AT 25°C
OPA602AM	TO-99	-25 to +85°C	±1000
OPA602BM	TO-99	-25 to +85°C	±500
OPA602CM	TO-99	-25 to +85°C	±250
OPA602SM	TO-99	-55 to +125°C	±500
OPA602AP	Plastic DIP	-25 to +85°C	±2000
OPA602BP	Plastic DIP	-25 to +85°C	±1000
OPA602AU	Plastic SOIC	-25 to +85°C	±3000

PIN CONFIGURATIONS



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DICE INFORMATION



PAD	FUNCTION
1	Offset Trim
2	-In
3	+In
4	-V _S
5	Offset Trim
6	Output
7	+V _S

Substrate Bias: -V_S

NC: No Connection.

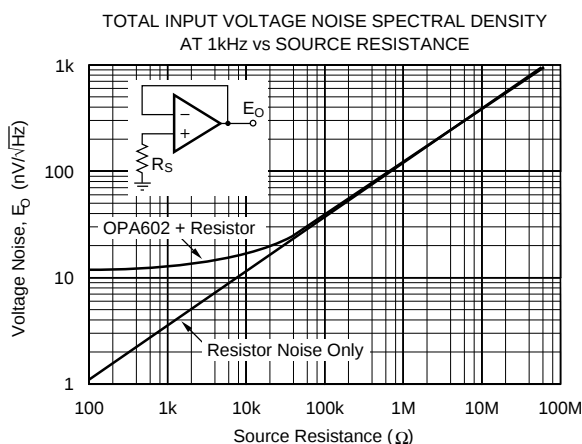
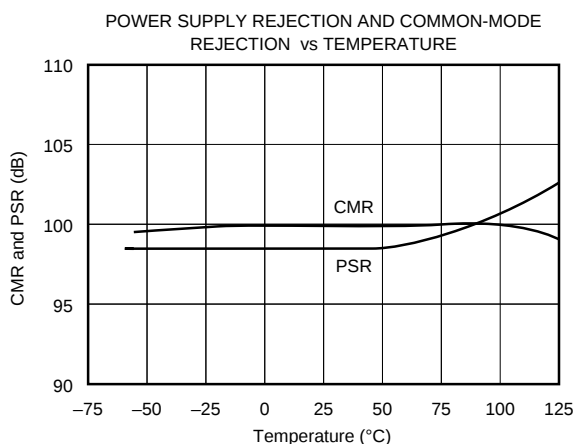
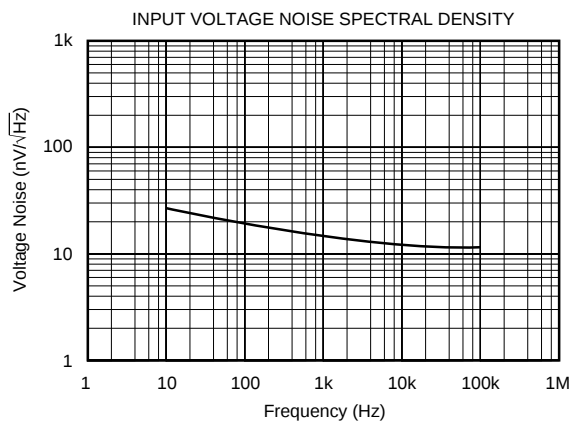
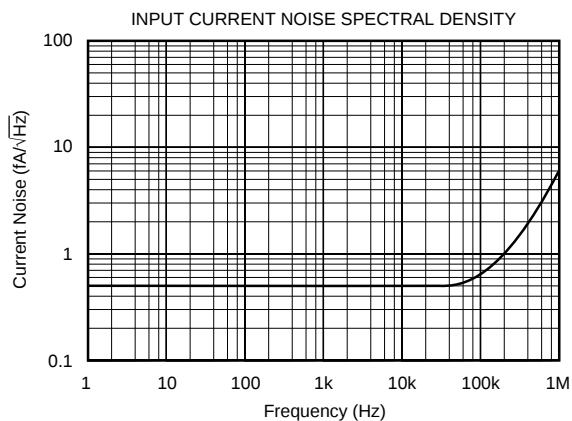
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	63 x 58 ±5	1.60 x 1.47 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	None	
Transistor Count	36	

OPA602 DIE TOPOGRAPHY

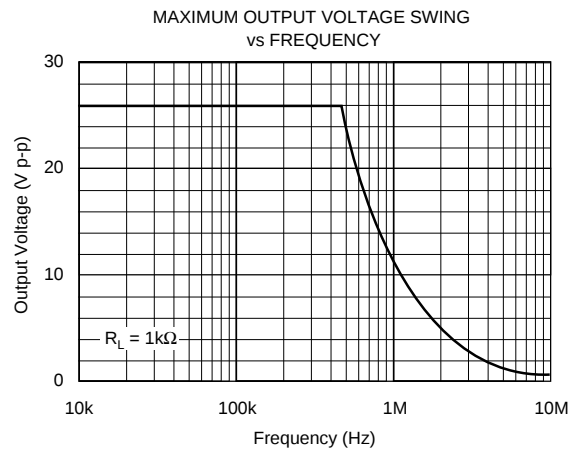
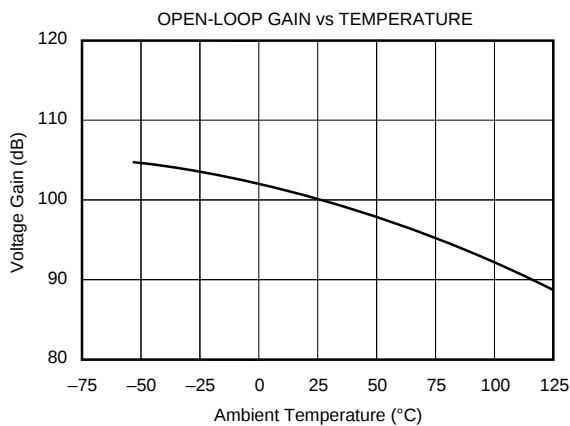
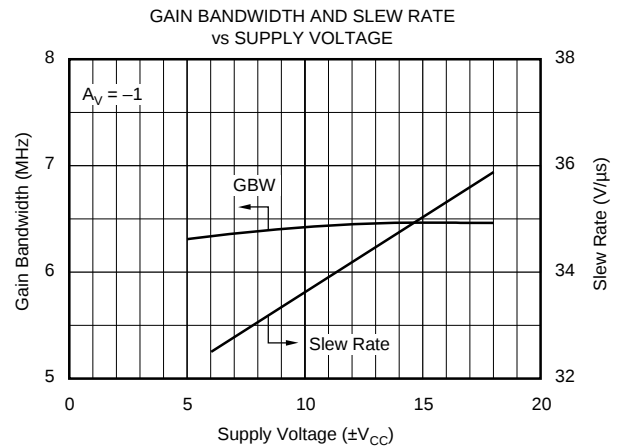
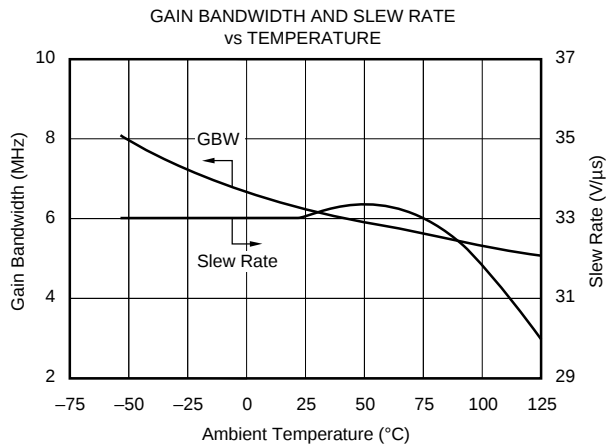
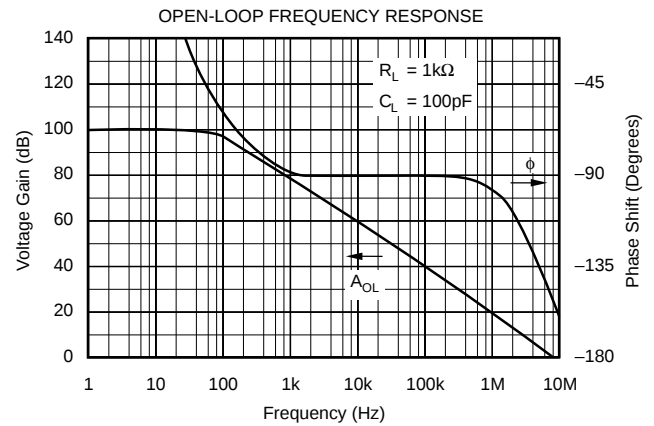
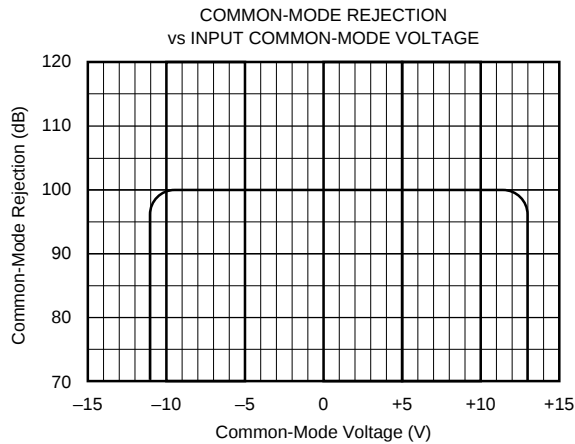
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15VDC unless otherwise noted.



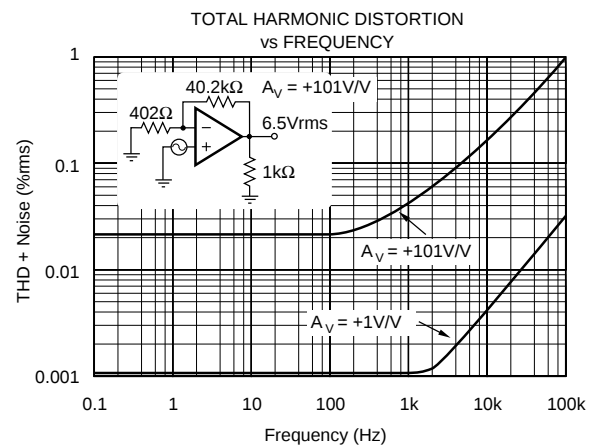
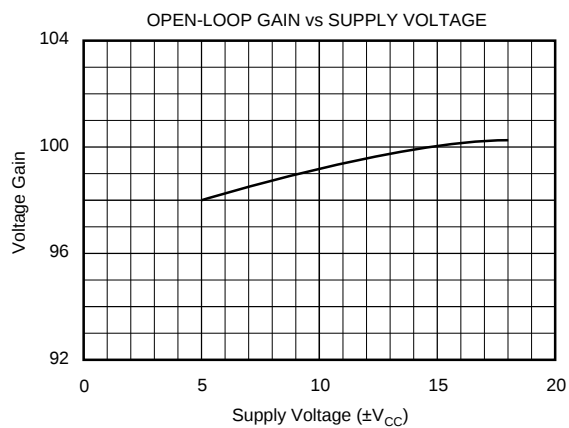
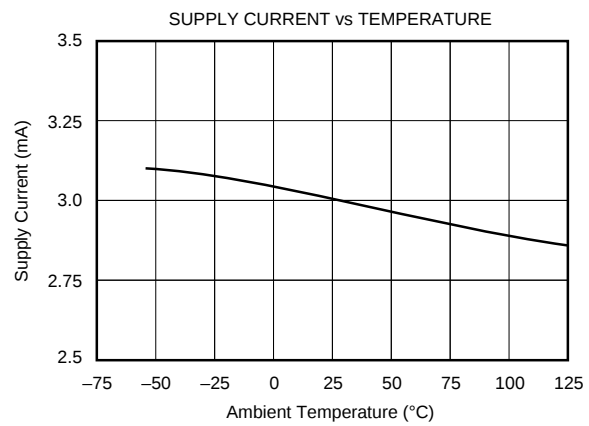
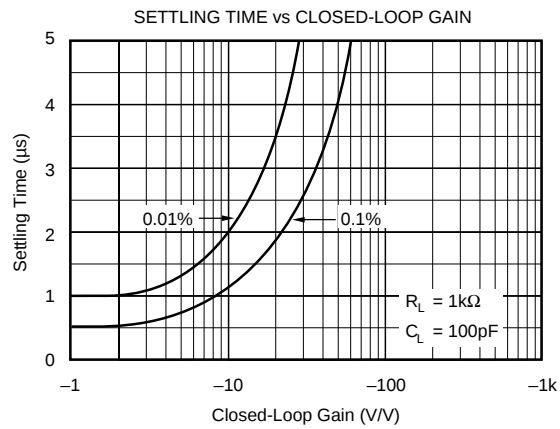
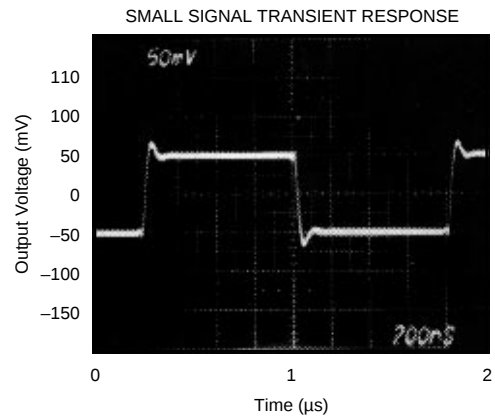
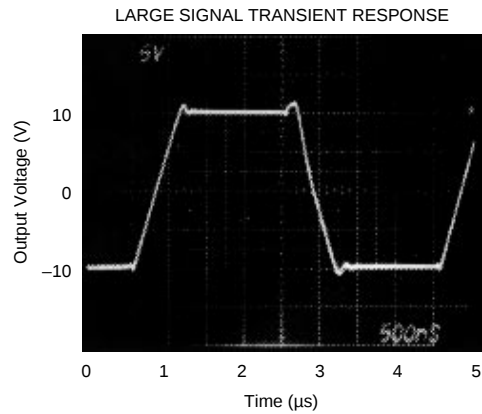
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{VDC}$ unless otherwise noted.



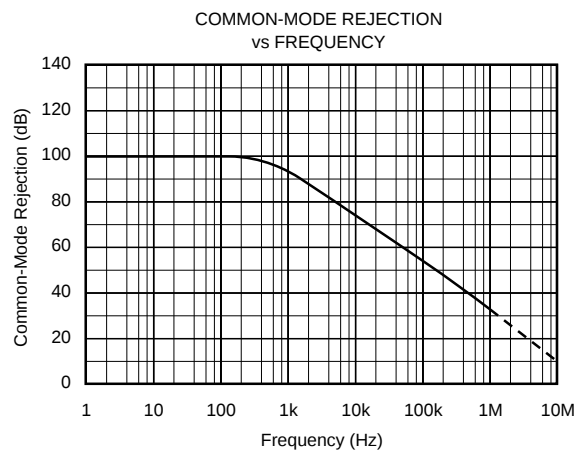
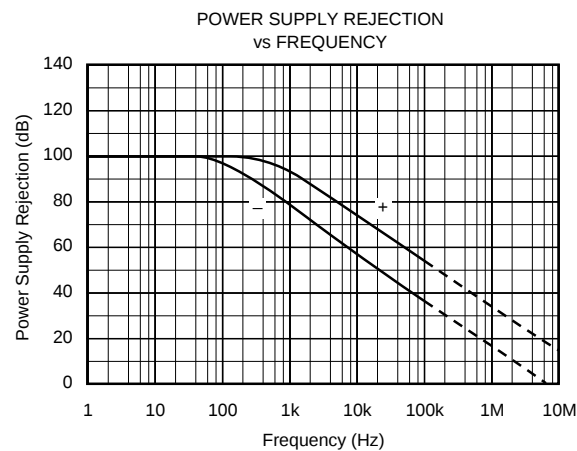
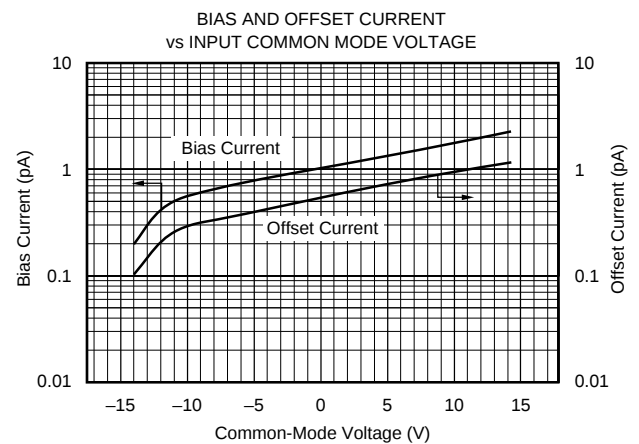
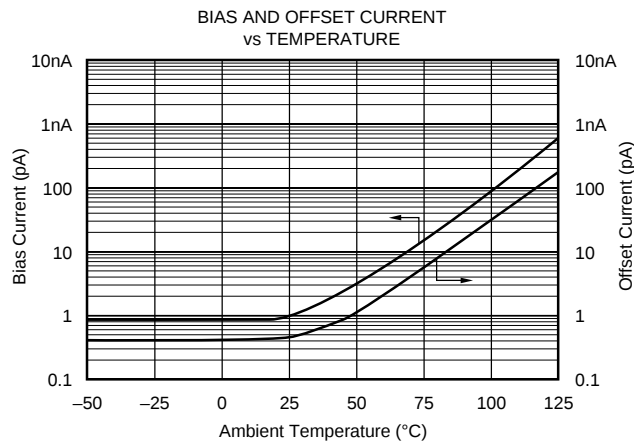
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{VDC}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{VDC}$ unless otherwise noted.



APPLICATIONS INFORMATION

Unity-gain stability with good phase margin and excellent output drive characteristics bring freedom from the subtle problems associated with other high speed amplifiers. But with any high speed, wide bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the inverting input pin.

Power supplies should be bypassed with good high frequency capacitors positioned close to the op amp pins. In most cases $0.1\mu\text{F}$ ceramic capacitors are adequate. Applications with heavier loads and fast transient waveforms may benefit from use of additional $1.0\mu\text{F}$ tantalum bypass capacitors.

INPUT BIAS CURRENT GUARDING

Leakage currents across printed circuit boards can easily exceed the input bias current of the OPA602. A circuit board “guard” pattern (Figure 1) is an effective solution to difficult leakage problems. This guard pattern must be repeated on all layers of a multilayer board. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage currents will flow harmlessly to the low impedance node.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be cleaned with appropriate solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at $+85^\circ\text{C}$.

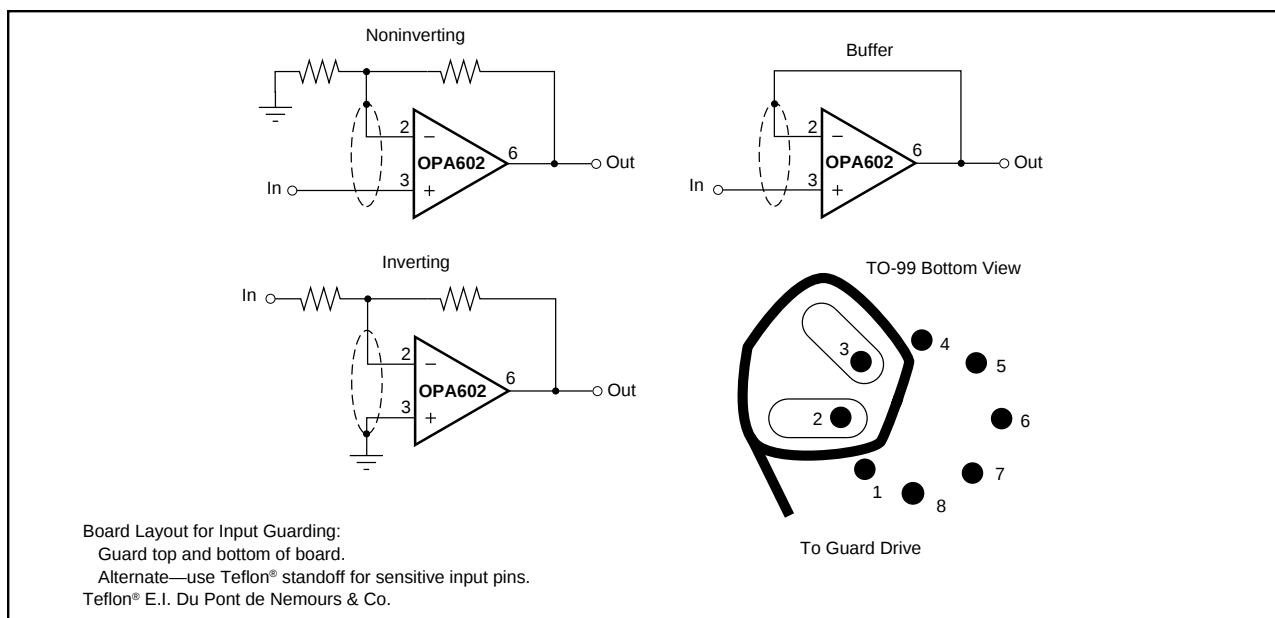


FIGURE 1. Connection of Input Guard.

APPLICATION CIRCUITS

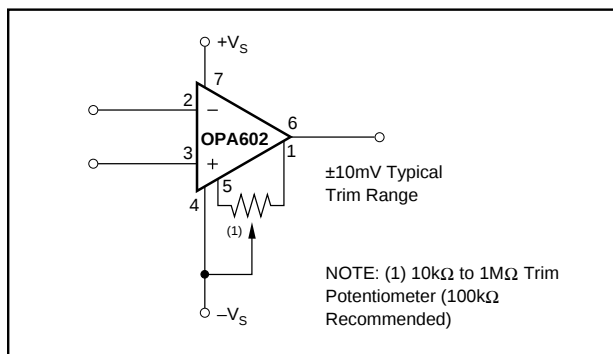


FIGURE 2. Offset Voltage Trim.

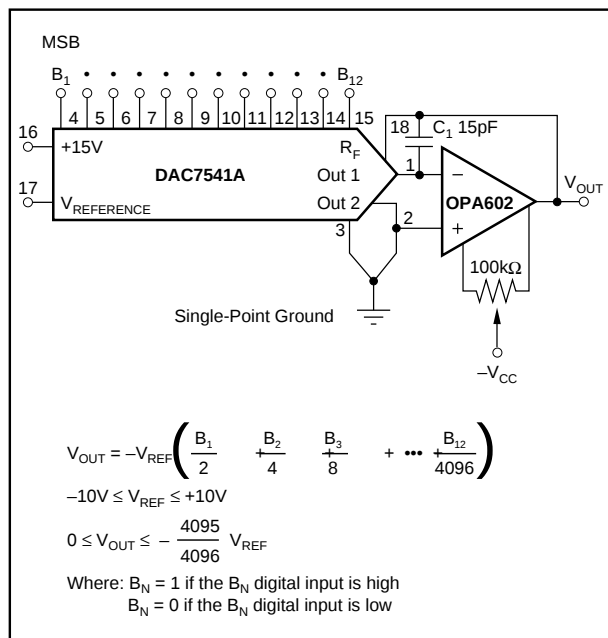


FIGURE 3. Voltage Output D/A Converter.

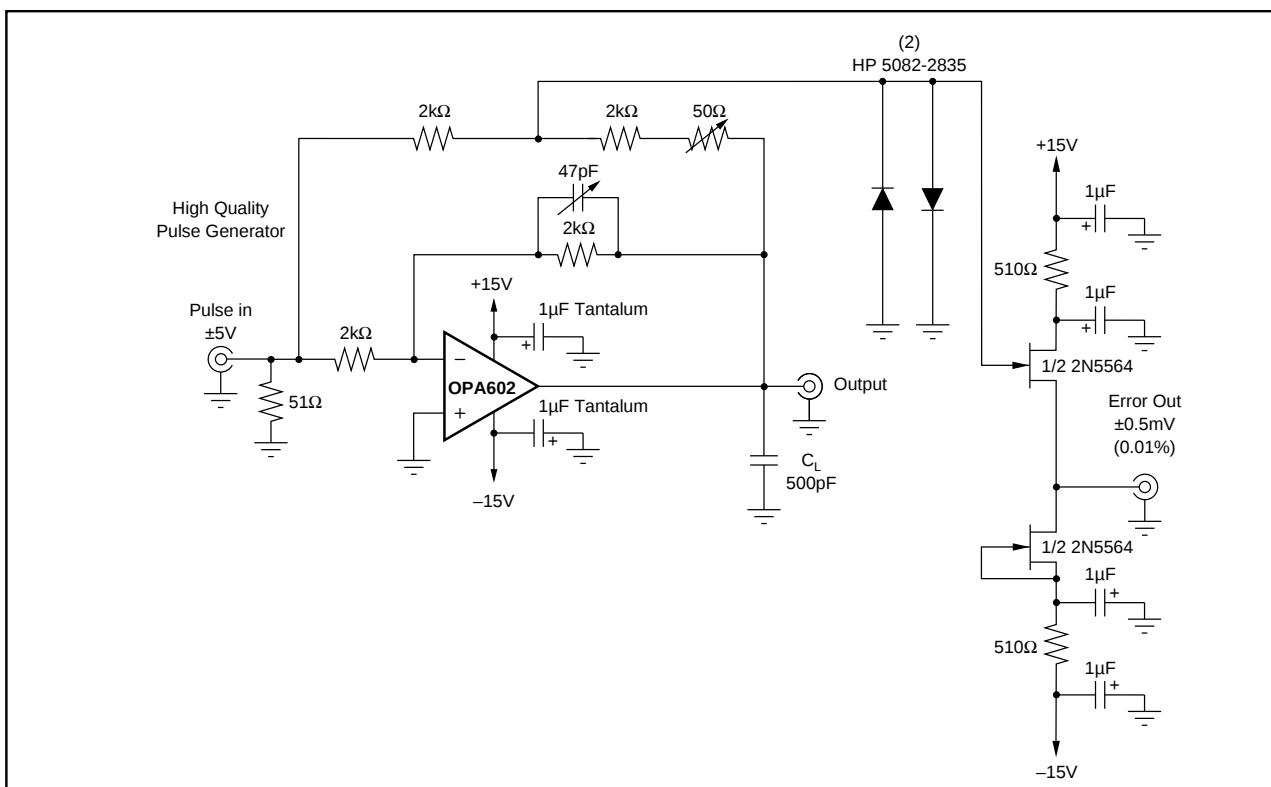


FIGURE 4. Settling Time and Slew Rate Test Circuit.