OPA2834 50-MHz, 170-µA, Negative-Rail In, Rail-to-Rail Out, Voltage-Feedback Amplifier

1 Features

- Ultra-low power:
  - Supply voltage: 2.7 V to 5.4 V
  - Quiescent current: 170 µA/ch (typical)
- Bandwidth: 50 MHz (G = 1 V/V)
- Slew rate: 26 V/µs
- HD_2, HD_3: –131 dBc, –146 dBc at 10 kHz (2 V_{PP})
- Input voltage noise: 12 nV/$\sqrt{Hz}$ (f = 10 kHz)
- Input offset voltage: 350 µV (±1.5 mV, maximum)
- Negative rail input, rail-to-rail output (RRO)
  - Input voltage range: –0.2 V to 3.9 V (5-V supply)
- Operating temperature range: –40°C to +125°C

2 Applications

- Current sensing in power supplies
- Low-power signal conditioning
- Vibration monitoring
- Field transmitters
- Wireless microphones
- Low-power SAR and ΔΣ ADC driver
- Ultrasonic flow meters

3 Description

The OPA2834 is a dual-channel, ultra-low-power, rail-to-rail output, negative-rail input, voltage-feedback (VFB) operational amplifier designed to operate over a power-supply range of 2.7 V to 5.4 V with a single supply, or ±1.35 V to ±2.7 V with a dual supply. Consuming only 170 µA per channel and with a unity-gain bandwidth of 50 MHz, this amplifier sets an industry-leading performance-to-power ratio for rail-to-rail amplifiers.

For battery-powered, portable applications where power is of key importance, the low power consumption, wide bandwidth, and ultra-low distortion performance of the OPA2834 offers performance versus power that is not attainable in other devices.

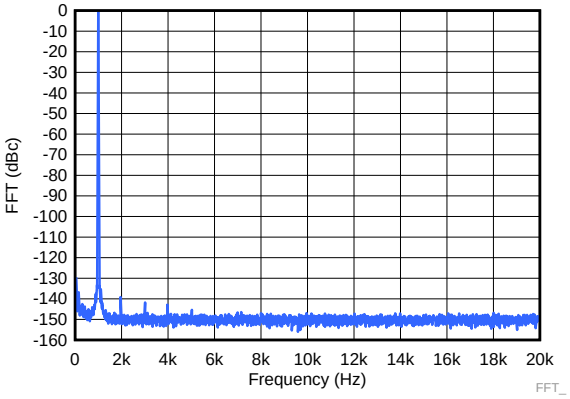
See the *Device Comparison Table* for a selection of low-power, low-noise, 5-V amplifiers from Texas Instruments with a gain-bandwidth product from 20 MHz to 300 MHz.

Device Information(1)

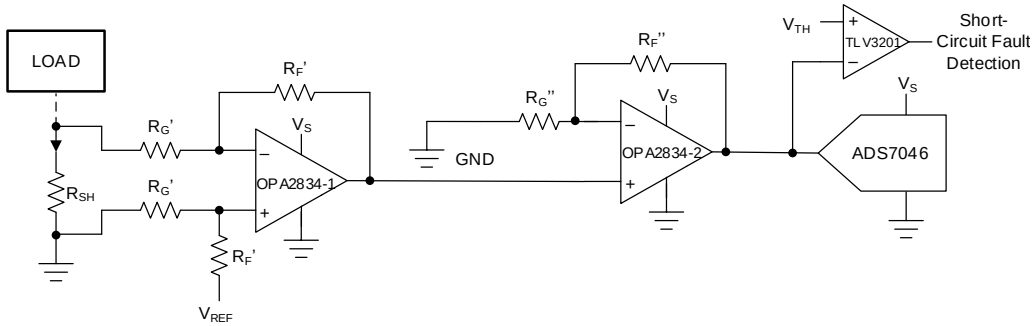
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2834	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

1-kHz FFT Plot; V_{OUT} = 1 V_{RMS}, R_L = 100 kΩ, G = 1



Low-Side Current-Shunt Monitoring Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

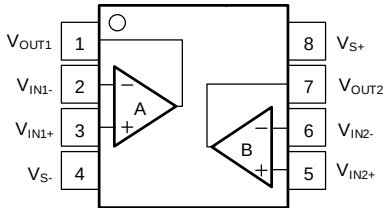
DATE	REVISION	NOTES
June 2019	*	Initial release.

5 Device Comparison Table

PART NUMBER	CHANNELS	A_V = +1 BANDWIDTH (MHz)	5-V I_Q (mA, Typ 25°C)	INPUT NOISE VOLTAGE (nV/√Hz)	2-V_{PP} THD (dBc, 100 kHz)	RAIL-TO-RAIL INPUT/OUTPUT	DUALS
OPA2834	2	50	0.17	12	–95	$V_{S–}$, output	—
OPA835	1	56	0.25	9.4	–104	$V_{S–}$, output	OPA2835
OPA836	1	205	1.0	4.6	–118	$V_{S–}$, output	OPA2836
OPA837	1	105	0.6	4.7	–118	$V_{S–}$, output	OPA2837
OPA838	1	—	0.96	1.9	–110	$V_{S–}$, output	—

6 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN		FUNCTION(1)	DESCRIPTION
NO.	NAME		
1	V_{OUT1}	O	Amplifier 1 output pin
2	$V_{IN1–}$	I	Amplifier 1 inverting input pin
3	V_{IN1+}	I	Amplifier 1 noninverting input pin
4	$V_{S–}$	P	Negative power-supply pin
5	V_{IN2+}	I	Amplifier 2 noninverting input pin
6	$V_{IN2–}$	I	Amplifier 2 inverting input pin
7	V_{OUT2}	O	Amplifier 2 output pin
8	V_{S+}	P	Positive power-supply input

(1) I = input, O = output, and P = power.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$V_{S–}$ to V_{S+}	Supply voltage (total bipolar supplies)(2)		5.5	V
	Supply turnon/off maximum dV/dT(3)		1	V/µs
V_I	Input voltage	$V_{S–}$ – 0.5	V_{S+} + 0.5	V
V_{ID}	Differential input voltage		±1	V
I_I	Continuous input current(4)		±10	mA
I_O	Continuous output current(5)		±20	mA
	Continuous power dissipation	See Thermal Information		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_S is the total supply voltage given by $V_S = V_{S+} – V_{S–}$.
(3) Staying below this ± supply turnon edge rate prevents the edge-triggered ESD absorption device across the supply pins from turning on.
(4) Continuous input current limit for both the ESD diodes to supply pins and amplifier differential input clamp diodes. The differential input clamp diodes limit the voltage across them to 1 V with this continuous input current flowing through them.
(5) Long-term continuous current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+}	Single-supply positive voltage	2.7	5	5.4	V
T_A	Ambient temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPA2834 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	114.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	15.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	112.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics: 5 V

at V_S = 5 V, R_F = 0 Ω, C_L = 4 pF, R_L = 5 kΩ referenced to mid-supply, G = 1 V/V, input and output V_{CM} = mid-supply, and T_A ≈ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1, < 1 dB peaking		50		MHz
		V_{OUT} = 20 mV_{PP}, G = 2, R_F = 3.65 kΩ		20		
GBWP	Gain-bandwidth product			20		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		6		MHz
	Bandwidth for 0.1-dB flatness	V_{OUT} = 20 mV_{PP}, G = 2, R_F = 3.65 kΩ		6		MHz
SR	Slew rate	V_{OUT} = 2–V step, 20% to 80%		26		V/µs
t_R, t_F	Rise, fall time	V_{OUT} = 200–mV step, input t_R = 1 ns		16		ns
	Settling time to 0.1%	V_{OUT} = 2–V step, input t_R = 50 ns		88		ns
	Settling time to 0.01%	V_{OUT} = 2–V step, input t_R = 50 ns		110		ns
	Over/Under Shoot	V_{OUT} = 2–V step, input t_R = 50 ns		0.45		%
	Overdrive recovery time	G = 2, 2x output overdrive		200		ns
HD2	Second-order harmonic distortion	f = 10 kHz, V_{OUT} = 2 V_{PP}		–131		dBc
HD3	Third-order harmonic distortion	f = 10 kHz, V_{OUT} = 2 V_{PP}		–146		dBc
e_N	Input voltage noise	f > 10 kHz		12		nV/√Hz
	Voltage noise 1/f corner frequency			150		Hz
i_N	Input current noise	f > 10 kHz		0.2		pA/√Hz
	Current noise 1/f corner frequency			900		Hz
z_O	Closed-loop output impedance	f = 100 kHz		0.15		Ω
	Channel-to-channel crosstalk	f = 100 kHz, V_{OUT} = 2 V_{PP}		–115		dBc
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = ±1 V	107	124		dB
V_{OS}	Input-referred offset voltage			0.35	1.5	mV
	Input offset voltage drift(1)	T_A = –40°C to +125°C		1.5		uV/°C
	Input bias current			50	90	nA
	Input offset current			8	30	nA
INPUT						
	Common-mode input range		V_{S-}–0.2		V_{S+}–1.1	V
CMRR	Common-mode rejection ratio	V_{CM} = V_{S-} to V_{S+}-1.1 V, T_A = 25°C	90	105		dB
	Input impedance common-mode			1050 || 1.1		MΩ || pF
	Input impedance differential mode			1 || 0.2		MΩ || pF
OUTPUT						
V_{OL}	Output voltage, low			V_{S-}+0.05	V_{S-}+0.1	V
V_{OH}	Output voltage, high		V_{S+}–0.1	V_{S+}–0.03		V
	Linear output drive (sourcing/sinking)	V_{OUT} = ±1 V, ΔV_{IO} < 1 mV	16	28		mA
	Closed-loop output impedance	G = 1, I_{OUT} = ±5 mA DC		1.1		mΩ
POWER SUPPLY						
I_Q	Quiescent current per amplifier			170	210	uA
PSRR	Power-supply rejection ratio	ΔV_S = 0.3 V	90	105		dB

(1) Based on electrical characterization of 32 devices. Minimum and maximum values are not specified by final automated test equipment (ATE) nor by QA sample testing. Typical specifications are ±1 sigma.

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7.6 Electrical Characteristics: 3 V

at V_S = 3 V, R_F = 0 Ω, C_L = 4 pF, R_L = 5 kΩ referenced to mid-supply, G = 1 V/V, input and output V_{CM} = mid-supply, and T_A ≈ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1, < 1 dB peaking		50		MHz
		V_{OUT} = 20 mV_{PP}, G = 2, R_F = 3.65 kΩ		20		
GBWP	Gain-bandwidth product			20		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}		9		MHz
	Bandwidth for 0.1-dB flatness	V_{OUT} = 20 mV_{PP}, G = 2, R_F = 3.65 kΩ		6		MHz
SR	Slew rate	V_{OUT} = 1–V step, 20% to 80%		17		V/µs
t_R, t_F	Rise, fall time	V_{OUT} = 200–mV step, input t_R = 1 ns		16		ns
	Settling time to 0.1%	V_{OUT} = 1–V step, input t_R = 25 ns		83		ns
	Settling time to 0.01%	V_{OUT} = 1–V step, input t_R = 25 ns		100		ns
	Over/Under Shoot	V_{OUT} = 1–V step, input t_R = 25 ns		0.6		%
	Overdrive recovery time	G = 2, 2x output overdrive		240		ns
HD2	Second-order harmonic distortion	f = 10 kHz, V_{OUT} = 1 V_{PP}		-136		dBc
HD3	Third-order harmonic distortion	f = 10 kHz, V_{OUT} = 1 V_{PP}		-143		dBc
e_N	Input voltage noise	f > 10 kHz		12		nV/√Hz
	Voltage noise 1/f corner frequency			150		Hz
i_N	Input current noise	f > 10 kHz		0.2		pA/√Hz
	Current noise 1/f corner frequency			900		Hz
z_O	Closed-loop output impedance	f = 100 kHz		0.15		Ω
	Channel-to-channel crosstalk	f = 100 kHz, V_{OUT} = 1 V_{PP}		–115		dBc
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = ±1 V	107	124		dB
V_{OS}	Input-referred offset voltage			0.35	1.5	mV
	Input offset voltage drift(1)	T_A = –40°C to +125°C		1.5		uV/°C
	Input bias current			50	90	nA
	Input offset current			8	30	nA
INPUT						
	Common-mode input range		V_{S-}–0.2		V_{S+}–1.1	V
CMRR	Common-mode rejection ratio	V_{CM} = V_{S-} to V_{S+}-1.1 V, T_A ≈ 25°C	90	104		dB
	Input impedance common-mode			1750 || 1.1		MΩ || pF
	Input impedance differential mode			1 || 0.2		MΩ || pF
OUTPUT						
V_{OL}	Output voltage, low			V_{S-}+0.05	V_{S-}+0.1	V
V_{OH}	Output voltage, high		V_{S+}–0.1	V_{S+}–0.03		V
	Linear output drive (sourcing/sinking)	V_{OUT} = ±1 V, ΔV_{IO} < 1 mV	11	13.5		mA
	Closed-loop output impedance	G = 1, I_{OUT} = ±5 mA DC		1.1		mΩ
POWER SUPPLY						
I_Q	Quiescent current per amplifier			165	198	uA
PSRR	Power-supply rejection ratio	ΔV_S = 0.3 V	90	103		dB

(1) Based on electrical characterization of 32 devices. Minimum and maximum values are not specified by final automated test equipment (ATE) nor by QA sample testing. Typical specifications are ±1 sigma.

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8 Detailed Description

8.1 Overview

The OPA2834 bipolar-input operational amplifier offers excellent bandwidth of 50 MHz with ultra-low THD of 0.00002% at 1 kHz. The device can swing to within 100 mV of the supply rails while driving a 5-kΩ load. The input common-mode of the amplifier can swing to 200 mV below the negative supply rail. This level of performance is achieved at 170 µA of quiescent current per amplifier channel.

8.2 Functional Block Diagrams

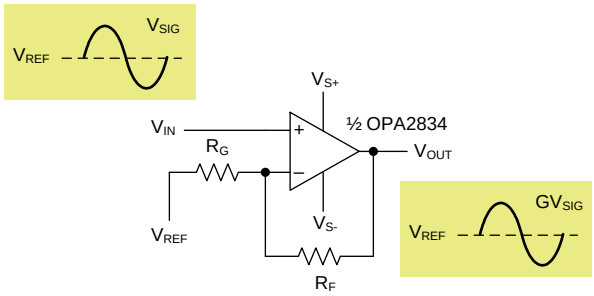

Figure 1. Noninverting Amplifier

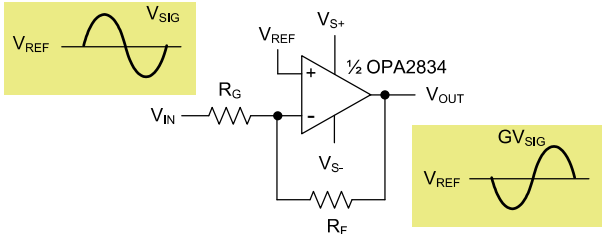

Figure 2. Inverting Amplifier

8.3 Feature Description

8.3.1 Input Common-Mode Voltage Range

When the primary design goal is a linear amplifier circuit with high CMRR, do not violate the input common-mode voltage range (V_{ICR}) of the op amp. The typical specifications are 0.2 V below the negative rail and 1.1 V below the positive rail. The limits cover all process variations, and most devices are better than specified.

Assuming the op amp is in linear operation, the voltage difference between the input pins is small (ideally 0 V); and the input common-mode voltage is analyzed at either input pin with the other input pin assumed to be at the same potential. The voltage at V_{IN+} is simple to evaluate. In a noninverting configuration, as shown in Figure 1, the input signal, V_{IN}, must not violate the V_{ICR}. In an inverting configuration, as shown in Figure 2, the reference voltage, V_{REF}, must be within the V_{ICR}.

The input voltage limits have fixed headroom to the power rails and track the power-supply voltages. For a 5-V supply, the linear input voltage ranges from –0.2 V to 3.9 V and –0.2 V to 1.6 V for a 2.7-V supply. The delta headroom from each power-supply rail is the same in either case: –0.2 V and 1.1 V.

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Feature Description (continued)

8.3.2 Output Voltage Range

The OPA2834 is a rail-to-rail output (RRO) op amp. Rail-to-rail output typically means that the output voltage swings within a couple hundred millivolts of the supply rails. There are different ways to specify this: one is with the output still in linear operation and another is with the output saturated. Saturated output voltages are closer to the power-supply rails than linear outputs, but the signal is not a linear representation of the input. Linear output is a better representation of how well a device performs when used as a linear amplifier. Saturation and linear operation limits are affected by the output current, where higher currents lead to more loss in the output transistors.

The specification tables list the saturated output voltage specifications with a 5-kΩ load. Given a light load, the output voltage limits have nearly constant headroom to the power rails and track the power-supply voltages. For example, with a 5-kΩ load and a single 5-V supply, the saturation output voltage ranges from 0.1 V to 4.9 V and ranges from 0.1 V to 2.6 V for a 2.7-V supply. The delta from each power-supply rail is the same in either case: 0.1 V and 0.1 V.

With a device such as the OPA2834 where the input range is lower than the output range, typically the input limits the available signal swing only in a noninverting gain of 1. Signal swing in noninverting configurations in gains greater than +1 and inverting configurations in any gain is typically limited by the output voltage limits of the op amp.

8.3.3 Low-Power Applications and the Effects of Resistor Values on Bandwidth

The OPA2834 is designed for the nominal value of R_F to be 3.6 kΩ in gains other than +1. This setting gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. This feedback resistor also loads the amplifier. For example, in a gain of 2 with $R_F = R_G = 3.6$ kΩ, R_G to ground, and $V_{OUT} = 4$ V, 555 µA of current flows through the feedback path to ground. In a gain of +1, R_G is open and no current flows to ground. In low-power applications, reduce the current in the feedback path by increasing the gain-setting resistors values. Using larger value gain resistors has two primary side effects (other than lower power) because of their interaction with parasitic circuit capacitance:

- Lowers the bandwidth
- Lowers the phase margin
  - Causes peaking in the frequency response
  - Causes overshoot and ringing in the pulse response

Figure 3 shows the small-signal frequency response for a noninverting gain of 2 with R_F and R_G equal to 2 kΩ, 3.6 kΩ, 5 kΩ, 10 kΩ, and 100 kΩ. The test was done with $R_L = 5$ kΩ. Because of the loading effects of R_L, lower R_L values can reduce the peaking, but higher values do not have a significant effect.

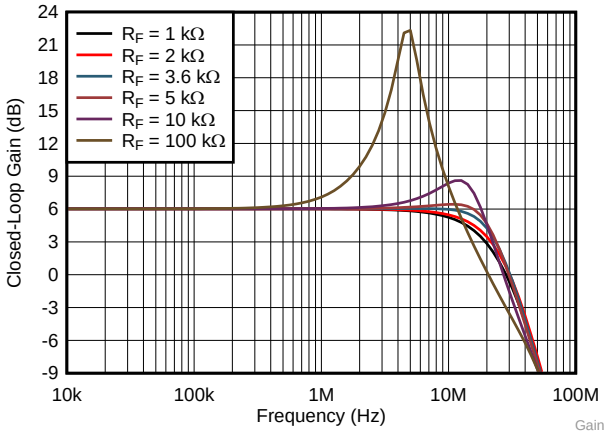

Figure 3. Frequency Response With Various Gain-Setting Resistor Values

Feature Description (continued)

As expected, larger value gain resistors cause lower bandwidth and peaking in the response (peaking in the frequency response is synonymous with overshoot and ringing in the pulse response). Adding 1-pF capacitors in parallel with R_F helps compensate the phase margin and restores flat frequency response. Figure 4 shows the test circuit.

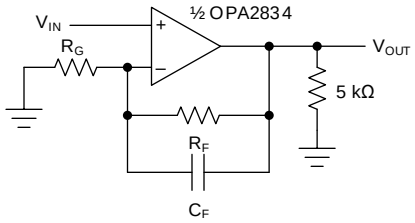

Figure 4. G = 2 Test Circuit for Various Gain-Setting Resistor Values

8.3.4 Driving Capacitive Loads

The OPA2834 drives up to a nominal capacitive load of 10 pF on the output with no special consideration. When driving capacitive loads greater than 10 pF, TI recommends using a small resistor (R_O) in series with the output as close to the device as possible. Without R_O, output capacitance interacts with the output impedance of the amplifier causing phase shift in the loop gain of the amplifier that reduces the phase margin. This reduction in the phase margin causes peaking in the frequency response and overshoot and ringing in the pulse response. Interaction with other parasitic elements can lead to instability or oscillation. Inserting R_O isolates the phase shift from the loop gain path and restores the phase margin; however R_O can limit the bandwidth slightly. Figure 5 shows a diagram of driving capacitive loads.

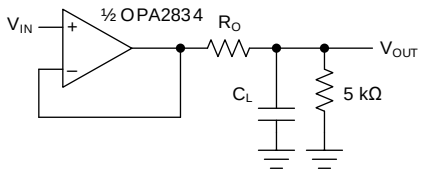

Figure 5. Driving Capacitive Loads With the OPA2834

8.4 Device Functional Modes

8.4.1 Split-Supply Operation (±1.35 V to ±2.7 V)

To facilitate testing with common lab equipment, the OPA2834EVM (see the *OPA2837DGK Evaluation Module* user guide) is built to allow split-supply operation. This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers, and other lab equipment have inputs and outputs with a ground reference.

Figure 6 shows a simple noninverting configuration analogous to Figure 1 with a ±2.5-V supply and V_{REF} equal to ground. The input and output swing symmetrically around ground. For ease of use, split supplies are preferred in systems where signals swing around ground.

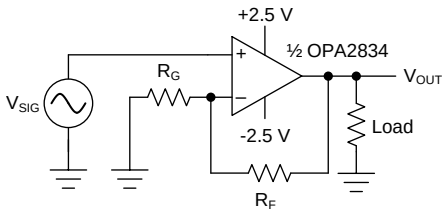

Figure 6. Split-Supply Operation

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Device Functional Modes (continued)

8.4.2 Single-Supply Operation (2.7 V to 5.4 V)

Often, newer systems use a single power supply to improve efficiency and reduce the cost of the power supply. The OPA2834 is designed for use with single-supply power operation and can be used with single-supply power with no change in performance from split supply, as long as the input and output are biased within the linear operation of the device.

To change the circuit from split-supply to single-supply, level shift all voltages by half the difference between the power-supply rails. For example, Figure 7 shows changing from a ±2.5-V split supply to a 5-V single-supply.

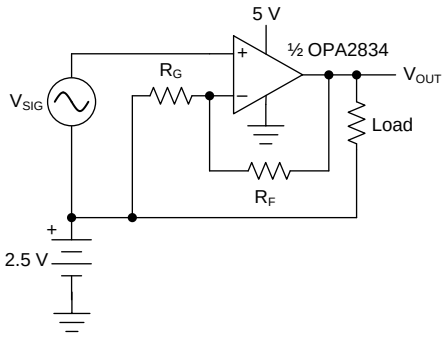


Figure 7. Single-Supply Concept

A practical circuit has an amplifier or some other circuit providing the bias voltage for the input, and the output of this amplifier stage provides the bias for the next stage.

Figure 8 shows a typical noninverting amplifier circuit. With a 5-V single-supply, a mid-supply reference generator is needed to bias the negative side through R_G. To cancel the voltage offset that is otherwise caused by the input bias currents, R_1 is selected to be equal to R_F in parallel with R_G. For example, if a gain of 2 is required and R_F = 3.6 kΩ, select R_G = 3.6 kΩ to set the gain, and R_1 = 1.8 kΩ for bias current cancellation. The value for C is dependent on the reference, and TI recommends a value of at least 0.1 µF to limit noise.

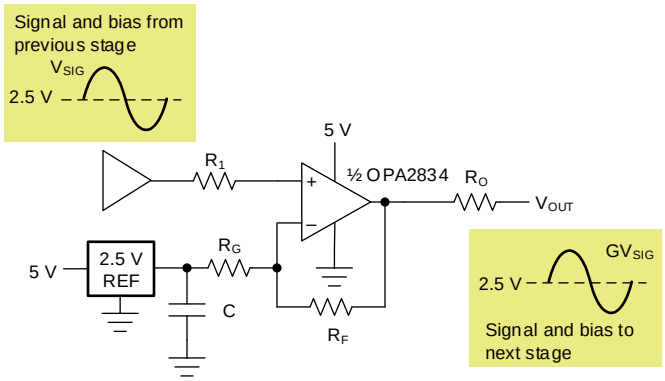


Figure 8. Noninverting Single Supply With Reference

Figure 9 illustrates a similar noninverting single-supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. R_G' and R_G" form a resistor divider from the 5-V supply and are used to bias the negative side with the parallel sum equal to the equivalent R_G to set the gain. To cancel the voltage offset that is otherwise caused by the input bias currents, R_1 is selected to be equal to R_F in parallel with R_G' in parallel with R_G" (R_1= R_F || R_G' || R_G"). For example, if a gain of 2 is required and R_F = 3.6 kΩ, selecting R_G' = R_G" = 7.2 kΩ gives an equivalent parallel sum of 3.6 kΩ, sets the gain to 2, and references the input to mid supply (2.5 V). R_1 is set to 1.8 kΩ for bias current cancellation. The resistor divider costs less than the 2.5-V reference in Figure 9 but can increase the current from the 5-V supply.

Device Functional Modes (continued)

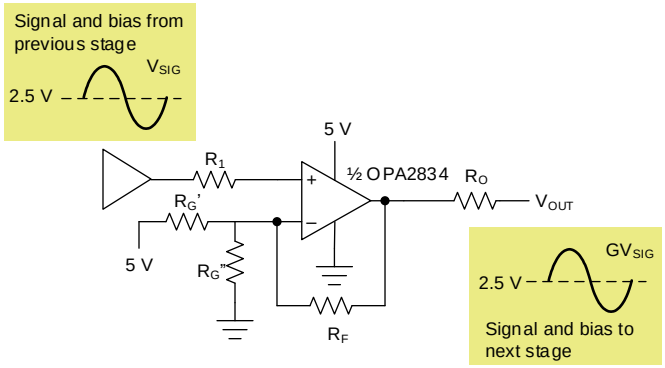


Figure 9. Noninverting Single Supply With Resistors

Figure 10 shows a typical inverting-amplifier circuit. With a 5-V single-supply, a mid-supply reference generator is needed to bias the positive side through R_1. To cancel the voltage offset that is otherwise caused by the input bias currents, R_1 is selected to be equal to R_F in parallel with R_G. For example, if a gain of –2 is required and R_F = 3.6 kΩ, select R_G = 1.8 kΩ to set the gain and R_1 = 1.2 kΩ for bias current cancellation. The value for C is dependent on the reference, but TI recommends a value of at least 0.1 µF to limit noise into the op amp.

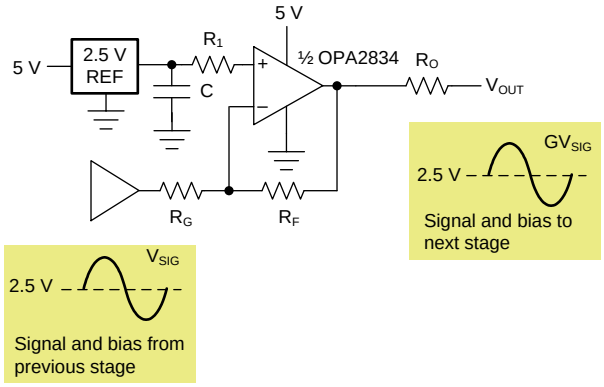


Figure 10. Inverting Single Supply With Reference

Figure 11 illustrates a similar inverting single-supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. R_1 and R_2 form a resistor divider from the 5-V supply and are used to bias the positive side. To cancel the voltage offset that is otherwise caused by the input bias currents, set the parallel sum of R_1 and R_2 equal to the parallel sum of R_F and R_G. C must be added to limit the coupling of noise into the positive input. For example, if a gain of –2 is required and R_F = 3.6 kΩ, select R_G = 1.8 kΩ to set the gain. R_1 = R_2 = 2.4 kΩ for the mid-supply voltage bias and for op-amp input-bias current cancellation. A good value for C is 0.1 µF. The resistor divider costs less than the 2.5-V reference in Figure 11 but can increase the current from the 5-V supply.

ADVANCE INFORMATION

Device Functional Modes (continued)

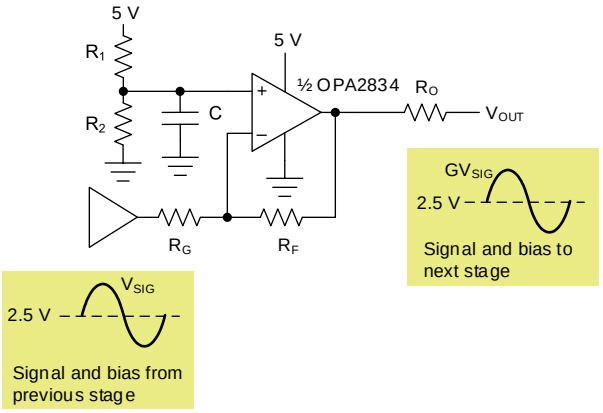


Figure 11. Inverting Single Supply With Resistors

ADVANCE INFORMATION

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Noninverting Amplifier

The OPA2834 can be used as a noninverting amplifier with a signal input to the noninverting input, V_{IN+}. Figure 1 shows a basic block diagram of the circuit.

The amplifier output can be calculated according to Equation 1 if $V_{IN} = V_{REF} + V_{SIG}$.

$$V_{OUT} = V_{SIG}\left(1 + \frac{R_F}{R_G}\right) + V_{REF} \quad (1)$$

The signal gain of the circuit is set by $G = 1 + \frac{R_F}{R_G}$, and V_{REF} provides a reference around which the input and output signals swing. Output signals are in-phase with the input signals.

The OPA2834 is designed for the nominal value of R_F to be 3.6 kΩ in gains other than +1. This value gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. R_F = 3.6 kΩ must be used as a default unless other design goals require changing to other values. All test circuits used to collect data for this document have R_F = 3.6 kΩ for all gains other than +1. A gain of +1 is a special case where R_F is shorted and R_G is left open.

9.1.2 Inverting Amplifier

The OPA2834 can be used as an inverting amplifier with a signal input to the inverting input, $V_{IN–}$, through the gain-setting resistor R_G. Figure 2 shows a basic block diagram of the circuit.

The output of the amplifier can be calculated according to Equation 2 if $V_{IN} = V_{REF} + V_{SIG}$.

$$V_{OUT} = V_{SIG}\left(\frac{-R_F}{R_G}\right) + V_{REF} \quad (2)$$

Application Information (continued)

The signal gain of the circuit is given by $G = \frac{-R_F}{R_G}$ and V_{REF} provides a reference point around which the input and output signals swing. Output signals are 180° out-of-phase with the input signals. The nominal value of R_F must be 3.6 kΩ for inverting gains.

9.2 Typical Applications

9.2.1 Low-Side Current Sensing

Power stages use current feedback for phase current control and regulation. One of the commonly used methods for this current measurement is low-side current shunt monitoring. Figure 12 shows a representative schematic of such a system. The use of the OPA2834 is described in this section for a low-side current-shunt monitoring application.

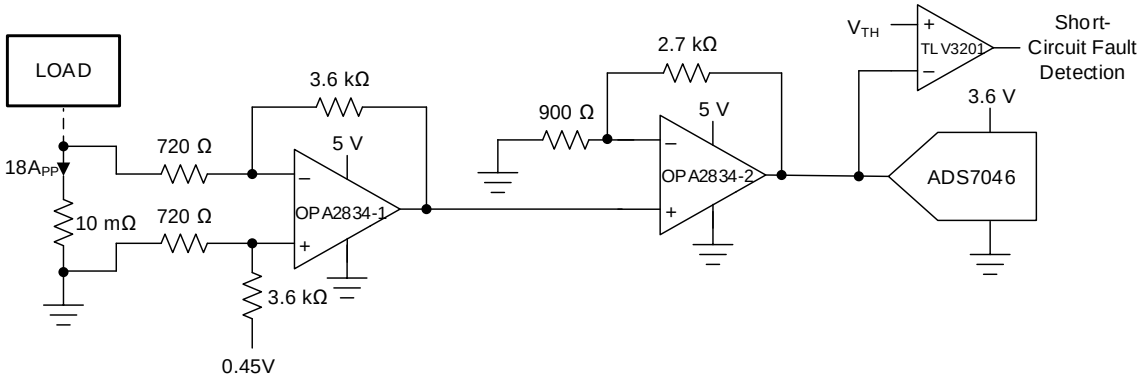


Figure 12. Low-Side Current Sensing

9.2.1.1 Design Requirements

The OPA2834 is used in a gain of 20 V/V while also driving the input of the ADS7046 when sampling at 1 MSPS. A comparator is connected to the ADC input for short-circuit fault detection. This design example is illustrated for the following specifications:

- Switching frequency: 50 kHz
- Shunt resistance: 10 mΩ
- Load current: 18 A_{PP}
- Output voltage: 3.6 V_{PP}
- Amplifier supply voltage: 5 V

9.2.1.2 Detailed Design Procedure

One of the channels of the OPA2834 is connected to the shunt resistor in Figure 12 in a 5-V/V difference amplifier configuration. Equation 3 gives the gain of this circuit.

$$V_{OUT} = \left(\frac{R_F}{R_G}\right)\left(V_2 - V_1\right) \quad (3)$$

where

- R_F and R_G are the feedback and gain resistors for channel A of the OPA2834

ADVANCE INFORMATION

Typical Applications (continued)

The values of R_F and R_G depend on multiple factors. Using small resistors in the feedback network helps reduce output noise and improve measurement accuracy. Small feedback resistors result in a larger power dissipation in the amplifier output stage. In order to reduce this power dissipation, large-value resistors reduce the phase margin and cause gain peaking; see Figure 3. Select the values of R_F and R_G from the recommended range of values for this device. As given in Equation 4, care must be taken to use a gain resistor value large enough to limit the current through the input ESD diodes to within 10 mA for a 10-V input transient with the amplifier powered off a 5-V supply.

$$R_G = \frac{V_{IN} - V_D - V_S}{I_{D,Max}} \quad (4)$$

where

- V_{IN} is the input transient voltage
- V_D is the ESD diode forward voltage drop
- I_D is the current resulting from this input transient flowing through the ESD diode

A total gain of 20 V/V is required from the amplifier stage. An amplifier bandwidth of 5 MHz is needed to drive the ADS7046 input. Because of this requirement, the two amplifier channels are configured in gains of 5 V/V and 4 V/V respectively. The ADC input common-mode voltage must be biased at mid-supply (that is, 1.8 V). The 0.45-V reference input to the noninverting input of channel 1 sets its output common-mode voltage to 0.45 V. This voltage is gained by 4 V/V with channel 2 to give a 1.8-V input common-mode voltage to the ADC. The two channels of the OPA2834 together provide a signal gain of 20 V/V.

The ADS7046 samples at 1 MSPS with a 40-MHz clock to allow for a sufficient acquisition time for the driver amplifier settling. The ADS7046, with this setting, exhibits an acquisition time of approximately 625 ns. The driver amplifier must settle within this time period. Figure 13 shows the TINA simulation plots for channel 2 of the OPA2834 driving the ADS7046. Here, V_{IN} is the signal swing at the channel noninverting input, CH-B Out is the signal at the ADC input, V_{SH} is the voltage on the sample-and-hold capacitor internal to the ADC, and error % is the percent error in V_{SH} from its steady state value. V_{SH} must settle within the acquisition time for the ADC to digitize the analog-input signal with the required accuracy. The OPA2834 settles to 0.1% accuracy within 500 ns with a worst-case, 3.6-V full-scale transient output. Using a slower clock with the same sampling rate causes the ENOB to reduce. This reduction in ENOB is restored with a lower sampling frequency or use of wider bandwidth amplifiers from the OPA83x family of products.

9.2.1.3 Application Curve

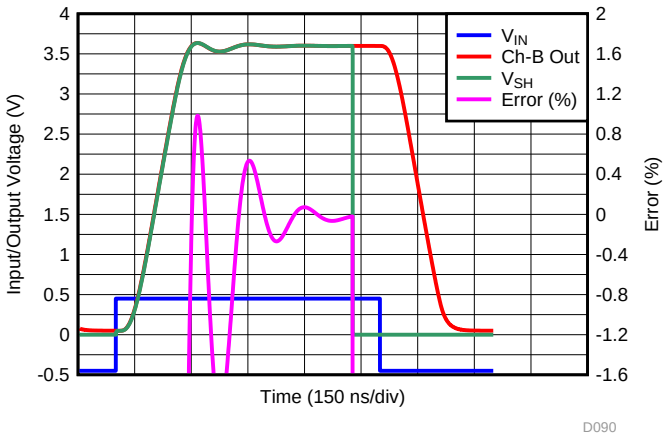


Figure 13. OPA2834 Settling Performance With the ADS7046

ADVANCE INFORMATION

Typical Applications (continued)

9.2.2 Field Transmitter Sensor Interface

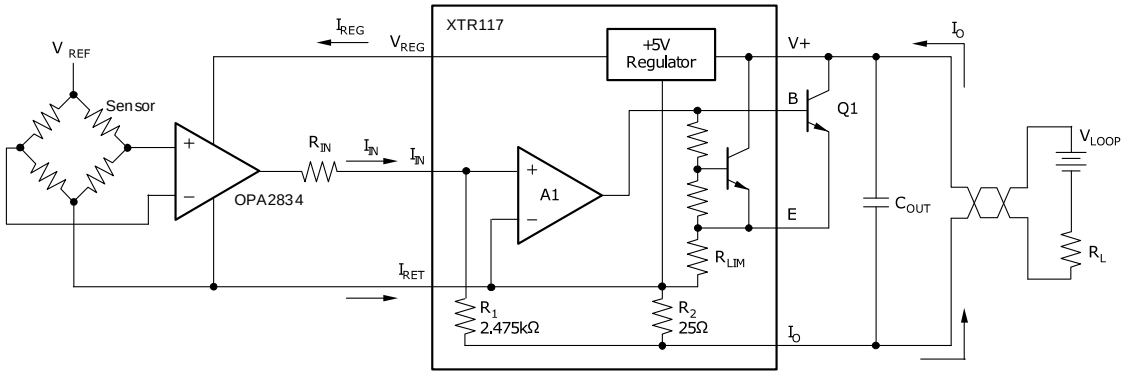


Figure 14. Field Transmitter Sensor Interface

9.2.3 Ultrasonic Flow Meters

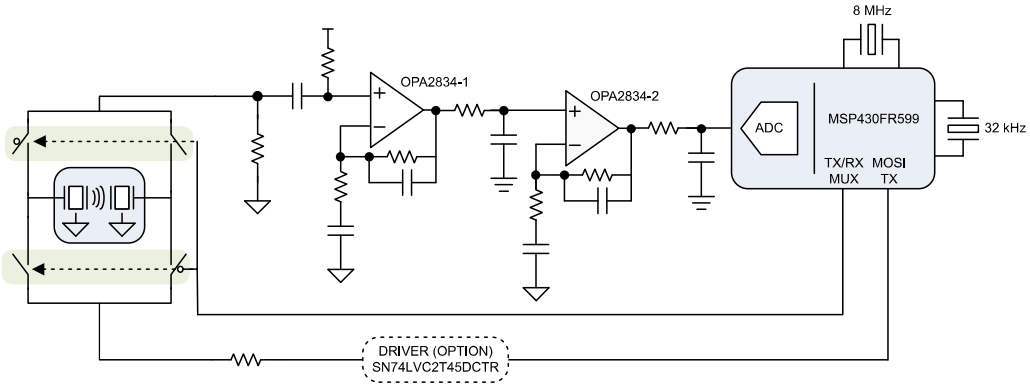


Figure 15. Ultrasonic Flow Meters Gain Stage

9.2.4 Microphone Pre-Amplifier

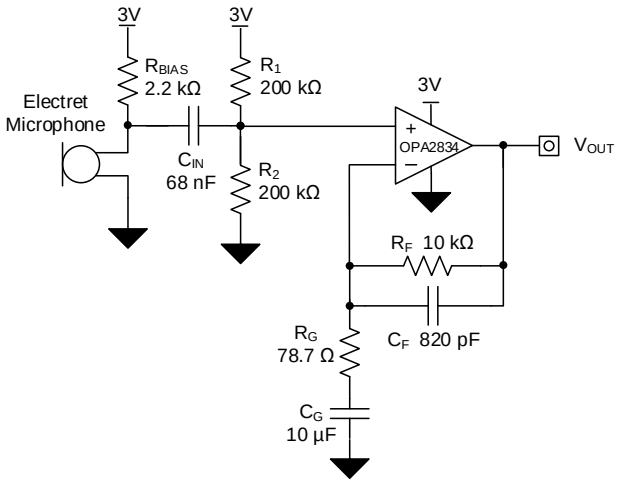


Figure 16. Low-Power Microphone Pre-Amplifier

ADVANCE INFORMATION

10 Power Supply Recommendations

The OPA2834 is intended to work in a nominal supply range of 3.0 V to 5.0 V. Supply-voltage tolerances are supported with the specified operating range of 2.7 V (–10% on a 3-V supply) and 5.4 V (8% on a 5-V supply). Good power-supply bypassing is required. Minimize the distance (< 0.1 inch) from the power-supply pins to high-frequency, 0.1-µF decoupling capacitors. A larger capacitor (2.2 µF is typical) is used along with a high-frequency, 0.1-µF supply-decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. When a split supply is used, use these capacitors for each supply to ground. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) reduces second-harmonic distortion.

11 Layout

11.1 Layout Guidelines

The *OPA2837EVM* can be used as a reference when designing the circuit board. TI recommends following the EVM layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. Follow these general guidelines:

1. Signal routing must be direct and as short as possible into and out of the op amp.
2. The feedback path must be short and direct avoiding vias if possible, especially with G = 1 V/V.
3. Ground or power planes must be removed from directly under the negative input and output pins of the amplifier.
4. TI recommends placing a series output resistor as close to the output pin as possible.
5. A 2.2-µF power-supply decoupling capacitor must be placed within two inches of the device and can be shared with other op amps. For split supply, a capacitor is required for both supplies.
6. A 0.1-µF power-supply decoupling capacitor must be placed as close to the supply pins as possible, preferably within 0.1 inch. For split supply, a capacitor is required for both supplies.

11.2 Layout Examples

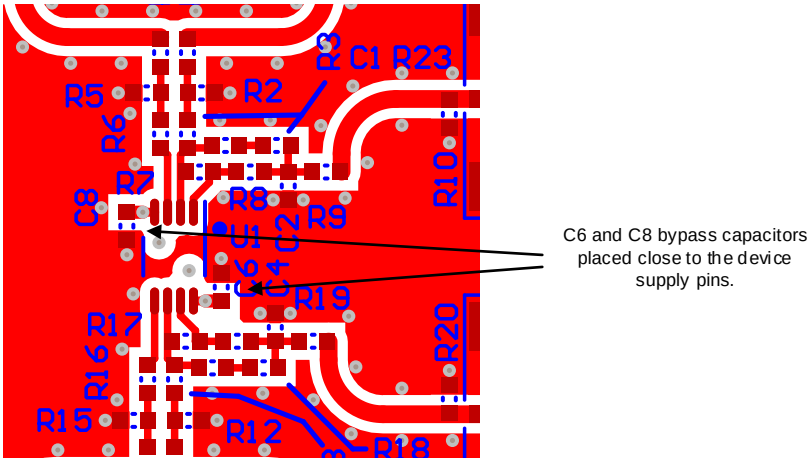


Figure 17. EVM Layout Top Layer

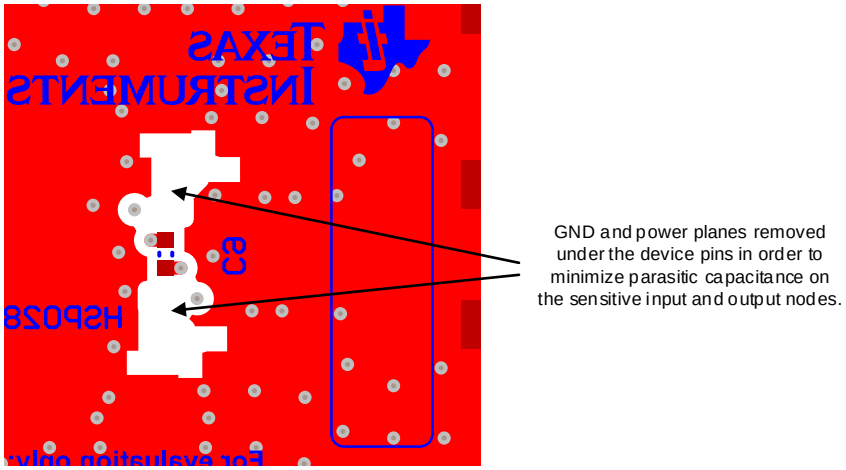


Figure 18. EVM Layout Bottom Layer

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *OPA2837DGK Evaluation Module* user guide
- Texas Instruments, *ADS7046 12-Bit, 3-MSPS, Single-Ended Input, Small-Size, Low-Power SAR ADC* data sheet
- Texas Instruments, *Single-Supply Op Amp Design Techniques* application report
- Texas Instruments, *Noise Analysis for High-Speed Op Amps* application report
- Texas Instruments, *TIDA-01565 Wired OR MUX and PGA Reference Design* design guide
- Texas Instruments, TINA model and simulation tool

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2834IDGKR	PREVIEW	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		
OPA2834IDGKT	PREVIEW	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-40 to 125		
XOPA2834IDGKT	ACTIVE	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

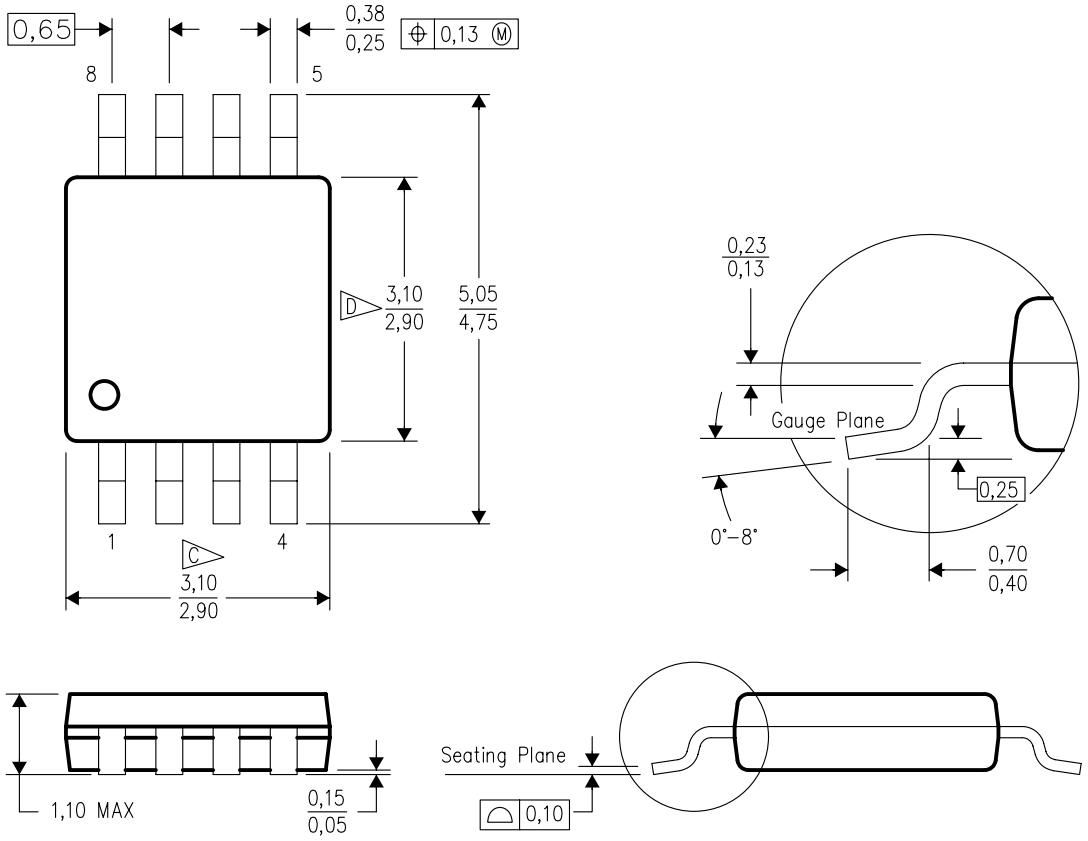
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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