OPAx626 High-Speed, High-Precision, Low-Distortion 16-Bit and 18-Bit Analog-to-Digital Converter (ADC) Drivers

1 Features

- Excellent Dynamic Performance:
  - Low Distortion: –122 dBc for HD2 and –140 dBc for HD3 at 100 kHz
  - Gain Bandwidth (G = 100): 120 MHz
  - Slew Rate: 115 V/µs
  - 16-Bit Settling at 4-V Step: 280 ns
  - Low Voltage Noise: 2.5 nV/√Hz at 10 kHz
  - Low Output Impedance: 1 Ω at 1 MHz
- Excellent DC Precision:
  - Offset Voltage: ±100 µV (Maximum)
  - Offset Voltage Drift: ±3 µV/ºC (Maximum)
  - Low Quiescent Current: 2 mA (Typical)
- Input Common-Mode Range Includes Negative Rail
- Rail-to-Rail Output
- Wide Temperature Range: Fully Specified from –40°C to +125°C

2 Applications

- Precision SAR ADC Drivers
- Precision Voltage Reference Buffers
- Programmable Logic Controllers
- Test and Measurement Equipment
- Scientific Instrumentation
- High Throughput Data Acquisition Systems
- High Density, Multiplexed Data Acquisition Systems

3 Description

The OPAx626 family of operational amplifiers are 16-bit and 18-bit, high-precision, SAR ADC drivers with low total harmonic distortion (THD) and noise. This family of precision op amps is fully characterized and specified with a 16-bit settling time of 280 ns that enables a true 16-bit effective number of bits (ENOB). With a high DC precision of only 100 µV offset voltage, a wide gain-bandwidth product of 120 MHz, and a low wideband noise of 2.5 nV/√Hz, this family is optimized for driving high-throughput, high-resolution SAR ADCs in applications such as the ADS88xx family of SAR ADCs.

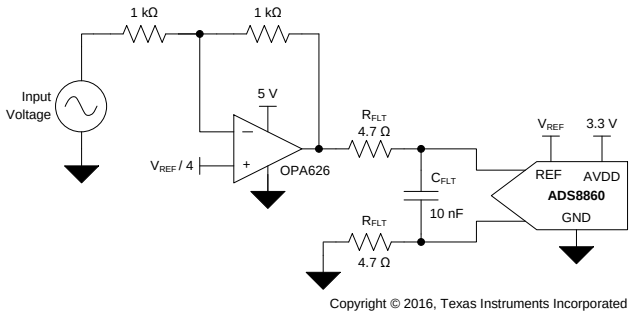
The OPAx626 family is available in 5-pin SOT and 8-pin VSSOP packages and is specified for operation from –40°C to +125°C.

Device Information(1)

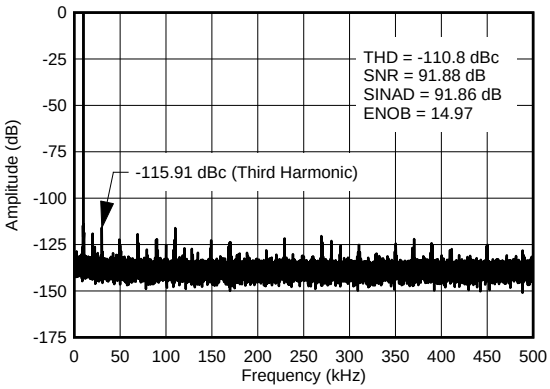
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA626	SOT (5)	2.90 mm × 1.60 mm
OPA2626	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

SAR ADC Driver



High Fidelity Topology Improves Dynamic Performance (f_{IN} = 10-kHz, 1-MSPS FFT)



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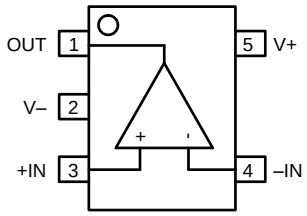
4 Revision History

DATE	REVISION	NOTES
July 2016	*	Initial release.

5 Pin Configuration and Functions

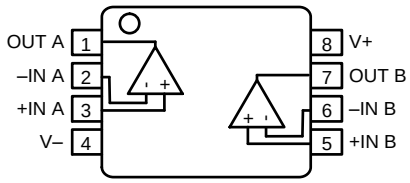
OPA626 DBV Package
5-Pin SOT
Top View



Pin Functions: OPA626

PIN		I/O	DESCRIPTION
NAME	NO		
+IN	3	I	Noninverting input
–IN	4	I	Inverting input
OUT	1	O	Output terminal
V+	5	—	Positive supply voltage
V–	2	—	Negative supply voltage

OPA2626 DGK Package
8-Pin VSSOP
Top View



Pin Functions: OPA2626

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input for channel A
–IN A	2	I	Inverting input for channel A
+IN B	5	I	Noninverting input for channel B
–IN B	6	I	Inverting input for channel B
OUT A	1	O	Output terminal for channel A
OUT B	7	O	Output terminal for channel B
V+	8	—	Positive supply voltage
V–	4	—	Negative supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S	(V+) – (V–)		6	V
Input voltage(2)	+IN	(V–) – 0.3	(V+) + 0.3	V
	–IN	(V–) – 0.3	(V+) + 0.3	
Output voltage	OUT	(V–)	(V+)	V
Sink current	+IN		10	mA
	–IN		10	
	OUT		150	
Source current	+IN		10	mA
	–IN		10	
	OUT		150	
Temperature	Operating junction	–40	150	°C
	Operating free-air temperature, T_A	–55	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For input voltages beyond the power-supply rails, voltage or current must be limited.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply input voltage, (V+) – (V–)		2.7		5.5	V
V_I	Input voltage	+IN	(V–)		(V+) – 1.15	V
		–IN	(V–)		(V+) – 1.15	
V_O	Output voltage		(V–)		(V+)	V
I_O	Output current		–120		120	mA
T_A	Operating free-air temperature		–40		125	°C
T_J	Operating junction temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA626 DBV (SOT) 5 PINS	OPA2626 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	184.9	171.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	123.6	68.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.7	91.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.1	9.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.2	90.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics: High-Supply

at T_A = 25°C, V+ = 5 V, V– = 0 V, $V_{COM} = V_O$ = 2.5 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
	Unity gain frequency	V_O = 10 mV_{PP}			80		MHz
φ_m	Phase margin				50		Degrees
GBW	Gain-bandwidth product	G = 100, V_O = 10 mV_{PP}			120		MHz
SR	Slew rate	V_O = 1-V step, G = 1			45		V/µs
		V_O = 4-V step, G = 2			115		
t_{settle}	Settling time	V_O = 4-V step, G = 2	Settling time to 0.1% (10-bit accuracy)		80		ns
			to 0.005% (14-bit accuracy)		110		
			to 0.00153% (16-bit accuracy)		280		
	Overshoot	V_O = 4-V step, G = 2			2.5%		
	Undershoot	V_O = 4-V step, G = 2			3%		
HD2	Second-order harmonic Distortion	V_O = 2 V_{PP}, G = 2	f = 10 kHz		144		dBc
			f = 100 kHz		122		
			f = 1 MHz		80		
HD3	Third-order harmonic Distortion	V_O = 2 V_{PP}, G = 2	f = 10 kHz		155		dBc
			f = 100 kHz		140		
			f = 1 MHz		80		
	Second-order intermodulation distortion	V_O = 2 V_{PP}, f = 1 MHz, 200-kHz tone spacing			90		dBc
	Third-order intermodulation distortion	V_O = 2 V_{PP}, f = 1 MHz, 200-kHz tone spacing			100		dBc
V_N	Input noise voltage	f = 0.1 Hz to 10 Hz, peak-to-peak			0.8		μV_{PP}
		f = 0.1 Hz to 10 Hz, rms			120		nV_{RMS}
V_n	Input voltage noise density	f = 1 kHz			3.2		$nV/\sqrt{Hz}$
		f = 10 kHz			2.5		
I_n	Input current noise density	f = 1 kHz			6.6		$pA/\sqrt{Hz}$
		f = 10 kHz			3.5		
t_{OR}	Overload recovery time	G = 5			50		ns
Z_o	Open-loop output impedance	f = 1 MHz			1		Ω
	Crosstalk	DC			150		dB
		f = 1 MHz			127		
DC PERFORMANCE							
V_{OS}	Input offset voltage				15	±100	µV
		T_A = –40°C to 125°C				±300	

Electrical Characteristics: High-Supply (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C			0.5	±3	µV/°C
		OPA2626 only, T_A = –40°C to 125°C			0.6	±4	
PSRR	Power-supply rejection ratio	2.7 V ≤ (V+) ≤ 5 V		100			dB
			T_A = –40°C to 125°C	90	120		
I_B	Input bias current				2	4	µA
		T_A = –40°C to 125°C				5.7	
		OPA2626 only, T_A = –40°C to 125°C				6.5	
dI_B/dT	Input bias current drift	T_A = –40°C to 125°C			15		nA/°C
I_{OS}	Input offset current				20	120	nA
		T_A = –40°C to 125°C				150	
		OPA2626 only, T_A = –40°C to 125°C				350	
dI_{OS}/dT	Input offset current drift	T_A = –40°C to 125°C			0.6		nA/°C
OPEN LOOP GAIN							
A_{OL}	Open-loop gain	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω		110			dB
		(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ		114			
		T_A = –40°C to 125°C	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω	106	128		
			(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ	110	132		
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	T_A = –40°C to 125°C		(V–)		(V+) – 1.15	V
CMRR	Common-mode rejection ratio	(V–) < V_{COM} < (V+) – 1.15 V		100	117		dB
			T_A = –40°C to 125°C	90	115		
INPUT IMPEDANCE							
Z_{ID}	Differential input impedance				27 || 1.2		KΩ || pF
Z_{IC}	Common-mode input impedance				47 || 1.5		MΩ || pF
OUTPUT							
	Output voltage swing to the rail	R_{LOAD} = 600 Ω			60	80	mV
			T_A = –40°C to 125°C			100	
		R_{LOAD} = 10 kΩ			20	35	
			T_A = –40°C to 125°C			40	
I_{sc}	Short-circuit current				130		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA,			2	2.2	mA
			T_A = –40°C to 125°C			3.1	

6.6 Electrical Characteristics: Low-Supply

at T_A = 25°C, V+ = 2.7 V, V– = 0 V, V_{COM} = V_O = 1.35 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 1 kΩ connected to 1.35 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
	Unity gain frequency	V_O = 10 mV_{PP}			76		MHz
φ_m	Phase margin				50		Degrees
GBW	Gain-bandwidth product	G = 100, V_O = 10 mV_{PP}			110		MHz
SR	Slew rate	V_O = 1-V step, G = 2			45		V/µs
t_{settle}	Settling time	V_O = 1-V step, G = 2	to 0.1%		80		ns
			to 0.01%		170		
			to 0.000763% (17-bit accuracy)		250		
	Overshoot	V_O = 1-V step, G = 2			6%		
	Undershoot	V_O = 1-V step, G = 2			5%		
HD2	Second order harmonic Distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1 V, V_O = 2 V_{PP}	f = 10 kHz		136		dBc
			f = 100 kHz		118		
			f = 1 MHz		80		
HD3	Third order harmonic Distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1 V, V_O = 2 V_{PP}	f = 10 kHz		143		dBc
			OPA2625 only, f = 10 kHz		143		
			f = 100 kHz		130		
			OPA2625 only, f = 100 kHz		125		
			f = 1 MHz		85		
			OPA2625 only, f = 1 MHz		74		
	Second order inter-modulation distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1 V, V_O = 2 V_{PP}, f = 1 MHz, 200-kHz tone spacing			95		dBc
	Third order inter-modulation distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1V, V_O = 1 V_{PP}, f = 1 MHz, 200-kHz tone spacing			104		dBc
V_N	Input noise voltage	f = 0.1 Hz to 10 Hz peak to peak			0.8		μV_{PP}
		f = 0.1 Hz to 10 Hz rms			120		nV_{RMS}
V_n	Input voltage noise density	f = 10 kHz			2.5		nV/√Hz
I_n	Input current noise density	f = 10 kHz			3.5		pA/√Hz
t_{OR}	Overload recovery time	G = 5			35		ns
Z_o	Open-loop output impedance	f = 1 MHz			1.3		Ω
	Crosstalk	DC			150		dB
		f = 1 MHz			127		
DC PERFORMANCE							
V_{OS}	Input offset voltage				15	±100	µV
		T_A = –40°C to 125°C				±300	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C			0.5	±3.1	µV/°C
		OPA2626 only, T_A = –40°C to 125°C			0.6	±4	
I_B	Input bias current				2	4	µA
		T_A = –40°C to 125°C				5.7	
		OPA2626 only, T_A = –40°C to 125°				6.5	
dI_B/dT	Input bias current drift	T_A = –40°C to 125°C			15		nA/°C
I_{OS}	Input offset current				20	120	nA
		T_A = –40°C to 125°C				150	
		OPA2626 only, T_A = –40°C to 125°				200	
dI_{OS}/dT	Input offset current drift	T_A = –40°C to 125°C			80		pA/°C
OPEN-LOOP GAIN							

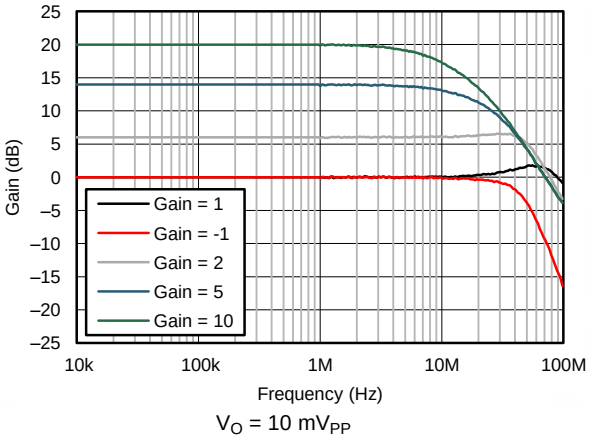
Electrical Characteristics: Low-Supply (continued)

at T_A = 25°C, V+ = 2.7 V, V– = 0 V, V_{COM} = V_O = 1.35 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 1 kΩ connected to 1.35 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_{OL}	Open-loop gain	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω		110			dB
		(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ		114			
		T_A = –40°C to 125°C	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω	100	128		
			(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ	104	132		
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	T_A = –40°C to 125°C		(V–)		(V+) – 1.15	V
CMRR	Common-mode rejection ratio	(V–) < V_{COM} < (V+) – 1.15 V		100	117		dB
			T_A = –40°C to 125°C	90	115		
INPUT IMPEDANCE							
Z_{ID}	Differential input impedance				27 || 0.8		KΩ || pF
Z_{IC}	Common-mode input impedance				47 || 1.2		MΩ || pF
OUTPUT							
	Output voltage swing to the rail	R_{LOAD} = 600 Ω			60	80	mV
			T_A = –40°C to 125°C			100	
		R_{LOAD} = 10 kΩ			20	35	
			T_A = –40°C to 125°C			40	
I_{SC}	Short-circuit current				80		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			2	2.1	mA
			T_A = –40°C to 125°C			2.8	

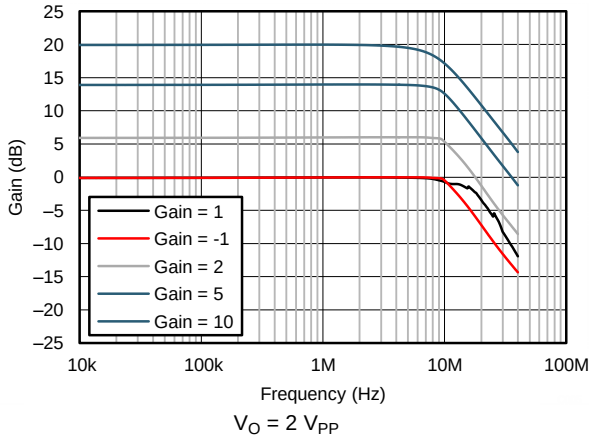
6.7 Typical Characteristics

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



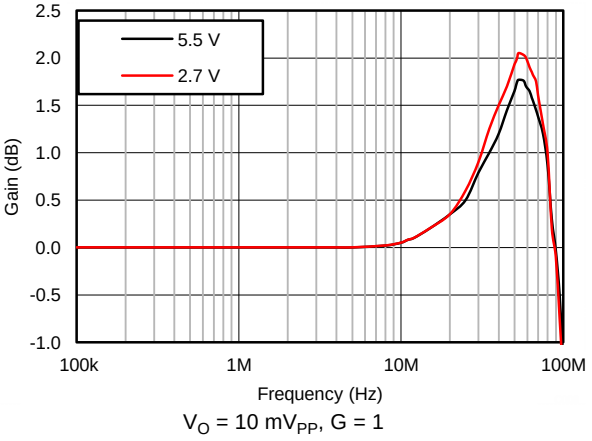
V_O = 10 mV_{PP}

Figure 1. Small-Signal Frequency Response for Various Gains



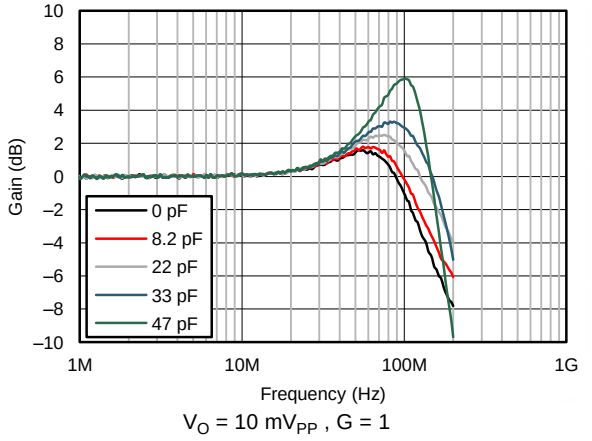
V_O = 2 V_{PP}

Figure 2. Large-Signal Frequency Response for Various Gains



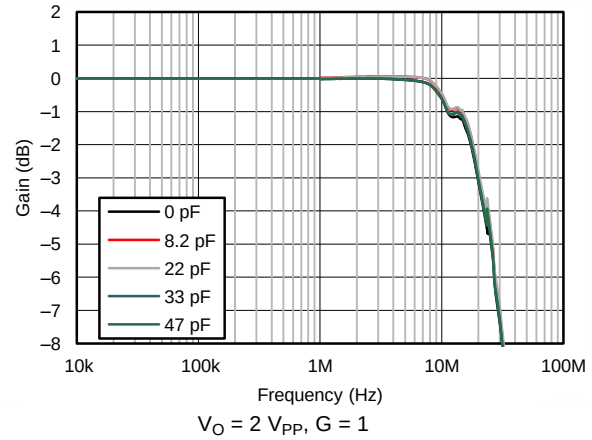
V_O = 10 mV_{PP}, G = 1

Figure 3. Small-Signal Frequency Response for Various Power Supply Voltages



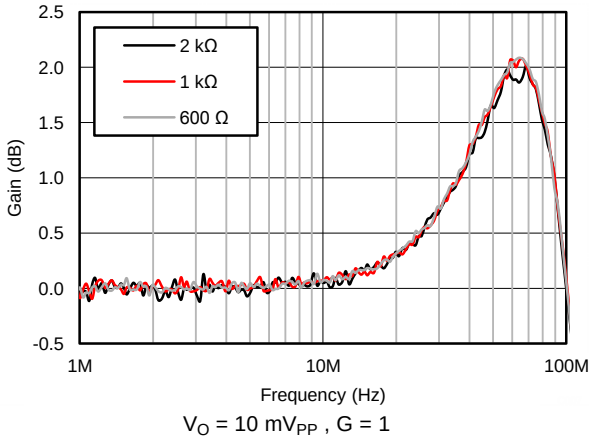
V_O = 10 mV_{PP} , G = 1

Figure 4. Small-Signal Frequency Response for Various Capacitive Loads



V_O = 2 V_{PP}, G = 1

Figure 5. Large-Signal Frequency Response for Various Capacitive Loads



V_O = 10 mV_{PP} , G = 1

Figure 6. Small-Signal Frequency Response for Various Resistive Loads

Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

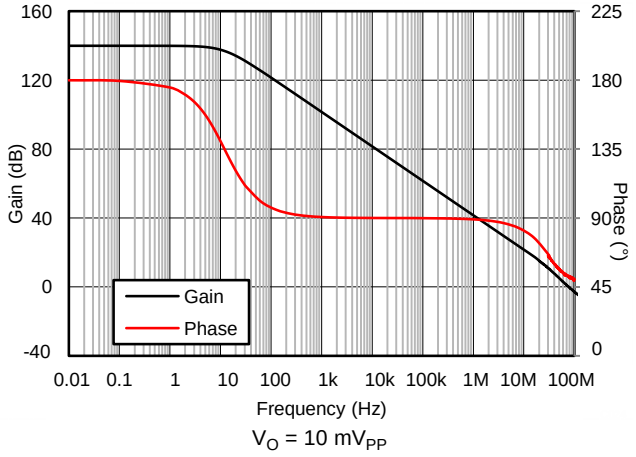


Figure 7. Open-Loop Gain and Phase vs Frequency

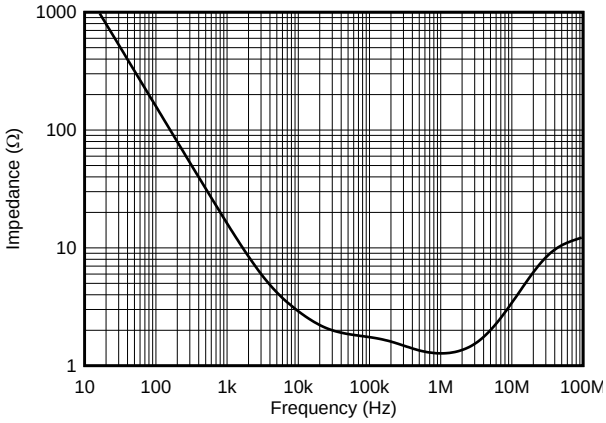


Figure 8. Open-Loop Output Impedance vs Frequency

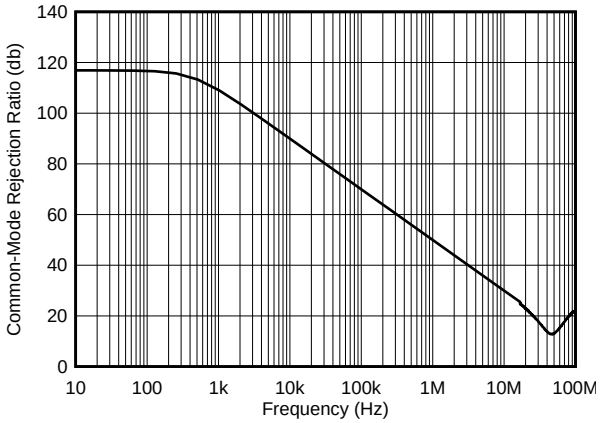


Figure 9. Common-Mode Rejection Ratio vs Frequency

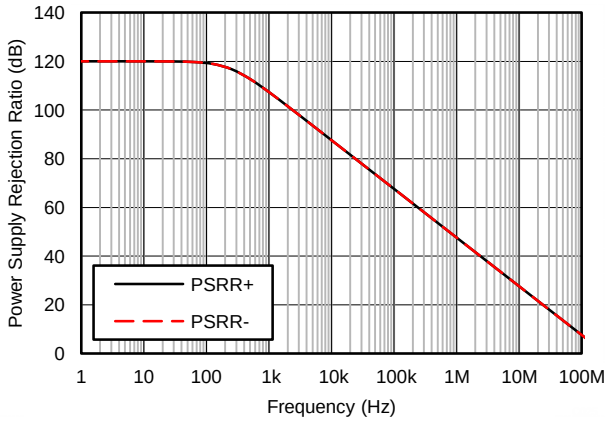


Figure 10. Power-Supply Rejection Ratio vs Frequency

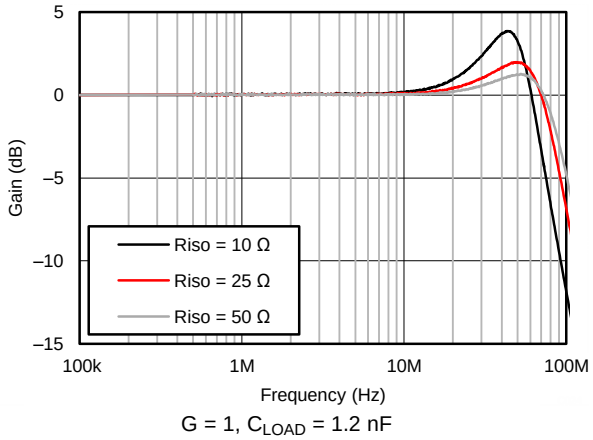


Figure 11. Series Resistance for Capacitive Load Stability

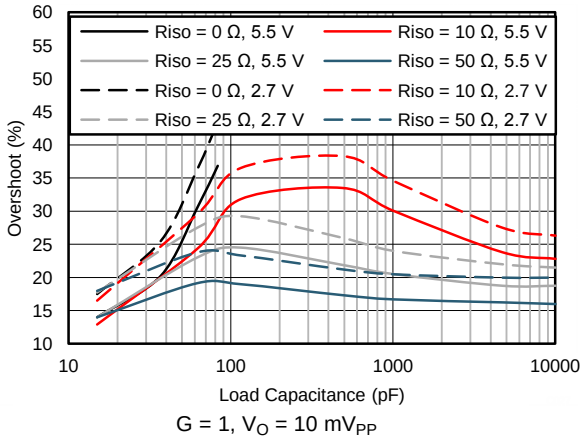


Figure 12. Overshoot vs Capacitive Load, G = 1

Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

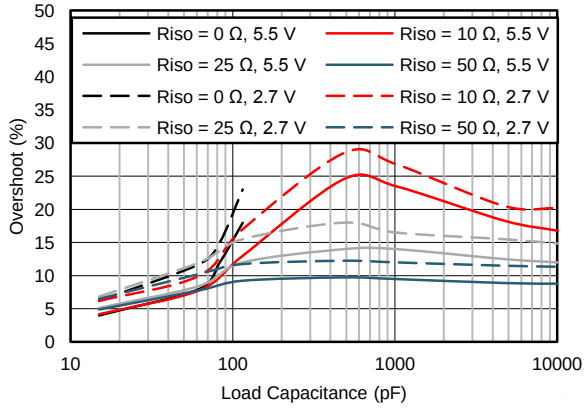


Figure 13. Overshoot vs Capacitive Load, G = –1

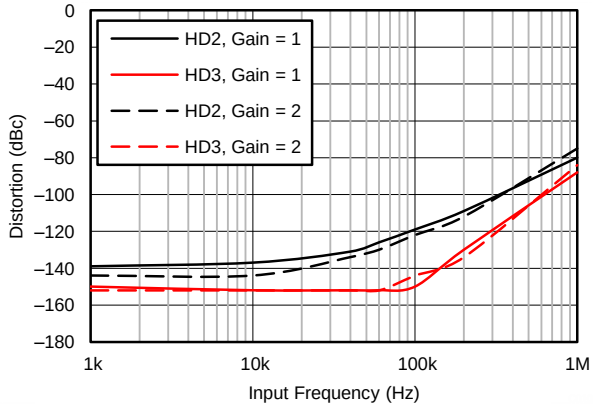


Figure 14. Distortion vs Frequency for Various Gains

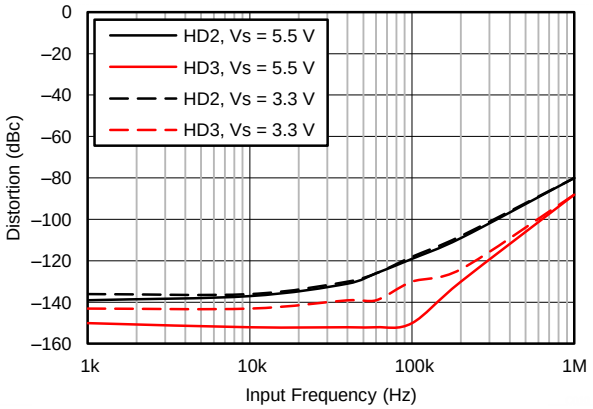


Figure 15. Distortion vs Frequency for Various Power Supplies

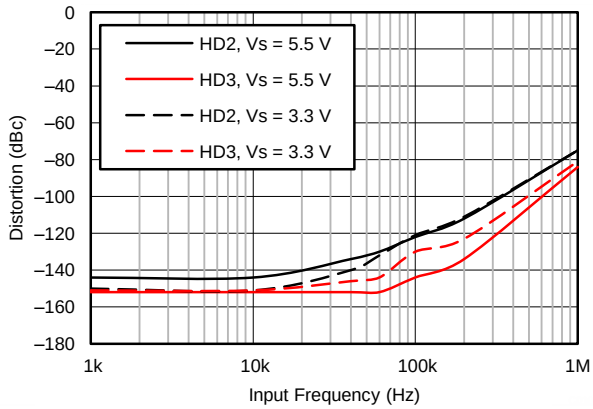


Figure 16. Distortion vs Frequency for Various Power Supplies

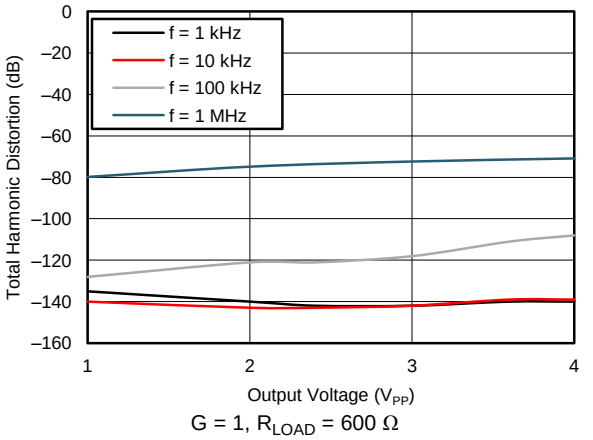


Figure 17. Total Harmonic Distortion vs Output Voltage for Various Frequencies

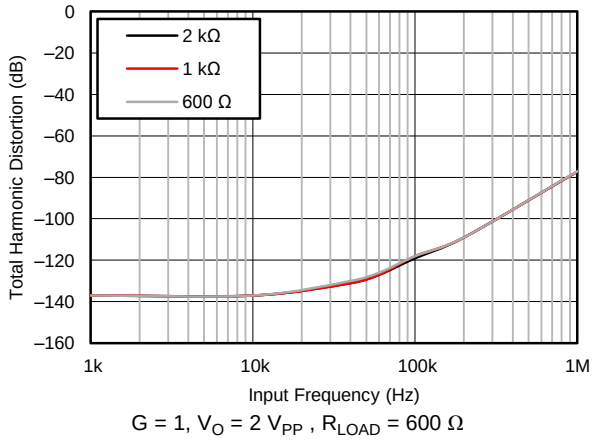


Figure 18. Total Harmonic Distortion vs Frequency for Various Loads

Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

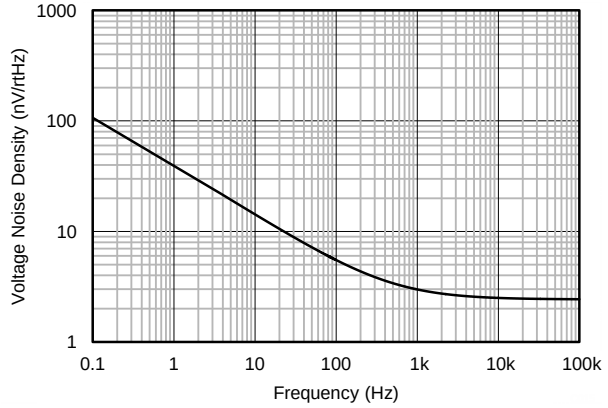


Figure 19. Voltage Noise Density vs Frequency

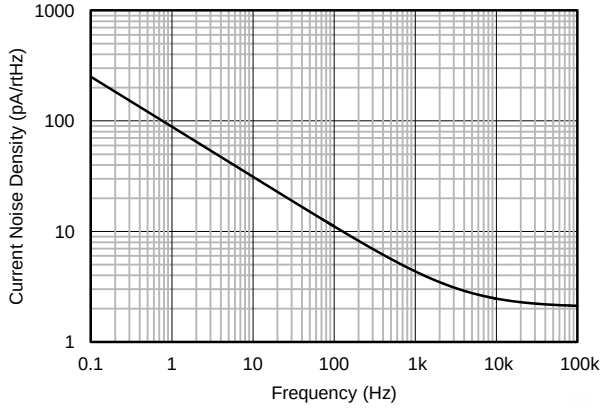


Figure 20. Current Noise Density vs Frequency

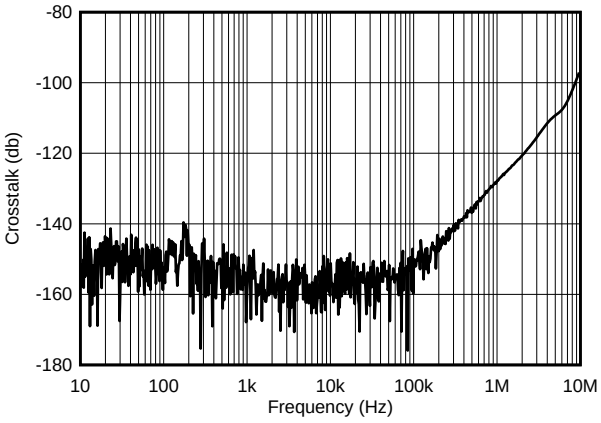


Figure 21. Crosstalk vs Frequency

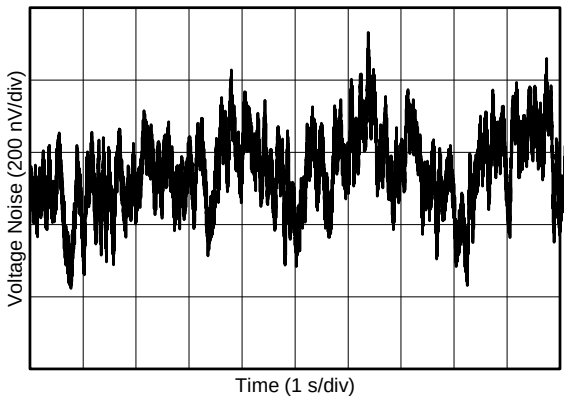


Figure 22. 0.1-Hz to 10-Hz Voltage Noise

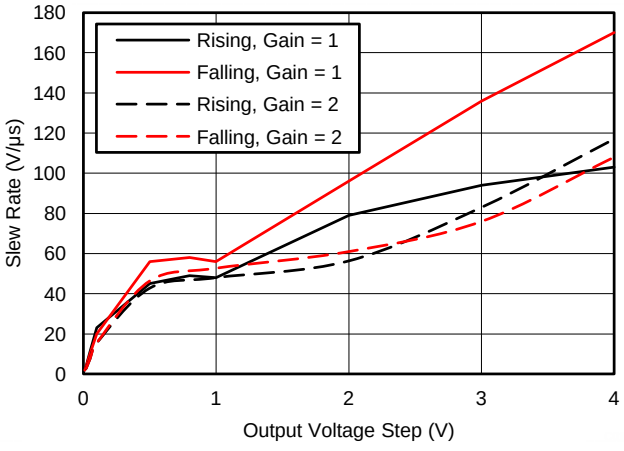


Figure 23. Slew Rate vs Output Step Size

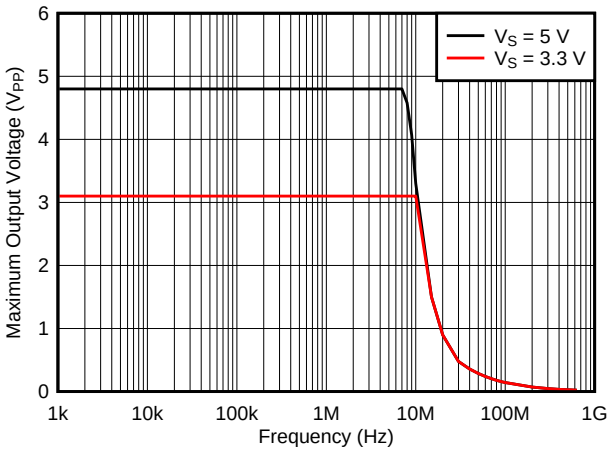
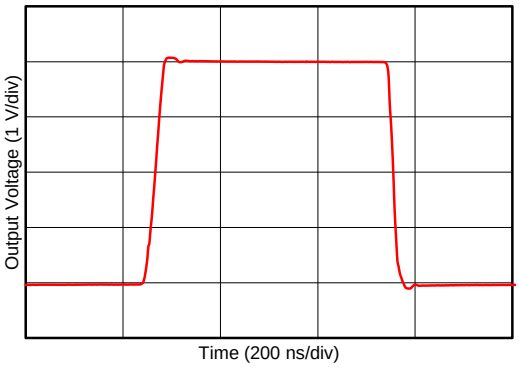


Figure 24. Maximum Output Voltage vs Frequency

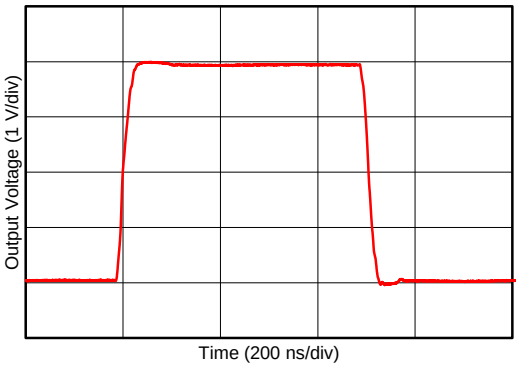
Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



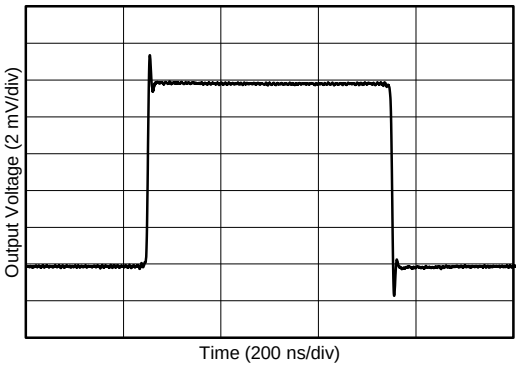
G = 1, V_O = 4-V step

Figure 25. Large-Signal Pulse Response



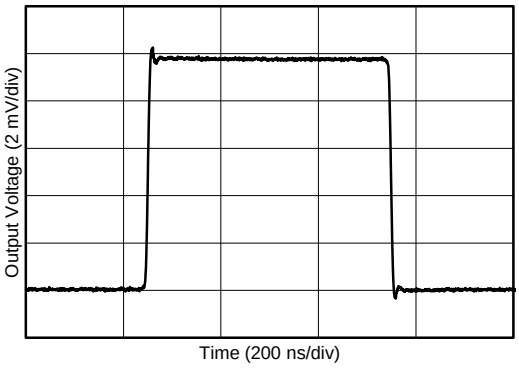
G = –1, V_O = 4-V step

Figure 26. Large-Signal Pulse Response



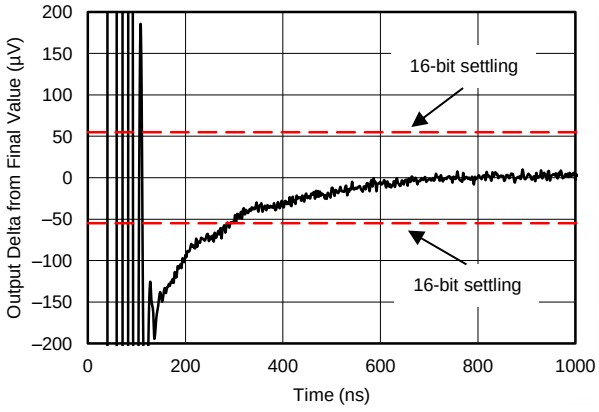
G = 1, V_O = 10-mV step

Figure 27. Small-Signal Pulse Response



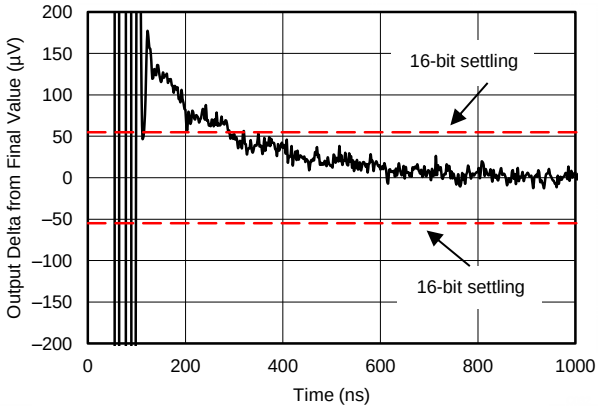
G = –1, V_O = 10-mV step

Figure 28. Small-Signal Pulse Response



V_O = 3.6-V step at t = 0 s

Figure 29. 16-Bit Negative Settling Time

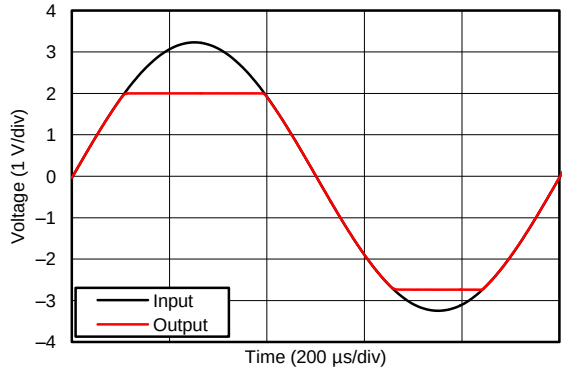


V_O = 3.6-V step at t = 0 s

Figure 30. 16-Bit Positive Settling Time

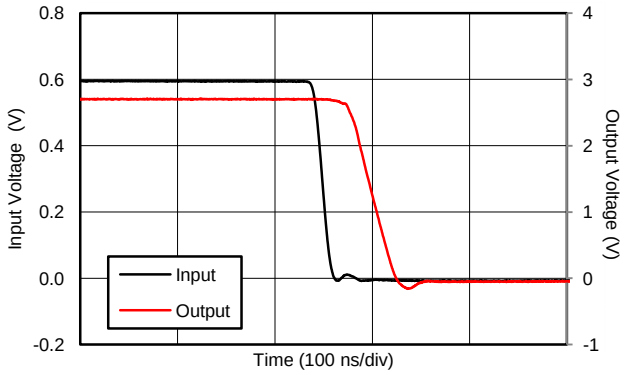
Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



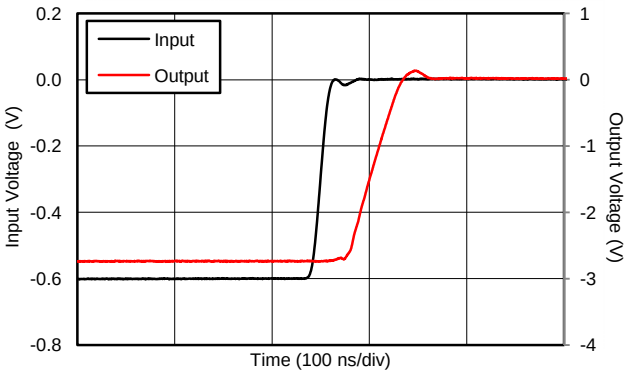
V_S = ±2.75 V, G = 1

Figure 31. No Phase Reversal



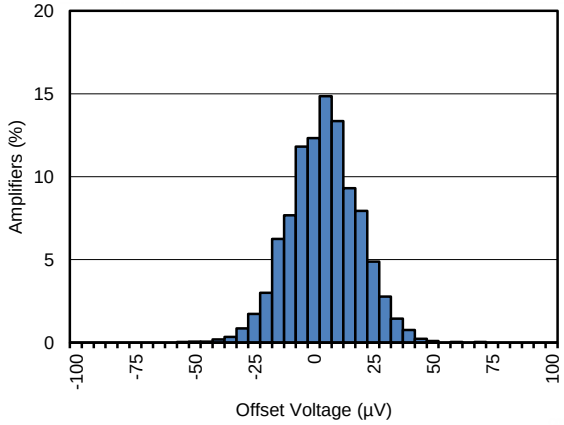
V_S = ±2.75 V, G = 5

Figure 32. Positive Overload Recovery



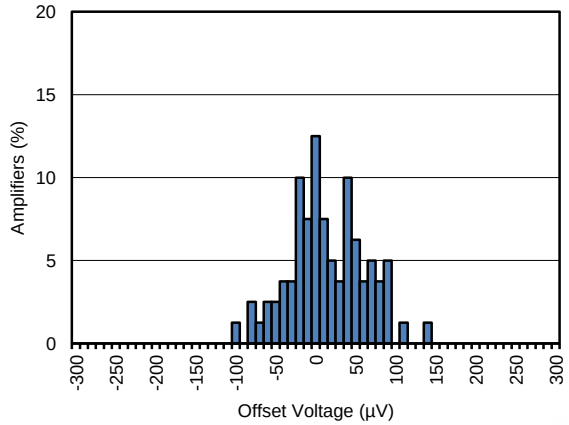
V_S = ±2.75 V, G = 5

Figure 33. Negative Overload Recovery



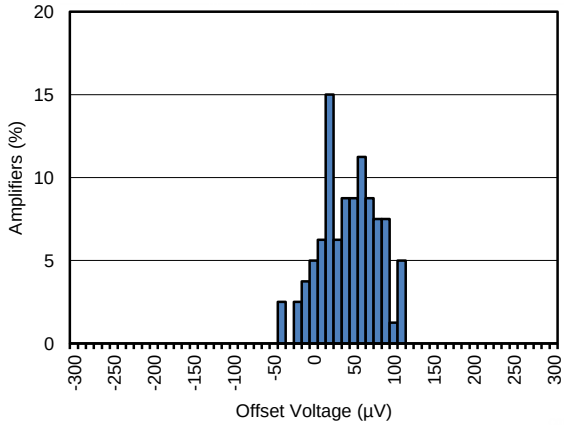
Distribution taken from 3139 amplifiers, T_A = 25°C

Figure 34. Input Offset Voltage Distribution



Distribution taken from 80 amplifiers, T_A = 125°C

Figure 35. Input Offset Voltage Distribution

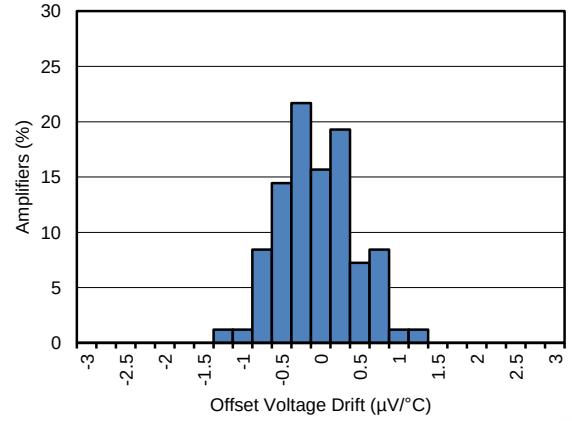


Distribution taken from 80 amplifiers, T_A = –40°C

Figure 36. Input Offset Voltage Distribution

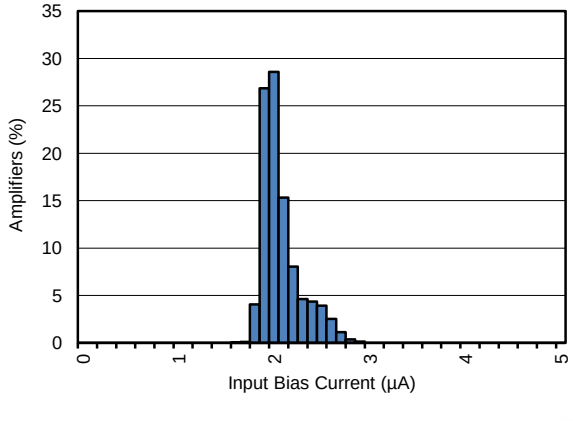
Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



Distribution taken from 75 amplifiers, T_A = –40°C to +125°C

Figure 37. Input Offset Voltage Drift Distribution



Distribution taken from 3139 amplifiers

Figure 38. Input Bias Current Distribution

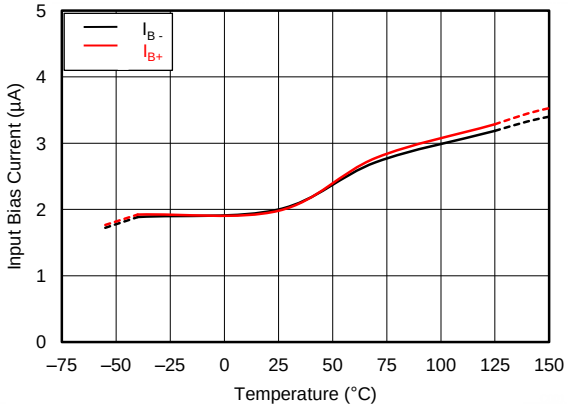
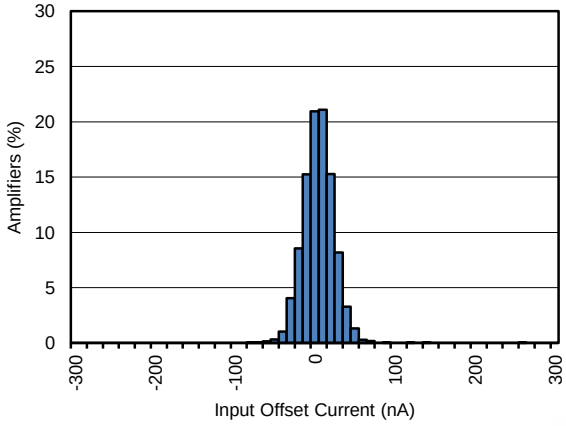


Figure 39. Input Bias Current vs Temperature



Distribution taken from 3139 amplifiers

Figure 40. Input Offset Current Distribution

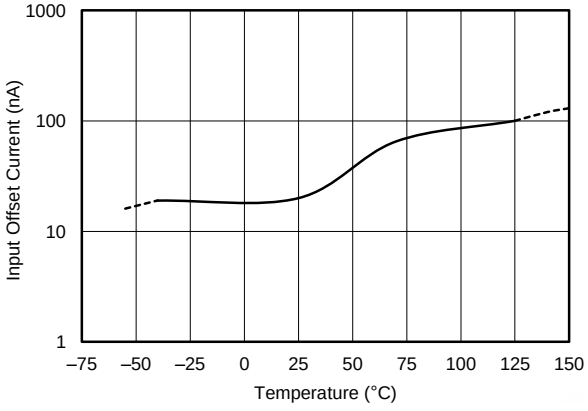


Figure 41. Input Offset Current vs Temperature

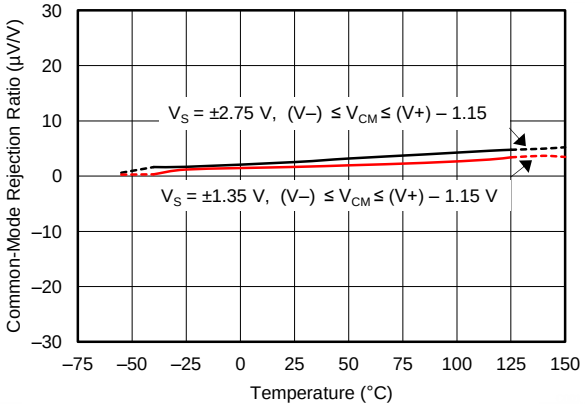


Figure 42. Common-Mode Rejection Ratio vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

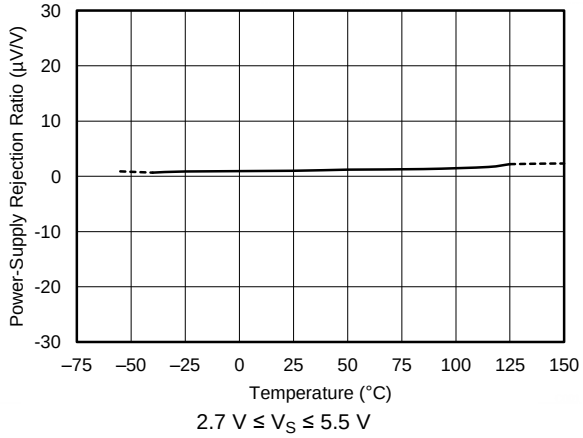


Figure 43. Power-Supply Rejection Ratio vs Temperature

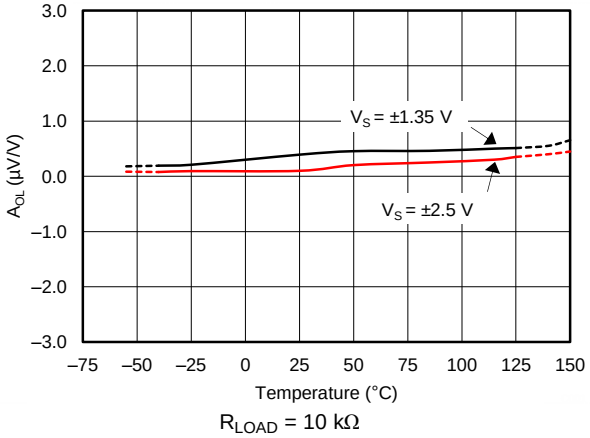


Figure 44. Open-Loop Gain vs Temperature with 10-kΩ Load

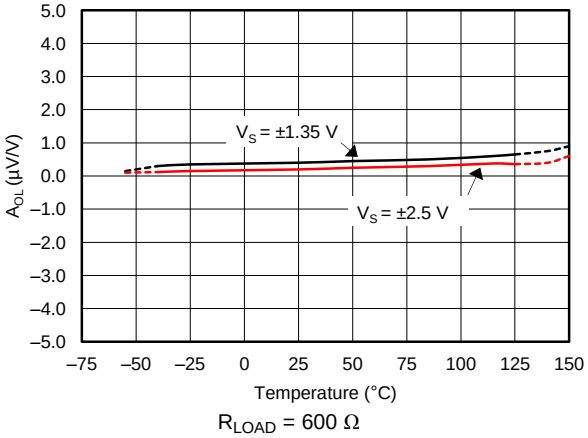


Figure 45. Open-Loop Gain vs Temperature with 600-Ω Load

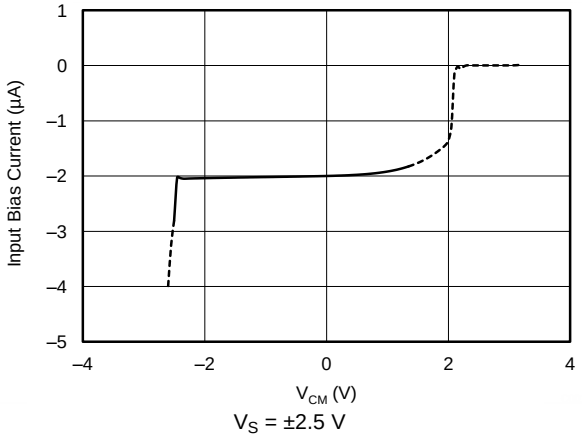


Figure 46. Input Bias Current vs Input Common-Mode Voltage

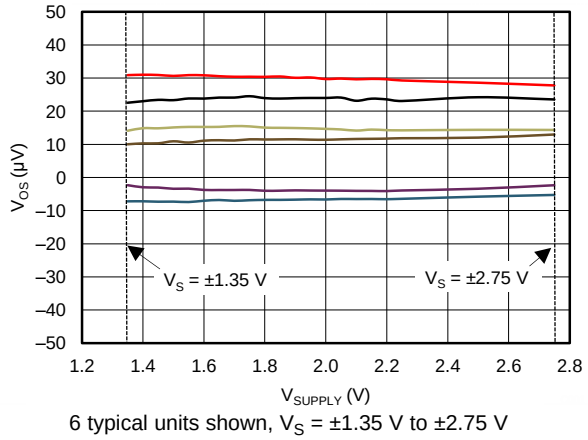


Figure 47. Input Offset Voltage vs Power-Supply Voltage

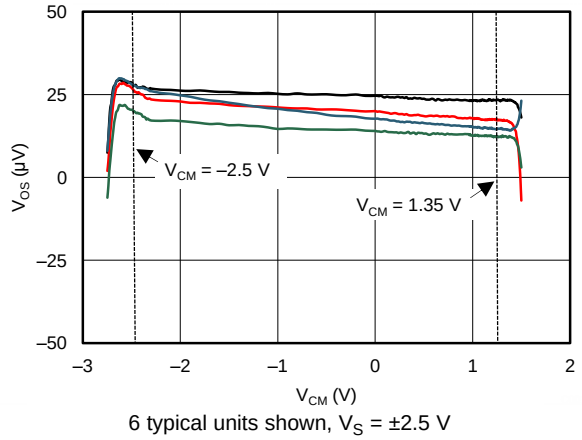


Figure 48. Input Offset Voltage vs Common-Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

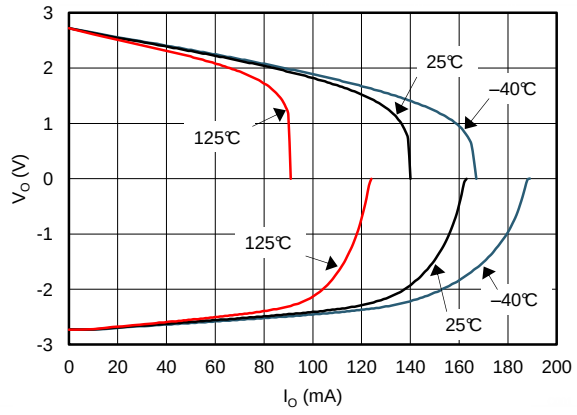


Figure 49. Output Voltage vs Output Current

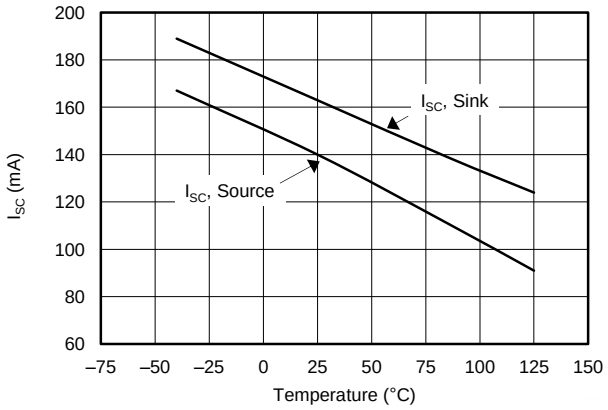


Figure 50. Short-Circuit Current vs Temperature

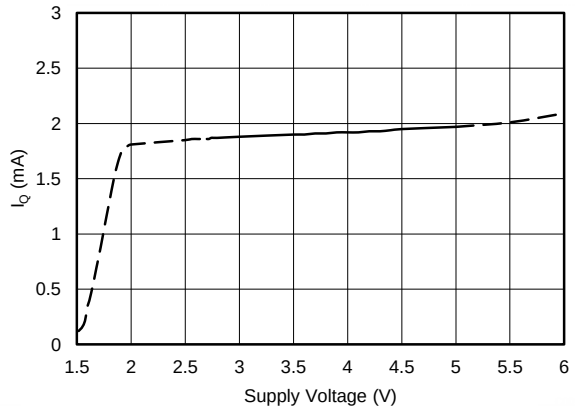


Figure 51. Quiescent Current vs Power-Supply Voltage

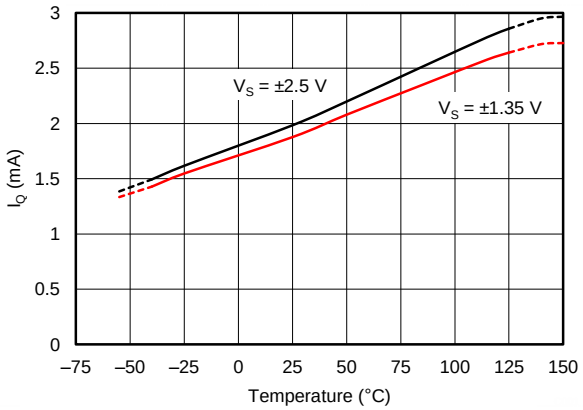
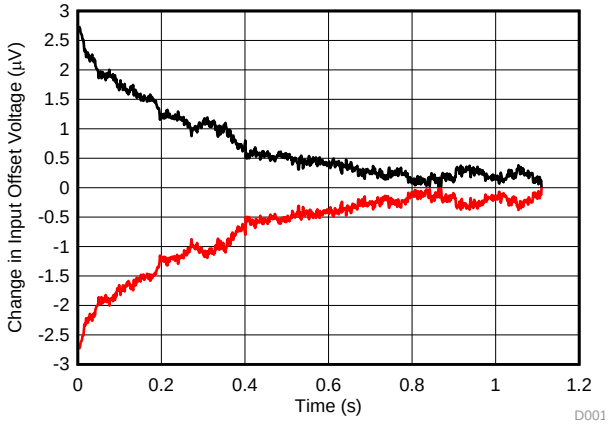


Figure 52. Quiescent Current vs Temperature



OPA626 powered on at t = 0 s, PCB dimensions: 4 in^2, 2 layer, FR4

Figure 53. Warm-Up Time

7 Parameter Measurement Information

7.1 DC Parameter Measurements

The circuit shown in Figure 54 measures the dc input offset related parameters of the OPAx626 family. Input offset voltage, power supply rejection ratio, common-mode rejection ratio and open loop gain can be measured with this circuit. The basic test procedure requires setting the inputs (the power-supply voltage, V_S, and the common-mode voltage, V_{CM}), to the desired values. V_O is set to the desired value by adjusting the loop-drive voltage while measuring V_O. After all inputs are configured, measure the input offset at the V_X measurement point. Calculate the input offset voltage by dividing the measured result by 101. Changing the voltages on the various inputs changes the input offset voltage. The input parameters can be measured according to the relationships illustrated in Equation 1 through Equation 5.

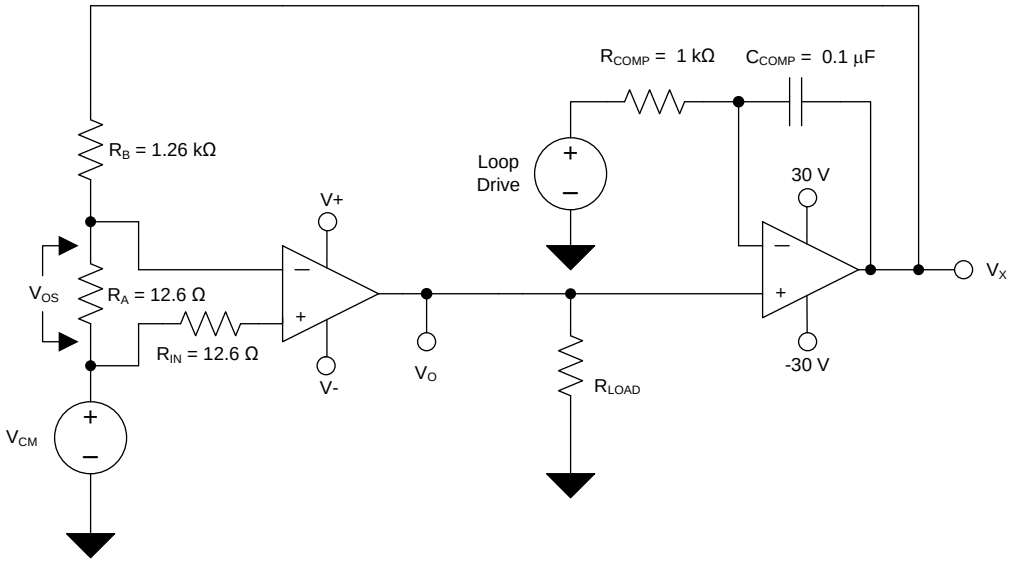


Figure 54. DC-Parameters Measurement Circuit

$$V_{OS} = \frac{V_X}{101} \quad (1)$$

$$V_{OSDrift} = \frac{\Delta V_{OS}}{\Delta Temperature} \quad (2)$$

$$PSRR = \frac{\Delta V_{OS}}{\Delta V_{SUPPLY}} \quad (3)$$

$$CMRR = \frac{\Delta V_{OS}}{\Delta V_{CM}} \quad (4)$$

$$AOL = \frac{\Delta V_O}{\Delta V_{OS}} \quad (5)$$

7.2 Transient Parameter Measurements

The circuit shown in Figure 55 measures the transient response of the OPAx626 family. Configure V+, V–, R_{ISO}, R_{LOAD}, and C_{LOAD} as desired. Monitor the input and output voltages on an oscilloscope or other signal analyzer. Use this circuit to measure large-signal and small-signal transient response, slew rate, overshoot, and capacitive-load stability.

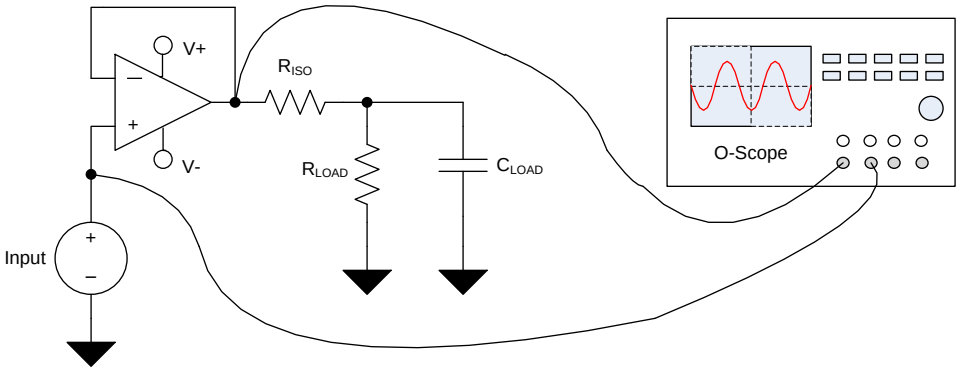


Figure 55. Pulse-Response Measurement Circuit

7.3 AC Parameter Measurements

The circuit shown in Figure 56 measures the ac parameters of the OPAx626 family. Configure V+, V–, and C_{LOAD} as desired. The THS4271 family is used to buffer the input and output of the OPAx626 family to prevent loading by the gain phase analyzer. Monitor the input and output voltages on a gain phase analyzer. Use this circuit to measure the gain bandwidth product, and open-loop gain versus frequency versus capacitive load.

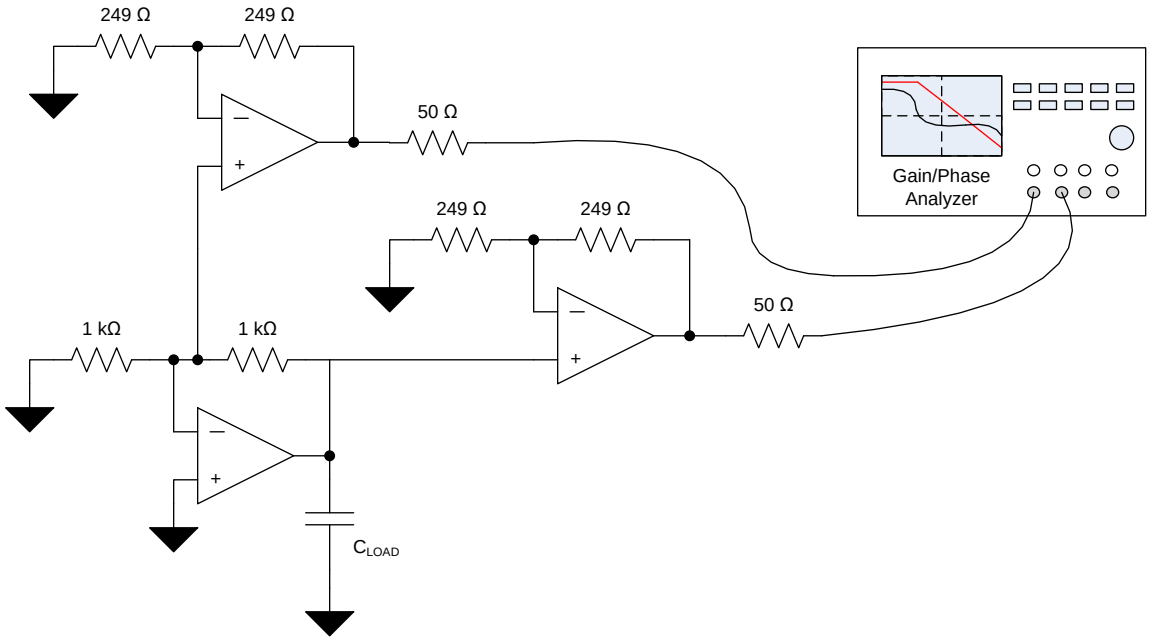


Figure 56. AC-Parameters Measurement Circuit

7.4 Noise Parameter Measurements

The circuit shown in Figure 57 measures the voltage noise of the OPAx626 family. Configure V+, V–, and C_{LOAD} as desired.

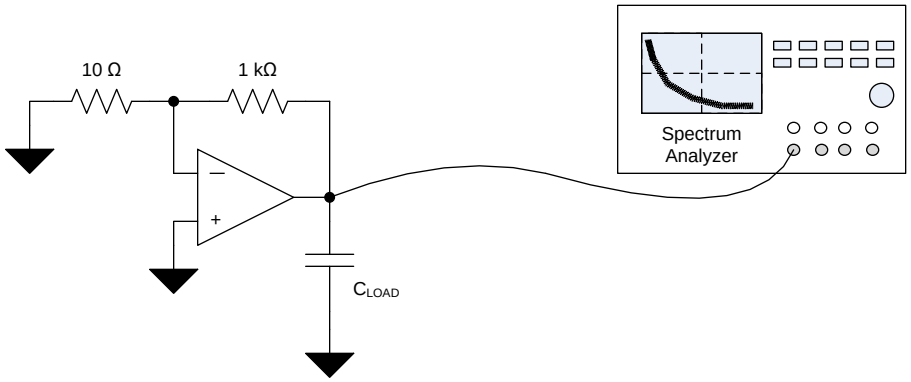


Figure 57. Voltage Noise Measurement Circuit

The circuit shown in Figure 58 measures the current noise of the OPAx626 family. Configure V+, V– and C_{LOAD} as desired.

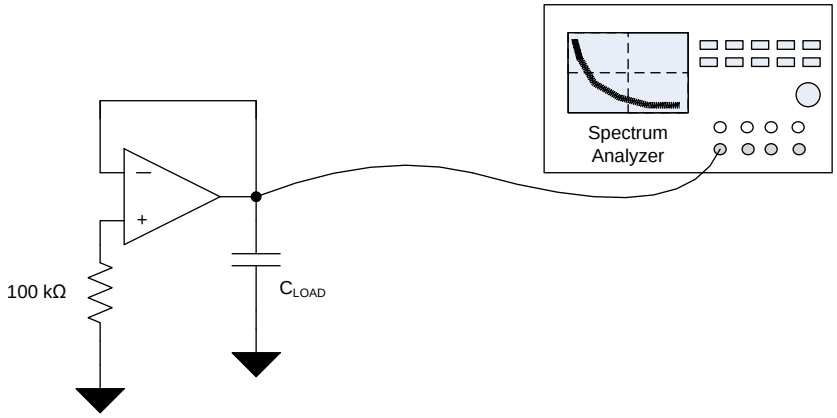


Figure 58. Current Noise Measurement Circuit

The circuit shown in Figure 59 measures the 0.1-Hz to 10-Hz voltage noise of the OPAx626 family . Configure V+, V–, and C_{LOAD} as desired.

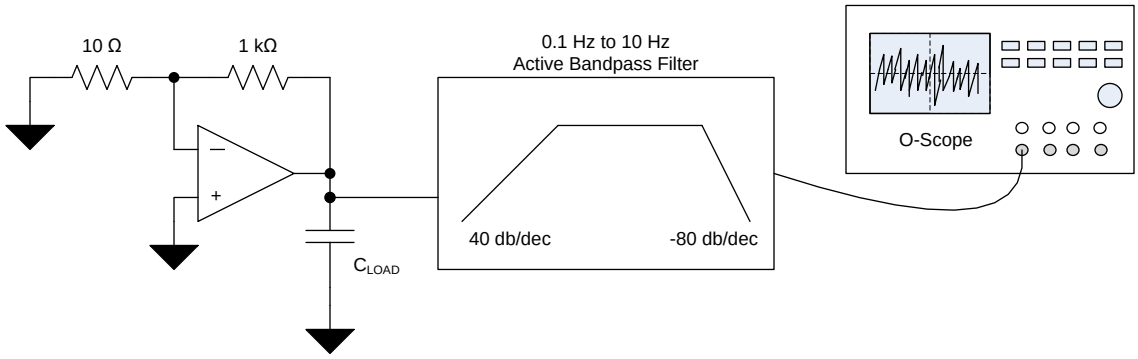


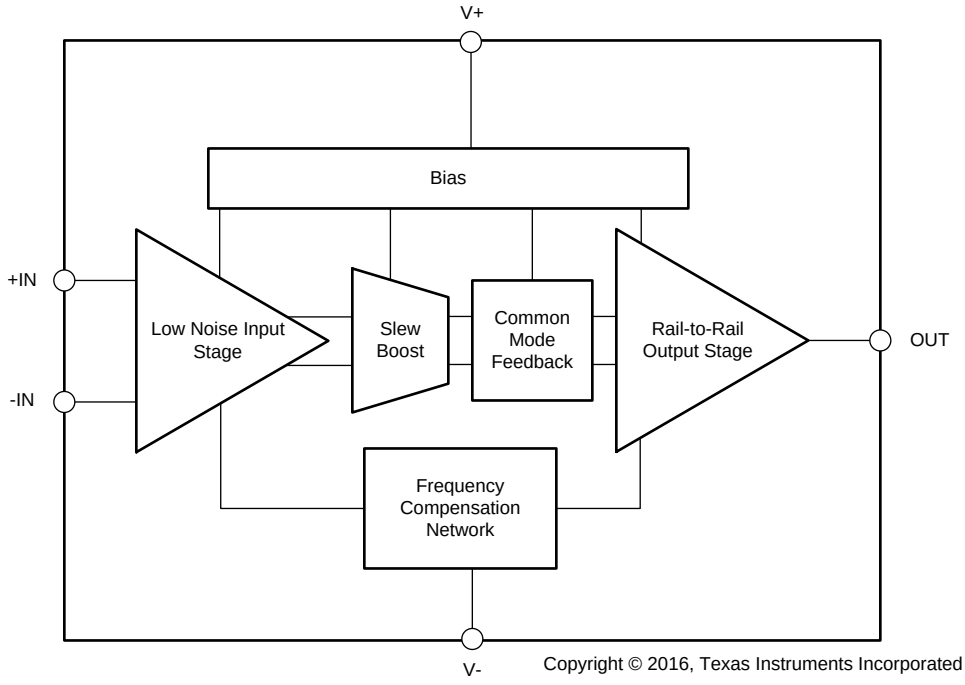
Figure 59. 0.1-Hz to 10-Hz Voltage-Noise Measurement Circuit

8 Detailed Description

8.1 Overview

The OPAx626 family **consists of** fast-settling, high slew rate, high-bandwidth, voltage-feedback operational amplifiers. Low offset and low offset drift combine with the superior dynamic performance and low output impedance, resulting in an amplifier suited for driving 16-bit SAR ADCs, and buffering precision voltage references in industrial applications. The OPAx626 family **consists of** low-noise input, slew boost, and rail-to-rail output stages.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 SAR ADC Driver

The OPAx626 family is designed to drive precision (16-bit and 18-bit) SAR ADCs at sample rates up to 1 MSPS. The combination of low output impedance, low THD, low noise, and fast settling time make the OPAx626 family the ideal choice for driving both the SAR ADC inputs, as well as the reference input to the ADC. Internal slew boost circuitry increases the slew rate as a function of the input signal magnitude, resulting in settling from a 4-V step input to 16-bit levels within 280 ns. Low output impedance (1 Ω at 1 MHz) ensures capacitive load stability with minimal overshoot.

8.3.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly. A good understanding of this basic ESD circuitry and how the ESD circuitry relates to an electrical overstress event is helpful. (See Figure 60 for an illustration of the ESD circuits contained in the OPAx626 family). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

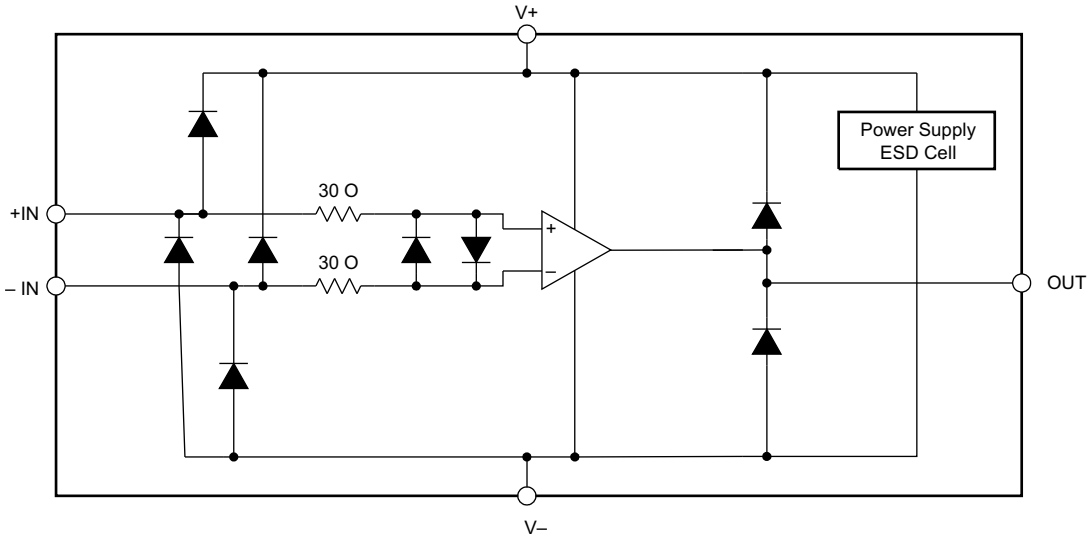


Figure 60. Simplified ESD Circuit

8.4 Device Functional Modes

The OPAx626 family has a single functional mode and is operational when the power supply voltage, V_S, is between 2.7 V (±1.35 V) and 5.5 V (±2.75 V).

8.4.1 High-Drive Mode

The OPAx626 family has 120-MHz gain bandwidth, 2.5-nV/√Hz input-referred noise, and consumes 2 mA of quiescent current. Additionally, the OPAx626 family has an offset voltage of 100 µV (maximum) and offset voltage drift of 1 µV/°C (typical). This combination of high precision, high speed, and low noise makes this device suitable for use as an input driver for high-precision, high-throughput SAR ADCs such as the ADS88xx family of SAR ADCs, as shown in Figure 61.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx626 family consists of precision, high-speed, voltage-feedback operational amplifiers. Fast settling to 16-bit levels, low THD, and low noise make the OPAx626 family suitable for driving SAR ADC inputs and buffering precision voltage references. With a wide power-supply voltage range from 2.7 V to 5.5 V, and operating from –40°C to +125°C, the OPAx626 family is suitable for a variety of high-speed, industrial applications. The following sections show application information for the OPAx626 family. For simplicity, power-supply decoupling capacitors are not shown in these diagrams.

9.2 Typical Applications

9.2.1 Single-Supply, 16-Bit, 1-MSPS SAR ADC Driver

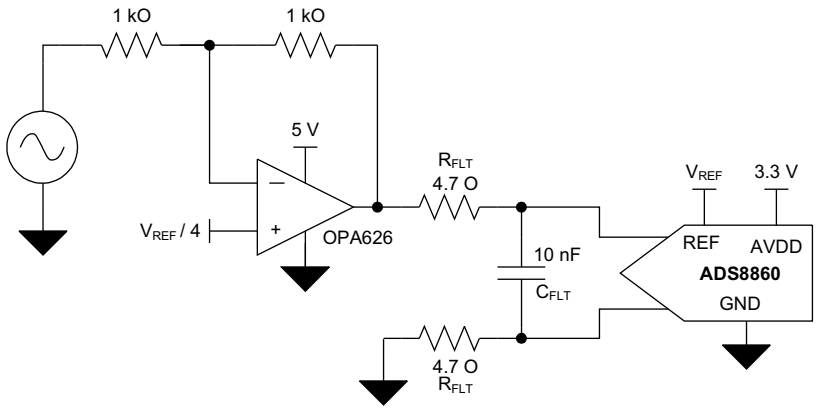


Figure 61. Single-Supply, 16-Bit, 1-MSPS SAR ADC Driver

9.2.1.1 Design Requirements

An SAR ADC, such as the ADS8860 device, uses sampling capacitors on the data converter input. During the signal acquisition phase, these sampling capacitors are connected to the ADC analog input terminals, AINP and AINN, through a set of switches. After the acquisition period has elapsed, the internal sampling capacitors are disconnected from the input terminals and connected to the ADC input through a second set of switches, during this period the ADC is performing the analog-to-digital conversion. Figure 62 illustrates this architecture.

Typical Applications (continued)

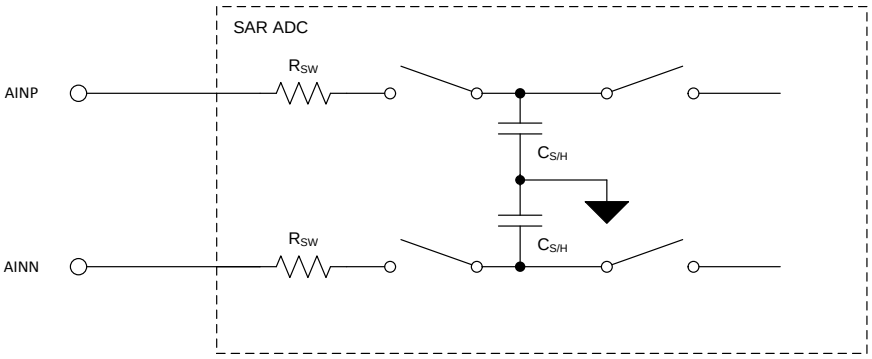


Figure 62. Simplified SAR ADC Input

The SAR ADC inputs and sampling capacitors must be driven by the OPA626 device to 16-bit levels within the acquisition time of the ADC. For the example illustrated in Figure 61, the OPA626 device is used to drive the ADS8860 device at a sample rate of 1 MSPS.

9.2.1.2 Detailed Design Procedure

The circuit illustrated in Figure 61 consists of the SAR ADC driver, a low-pass filter and the SAR ADC. The SAR ADC driver circuit consists of an OPA626 device configured in an inverting gain of 1. The filter consists of R_{FLT} and C_{FLT}, connected between the OPA626 output and the ADS8860 input. Selecting the proper values for each of these passive components is critical to obtain the best performance from the ADC. Capacitor C_{FLT} serves as a charge reservoir, providing the necessary charge to the ADC sampling capacitors. The dynamic load presented by the ADC creates a glitch on the filter capacitor, C_{FLT}. To minimize the magnitude of this glitch, choose a value for C_{FLT} large enough to maintain a glitch amplitude of less than 100 mV. Maintaining such a low glitch amplitude at the amplifier output makes sure that the amplifier remains in the linear operating region, and results in a minimum settling time. Using Equation 6, a 10-nF capacitor is selected for C_{FLT}.

$$C_{FLT} \geq 15 \times C_{SH} \tag{6}$$

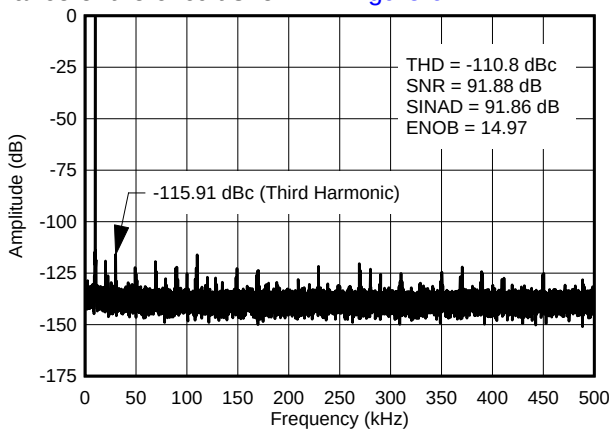
Connecting a 10-nF capacitor directly to the OPA626 output degrades the OPA626 phase margin and results in stability and settling-time problems. To properly drive the 10-nF capacitor, use a series resistor (R_{FLT}) to isolate the capacitor, C_{FLT}, from the OPA626 device. R_{FLT} must be sized based upon several constraints. To determination a suitable value for R_{FLT}, consider the impact upon the THD due to the voltage divider effect from R_{FLT} reacting with the switch resistance (R_{SW}) of the ADC input circuit, as well as the impact of the output impedance upon amplifier stability. In this example, 4.7-Ω resistors are selected. In this design example, Figure 13 can be used to estimate a suitable value for R_{ISO}. R_{ISO} represents the total resistance in series with C_{FLT}, and in this example is equivalent to 2 × R_{FLT}.

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Precision Design, TIDU014, "Power-optimized 16-bit 1MSPS Data Acquisition Block for Lowest Distortion and Noise Reference Design".

9.2.1.3 Application Curves

Figure 63 illustrates the performance of the circuit shown in Figure 61.



4096-point FFT at 1 MSPS, f_{IN} = 10 kHz , V_{IN} = 1.5 V_{RMS}

Figure 63. ADC Output FFT for Figure 61

9.2.2 Single-Supply, 16-Bit, 1-MSPS, Multiplexed, SAR ADC Driver

In order to operate a high-resolution, 16-bit ADC at its maximum throughput, the full-scale voltage step must settle to better than 16-bit accuracy at the ADC inputs within the minimum specified acquisition time (t_{ACQ}). This settling imposes very stringent requirements on the driver amplifier in terms of large-signal bandwidth, slew rate, and settling time. Figure 64 illustrates a typical multiplexed ADC driver application using the OPA626 device.

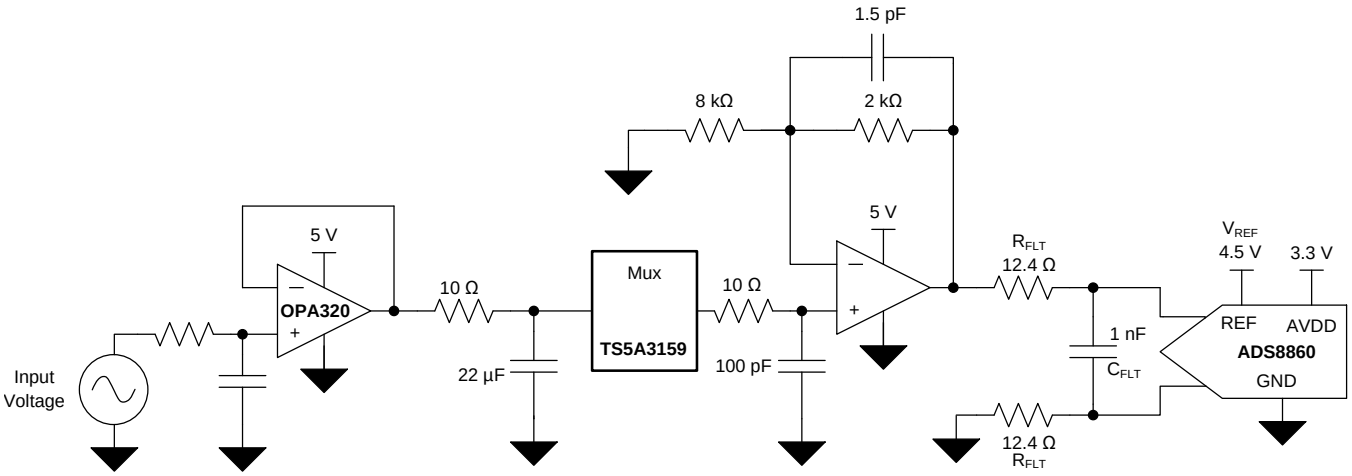


Figure 64. Single-Supply, 16-Bit, 1-MSPS, Multiplexed, SAR ADC Driver

9.2.2.1 Design Requirements

To optimize this circuit for performance, this design does not allow any large signal input transients at the driver circuit inputs for a small quiet-time period (t_{QT}) towards the end of the previous conversion. The input step voltage can appear anytime from the beginning of conversion (CONVST rising edge) until the elapse of a half cycle time ($0.5 \times t_{CYC}$). This timing constraint on the input step allows a minimum settling time of ($t_{QT} + t_{ACQ}$) for the ADC input to settle within the required accuracy, in the worst-case scenario. This provides more time for the output of the amplifer to slew and settle within the required accuracy before the next conversion starts. Figure 65 illustrates this timing sequence.

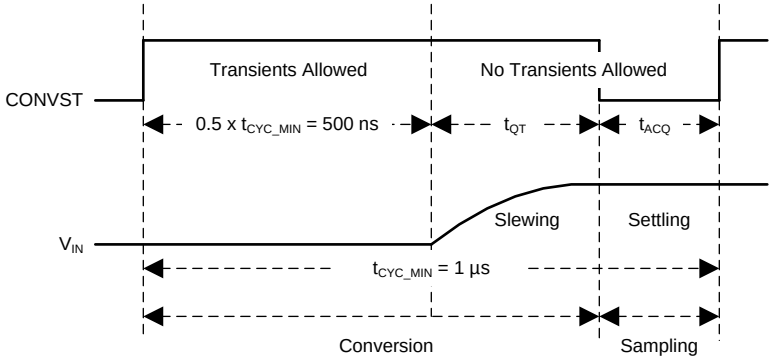


Figure 65. Timing Diagram for Input Signals

9.2.2.2 Detailed Design Procedure

An ADC input driver circuit consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and the low output impedance provides a buffer between the signal source and the ADC input. The RC filter helps attenuate the sampling charge-injection from the switched-capacitor input stage of the ADC and acts as an anti-aliasing filter to band-limit the wideband noise contributed by the front-end circuit. The design of the ADC input driver involves optimizing the bandwidth of the circuit, driven by the following requirements:

- The $R_{FLT}C_{FLT}$ filter bandwidth must be low to band-limit the noise fed into the input of the ADC thereby increasing the signal-to-noise ratio (SNR) of the system.
- The overall system bandwidth must be large enough to accommodate optimal settling of the input signal at the ADC input before the conversion starts.

C_{FLT} is chosen based upon Equation 7 . C_{FLT} is chosen to be 1 nF.

$$C_{FLT} \geq 15 \times C_{SH} \tag{7}$$

Connecting a 1-nF capacitor directly to the output of the OPA626 device would degrade the OPA626 phase margin and result in stability and settling time problems. To properly drive the 1-nF capacitor, a series resistor, R_{FLT}, is used to isolate the capacitor, C_{FLT}, from the OPA626 device. R_{FLT} must be sized based upon several constraints. To determination a suitable value for R_{FLT}, the system designer must consider the impact upon the THD due to the voltage divider effect from R_{FLT} reacting with the switch resistance, R_{SW}, of the ADC input circuit as well as the impact of the output impedance upon amplifier stability. In this example 12.4-Ω resistors are selected. In this design example, Figure 12 can be used to estimate a suitable value for R_{ISO}. R_{ISO} represents the total resistance in series with C_{FLT}, which in this example is equivalent to 2 × R_{FLT}.

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Precision Design, TIDU012, "Power-optimized 16-bit 1MSPS Data Acquisition Block for Lowest Distortion and Noise Reference Design".

9.2.2.3 Application Curves

Figure 66 illustrates the performance of the circuit shown in Figure 64.

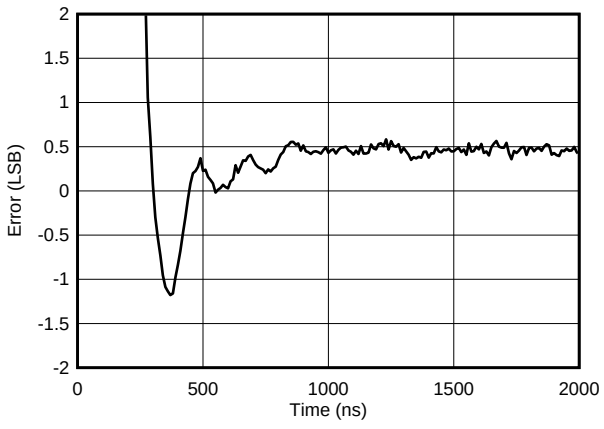


Figure 66. Positive Transient Response for Figure 64

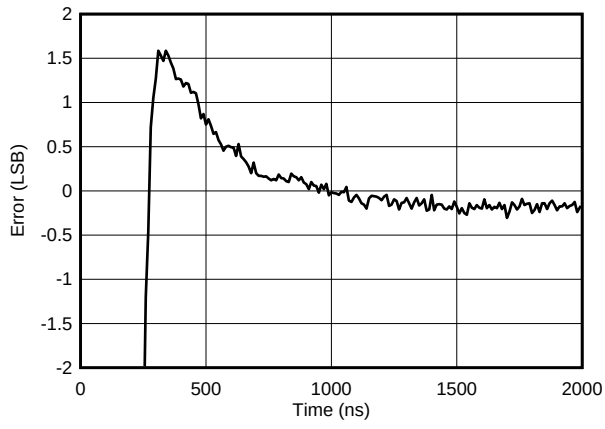


Figure 67. Negative Transient Response for Figure 64

10 Power Supply Recommendations

The OPAx626 family is specified for operation from 2.7 V to 5.5 V (±1.35 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section. Place bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

CAUTION

Supply voltages larger than 6 V can cause permanent damage to the device. See to the section.

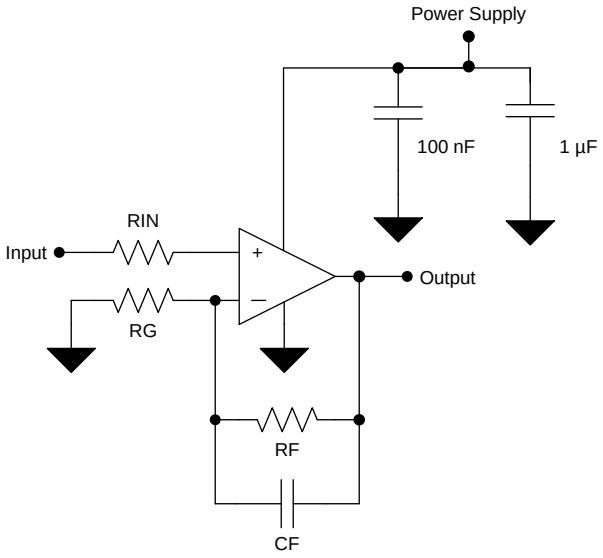
11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Use bypass capacitors to reduce the noise coupled from the power supply. Connect low ESR, ceramic, bypass capacitors between the power supply pins (V+ and V–) and the ground plane. Place the bypass capacitors as close to the device as possible with the 100-nF capacitor closest to the device, as indicated in Figure 68. For single-supply applications, bypass capacitors on the V– pin are not required.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. (For more details, refer to *Circuit Board Layout Techniques*.)
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Minimize parasitic coupling between +IN and OUT for best ac performance.
- Place the external components as close to the device as possible. As shown in Figure 68, keeping RF, CF, and RG close to the inverting input will minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example



(Schematic Representation)

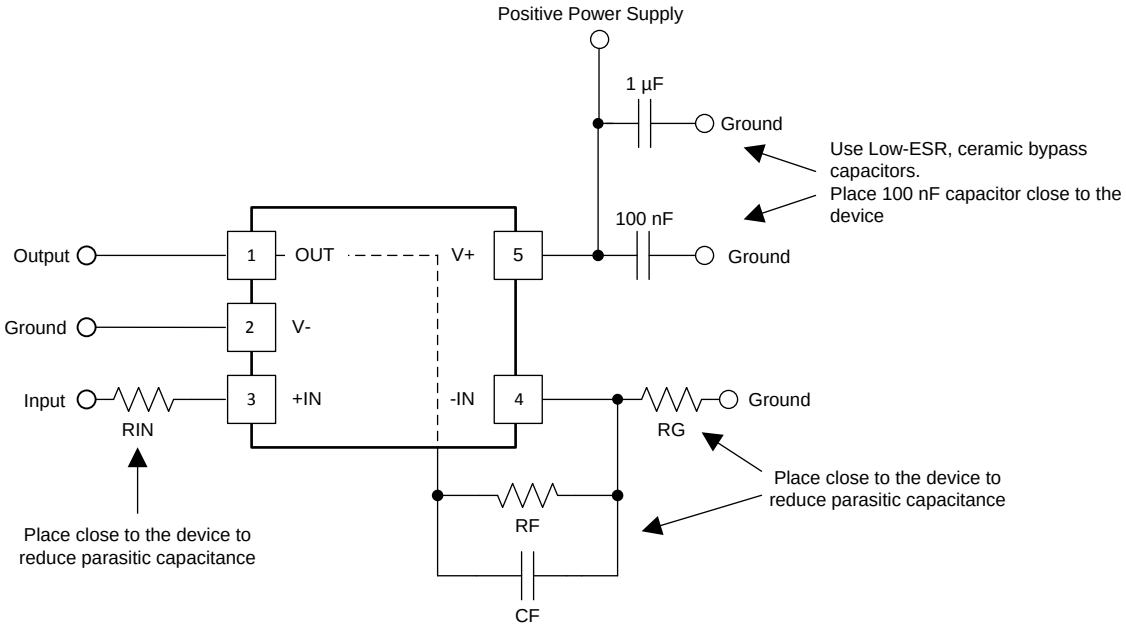


Figure 68. PCB Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

12.1.1.2 TI Precision Designs

TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

12.2 Documentation Support

12.2.1 Related Documentation

16-Bit, 1MSPS Multiplexed Data Acquisition Reference Design Guide

Power-optimized 16-bit 1MSPS Data Acquisition Block for Lowest Distortion and Noise Reference Design

Circuit Board Layout Techniques

12.3 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA626	Click here	Click here	Click here	Click here	Click here
OPA2626	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

E2E is a trademark of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
TINA is a trademark of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2626IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	16R6	Samples
OPA2626IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	16R6	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

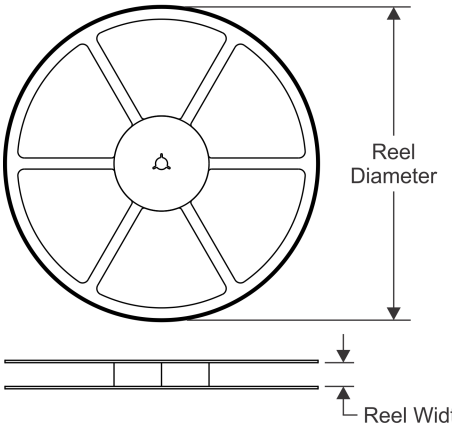
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

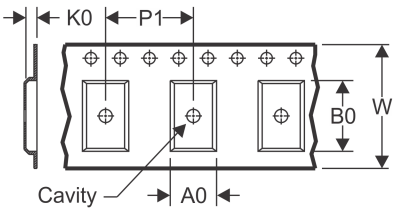
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

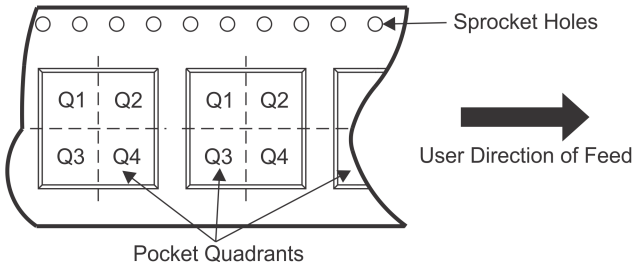


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

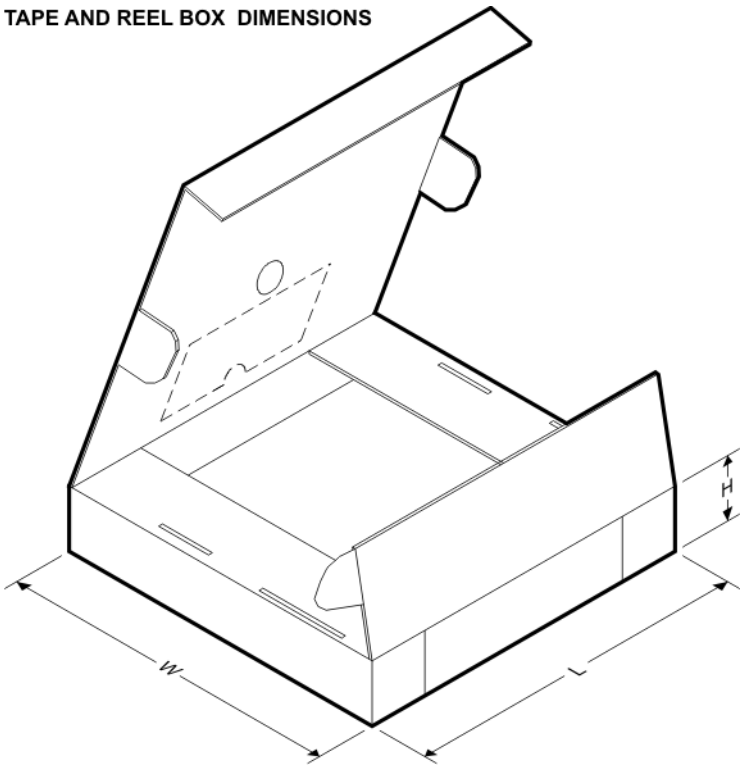
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2626IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2626IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

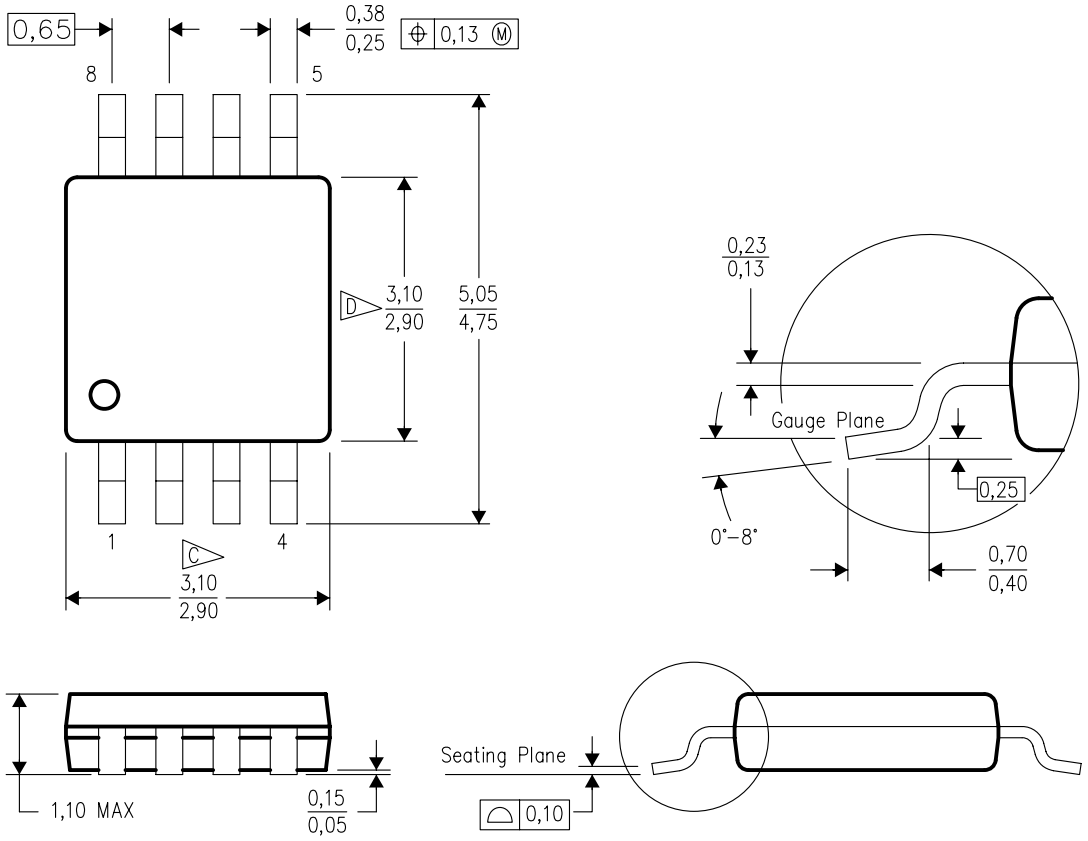
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2626IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2626IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0

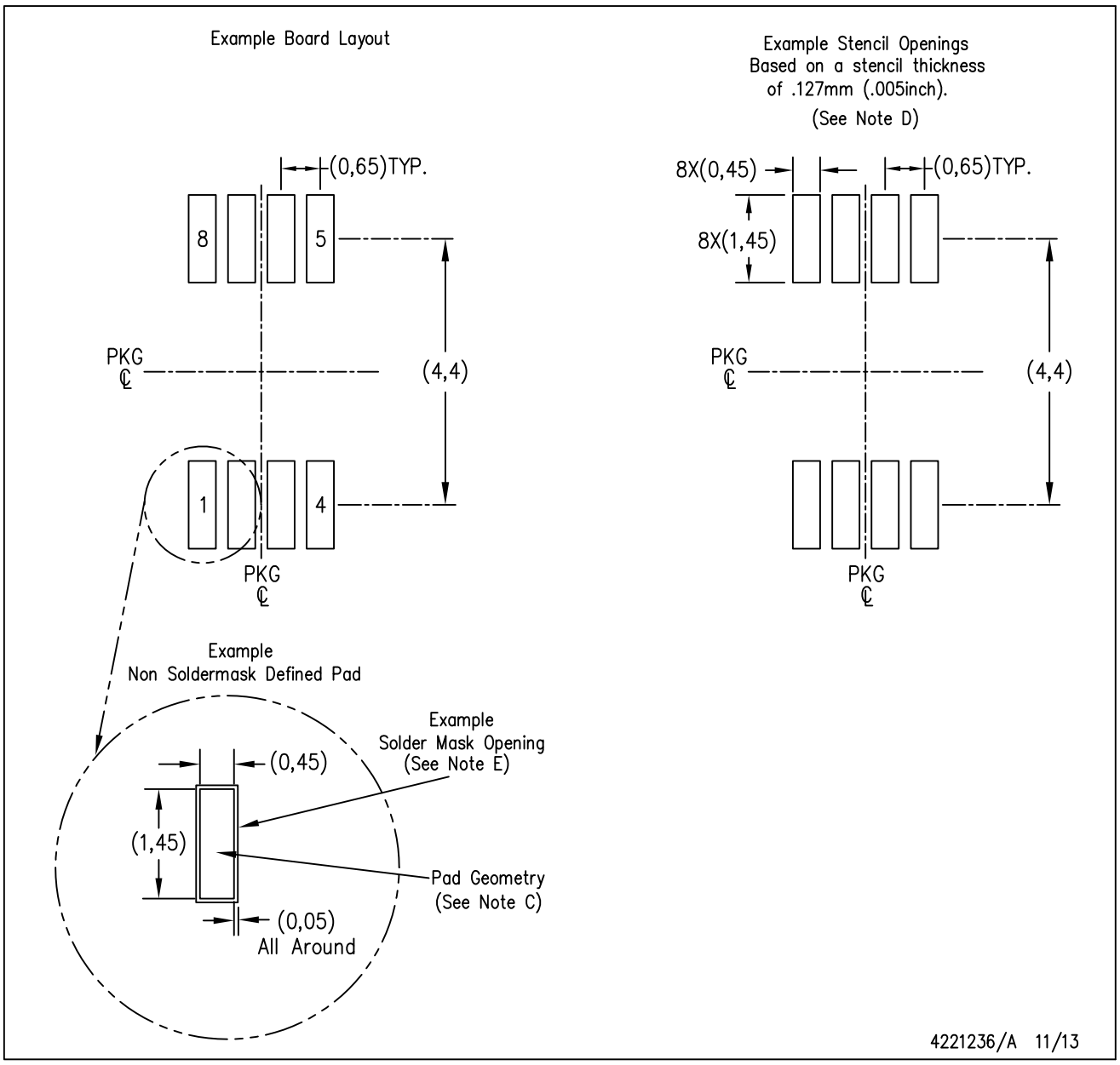
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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