OPAx388 Precision, Zero-Drift, Zero-Crossover, True Rail-to-Rail, Input/Output Operational Amplifiers

1 Features

- Ultra-low offset voltage: ±0.25 µV
- Zero drift: ±0.005 µV/°C
- Zero crossover: 140-dB CMRR true RRIO
- Low noise: 7.0 nV√Hz at 1 kHz
- No 1/f noise: 140 nV_{PP} (0.1 Hz to 10 Hz)
- Fast settling: 2 µs (1 V to 0.01%)
- Gain bandwidth: 10 MHz
- Single supply: 2.5 V to 5.5 V
- Dual supply: ±1.25 V to ±2.75 V
- True rail-to-rail input and output
- EMI/RFI filtered inputs
- Industry-standard packages:
  - Single in SOIC-8, SOT-23-5, and VSSOP-8
  - Dual in SOIC-8 and VSSOP-8
  - Quad in SOIC-14 and TSSOP-14

2 Applications

- Bridge amplifiers
- Strain gauges
- Test equipment
- Current shunt measurement
- Thermocouples, thermopiles
- Electronic scales
- Medical instrumentation
- Resistor thermal detectors
- Precision active filters

3 Description

The OPAx388 (OPA388, OPA2388, and OPA4388) series of precision operational amplifiers are ultra-low noise, fast-settling, zero-drift, zero-crossover devices that provide rail-to-rail input and output operation. These features and excellent ac performance, combined with only 0.25 µV of offset and 0.005 µV/°C of drift over temperature, makes the OPAx388 a great choice for driving high-precision, analog-to-digital converters (ADCs) or buffering the output of high-resolution, digital-to-analog converters (DACs). This design results in excellent performance when driving analog-to-digital converters (ADCs) without degradation of linearity. The OPA388 (single version) is available in the VSSOP-8, SOT23-5, and SOIC-8 packages. The OPA2388 (dual version) is offered in the VSSOP-8 and SO-8 packages. The OPA4388 (quad version) is offered in the TSSOP-14 and SO-14 packages. All versions are specified over the industrial temperature range of –40°C to +125°C.

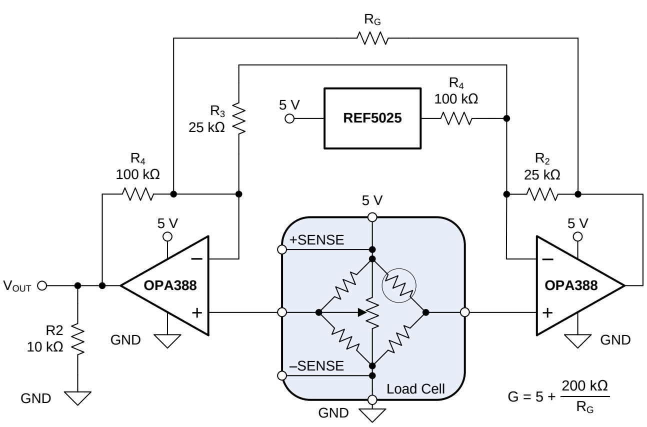
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA388	SOIC (8)	4.90 mm × 3.90 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA2388	SOIC (8)(2)	4.90 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA4388	SOIC (14)	8.65 mm x 3.90 mm
	TSSOP (14)	5.00 mm x 4.40 mm

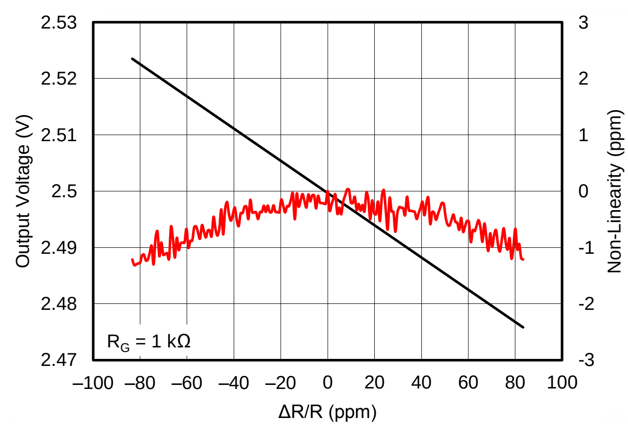
(1) For all available packages, see the package option addendum at the end of the data sheet.

(2) The OPA2388 SOIC (D) package is preview.

The OPA388 in a High-CMRR, Instrumentation Amplifier Application



The OPA388 Allows Precision, Low-Error Measurements



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

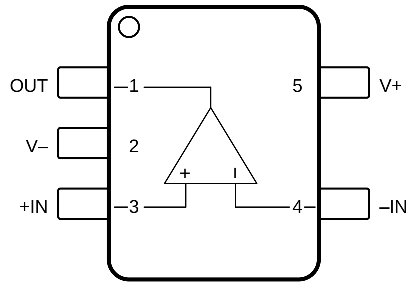
Changes from Revision B (January 2019) to Revision C	Page
• Changed OPA4388 from advanced information (preview) to production data (active)	1
• Added V_{OS} specifications OPA4388.	8
• Added dV_{OS}/dT specifications for OPA4388.	8
• Added PSRR specifications for OPA4388	8
• Added I_B specifications for OPA4388	8
• Added I_{OS} specifications for OPA4388	8
• Added CMRR specifications for OPA4388	8
• Added AOL specifications for OPA4388.	9

Changes from Revision A (July 2018) to Revision B	Page
• Changed OPA388 DBV (SOT-23) package from preview to production data	1
• Deleted redundant temperature specification in EC table.	9
• Added Figure 6, *Offset Voltage vs Supply Voltage: OPA4388*	11
• Added Figure 7, *Offset Voltage Long Term Drift*	12
• Changed Figure 50, *OPA388 Layout Example*; updated for accuracy	26

Changes from Original (December 2016) to Revision A	Page
• Changed device status from Production Data to Production Data/Mixed Status	1
• Added top navigator link for TI reference design	1
• Added preview notes to 5-pin SOT-23 (OPA388), 8-pin SOIC (OPA2388), 14-pin SOIC, and 14-pin TSSOP (OPA4388) packages in *Device Information* table	1
• Added package preview notes to *Pin Configuration and Functions* section	4
• AOL test condition changed to 0.15 V from 0.1 V	9

5 Pin Configuration and Functions

**OPA388 DBV Package
5-Pin SOT-23
Top View**



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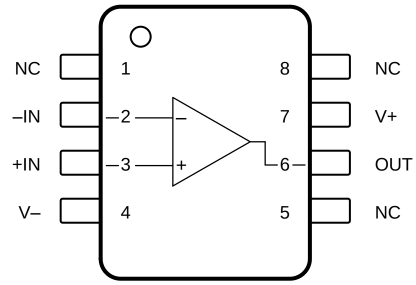
**OPA388 D and DGK Packages
8-Pin SOIC and VSSOP
Top View**



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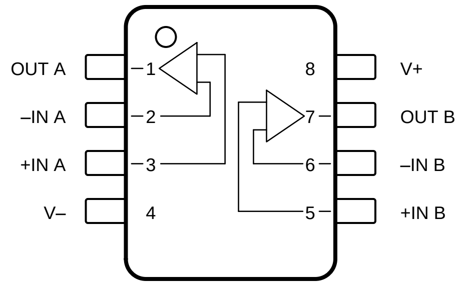
Pin Functions: OPA388

PIN			I/O	DESCRIPTION
NAME	OPA388 D (SOIC), DGK (VSSOP)	OPA388 DBV (SOT-23)		
–IN	2	4	I	Inverting input
+IN	3	3	I	Noninverting input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V–	4	2	—	Negative (lowest) power supply
V+	7	5	—	Positive (highest) power supply

OPA2388 D[(1)] and DGK Packages
8-Pin SOIC and VSSOP
Top View



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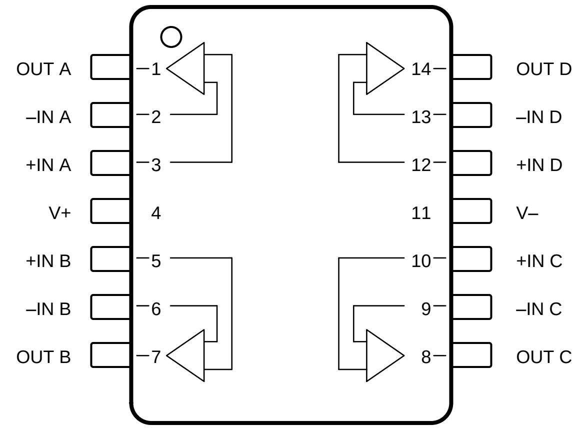
(1) OPA2388 D package is preview.

OPA4388 D and PW Packages
14-Pin SOIC and TSSOP
Top View



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Pin Functions: OPA2388 and OPA4388

PIN			I/O	DESCRIPTION
NAME	OPA2388 D (SOIC), DGK (VSSOP)	OPA4388 D (SOIC), PW (TSSOP)		
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	—	9	I	Inverting input, channel C
–IN D	—	13	I	Inverting input, channel D
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	—	10	I	Noninverting input, channel C
+IN D	—	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	—	8	O	Output, channel C
OUT D	—	14	O	Output, channel D
V–	4	11	—	Negative (lowest) power supply
V+	8	4	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
Supply voltage	V_S = (V+) – (V–)	Single-supply		6	V
		Dual-supply		±3	
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current			±10	mA
Output short circuit[2]			Continuous	Continuous	
Temperature	Operating, T_A		–55	150	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Single-supply	2.5		5.5	V
	Dual-supply	±1.25		±2.75	
Specified temperature		–40		125	°C

6.4 Thermal Information: OPA388

THERMAL METRIC[(1)]		OPA388 D (SOIC) 8 PINS	OPA388 DBV (SOT-23) 5 PINS	OPA388 DGK (VSSOP) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116	145.7	177	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60	94.8	69	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56	43.4	100	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	12.8	24.7	9.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	55.9	43.1	98.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information: OPA2388

THERMAL METRIC[(1)]		OPA2388 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	85	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Thermal Information: OPA4388

THERMAL METRIC[(1)]		OPA4388 D (SOIC) 14 PINS	OPA4388 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.4	109.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.3	27.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.0	56.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.3	1.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.7	54.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.7 Electrical Characteristics: V_S = ±1.25 V to ±2.75 V (V_S = 2.5 to 5.5 V)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage		OPA388, OPA2388		±0.25	±5	µV
		V_S = 5.5 V	OPA4388		±2.25	±8	
		T_A = –40°C to +125°C	OPA388, OPA2388			±7.5	
		T_A = –40°C to +125°C, V_S = 5.5 V	OPA4388			±10.5	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C	OPA388, OPA2388		±0.005	±0.05	µV/°C
		T_A = –40°C to +125°C, V_S = 5.5 V	OPA4388		±0.005	±0.05	
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C	OPA388, OPA2388		±0.1	±1	µV/V
			OPA4388		±1.25	±3.5	
INPUT BIAS CURRENT							
I_B	Input bias current	R_{IN} = 100 kΩ, OPA388, OPA2388			±30	±350	pA
			T_A = 0°C to +85°C			±400	
			T_A = –40°C to +125°C			±700	
		R_{IN} = 100 kΩ, OPA4388			±30	±500	
			T_A = 0°C to +85°C			±600	
			T_A = –40°C to +125°C			±800	
I_{OS}	Input offset current	R_{IN} = 100 kΩ, OPA388, OPA2388				±700	
			T_A = 0°C to +85°C			±800	
			T_A = –40°C to +125°C			±800	
		R_{IN} = 100 kΩ, OPA4388				±1000	
			T_A = 0°C to +85°C			±1100	
			T_A = –40°C to +125°C			±1100	
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			0.14		μV_{PP}
e_N	Input voltage noise density	f = 10 Hz			7		nV/√Hz
		f = 100 Hz			7		
		f = 1 kHz			7		
		f = 10 kHz			7		
I_N	Input current noise density	f = 1 kHz			100		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	V_S = ±1.25 V OPA388, OPA2388	124	138		dB
			V_S = ±1.25 V OPA4388	102	110		
			V_S = ±2.75 V	124	140		
		(V–) < V_{CM} < (V+) + 0.1 V, T_A = –40°C to +125°C	V_S = ±1.25 V OPA388, OPA2388	114	134		
			V_S = ±1.25 V OPA4388	102	107		
		(V–) – 0.05 V < V_{CM} < (V+) + 0.1 V, T_A = –40°C to +125°C	V_S = ±2.75 V	124	140		
INPUT IMPEDANCE							
z_{id}	Differential input impedance				100 || 2		MΩ || pF
z_{ic}	Common-mode input impedance				60 || 4.5		TΩ || pF

Electrical Characteristics: V_S = ±1.25 V to ±2.75 V (V_S = 2.5 to 5.5 V) (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ		126	148		dB
		(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ, T_A = –40°C to +125°C	OPA388, OPA2388	120	126		
		(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ, V_S = 5.5 V T_A = –40°C to +125°C	OPA4388	120	126		
		(V–) + 0.25 V < V_O < (V+) – 0.25 V, R_{LOAD} = 2 kΩ		126	148		
		(V–) + 0.30 V < V_O < (V+) – 0.30 V, R_{LOAD} = 2 kΩ	OPA388, OPA2388	120	148		
		(V–) + 0.30 V < V_O < (V+) – 0.30 V, R_{LOAD} = 2 kΩ, V_S = 5.5 V T_A = –40°C to +125°C	OPA4388	120	126		
FREQUENCY RESPONSE							
GBW	Unity-gain bandwidth				10		MHz
SR	Slew rate	G = 1, 4-V step			5		V/µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 1 V_{RMS}			0.0005%		
t_S	Settling time	To 0.1%	V_S = ±2.5 V, G = 1, 1-V step		0.75		µs
		To 0.01%	V_S = ±2.5 V, G = 1, 1-V step		2		µs
t_{OR}	Overload recovery time	V_{IN} × G = V_S			10		µs
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		1	15	mV
			R_{LOAD} = 10 kΩ		5	20	
			R_{LOAD} = 2 kΩ		20	50	
		Negative rail	No load		5	15	
			R_{LOAD} = 10 kΩ		10	20	
			R_{LOAD} = 2 kΩ		40	60	
		T_A = –40°C to +125°C, both rails, R_{LOAD} = 10 kΩ			10	25	
I_{SC}	Short-circuit current	V_S = 5.5 V			±60		mA
		V_S = 2.5 V			±30		mA
C_{LOAD}	Capacitive load drive	See Figure 26					
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A, see Figure 25			100		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = ±1.25 V (V_S = 2.5 V)	I_O = 0 A		1.7	2.4	mA
			T_A = –40°C to +125°C, I_O = 0 A		1.7	2.4	
		V_S = ±2.75 V (V_S = 5.5 V)	I_O = 0 A		1.9	2.6	
			T_A = –40°C to +125°C, I_O = 0 A		1.9	2.6	

6.8 Typical Characteristics

Table 1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution From –40°C to +125°C	Figure 2
Offset Voltage vs Temperature	Figure 3
Offset Voltage vs Common-Mode Voltage	Figure 4
Offset Voltage vs Power Supply: OPA388 and OPA2388	Figure 5
Offset Voltage vs Power Supply: OPA4388	Figure 6
Offset Voltage Long Term Drift	Figure 7
Open-Loop Gain and Phase vs Frequency	Figure 8
Closed-Loop Gain and Phase vs Frequency	Figure 9
Input Bias Current vs Common-Mode Voltage	Figure 10
Input Bias Current vs Temperature	Figure 11
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 12
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PSRR vs Temperature	Figure 15
0.1-Hz to 10-Hz Noise	Figure 16
Input Voltage Noise Spectral Density vs Frequency	Figure 17
THD+N Ratio vs Frequency	Figure 18
THD+N vs Output Amplitude	Figure 19
Spectral Content	Figure 20, Figure 21
Quiescent Current vs Supply Voltage	Figure 22
Quiescent Current vs Temperature	Figure 23
Open-Loop Gain vs Temperature	Figure 24
Open-Loop Output Impedance vs Frequency	Figure 25
Small-Signal Overshoot vs Capacitive Load (10-mV Step)	Figure 26
No Phase Reversal	Figure 27
Positive Overload Recovery	Figure 28
Negative Overload Recovery	Figure 29
Small-Signal Step Response (10-mV Step)	Figure 30, Figure 31
Large-Signal Step Response (4-V Step)	Figure 32 , Figure 33
Settling Time	Figure 34, Figure 35
Short-Circuit Current vs Temperature	Figure 36
Maximum Output Voltage vs Frequency	Figure 37
EMIRR vs Frequency	Figure 38

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

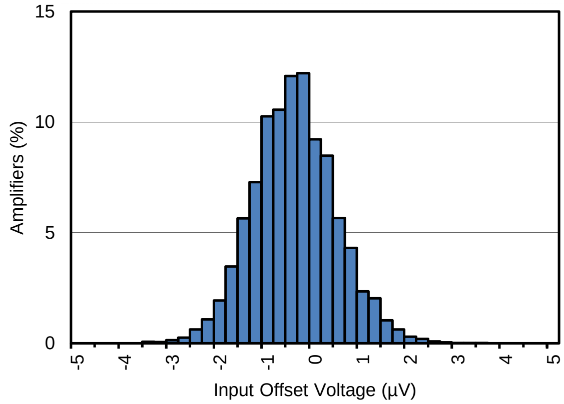


Figure 1. Offset Voltage Production Distribution

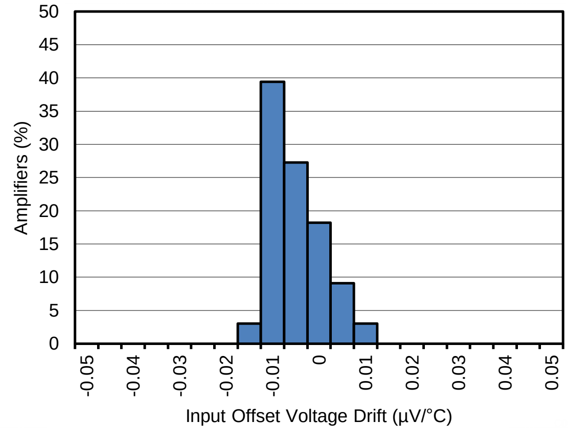


Figure 2. Offset Voltage Drift Distribution From –40°C to +125°C

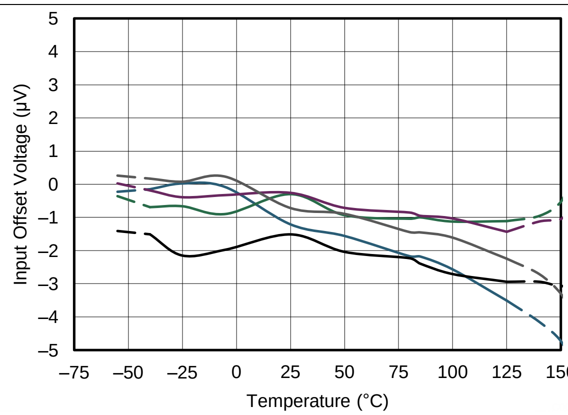


Figure 3. Offset Voltage vs Temperature

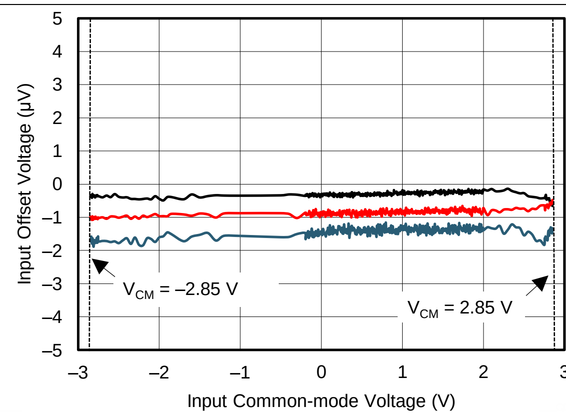


Figure 4. Offset Voltage vs Common-Mode Voltage

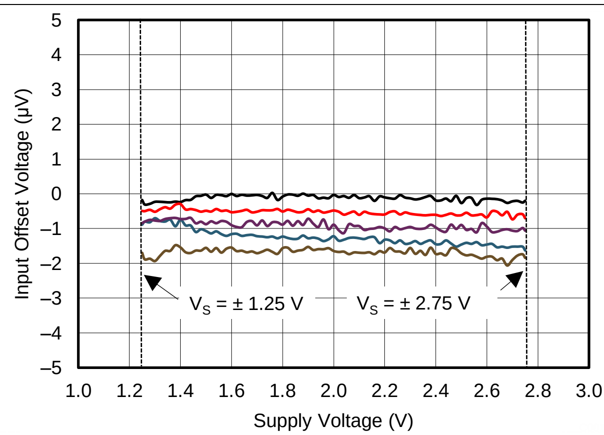


Figure 5. Offset Voltage vs Supply Voltage: OPA388 and OPA2388

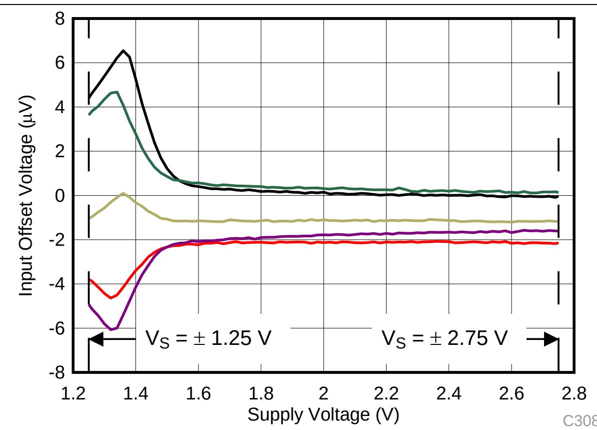


Figure 6. Offset Voltage vs Supply Voltage: OPA4388

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

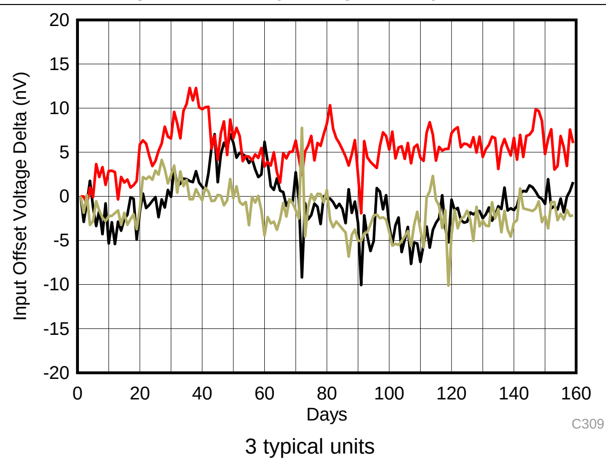


Figure 7. Offset Voltage Long Term Drift

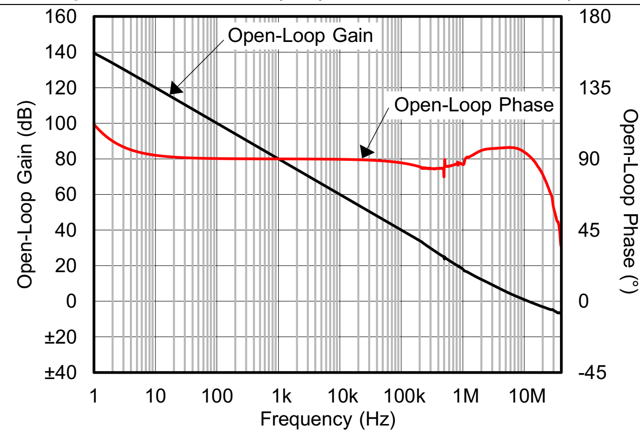


Figure 8. Open-Loop Gain and Phase vs Frequency

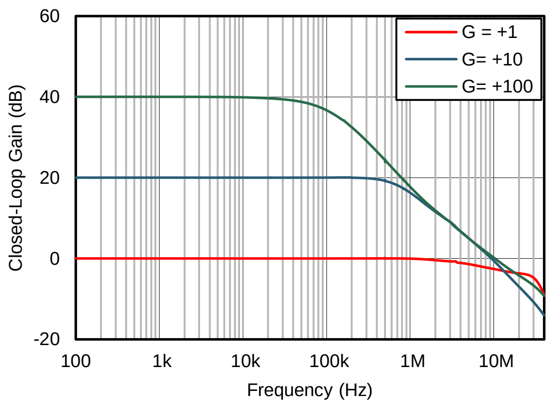


Figure 9. Closed-Loop Gain and Phase vs Frequency

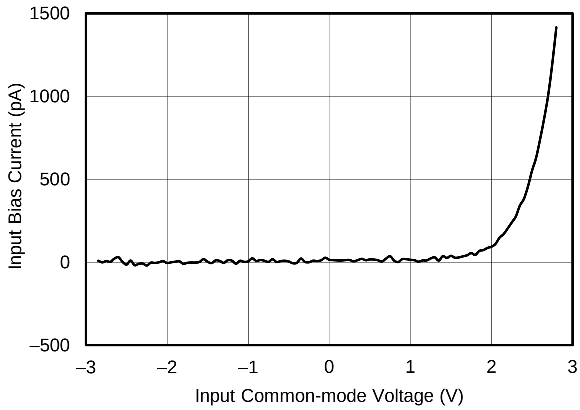


Figure 10. Input Bias Current vs Common-Mode Voltage

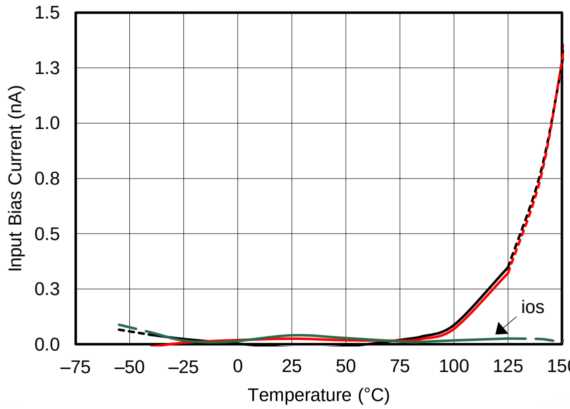


Figure 11. Input Bias Current vs Temperature

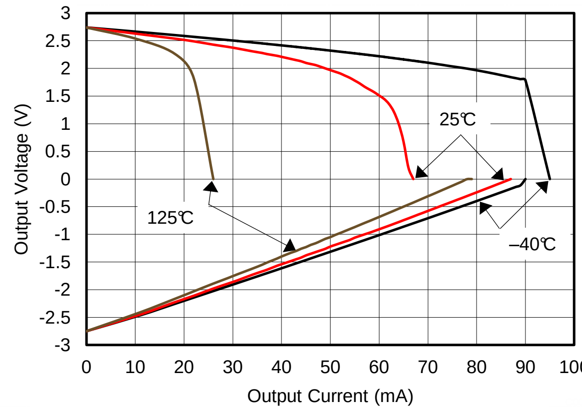


Figure 12. Output Voltage Swing vs Output Current (Maximum Supply)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

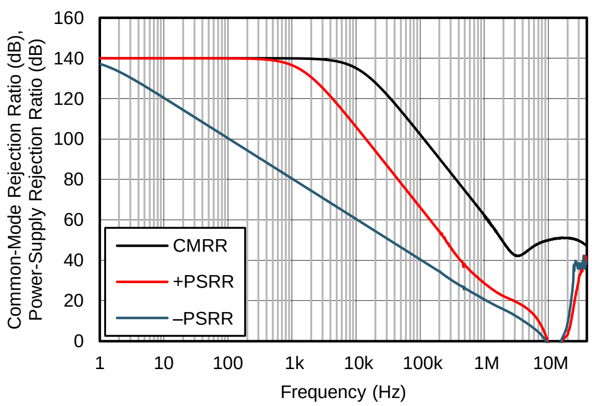


Figure 13. CMRR and PSRR vs Frequency

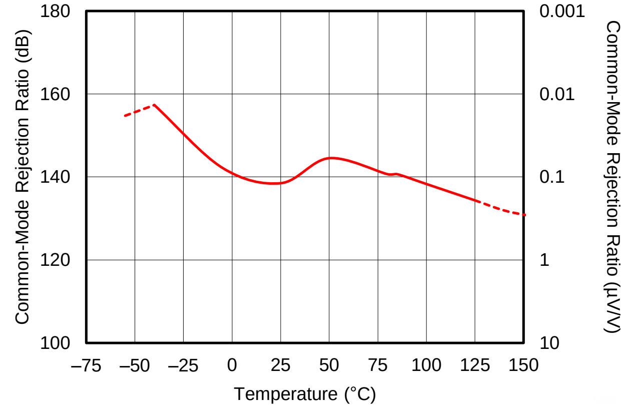


Figure 14. CMRR vs Temperature

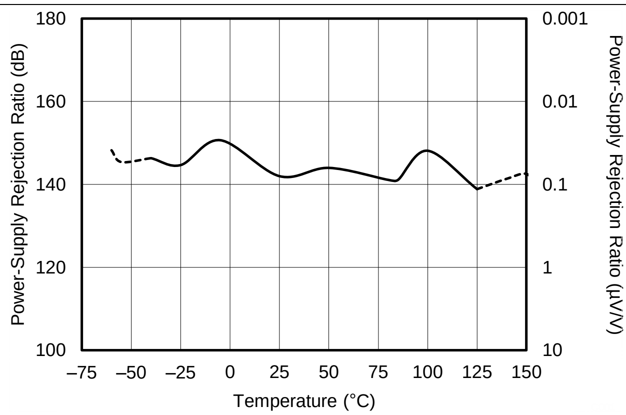


Figure 15. PSRR vs Temperature

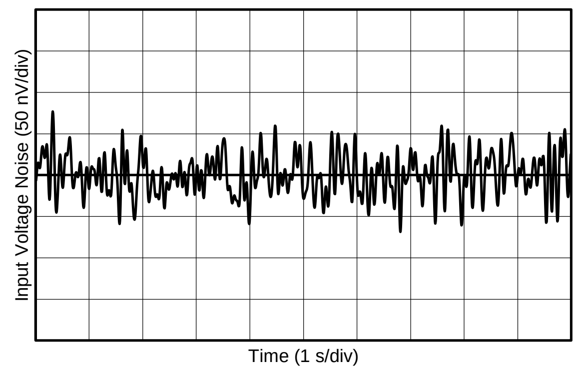


Figure 16. 0.1-Hz to 10-Hz Noise

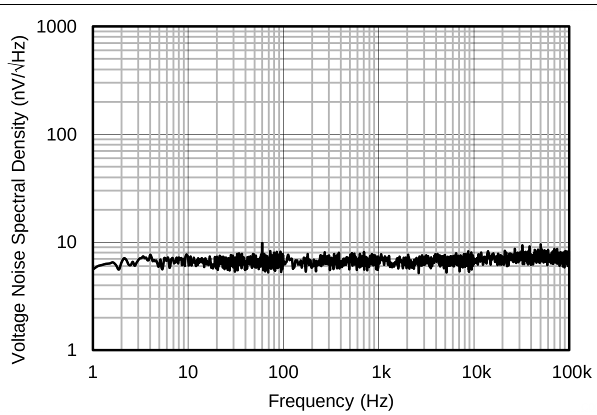


Figure 17. Input Voltage Noise Spectral Density vs Frequency

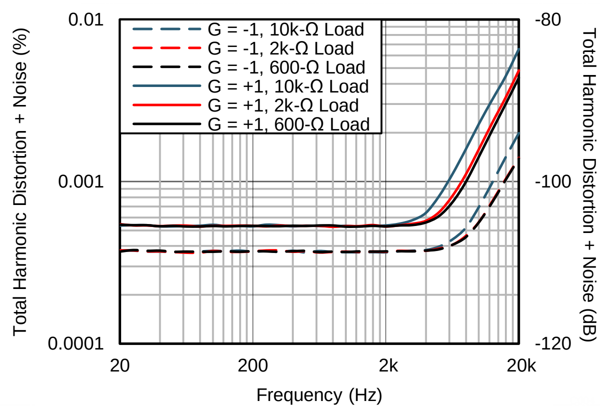


Figure 18. THD+N Ratio vs Frequency

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

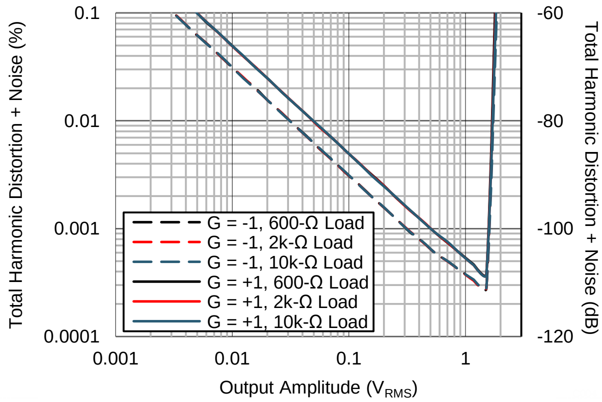
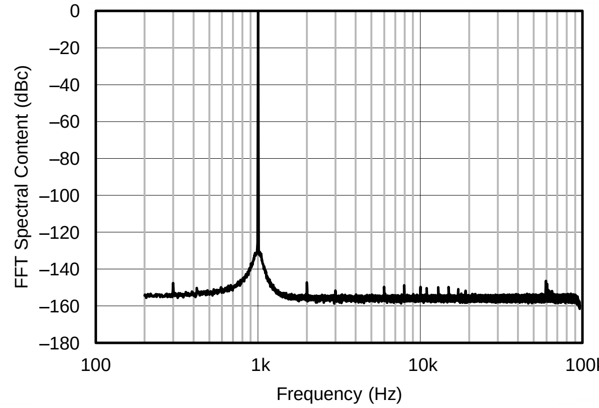
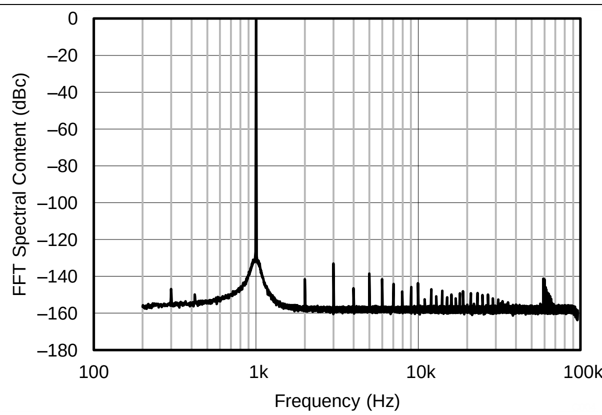


Figure 19. THD+N vs Output Amplitude



G = +1, f = 1 kHz, V_O = 4.5 V_{PP}, R_L = 10 kΩ, BW = 90 kHz

Figure 20. Spectral Content (With 10-kΩ Load)



G = +1, f = 1 kHz, V_O = 4.5 V_{PP}, R_L = 2 kΩ, BW = 90 kHz

Figure 21. Spectral Content (With 2-kΩ Load)

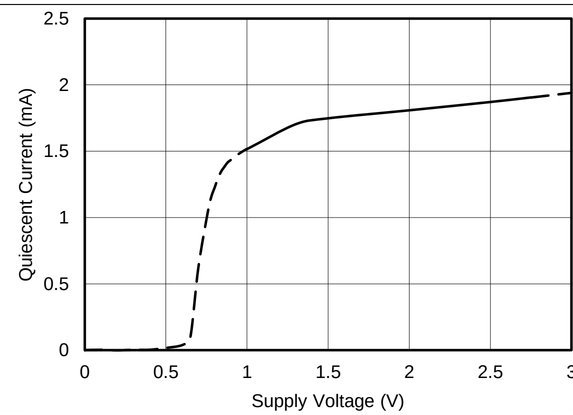


Figure 22. Quiescent Current vs Supply Voltage

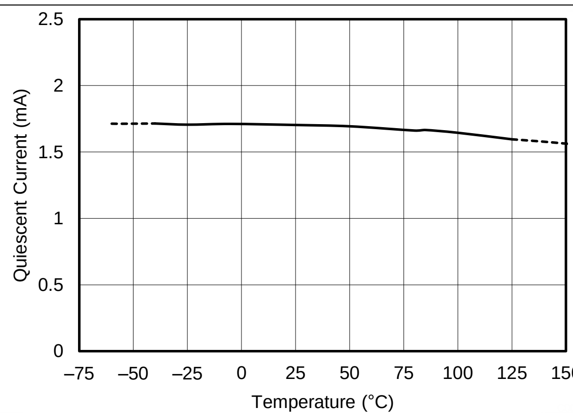


Figure 23. Quiescent Current vs Temperature

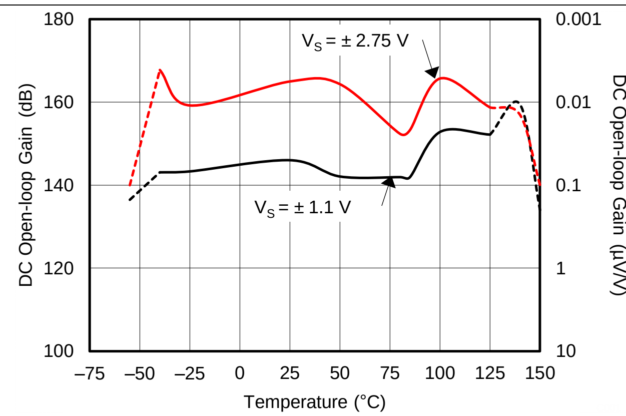


Figure 24. Open-Loop Gain vs Temperature

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

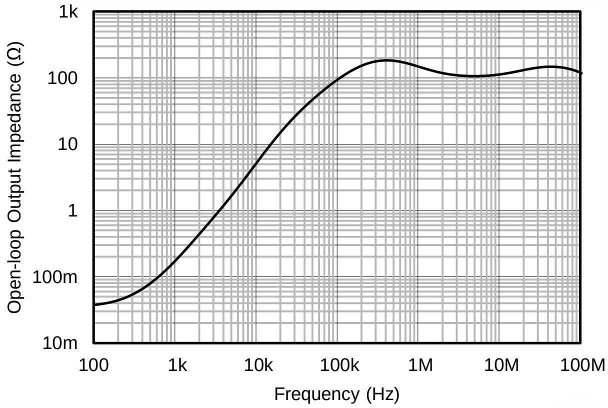


Figure 25. Open-Loop Output Impedance vs Frequency

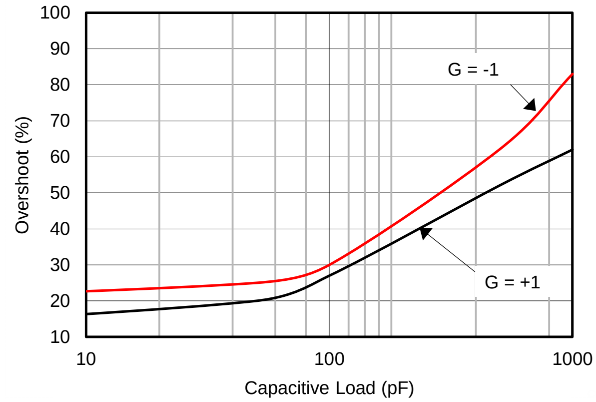


Figure 26. Small-Signal Overshoot vs Capacitive Load (10-mV Step)

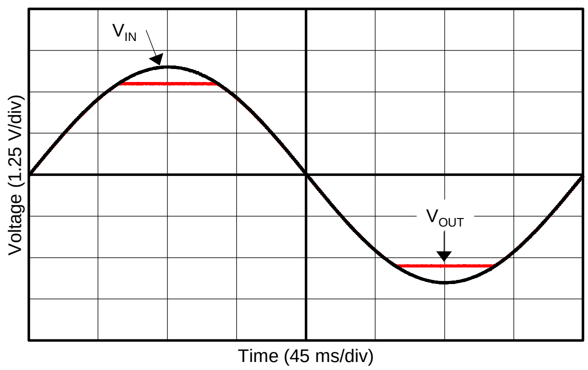


Figure 27. No Phase Reversal

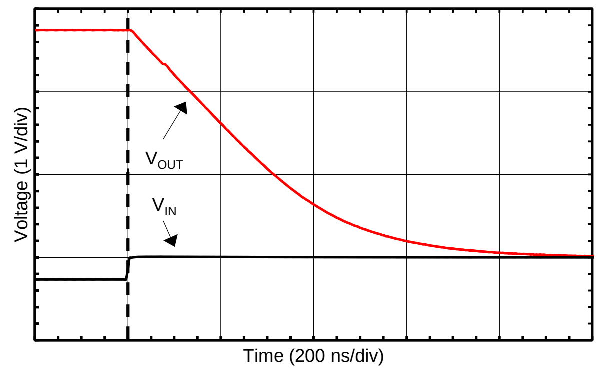


Figure 28. Positive Overload Recovery

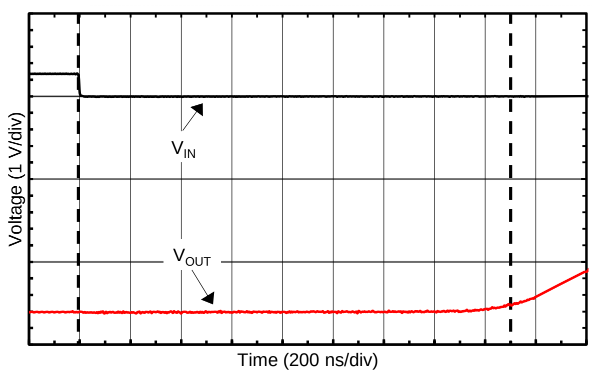
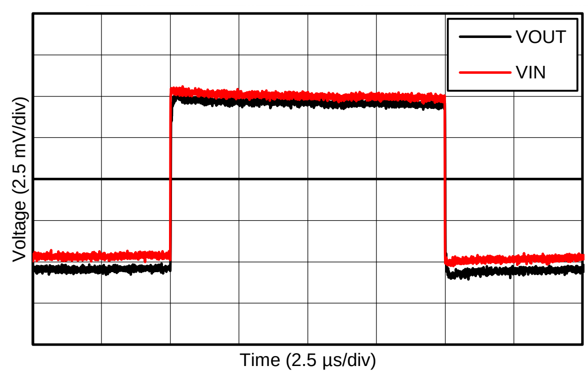


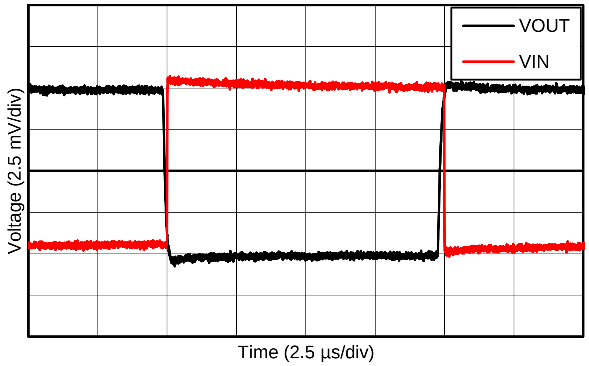
Figure 29. Negative Overload Recovery



G = +1

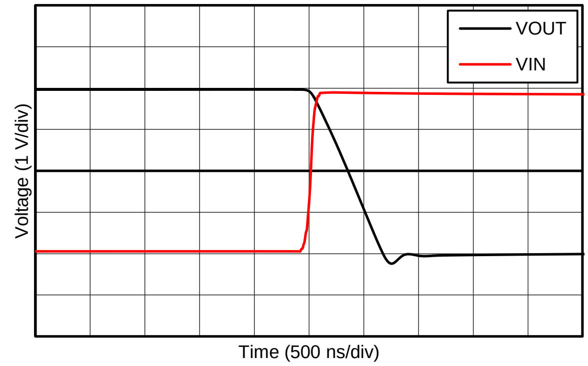
Figure 30. Small-Signal Step Response (10-mV Step)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



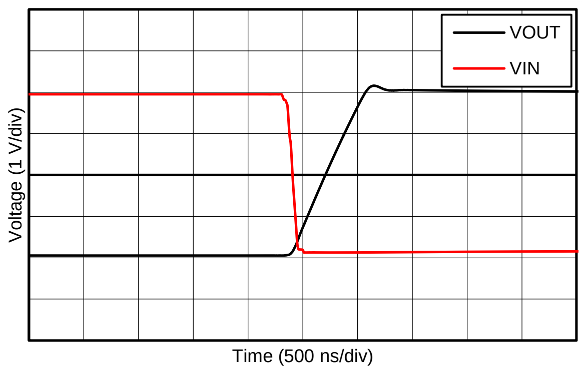
G = –1

Figure 31. Small-Signal Step Response (10-mV Step)



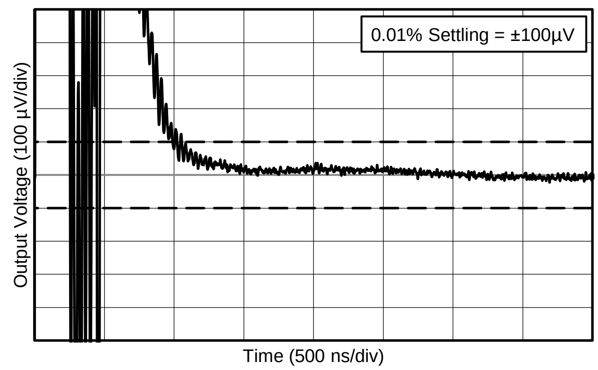
Falling output

Figure 32. Large-Signal Step Response (4-V Step)



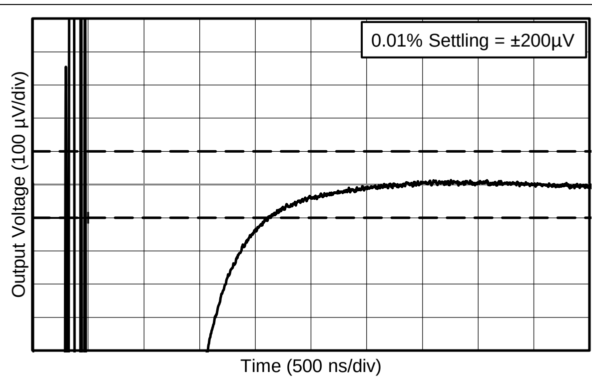
Rising output

Figure 33. Large-Signal Step Response (4-V Step)



0.01% settling = ±100 µV

Figure 34. Settling Time (1-V Positive Step)



0.01% settling = ±200 µV

Figure 35. Settling Time (1-V Negative Step)

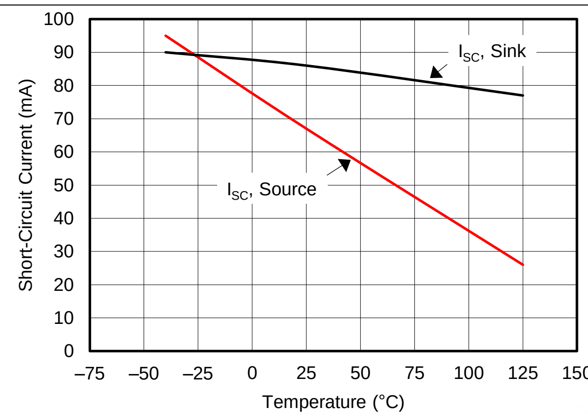


Figure 36. Short-Circuit Current vs Temperature

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

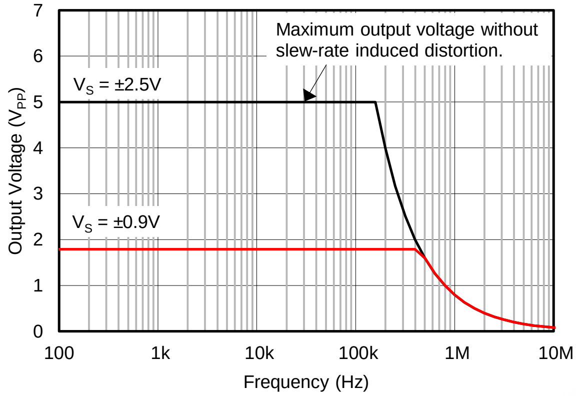


Figure 37. Maximum Output Voltage vs Frequency

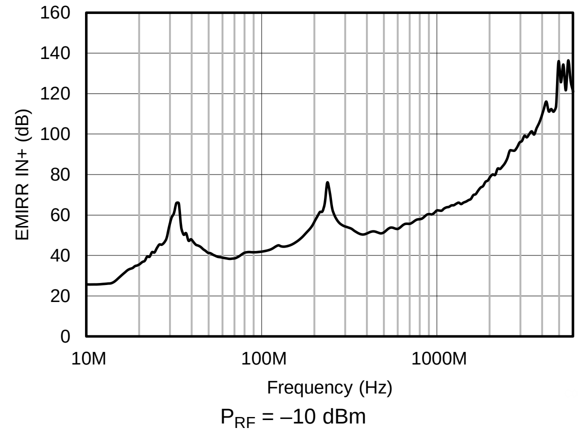


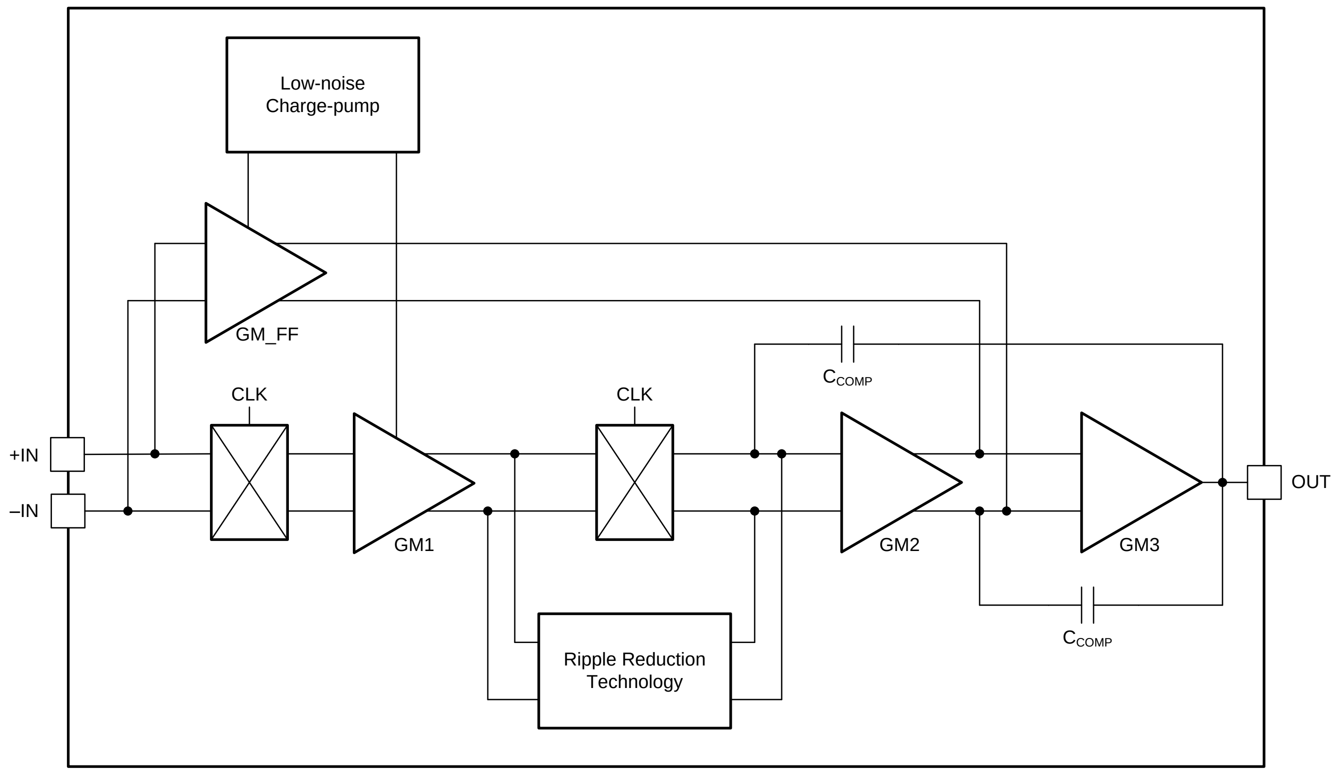
Figure 38. EMIRR vs Frequency

7 Detailed Description

7.1 Overview

The OPAx388 family of zero-drift amplifiers is engineered with the unique combination of a proprietary precision auto-calibration technique paired with a low-noise, low-ripple, input charge pump. These amplifiers offer ultra-low input offset voltage and drift and achieve excellent input and output dynamic linearity. The OPAx388 operates from 2.5 V to 5.5 V, is unity-gain stable, and is suitable for a wide range of general-purpose and precision applications. The integrated, low-noise charge pump allows true rail-to-rail input common-mode operation without distortion associated with complementary rail-to-rail input topologies (input crossover distortion). The OPAx388 strengths also include 10-MHz bandwidth, 7-nV/√Hz noise spectral density, and no 1/f noise, making the OPAx388 optimal for interfacing with sensor modules and buffering high-fidelity, digital-to-analog converters (DACs).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPA3x88 family of operational amplifiers can be used with single or dual supplies from an operating range of V_S = 2.5 V (±1.25 V) up to 5.5 V (±2.75 V). Supply voltages greater than 7 V can permanently damage the device (see *Absolute Maximum Ratings*). Key parameters that vary over the supply voltage or temperature range are shown in the *Typical Characteristics* section.

7.3.2 Input Voltage and Zero-Crossover Functionality

The OPAx388 input common-mode voltage range extends 0.1 V beyond the supply rails. This amplifier family is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers. Operating a complementary rail-to-rail input amplifier with signals traversing the transition region results in unwanted non-linear behavior and polluted spectral content. Figure 39 and Figure 40 contrast the performance of a traditional complementary rail-to-rail input stage amplifier with the performance of the zero-crossover OPA388. Significant harmonic content and distortion is generated during the differential pair transition (such a transition does not exist in the OPA388). Crossover distortion is eliminated through the use of a single differential pair coupled with an internal low-noise charge pump. The OPAx388 maintains noise, bandwidth, and offset performance throughout the input common-mode range, thus reducing printed circuit board (PCB) and bill of materials (BOM) complexity through the reduction of power-supply rails.

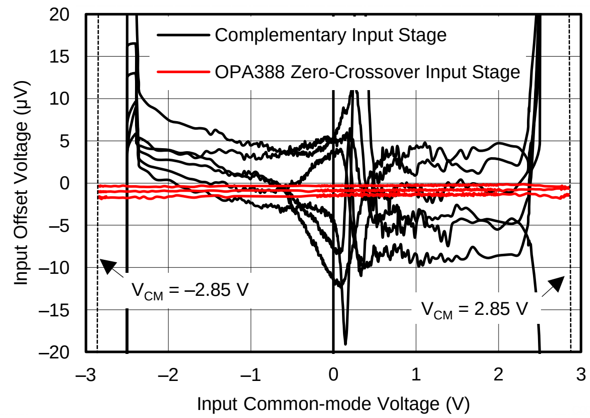


Figure 39. Input Crossover Distortion Nonlinearity

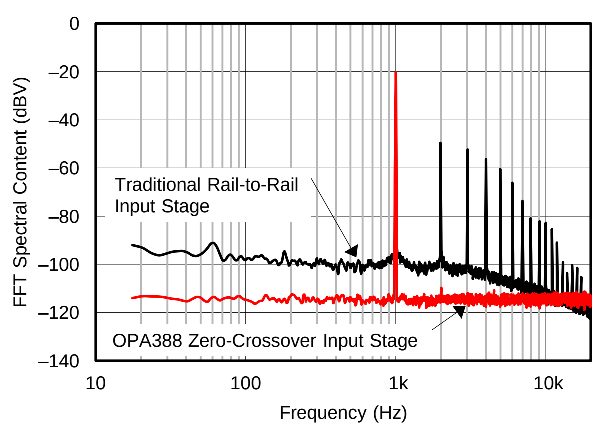


Figure 40. Input Crossover Distortion Spectral Content

Feature Description (continued)

Typically, input bias current is approximately ±30 pA. Input voltages exceeding the power supplies, however, can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 41.

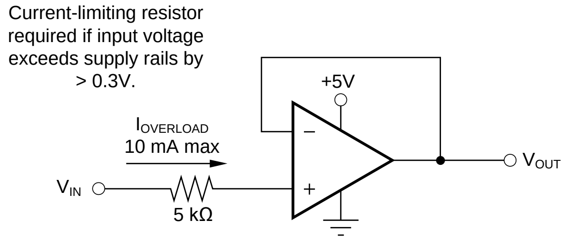


Figure 41. Input Current Protection

7.3.3 Input Differential Voltage

The typical input bias current of the OPAx388 during normal operation is approximately 30 pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with 10-kΩ electromagnetic interference (EMI) filter resistors to create the equivalent circuit shown in Figure 42. Notice that the input bias current remains within specification in the linear region.

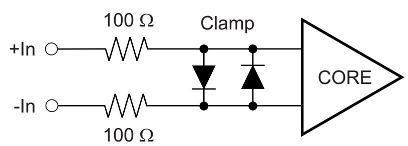


Figure 42. Equivalent Input Circuit

7.3.4 Internal Offset Correction

The OPA388 family of operational amplifiers uses an auto-calibration technique with a time-continuous, 200-kHz operational amplifier in the signal path. This amplifier is zero-corrected every 5 µs using a proprietary technique. At power-up, the amplifier requires approximately 1 ms to achieve the specified V_{OS} accuracy. This design has no aliasing or flicker noise.

7.3.5 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPAx388 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential-mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 20 MHz (–3 dB), with a rolloff of 20 dB per decade.

7.4 Device Functional Modes

The OPA388 has a single functional mode and is operational when the power-supply voltage is greater than 2.5 V (±1.25 V). The maximum specified power-supply voltage for the OPAx388 is 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx388 is a unity-gain stable, precision operational amplifier family free from unexpected output and phase reversal. The use of proprietary zero-drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lowering the 1/f noise component. As a result of the high PSRR, these devices work well in applications that run directly from battery power without regulation. The OPAx388 family is optimized for full rail-to-rail input, allowing for low-voltage, single-supply operation or split-supply use. These miniature, high-precision, low-noise amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies without input crossover distortion and a rail-to-rail output that swings within 5 mV of the supplies under normal test conditions. The OPAx388 series of precision amplifiers is suitable for upstream analog signal chain applications in low or high gains, as well as downstream signal chain functions such as DAC buffering.

8.2 Typical Applications

8.2.1 Bidirectional Current-Sensing

This single-supply, low-side, bidirectional current-sensing solution detects load currents from –1 A to +1 A. The single-ended output spans from 110 mV to 3.19 V. This design uses the OPAx388 because of its low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage.

Figure 43 shows the solution.

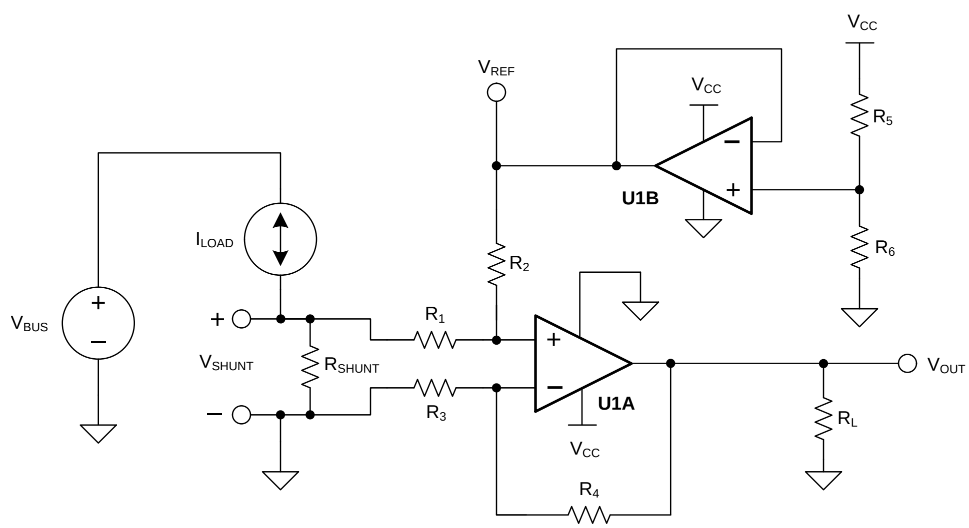


Figure 43. Bidirectional Current-Sensing Schematic

Typical Applications (continued)

8.2.1.1 Design Requirements

This solution has the following requirements:

- Supply voltage: 3.3 V
- Input: –1 A to 1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

8.2.1.2 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor (R_{SHUNT}) to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier consisting of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{REF}$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff\_Amp} = \dfrac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\dfrac{R_6}{R_5 + R_6}\right)$ (1)

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4 / R_3 matches R_2 / R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of V_{SHUNT} is the ground potential for the system load because V_{SHUNT} is a low-side measurement. Therefore, a maximum value must be placed on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100 mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT(Max)} = \frac{V_{SHUNT(Max)}}{I_{LOAD(Max)}} = \frac{100\text{ mV}}{1\text{ A}} = 100\text{ m}\Omega \quad (2)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100 mV to 100 mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Take care to ensure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Therefore, use an operational amplifier, such as the OPA388, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, note that the OPA388 has a typical offset voltage of merely ±0.25 µV (±5 µV maximum).

Given a symmetric load current of –1 A to 1 A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10-kΩ resistors were used.

To set the gain of the difference amplifier, the common-mode range and output swing of the OPA388 must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the OPA388 given a 3.3-V supply.

$$-100\text{ mV} < V_{CM} < 3.4\text{ V} \quad (3)$$

$$100\text{ mV} < V_{OUT} < 3.2\text{ V} \quad (4)$$

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$Gain_{Diff\_Amp} = \frac{V_{OUT\_Max} - V_{OUT\_Min}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2\text{ V} - 100\text{ mV}}{100\text{ m}\Omega \times [1\text{ A} - (-1\text{A})]} = 15.5\ \frac{\text{V}}{\text{V}} \quad (5)$$

Typical Applications (continued)

The resistor value selected for R_1 and R_3 was 1 kΩ. 15.4 kΩ was selected for R_2 and R_4 because this number is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

8.2.1.3 Application Curve

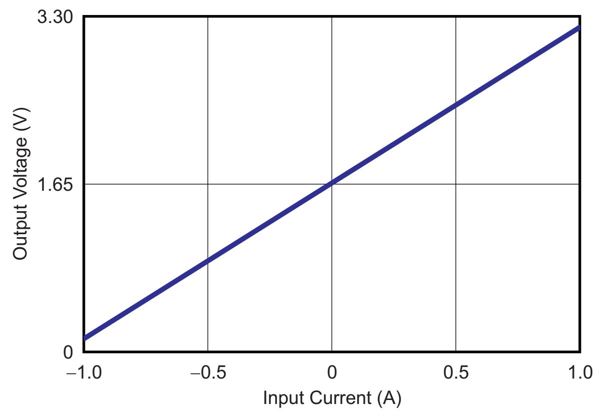


Figure 44. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

Typical Applications (continued)

8.2.2 Single Operational Amplifier Bridge Amplifier

Figure 45 shows the basic configuration for a bridge amplifier.

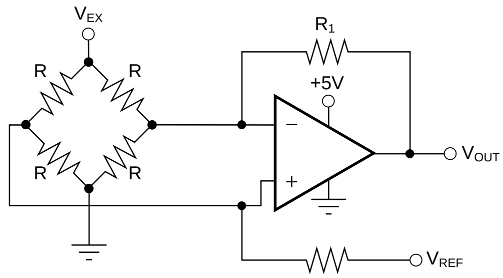


Figure 45. Single Operational Amplifier Bridge Amplifier Schematic

8.2.3 Precision, Low-Noise, DAC Buffer

The OPA388 can be used for a precision DAC buffer, as shown in Figure 46, in conjunction with the DAC8830.

The OPA388 provides an ultra-low drift, precision output buffer for the DAC. A wide range of DAC codes can be used in the linear region because the OPA388 employs zero-crossover technology. A precise reference is essential for maximum accuracy because the DAC8830 is a 16-bit converter.

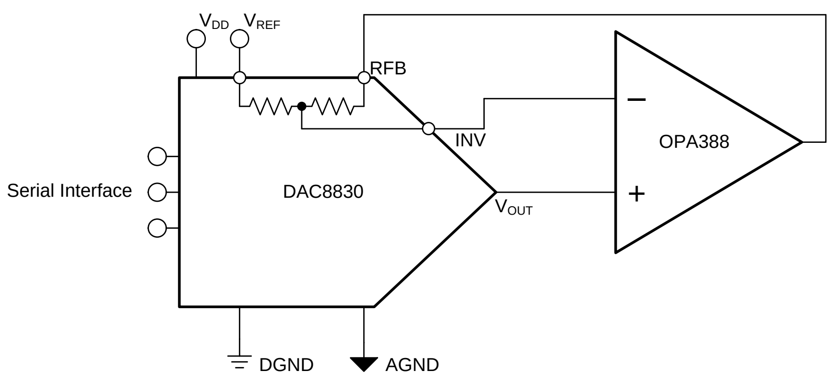


Figure 46. Precision DAC Buffer

Typical Applications (continued)

8.2.4 Load Cell Measurement

Figure 47 shows the OPA388 in a high-CMRR dual-op amp instrumentation amplifier with a trim resistor and 6-wire load cell for precision measurement. Figure 48 illustrates the output voltage as a function of load cell resistance change, along with the nonlinearity of the system.

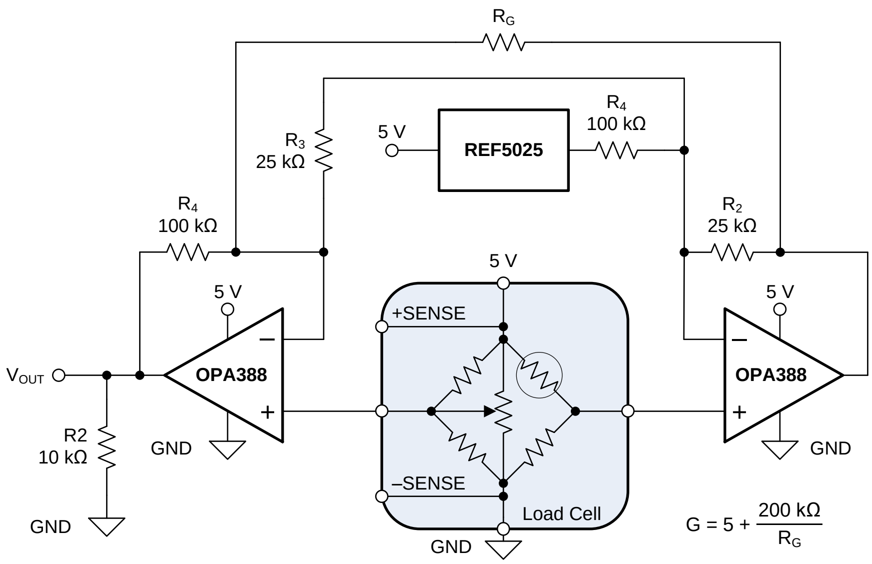


Figure 47. Load Cell Measurement Schematic

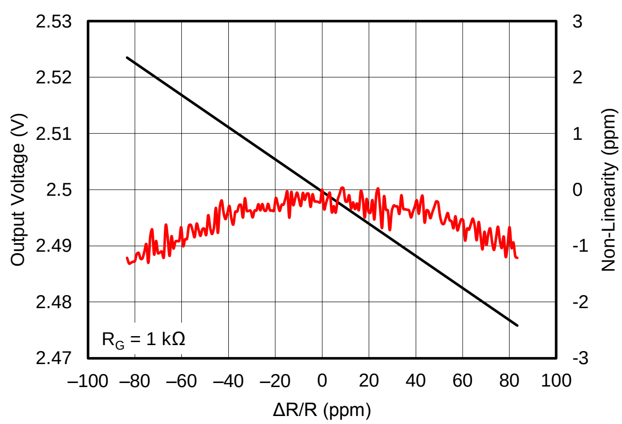


Figure 48. Load Cell Measurement Output

9 Power Supply Recommendations

The OPAx388 family of devices is specified for operation from 2.5 V to 5.5 V (±1.25 V to ±2.75 V). Parameters that can exhibit significant variance with regard to operating voltage are presented in the *Typical Characteristics* section.

10 Layout

10.1 Layout Guidelines

Paying attention to good layout practice is always recommended. Keep traces short and, when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor closely across the supply pins. These guidelines must be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions must be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1 µV/°C or higher, depending on materials used.

10.2 Layout Example

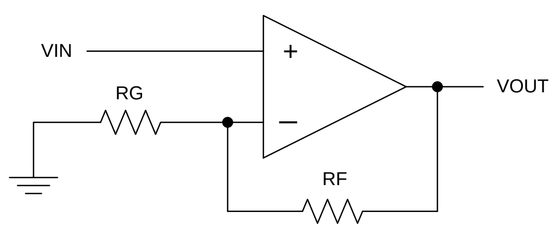


Figure 49. Schematic Representation

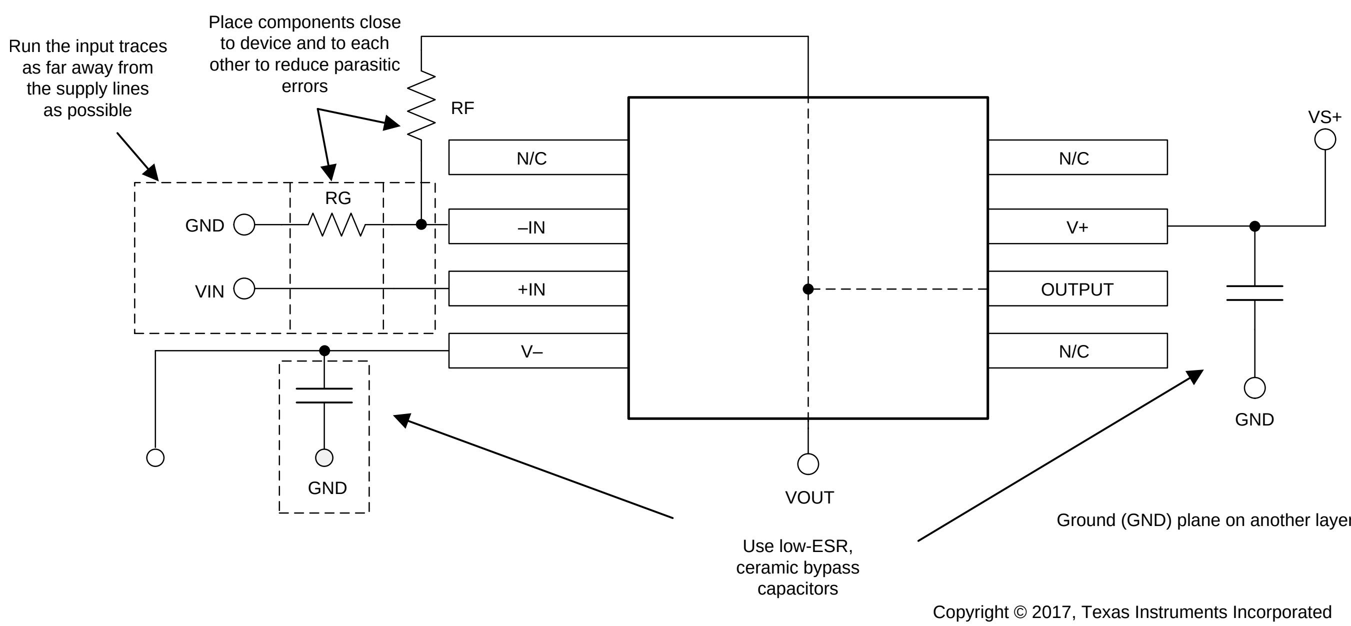


Figure 50. OPA388 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA-TI™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA-TI™ provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI™ offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI™ software be installed. Download the free TINA-TI™ software from the TINA-TI™ folder.

11.1.1.2 TI Precision Designs

The OPAx388 family is featured on TI Precision Designs, available online at www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Circuit board layout techniques*
- Texas Instruments, *DAC883x 16-Bit, Ultra-Low Power, Voltage-Output Digital-to-Analog Converters* data sheet

11.3 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA388	Click here	Click here	Click here	Click here	Click here
OPA2388	Click here	Click here	Click here	Click here	Click here
OPA4388	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2388ID	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2388	
OPA2388IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1D36	Samples
OPA2388IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1D36	Samples
OPA2388IDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	OP2388	
OPA388ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA388	Samples
OPA388IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	14KV	Samples
OPA388IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	14KV	Samples
OPA388IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	14LV	Samples
OPA388IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	14LV	Samples
OPA388IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA388	Samples
OPA4388ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4388	Samples
OPA4388IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4388	Samples
OPA4388IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4388	Samples
OPA4388IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4388	Samples
POPA2388IDR	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

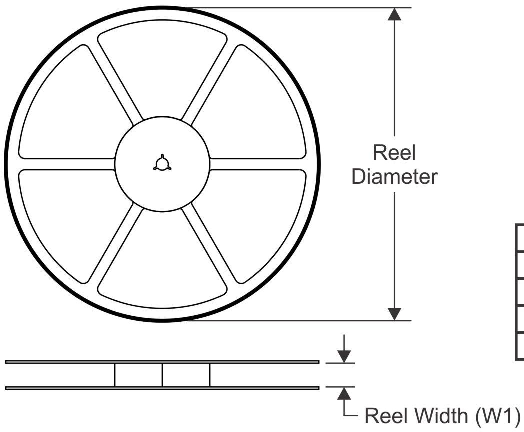
[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

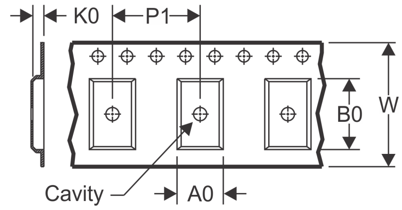
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

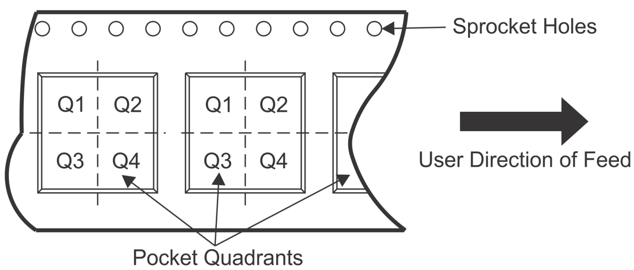


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

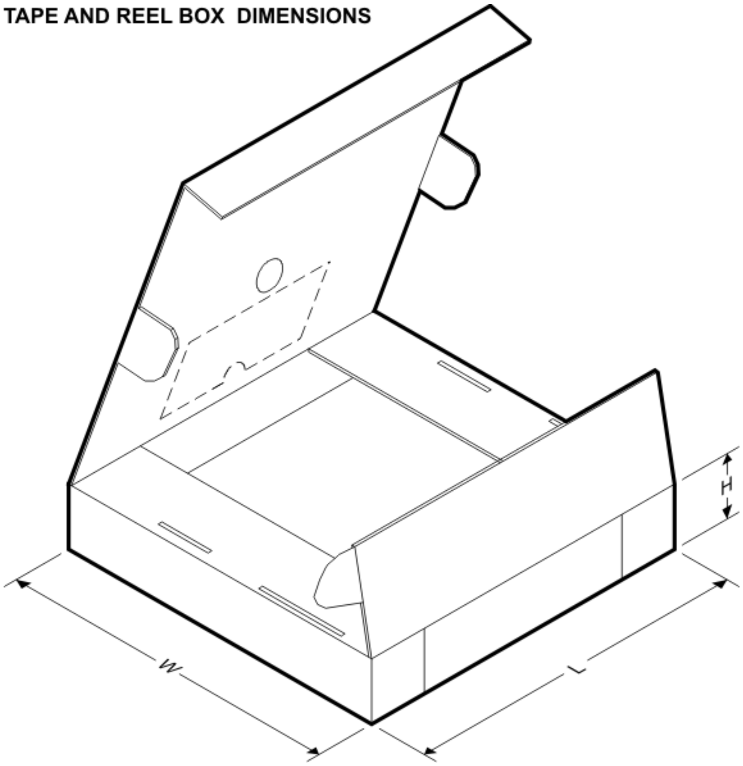
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

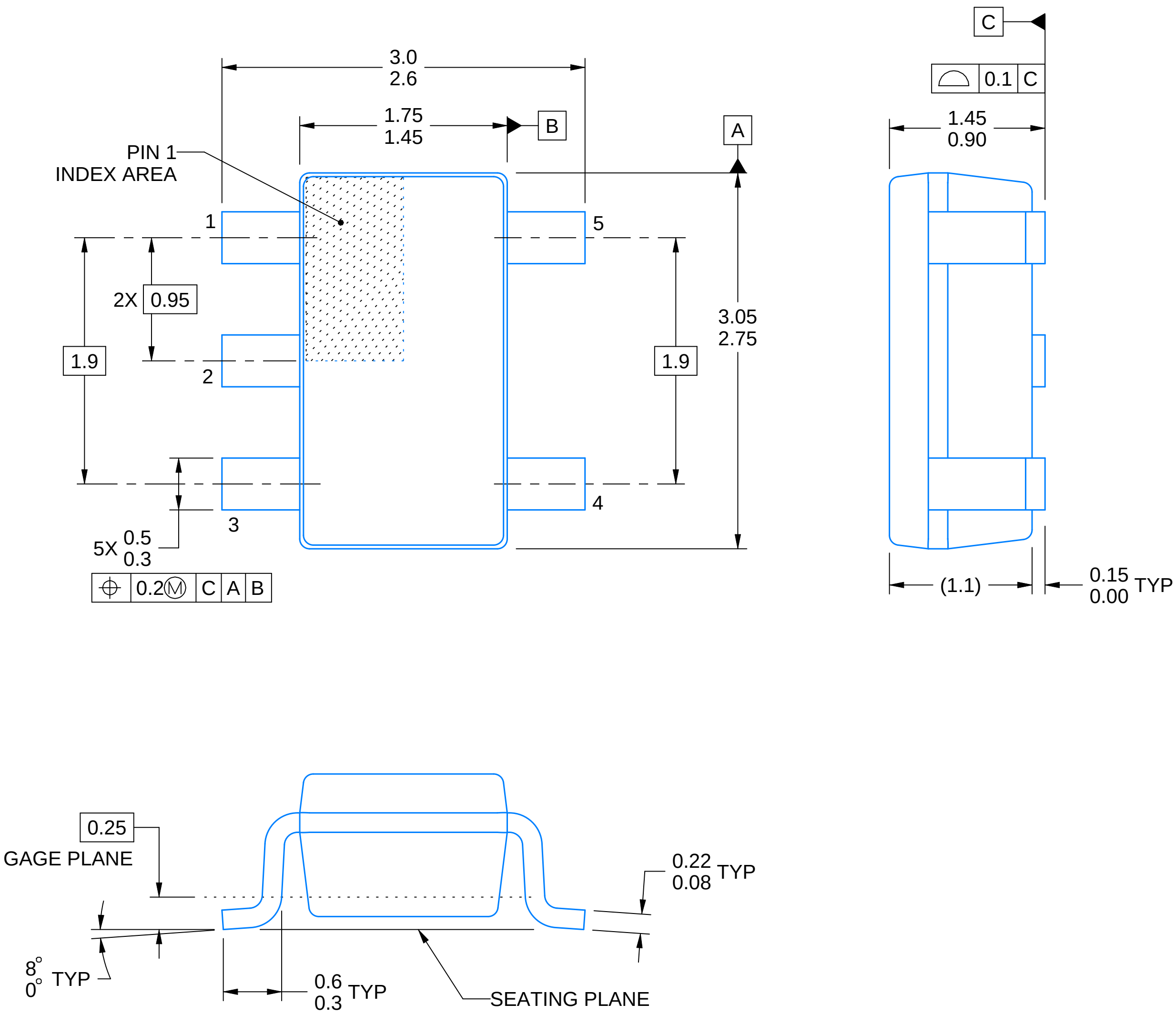
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2388IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2388IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA388IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA388IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA388IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA388IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA388IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4388IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4388IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

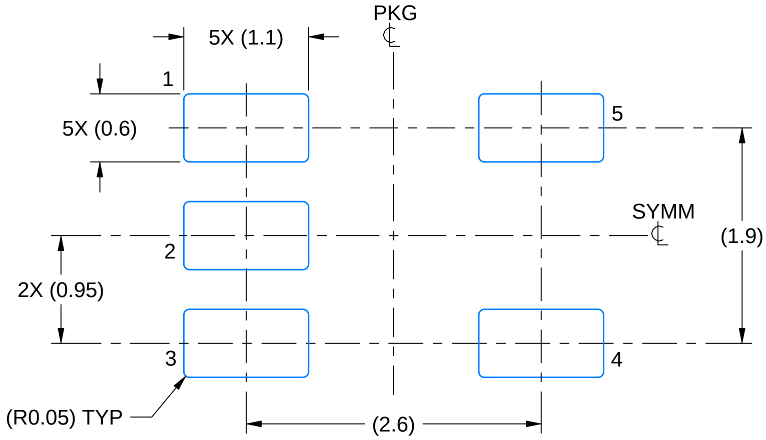
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2388IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2388IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA388IDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA388IDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA388IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA388IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA388IDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA4388IDR	SOIC	D	14	2500	367.0	367.0	38.0
OPA4388IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0



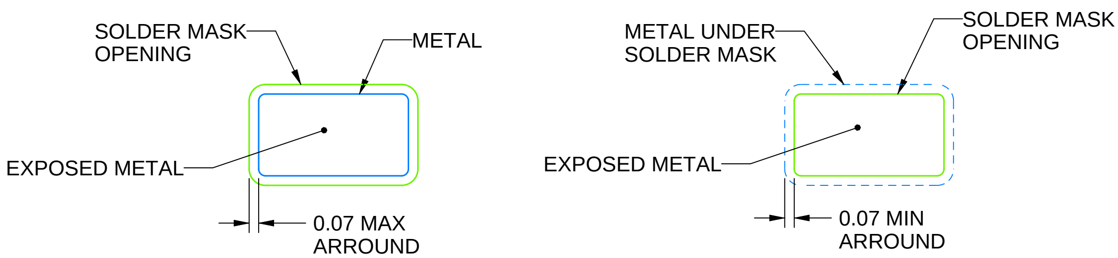
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

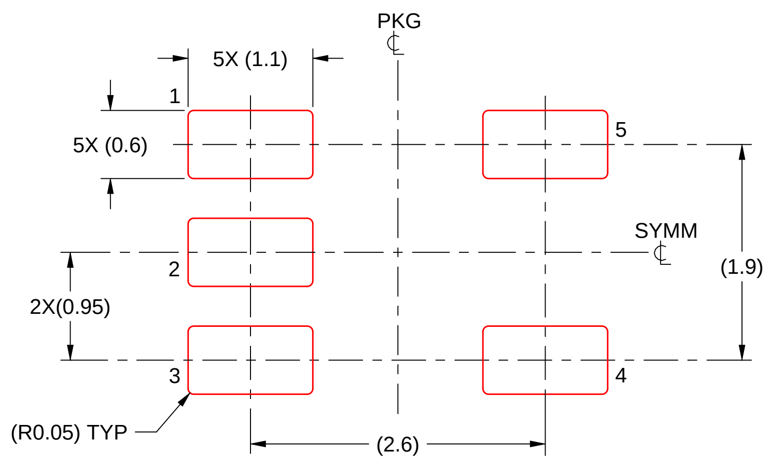
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



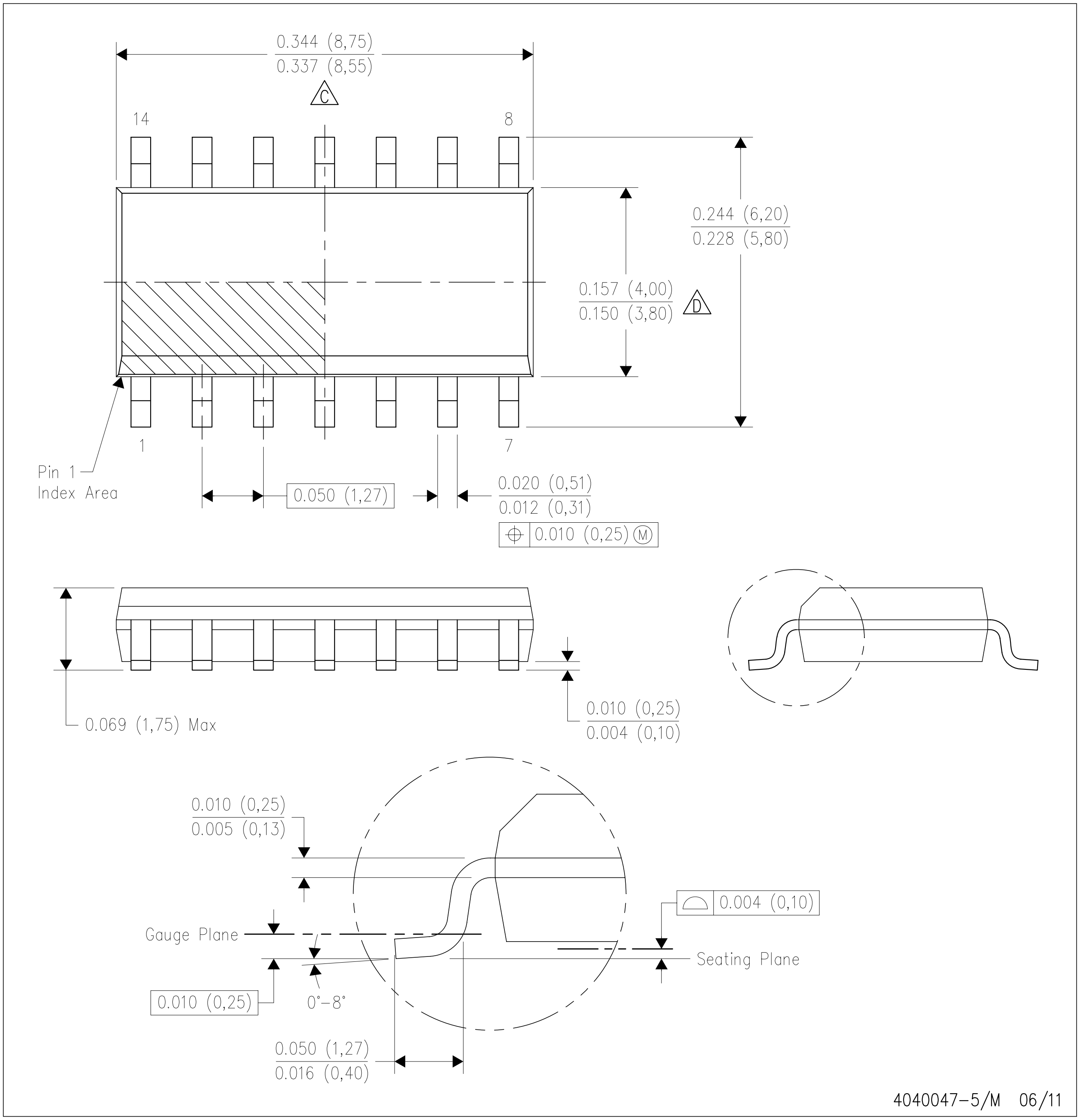
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

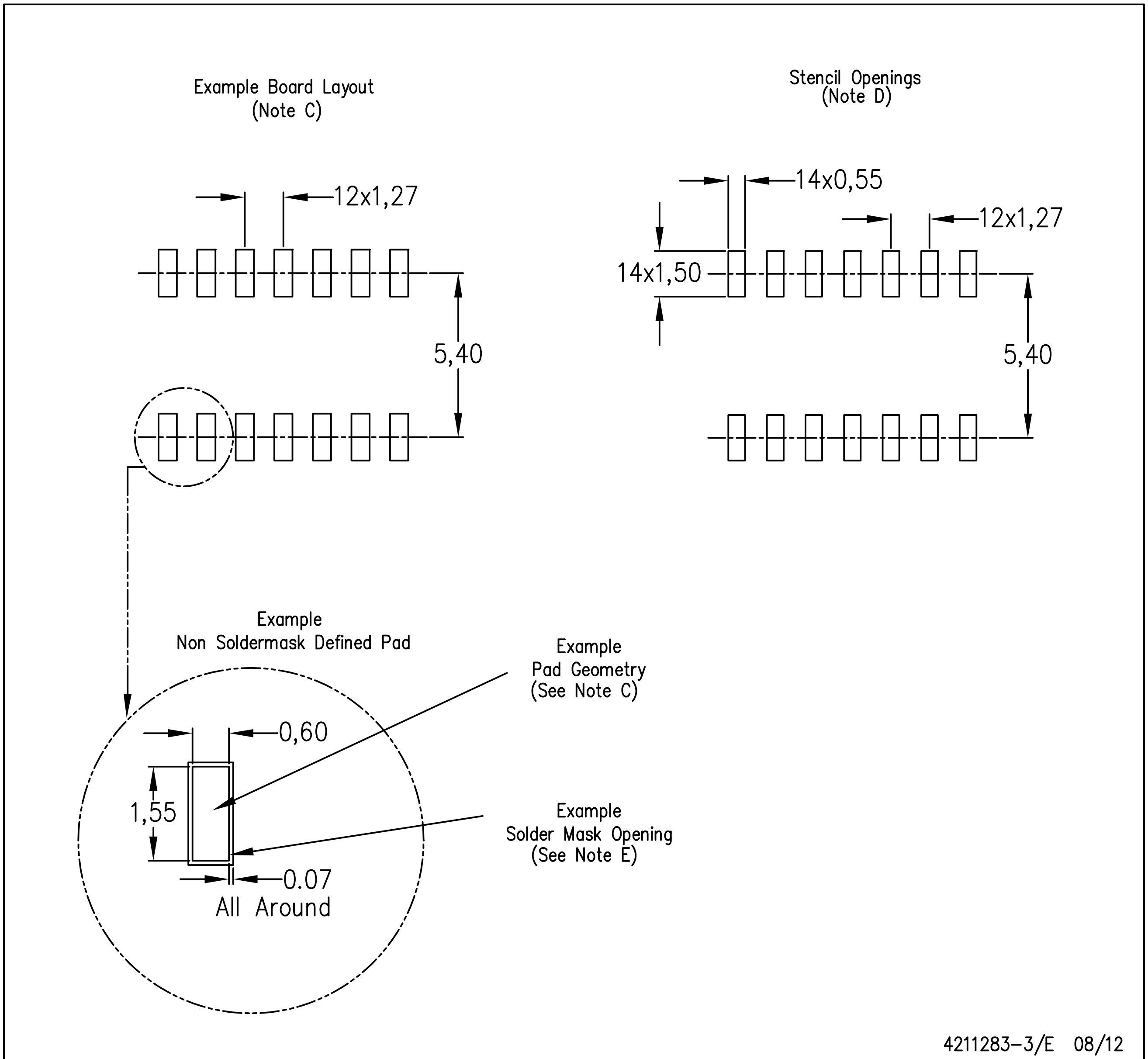
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



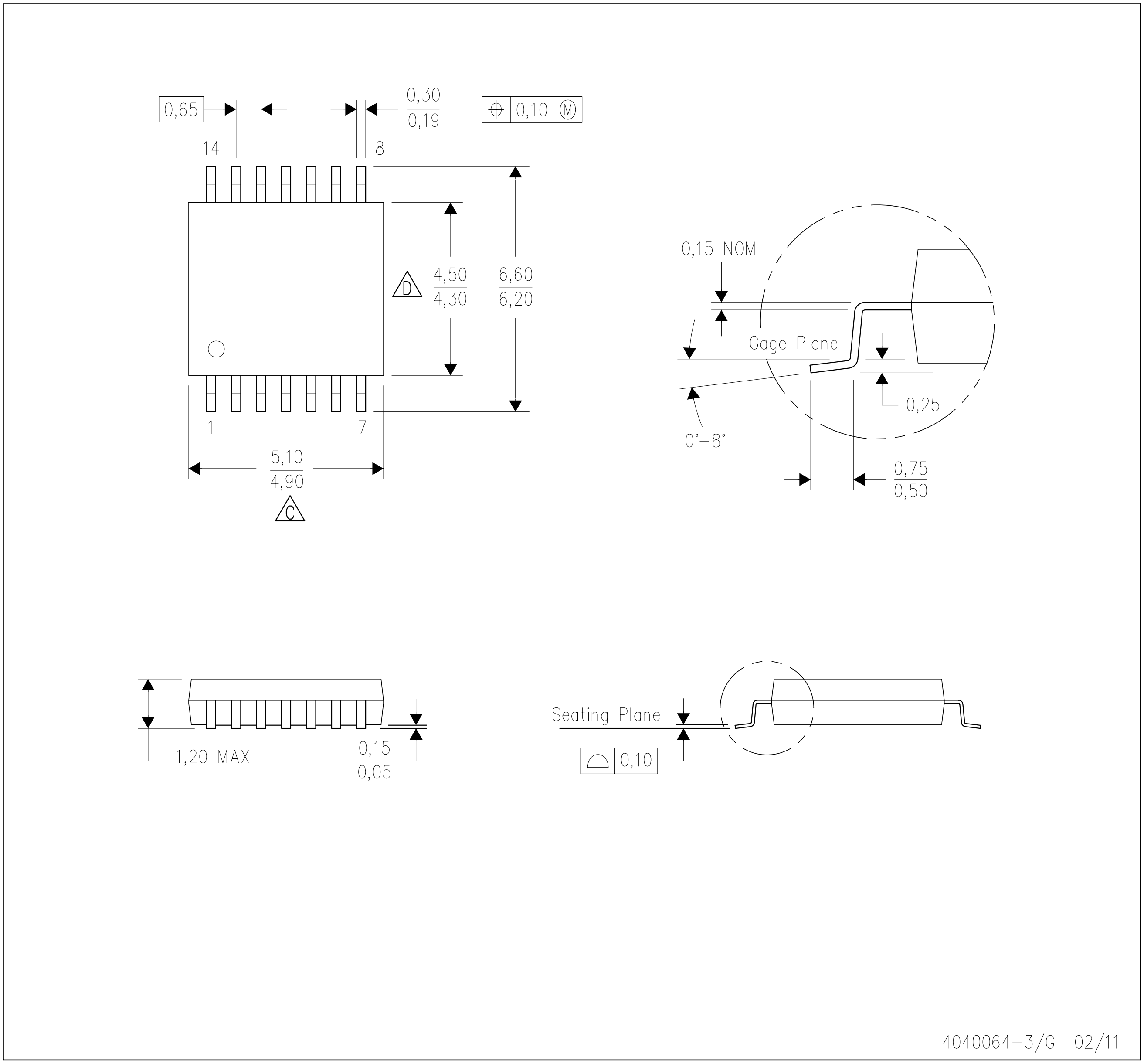
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



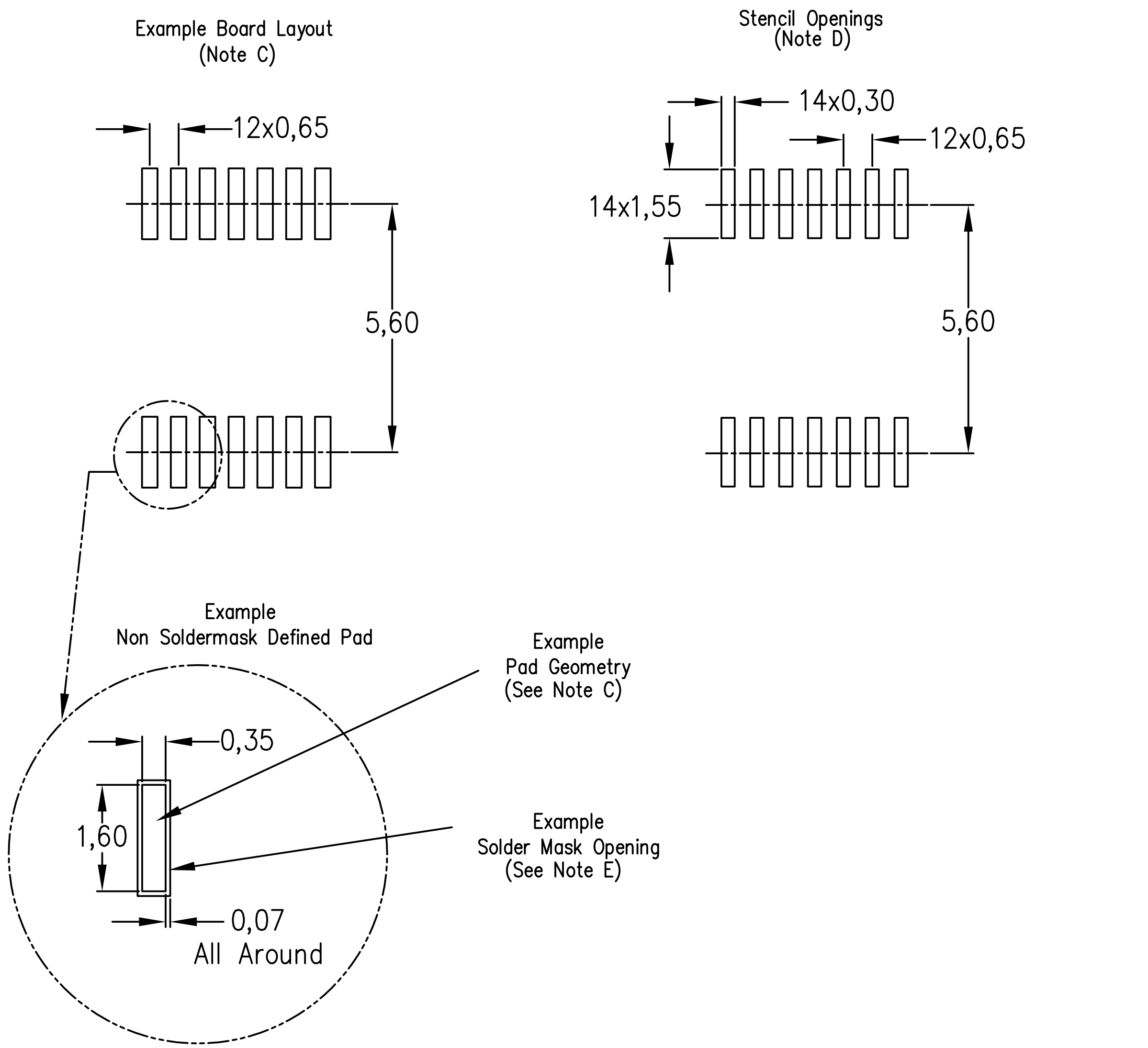
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



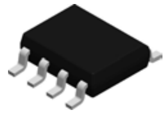
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



4211284-2/G 08/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

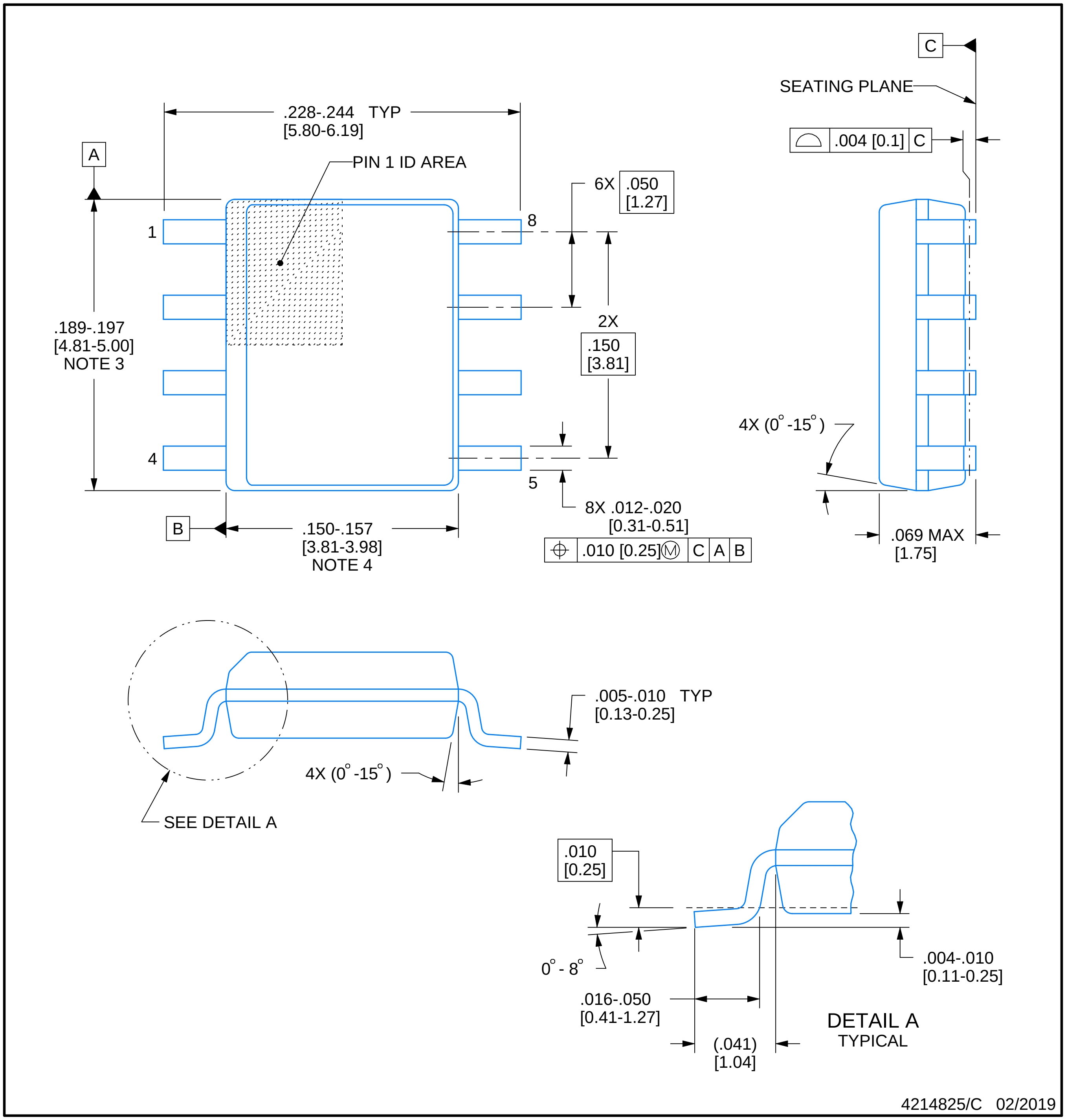


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

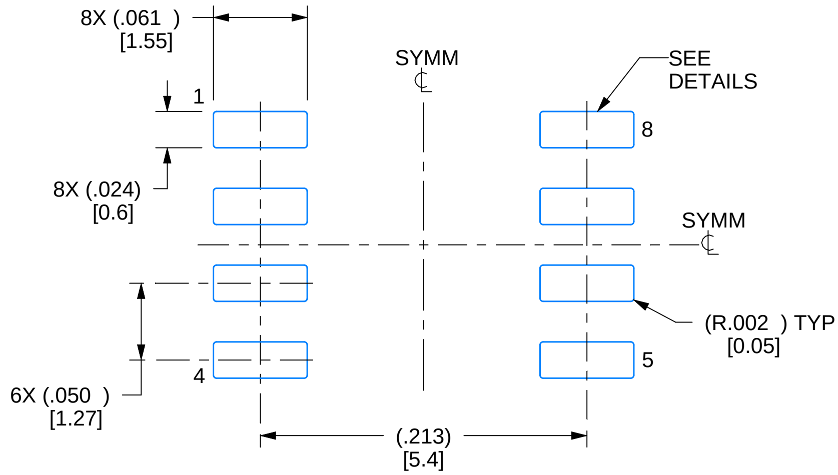
SMALL OUTLINE INTEGRATED CIRCUIT



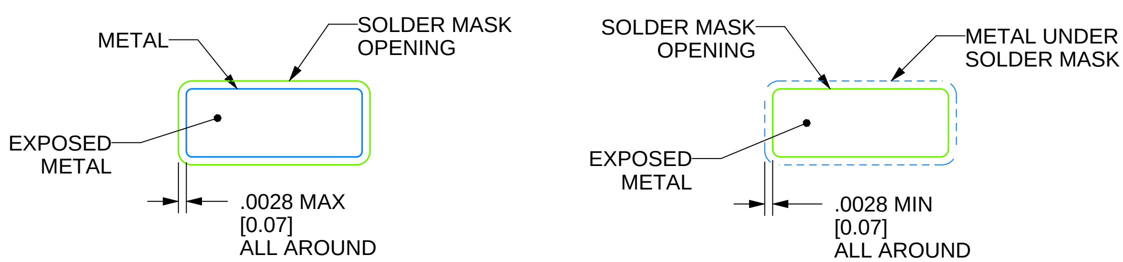
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

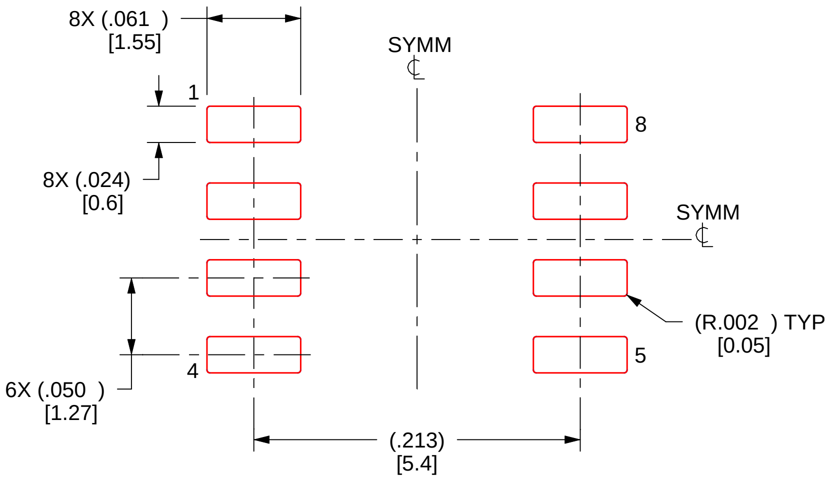
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



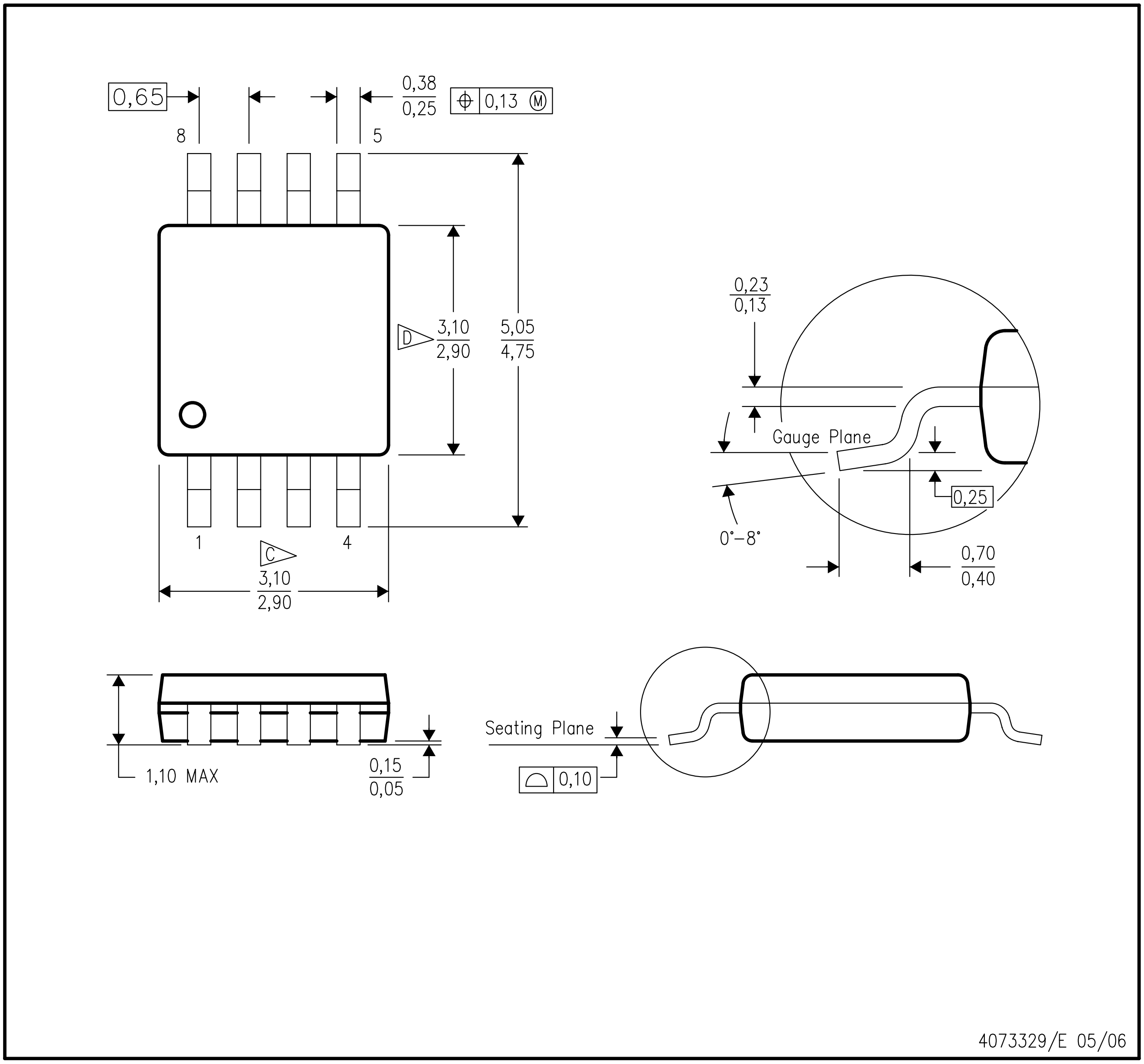
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

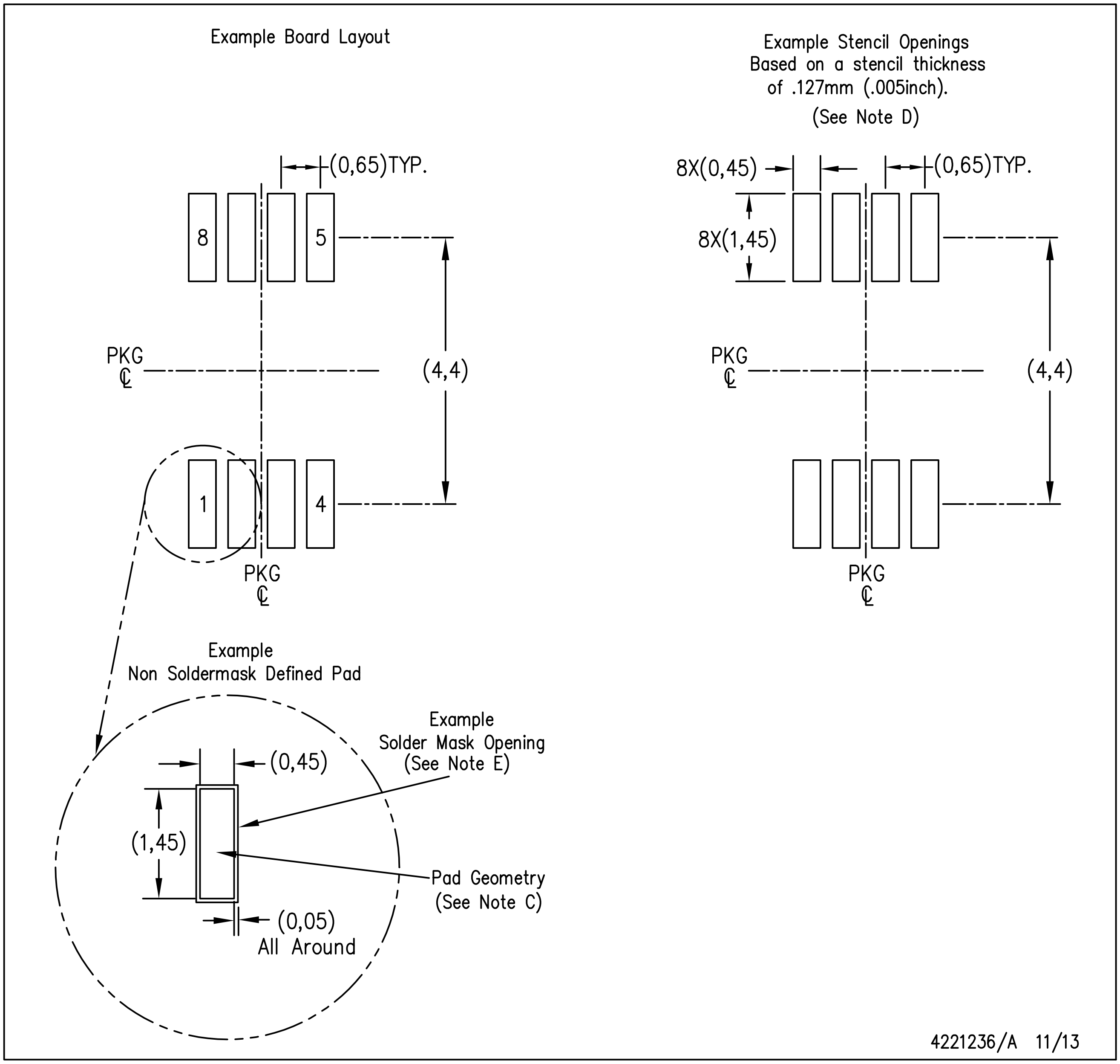
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265