# NUP4301MR6T1

# Low Capacitance Diode Array for ESD Protection in Four Data Lines

NUP4301MR6T1 is a MicroIntegration™ device designed to provide protection for sensitive components from possible harmful electrical transients; for example, ESD (electrostatic discharge).

### Features

- Low Capacitance (1.5 pf Maximum Between I/O Lines)
- Single Package Integration Design
- Provides ESD Protection for JEDEC Standards JESD22
  - Machine Model = Class C
  - Human Body Model = Class 3B
- Protection for IEC61000−4−2 (Level 4)
  - 8.0 kV (Contact)
  - 15 kV (Air)
- Ensures Data Line Speed and Integrity
- Fewer Components and Less Board Space
- Direct the Transient to Either Positive Side or to the Ground
- Pb−Free Package is Available

### Applications

- USB 1.1 and 2.0 Data Line Protection
- T1/E1 Secondary IC Protection
- T3/E3 Secondary IC Protection
- HDSL, IDSL Secondary IC Protection
- Video Line Protection
- Microcontroller Input Protection
- Base Stations
- $I^2C$ Bus Protection

**MAXIMUM RATINGS** (Each Diode) ($T_J$ = 25°C unless otherwise noted)

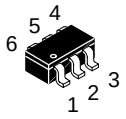
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Reverse Voltage | $V_R$ | 70 | Vdc |
| Forward Current | $I_F$ | 200 | mAdc |
| Peak Forward Surge Current | $I_{FM(surge)}$ | 500 | mAdc |
| Repetitive Peak Reverse Voltage | $V_{RRM}$ | 70 | V |
| Average Rectified Forward Current (Note 1) (averaged over any 20 ms period) | $I_{F(AV)}$ | 715 | mA |
| Repetitive Peak Forward Current | $I_{FRM}$ | 450 | mA |
| Non−Repetitive Peak Forward Current<br>t = 1.0 μs<br>t = 1.0 ms<br>t = 1.0 S | $I_{FSM}$ | <br>2.0<br>1.0<br>0.5 | A |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR−5 = 1.0 × 0.75 × 0.062 in.

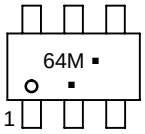
**ON Semiconductor®**

**http://onsemi.com**




**TSOP−6**
**CASE 318F**
**PLASTIC**

### MARKING DIAGRAM

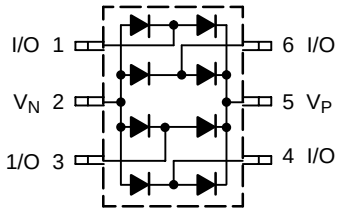



64 = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location.

*Date Code orientation may vary depending upon manufacturing location.

### PIN CONFIGURATION AND SCHEMATIC




### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NUP4301MR6T1 | TSOP−6 | 3000/Tape & Reel |
| NUP4301MR6T1G | TSOP−6 (Pb−Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction−to−Ambient | $R_{\theta JA}$ | 556 | °C/W |
| Lead Solder Temperature, Maximum 10 Seconds Duration | $T_L$ | 260 | °C |
| Junction Temperature | $T_J$ | −40 to +85 | °C |
| Storage Temperature | $T_{stg}$ | −55 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Each Diode)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Reverse Breakdown Voltage ($I_{(BR)}$ = 100 μA) | $V_{(BR)}$ | 70 | − | − | Vdc |
| Reverse Voltage Leakage Current ($V_R$ = 70 Vdc)<br>($V_R$ = 25 Vdc, $T_J$ = 150°C)<br>($V_R$ = 70 Vdc, $T_J$ = 150°C) | $I_R$ | −<br>−<br>− | −<br>−<br>− | 2.5<br>30<br>50 | μAdc |
| Capacitance (between I/O pins)<br>($V_R$ = 0 V, f = 1.0 MHz) | $C_D$ | − | 0.8 | 1.5 | pF |
| Capacitance (between I/O pin and ground)<br>($V_R$ = 0 V, f = 1.0 MHz) | $C_D$ | − | 1.6 | 3 | pF |
| Forward Voltage ($I_F$ = 1.0 mAdc)<br>($I_F$ = 10 mAdc)<br>($I_F$ = 50 mAdc)<br>($I_F$ = 150 mAdc) | $V_F$ | −<br>−<br>−<br>− | −<br>−<br>−<br>− | 715<br>855<br>1000<br>1250 | $mV_{dc}$ |

2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.

**Curves Applicable to Each Cathode**

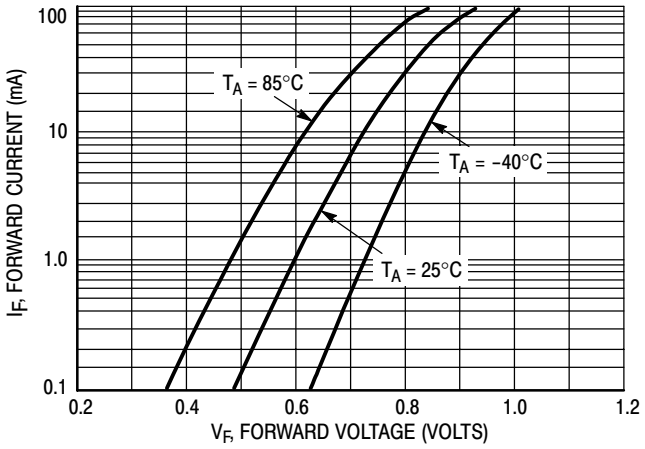



**Figure 1. Forward Voltage**

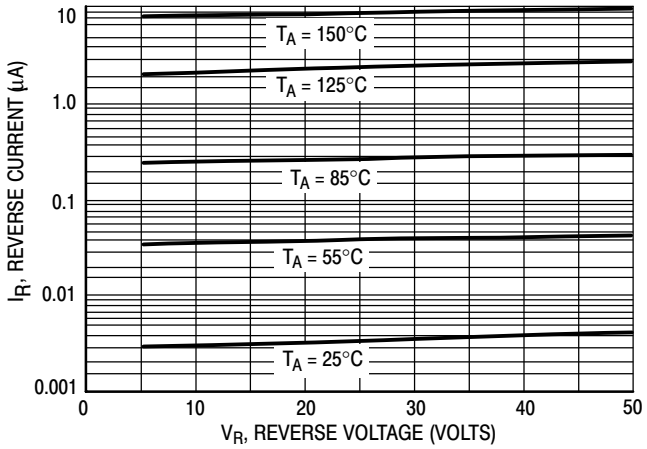



**Figure 2. Leakage Current**

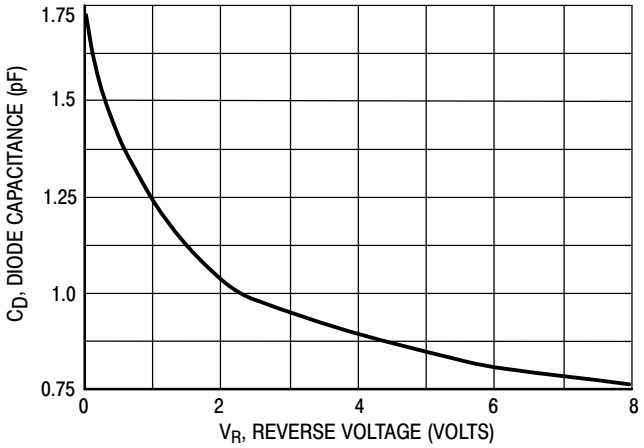
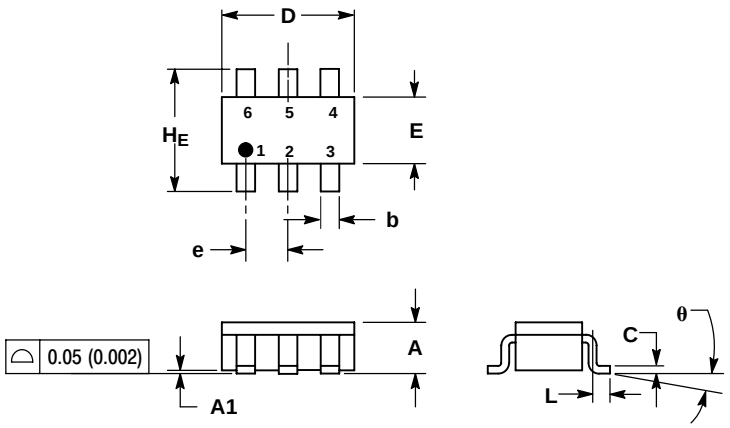



**Figure 3. Capacitance**

## PACKAGE DIMENSIONS

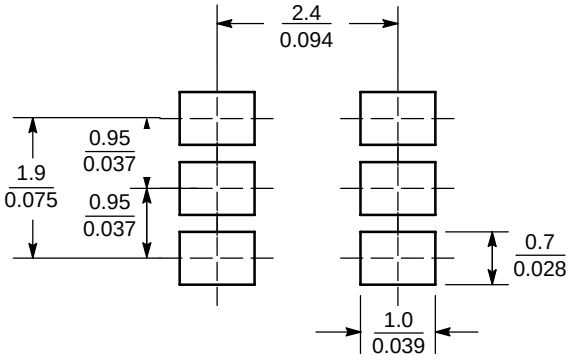
**TSOP−6**
CASE 318F−05
ISSUE L




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03 OBSOLETE. NEW STANDARD 318F−04.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 | 0.035 | 0.039 | 0.043 |
| A1 | 0.01 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.25 | 0.37 | 0.50 | 0.010 | 0.015 | 0.020 |
| c | 0.10 | 0.18 | 0.26 | 0.004 | 0.007 | 0.010 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 1.30 | 1.50 | 1.70 | 0.051 | 0.059 | 0.067 |
| e | 0.85 | 0.95 | 1.05 | 0.034 | 0.037 | 0.041 |
| L | 0.20 | 0.40 | 0.60 | 0.008 | 0.016 | 0.024 |
| $H_E$ | 2.50 | 2.75 | 3.00 | 0.099 | 0.108 | 0.118 |
| θ | 0° | – | 10° | 0° | – | 10° |

## SOLDERING FOOTPRINT*




SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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