

NTZD5110N

Small Signal MOSFET

60 V, 310 mA, Dual N-Channel
with ESD Protection, SOT-563

Features

- Low $R_{DS(on)}$ Improving System Efficiency
- Low Threshold Voltage
- ESD Protected Gate
- Small Footprint 1.6 x 1.6 mm
- These are Pb-Free Devices

Applications

- Load/Power Switches
- Driver Circuits: Relays, Lamps, Displays, Memories, etc.
- Battery Management/Battery Operated Systems
- Cell Phones, Digital Cameras, PDAs, Pagers, etc.

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	60	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	294	mA
		$T_A = 85^{\circ}\text{C}$		212	
Power Dissipation (Note 1)	Steady State		P_D	250	mW
Continuous Drain Current (Note 1)	$t \leq 5 \text{ s}$	$T_A = 25^{\circ}\text{C}$	I_D	310	mA
		$T_A = 85^{\circ}\text{C}$		225	
Power Dissipation (Note 1)	$t \leq 5 \text{ s}$		P_D	280	mW
Pulsed Drain Current	$t_p = 10 \mu\text{s}$		I_{DM}	590	mA
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	350	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$
Gate-Source ESD Rating (HBM, Method 3015)			ESD	1800	V

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	500	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 5 \text{ s}$ (Note 1)		447	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

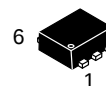
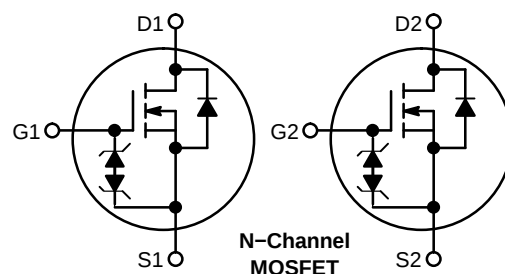
1. Surface mounted on FR4 board using 1 in sq pad size (Cu. area = 1.127 in sq [1 oz] including traces).



ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ Max}$
60	1.6 Ω @ 10 V	310 mA
	2.5 Ω @ 4.5 V	



**SOT-563
CASE 463A**

MARKING DIAGRAM

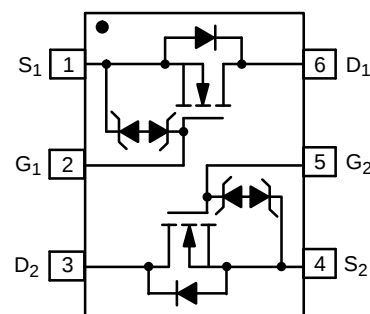


S7 = Specific Device Code

M = Date Code

(Note: Microdot may be in either location)

PINOUT: SOT-563



Top View

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		60	–	–	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	–		–	71	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$	–	–	1.0	μA
			$T_J = 125^\circ\text{C}$	–	–	500	
		$V_{GS} = 0\text{ V}$ $V_{DS} = 50\text{ V}$	$T_J = 25^\circ\text{C}$	–	–	100	nA
			$T_J = 85^\circ\text{C}$	–	–	100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		–	–	± 10	μA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 10\text{ V}$		–	–	450	nA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 5.0\text{ V}$		–	–	150	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.0	–	2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	–	–	4.0	–	mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$	–	1.19	1.6	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 200\text{ mA}$	–	1.33	2.5	
Forward Transconductance	g_{FS}	$V_{DS} = 5.0\text{ V}, I_D = 200\text{ mA}$	–	80	–	S

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz},$ $V_{DS} = 20\text{ V}$	–	24.5	–	pF
Output Capacitance	C_{OSS}		–	4.2	–	
Reverse Transfer Capacitance	C_{RSS}		–	2.2	–	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V};$ $I_D = 200\text{ mA}$	–	0.7	–	nC
Threshold Gate Charge	$Q_{G(TH)}$		–	0.1	–	
Gate-to-Source Charge	Q_{GS}		–	0.3	–	
Gate-to-Drain Charge	Q_{GD}		–	0.1	–	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 30\text{ V},$ $I_D = 200\text{ mA}, R_G = 10\text{ }\Omega$	–	12	–	ns
Rise Time	t_r		–	7.3	–	
Turn-Off Delay Time	$t_{d(OFF)}$		–	63.7	–	
Fall Time	t_f		–	30.6	–	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 200\text{ mA}$	$T_J = 25^\circ\text{C}$	–	0.8	1.2	V
			$T_J = 85^\circ\text{C}$	–	0.7	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Surface-mounted on FR4 board using 1 in. sq. pad size (Cu. area = 1.127 in sq [1 oz] including traces).

3. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

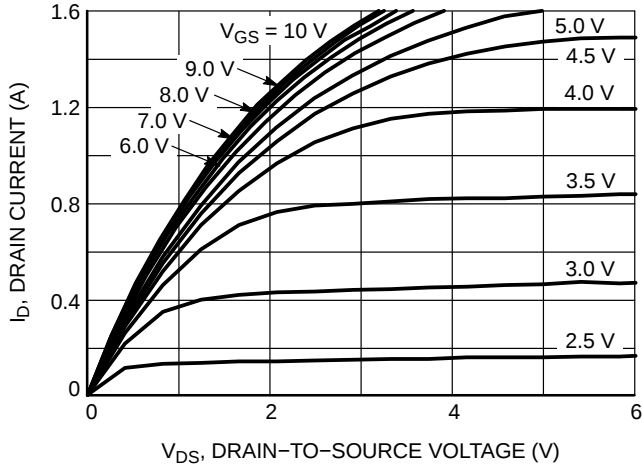


Figure 1. On-Region Characteristics

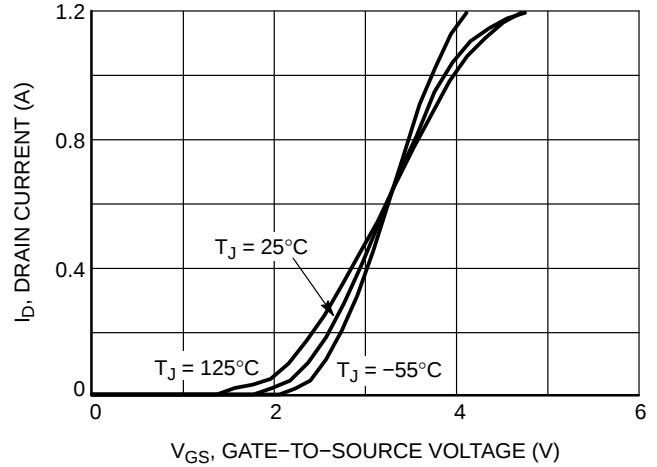


Figure 2. Transfer Characteristics

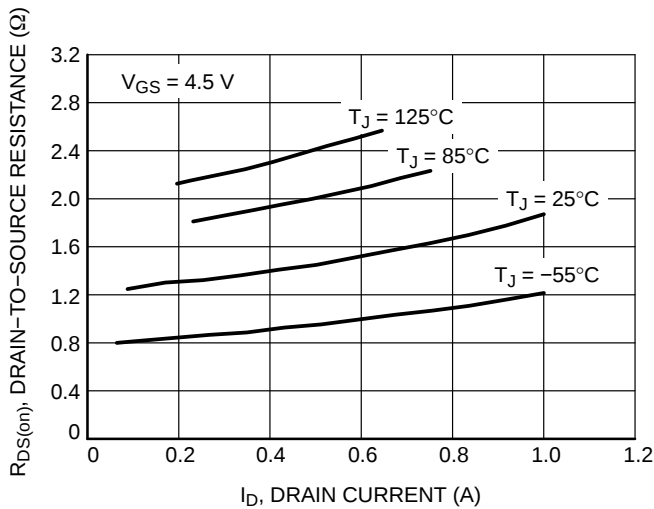


Figure 3. On-Resistance vs. Drain Current and Temperature

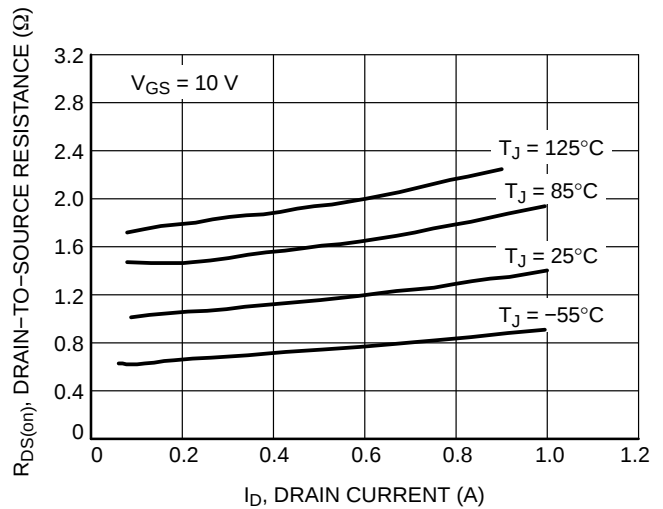


Figure 4. On-Resistance vs. Drain Current and Temperature

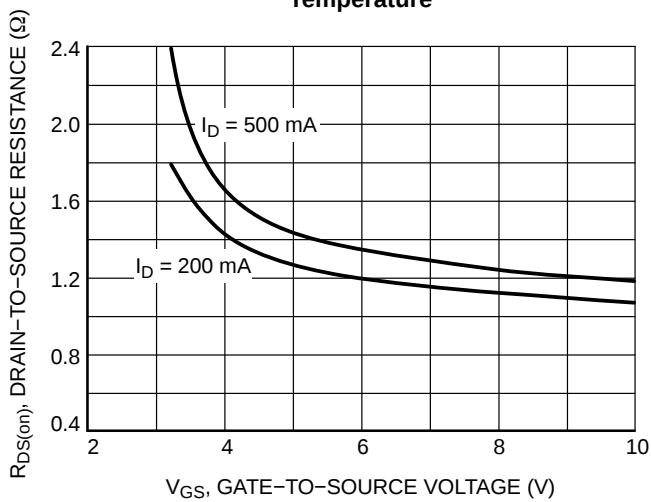


Figure 5. On-Resistance vs. Gate-to-Source Voltage

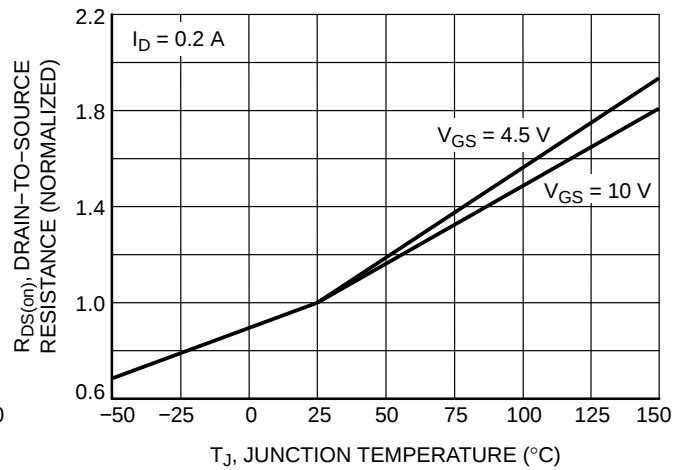


Figure 6. On-Resistance Variation with Temperature

NTZD5110N

TYPICAL CHARACTERISTICS

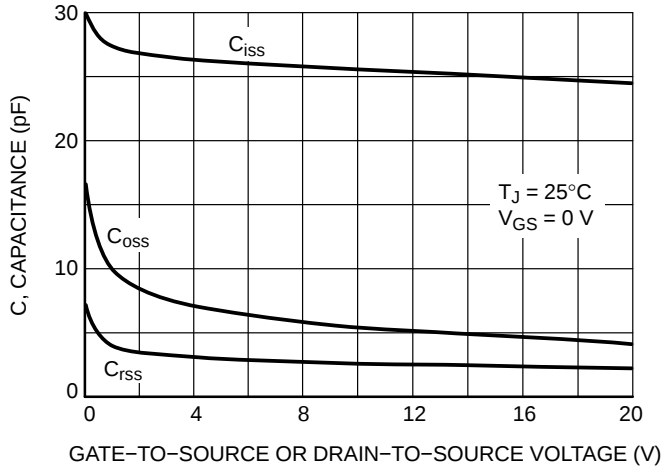


Figure 7. Capacitance Variation

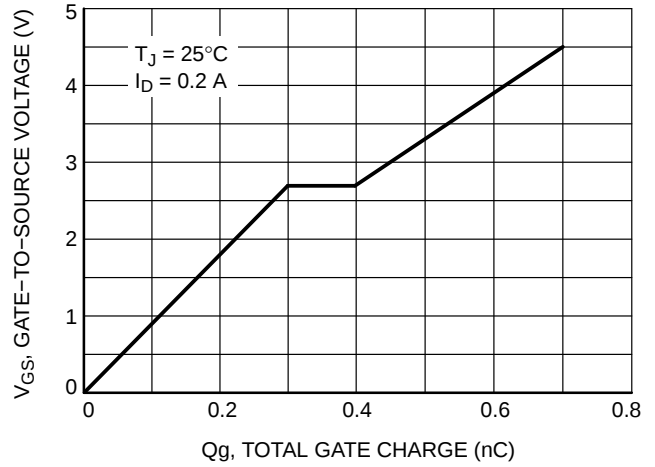


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

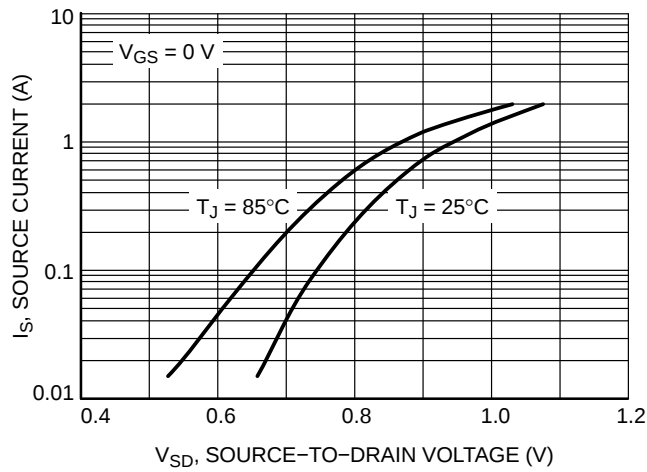


Figure 9. Diode Forward Voltage vs. Current

ORDERING INFORMATION

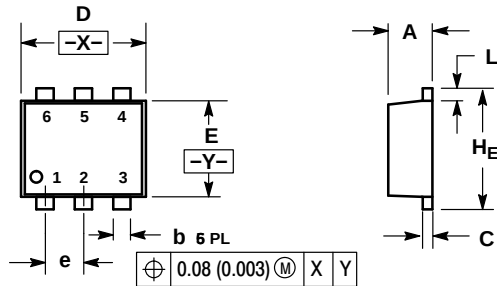
Device	Package	Shipping
NTZD5110NT1G	SOT-563 (Pb-Free)	4000 / Tape & Reel
NTZD5110NT5G	SOT-563 (Pb-Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTZD5110N

PACKAGE DIMENSIONS

SOT-563, 6 LEAD CASE 463A ISSUE F

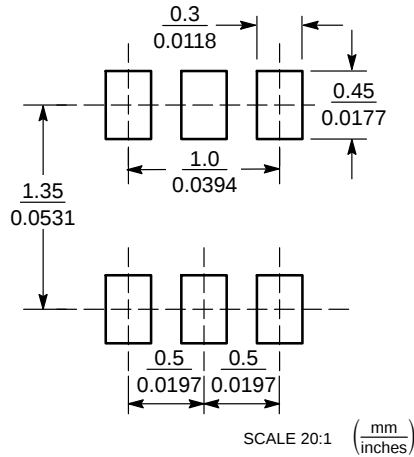


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H _E	1.50	1.60	1.70	0.059	0.062	0.066

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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