NTMFS4H01N

Power MOSFET

25 V, 334 A, Single N−Channel, SO−8FL

Features

- Optimized Design to Minimize Conduction and Switching Losses
- Optimized Package to Minimize Parasitic Inductances
- Optimized material for improved thermal performance
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Performance DC-DC Converters
- System Voltage Rails
- Netcom, Telecom
- Servers & Point of Load

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Value	Units
Drain-to-Source Voltage	V_{DSS}	25	V
Gate-to-Source Voltage	V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (T_A = 25°C, Note 1)	I_D	54	A
Power Dissipation $R_{\theta JA}$ (T_A = 25°C, Note 1)	P_D	3.2	W
Continuous Drain Current $R_{\theta JC}$ (T_C = 25°C, Note 1)	I_D	334	A
Power Dissipation $R_{\theta JC}$ (T_C = 25°C, Note 1)	P_D	125	W
Pulsed Drain Current (t_p = 10 μs)	I_{DM}	568	A
Single Pulse Drain-to-Source Avalanche Energy (Note 1) (I_L = 58 A_{pk}, L = 0.3 mH)	E_{AS}	505	mJ
Drain to Source dV/dt	dV/dt	7	V/ns
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 2)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Values based on copper area of 645 mm^2 (or 1 in^2) of 2 oz copper thickness and FR4 PCB substrate.
2. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
3. This is the absolute maximum rating. Parts are 100% UIS tested at T_J = 25°C, V_{GS} = 10 V, I_L = 38 A, E_{AS} = 217 mJ.

THERMALCHARACTERISTICS

Parameter	Symbol	Max	Units
Thermal Resistance, Junction-to-Ambient (Note 1 and 4)	$R_{\theta JA}$	38.9	°C/W
Junction-to-Case (Note 1 and 4)	$R_{\theta JC}$	1.0	

4. Thermal Resistance $R_{\theta JA}$ and $R_{\theta JC}$ as defined in JESD51−3.

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http://onsemi.com

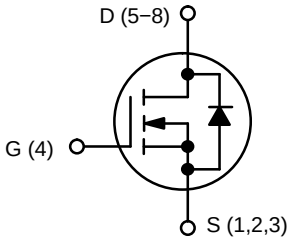
V_{GS}	MAX $R_{DS(on)}$	TYP Q_{GTOT}
4.5 V	0.97 mΩ	39 nC
10 V	0.7 mΩ	85 nC

PIN CONNECTIONS

SO8−FL (5 x 6 mm)

(Top View) (Bottom View)

N−CHANNEL MOSFET



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		25			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$/T_J				13		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 20 V	T_J = 25°C			1	μA
			T_J = 125°C			30	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = +20 V				+100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.2		2.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}$/T_J				4		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 30 A		0.55	0.7	mΩ
		V_{GS} = 4.5 V	I_D = 30 A		0.76	0.97	
Forward Transconductance	g_{FS}	V_{DS} = 12 V, I_D = 15 A			101		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 12 V			5693		pF
Output Capacitance	C_{OSS}				3718		
Reverse Transfer Capacitance	C_{RSS}				212		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 12 V; I_D = 30 A			39		nC
Threshold Gate Charge	$Q_{G(TH)}$				2.4		
Gate−to−Source Charge	Q_{GS}				14		
Gate−to−Drain Charge	Q_{GD}				8.5		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 12 V; I_D = 30 A			85		nC
Gate Resistance	R_G	T_A = 25°C			1.2	2	Ω
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 12 V, I_D = 15 A, R_G = 3.0 Ω			18		ns
Rise Time	t_r				49		
Turn−Off Delay Time	$t_{d(OFF)}$				46		
Fall Time	t_f				35		
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 11.5 V, V_{DS} = 12 V, I_D = 15 A, R_G = 3.0 Ω			11		ns
Rise Time	t_r				33.6		
Turn−Off Delay Time	$t_{d(OFF)}$				46		
Fall Time	t_f				34		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.75	1.1	V
			T_J = 125°C		0.55		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 30 A			68.7		ns
Charge Time	t_a				34.1		
Discharge Time	t_b				34.6		
Reverse Recovery Charge	Q_{RR}				90		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

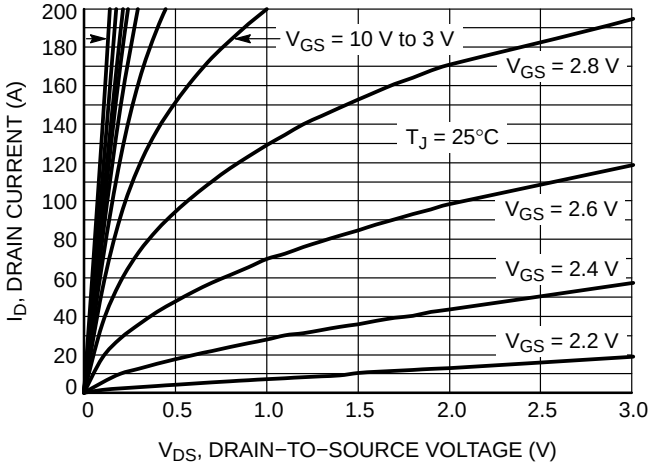


Figure 1. On−Region Characteristics

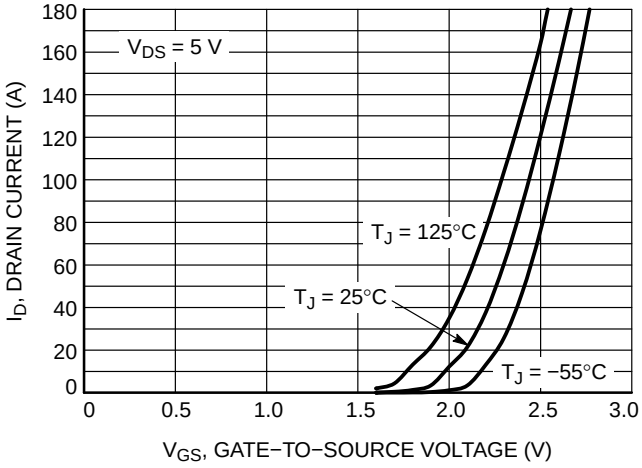


Figure 2. Transfer Characteristics

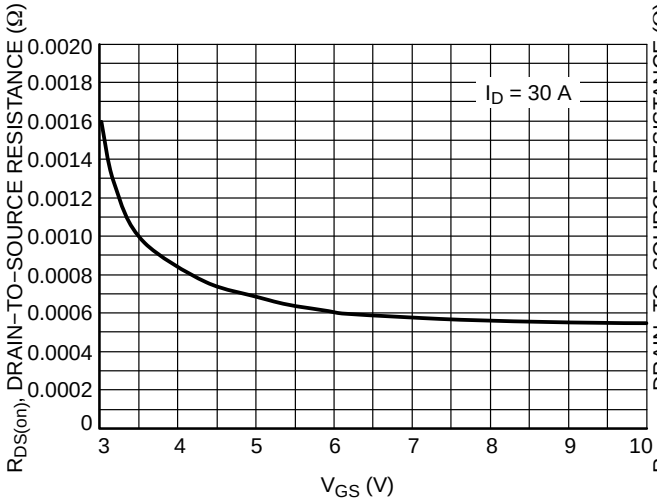


Figure 3. On−Resistance vs. V_{GS}

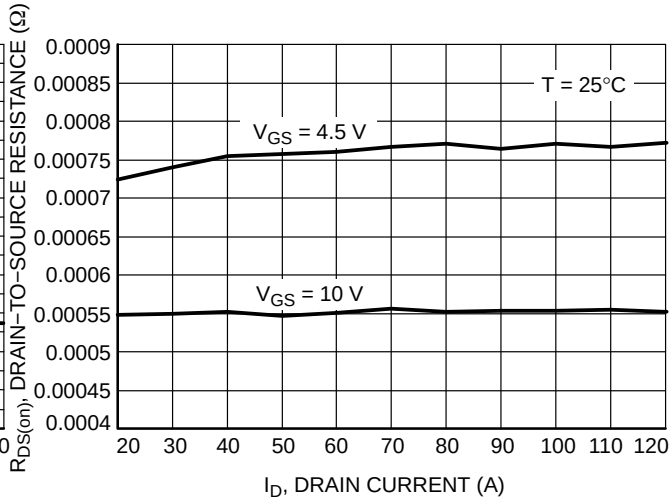


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

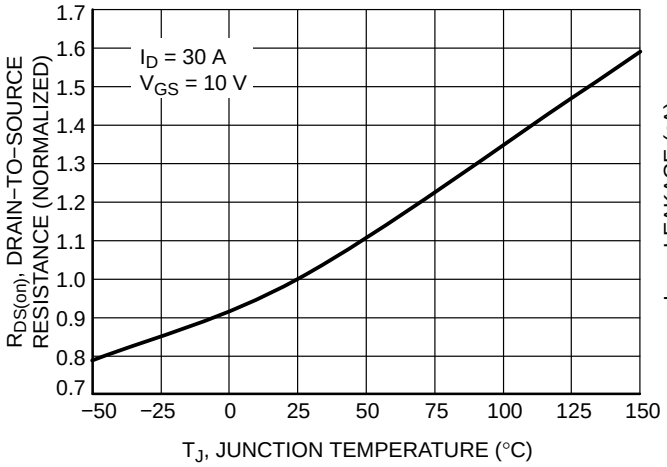


Figure 5. On−Resistance Variation with Temperature

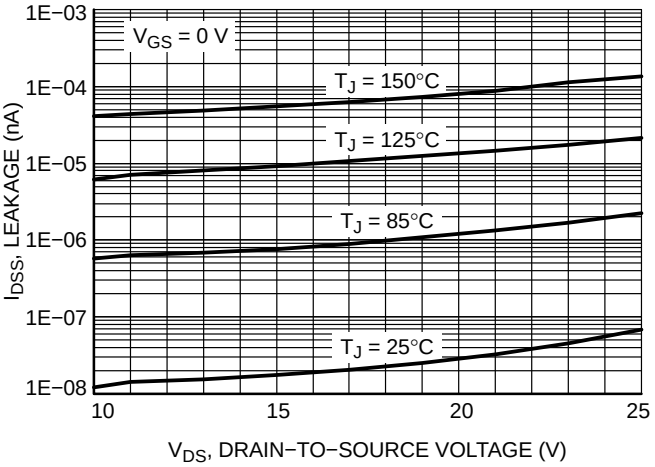


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

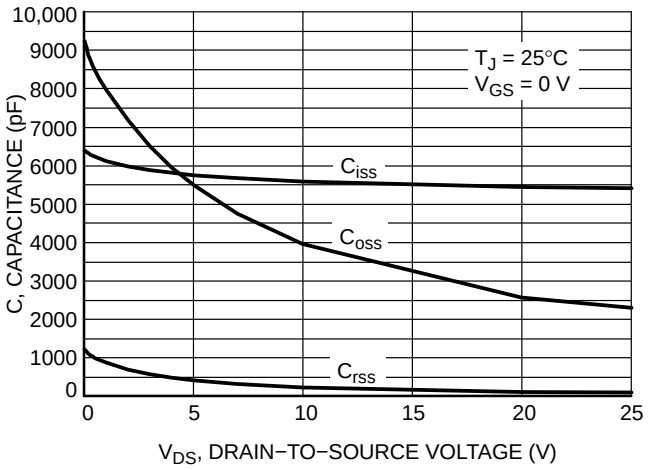


Figure 7. Capacitance Variation

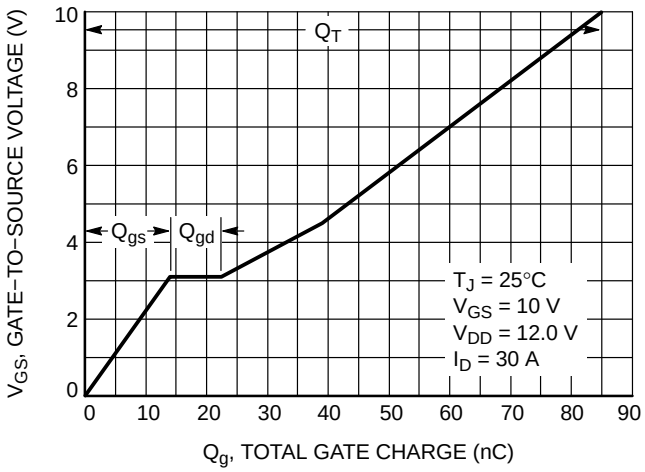


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

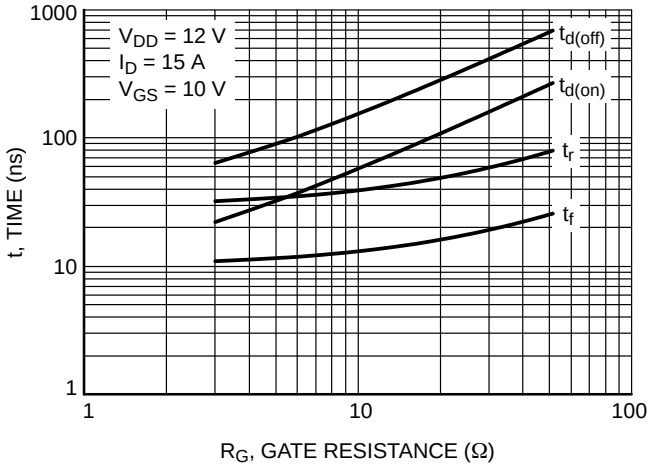


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

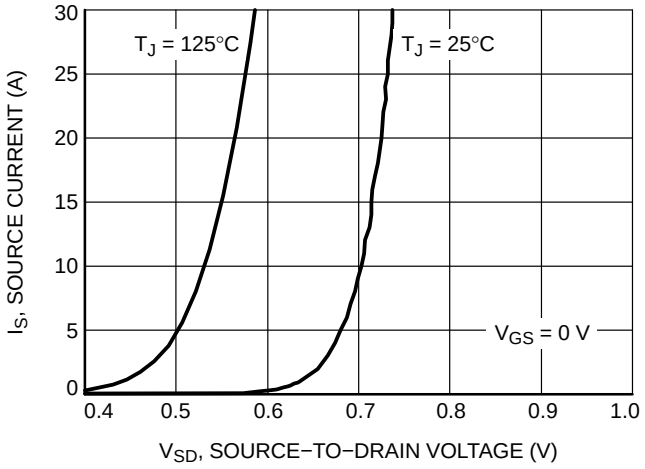


Figure 10. Diode Forward Voltage vs. Current

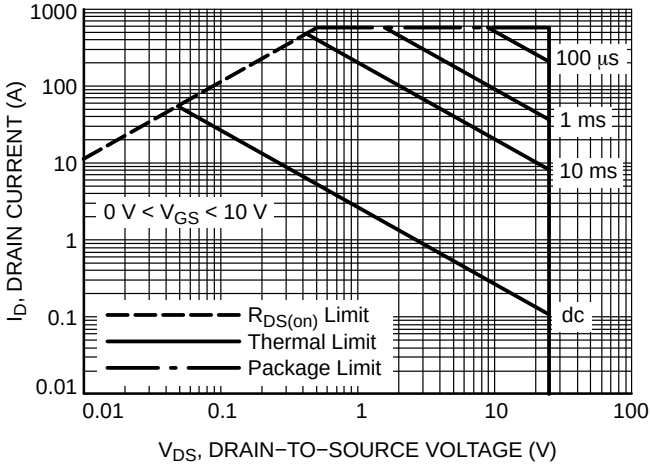


Figure 11. Maximum Rated Forward Biased Safe Operating Area

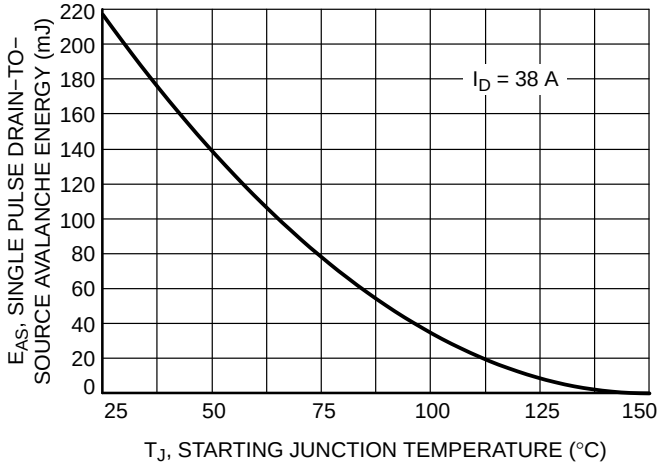


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS

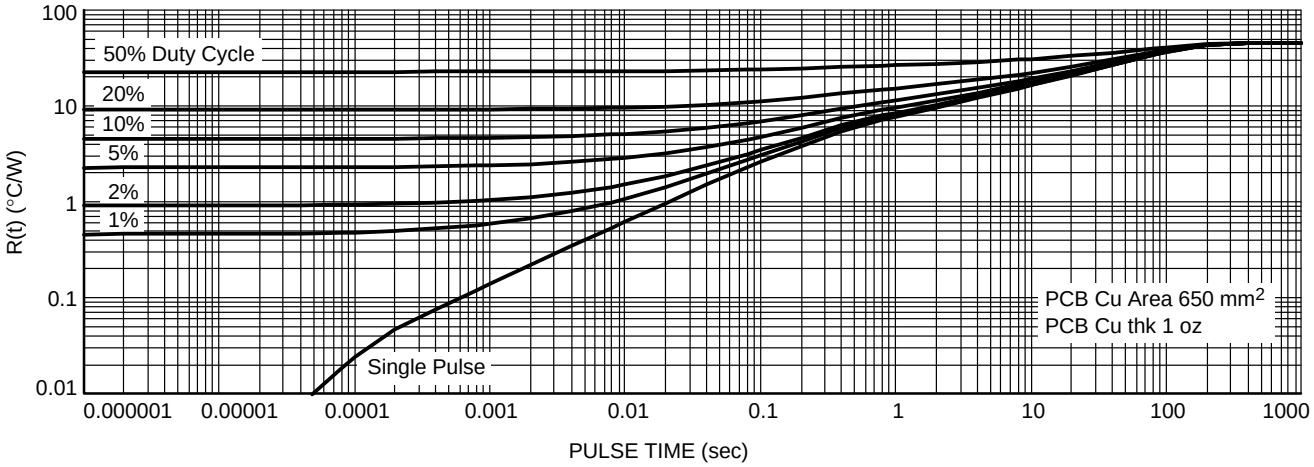


Figure 13. Thermal Characteristics

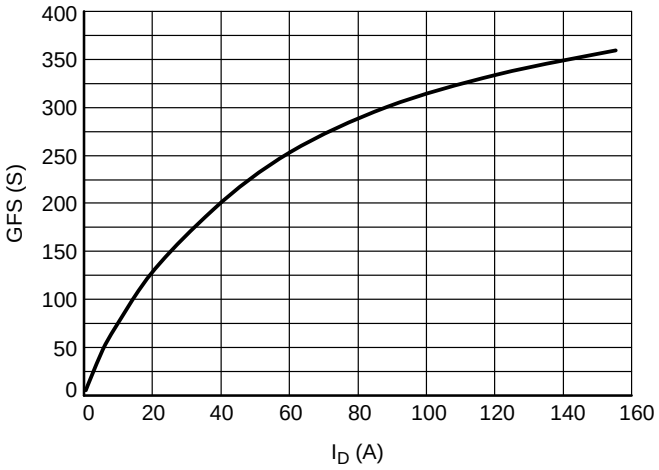


Figure 14. GFS vs. I_D

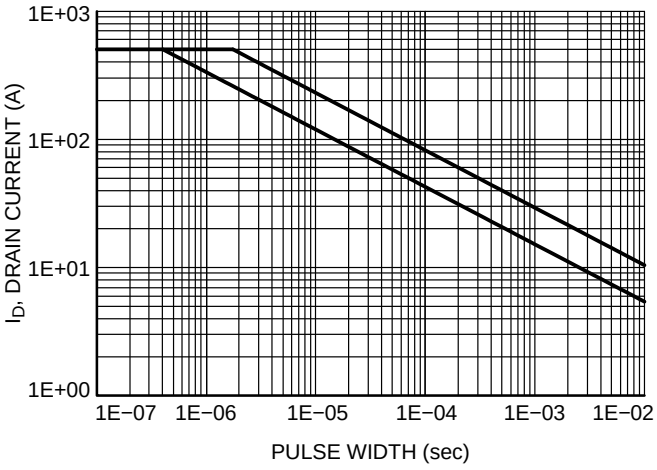
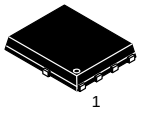


Figure 15. Avalanche Characteristics

ORDERING INFORMATION

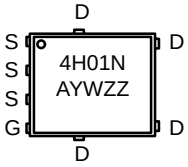
Device	Package	Shipping†
NTMFS4H01NT1G	SO8−FL (Pb-Free)	1500 / Tape & Reel
NTMFS4H01NT3G	SO8−FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SO−8 FLAT LEAD
CASE 488AA
STYLE 1

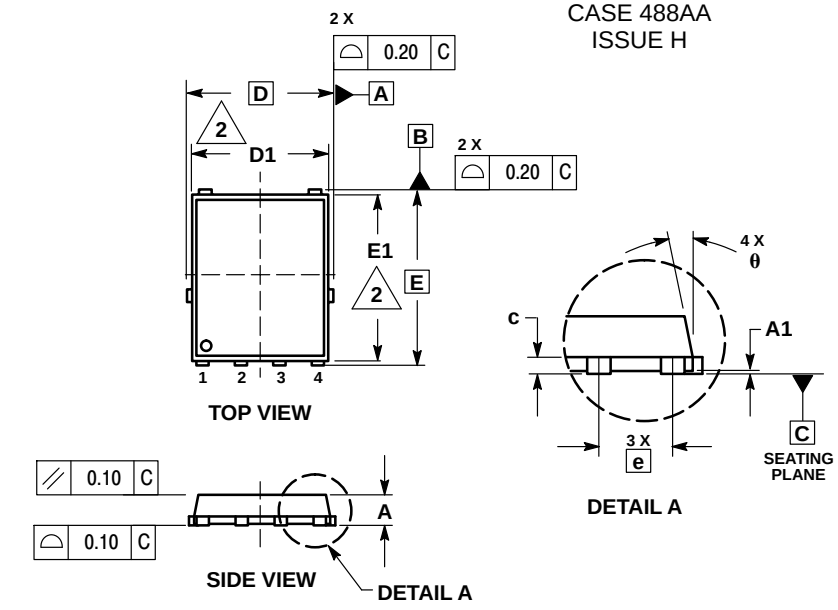
MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

PACKAGE DIMENSIONS

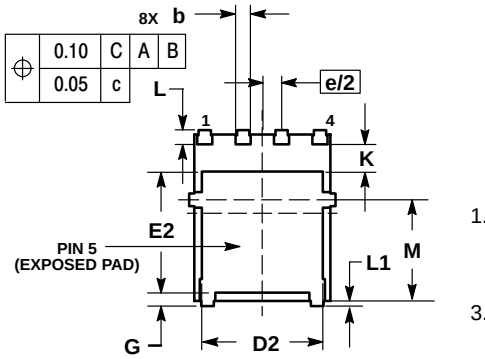
DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE H



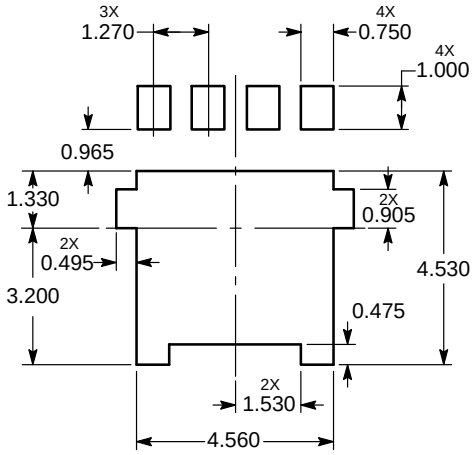
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	−−−	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.15 BSC		
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.61	0.71
K	1.20	1.35	1.50
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0 °	−−−	12 °

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN



SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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Phone: 421 33 790 2910
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