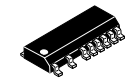
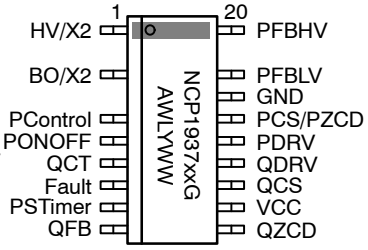
Combination Power Factor Correction and Quasi-Resonant Flyback Controllers for Adapters

NCP1937



SOIC−20
Narrow Body
CASE 751BS

MARKING DIAGRAM



NCP1937 = Specific Device Code
xx = A1, A2, A3, B1, B2, B3, B51, C1, C4 or C61
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

This combination IC integrates power factor correction (PFC) and quasi−resonant flyback functionality necessary to implement a compact and highly efficient Switched Mode Power Supply for an adapter application.

The PFC stage exhibits near−unity power factor while operating in a Critical Conduction Mode (CrM) with a maximum frequency clamp. The circuit incorporates all the features necessary for building a robust and compact PFC stage while minimizing the number of external components.

The quasi−resonant current−mode flyback stage features a proprietary valley−lockout circuitry, ensuring stable valley switching. This system works down to the 4th valley and toggles to a frequency foldback mode with a minimum frequency clamp beyond the 4th valley to eliminate audible noise. Skip mode operation allows excellent efficiency in light load conditions while consuming very low standby power consumption.

Common General Features

- Wide V_{CC} Range from 9 V to 30 V with Built−in Overvoltage Protection
- High−Voltage Startup Circuit and Active Input Filter Capacitor Discharge Circuitry for Reduced Standby Power
- Integrated High−Voltage Brown−Out Detector
- Integrated High−Voltage Switch Disconnects PFC Feedback Resistor Divider to Reduce Standby Power
- Fault Input for Severe Fault Conditions, NTC Compatible (Latch and Auto−Recovery Options)
- 0.5 A / 0.8 A Source / Sink Gate Drivers
- Internal Temperature Shutdown
- Power Savings Mode Reduces Supply Current Consumption to 70 μA Enabling Very Low Input Power Applications

PFC Controller Features

- Critical Conduction Mode with Constant On Time Control (Voltage Mode) and Maximum Frequency Clamp
- Accurate Overvoltage Protection
- Bi−Level Line−Dependent Output Voltage
- Fast Line / Load Transient Compensation
- Boost Diode Short−Circuit Protection
- Feed−Forward for Improved Operation across Line and Load
- Adjustable PFC Disable Threshold Based on Output Power

QR Flyback Controller Features

- Valley Switching Operation with Valley−Lockout for Noise−Free Operation
- Frequency Foldback with Minimum Frequency Clamp for Highest Performance in Standby Mode
- Minimum Frequency Clamp Eliminates Audible Noise
- Timer−Based Overload Protection (Latched or Auto−Recovery options)
- Adjustable Overpower Protection
- Winding and Output Diode Short−Circuit Protection
- 4 ms Soft−Start Timer

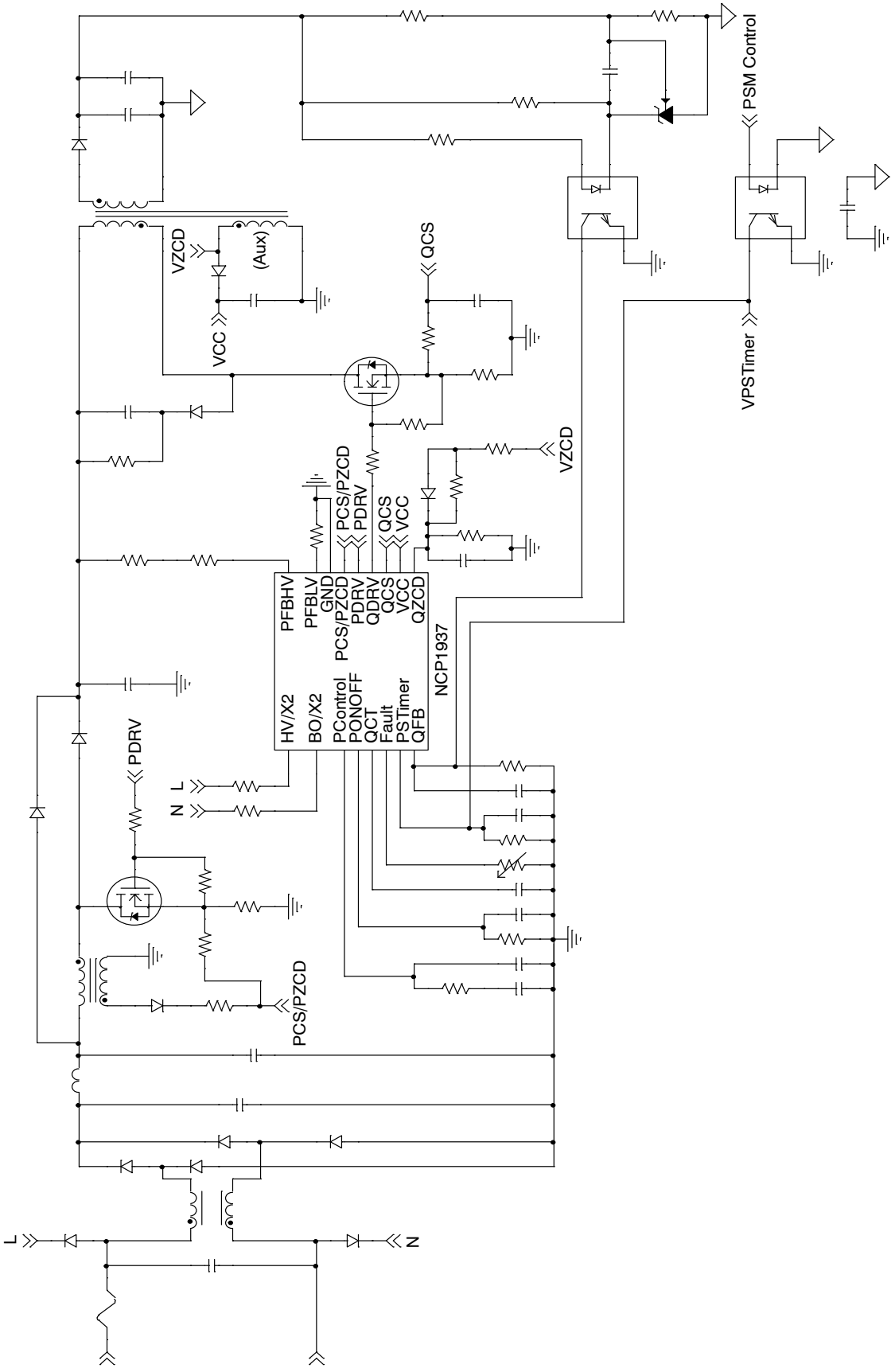


Figure 1. Typical Application Circuit

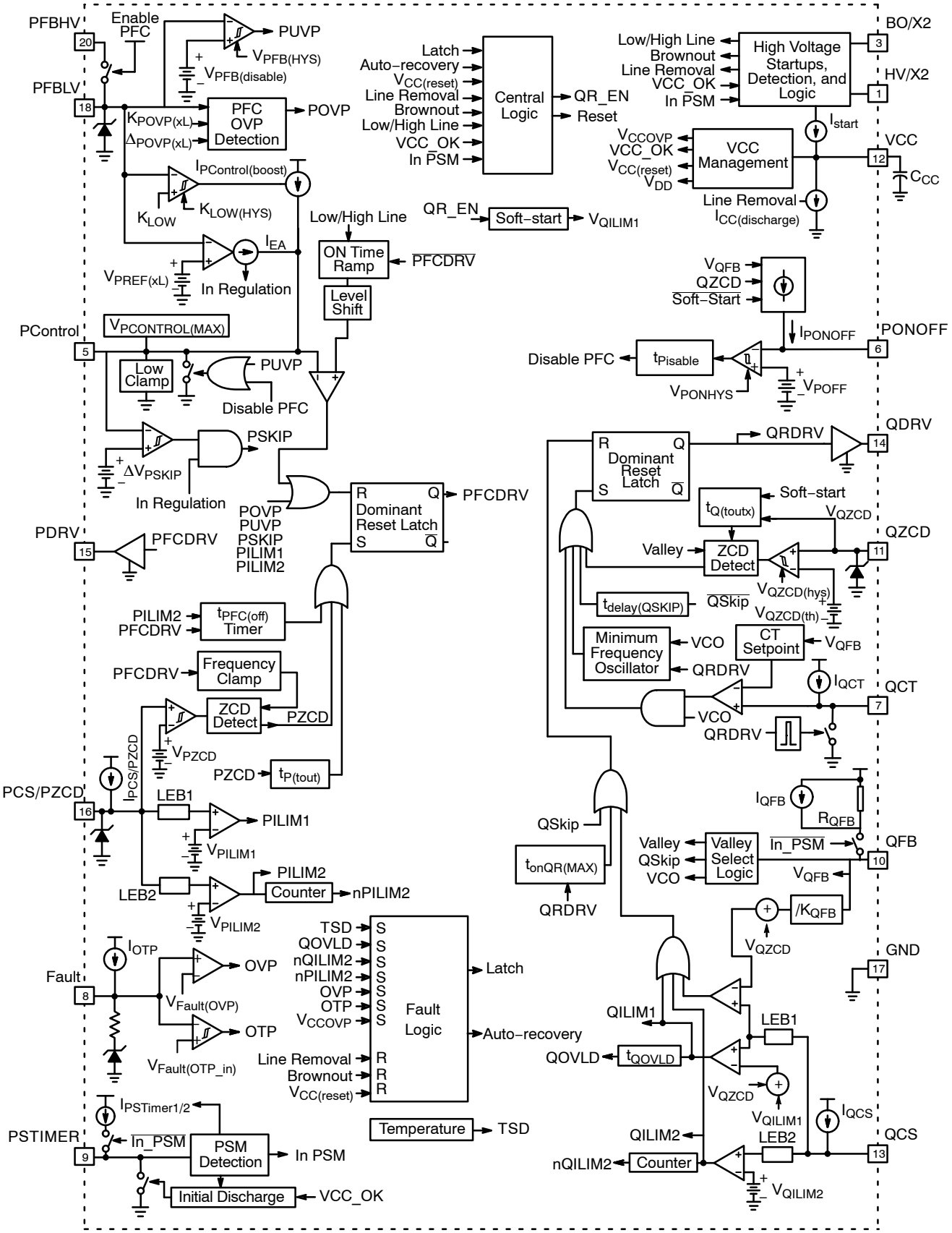


Figure 2. Functional Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin Out	Name	Function
1	HV/X2	High voltage startup circuit input. It is also used to discharge the input filter capacitors.
2		Removed for creepage distance.
3	BO/X2	Performs brown−out detection for the whole IC and it is also used to discharge the input filter capacitors and detect the line voltage range.
4		Removed for creepage distance.
5	PControl	Output of the PFC transconductance error amplifier. A compensation network is connected between this pin and ground to set the loop bandwidth.
6	PONOFF	A resistor between this pin and ground sets the PFC turn off threshold. The voltage on this pin is compared to an internal voltage signal proportional to the output power. The PFC disable threshold is determined by the resistor on this pin and the internal pull−up current source, I_{PONOFF}.
7	QCT	An external capacitor sets the frequency in VCO mode for the QR flyback controller.
8	Fault	The controller enters fault mode if the voltage of this pin is pulled above or below the fault thresholds. A precise pull up current source allows direct interface with an NTC thermistor. Fault detection triggers a latch or auto−recovery depending on device option.
9	PSTimer	Power savings mode (PSM) control and timer adjust. Compatible with an optocoupler for secondary control of PSM. The device enters PSM if the voltage on this pin exceeds the PSM threshold, V_{PS_in}. A capacitor between this pin and GND sets the delay time before the controller enters power savings mode. Once the controller enters power savings mode the IC is disabled and the current consumption is reduced to a maximum of 70 μA. The input filter capacitor discharge function is available while in power savings mode. The controller is enabled once $V_{PSTimer}$ drops below V_{PS_out}.
10	QFB	Feedback input for the QR Flyback controller. Allows direct connection to an optocoupler.
11	QZCD	Input to the demagnetization detection comparator for the QR Flyback controller. Also used to set the overpower compensation.
12	VCC	Supply input.
13	QCS	Input to the cycle−by−cycle current limit comparator for the QR Flyback section.
14	QDRV	QR flyback controller switch driver.
15	PDRV	PFC controller switch driver.
16	PCS/PZCD	Input to the cycle−by−cycle current limit comparator for the PFC section. Also used to perform the demagnetization detection for the PFC controller.
17	GND	Ground reference.
18	PFBLV	Low voltage PFC feedback input. An external resistor divider is used to sense the PFC bulk voltage. The divider low side resistor connects to this pin. This voltage is compared to an internal reference. The reference voltage is 2.5 V at low line and 4 V at high line. An internal high−voltage switch disconnects the low side resistor from the high side resistor chain when the PFC is disabled in order to reduce input power.
19		Removed for creepage distance.
20	PFBHV	High voltage PFC feedback input. An external resistor divider is used to sense the PFC bulk voltage. The divider high side resistor chain from the PFC bulk voltage connects to this pin. An internal high−voltage switch disconnects the high side resistor chain from the low side resistor when the PFC is disabled in order to reduce input power.

Table 2. NCP1937 DEVICE OPTIONS

Device	Overload Protection	Fault OTP	$V_{BO(start)}$ Typ	$V_{BO(stop)}$ Typ	PFC Disable Time	PFC Frequency Clamp	Package	Shipping†
NCP1937A1DR2G	Auto−Recovery	Latch	111 V	101 V	0.5 s	250 kHz	SOIC−20 (Pb−Free)	2500 / Tape & Reel
NCP1937A2DR2G	Auto−Recovery	Latch	111 V	101 V	0.5 s	131 kHz		
NCP1937A3DR2G	Auto−Recovery	Latch	111 V	101 V	4 s	131 kHz		
NCP1937B1DR2G	Auto−Recovery	Auto−Recovery	111 V	101 V	0.5 s	250 kHz		
NCP1937B2DR2G	Auto−Recovery	Auto−Recovery	111 V	101 V	0.5 s	131 kHz		
NCP1937B3DR2G	Auto−Recovery	Auto−Recovery	111 V	101 V	4 s	131 kHz		
NCP1937B51DR2G	Auto−Recovery	Auto−Recovery	97 V	87 V	0.5 s	131 kHz		
NCP1937C1DR2G	Latch	Latch	111 V	101 V	0.5 s	250 kHz		
NCP1937C4DR2G	Latch	Latch	111 V	101 V	13 s	131 kHz		
NCP1937C61DR2G	Latch	Latch	97 V	87 V	4 s	131 kHz		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 3. MAXIMUM RATINGS (Notes 1 − 6)

Rating	Pin	Symbol	Value	Unit
High Voltage Startup Circuit Input Voltage	1	$V_{HV/X2}$	−0.3 to 700	V
High Voltage Startup Circuit Input Current	1	$I_{HV/X2}$	20	mA
High Voltage Brownout Detector Input Voltage	3	$V_{BO/X2}$	−0.3 to 700	V
High Voltage Brownout Detector Input Current	3	$I_{BO/X2}$	20	mA
PFC High Voltage Feedback Input Voltage	20	V_{PFBHV}	−0.3 to 700	V
PFC High Voltage Feedback Input Current	20	I_{PFBHV}	0.5	mA
PFC Low Voltage Feedback Input Voltage	18	V_{PFBLV}	−0.3 to 9	V
PFC Low Voltage Feedback Input Current	18	I_{PFBLV}	0.5	mA
PFC Zero Current Detection and Current Sense Input Voltage (Note 1)	16	$V_{PCS/PZCD}$	−0.3 to $V_{PCS/PZCD(MAX)}$	V
PFC Zero Current Detection and Current Sense Input Current	16	$I_{PCS/PZCD}$	−2/+5	mA
PFC Control Input Voltage	5	$V_{PControl}$	−0.3 to 5	V
PFC Control Input Current	5	$I_{PControl}$	10	mA
Supply Input Voltage	12	$V_{CC(MAX)}$	−0.3 to 30	V
Supply Input Current	12	$I_{CC(MAX)}$	30	mA
Supply Input Voltage Slew Rate	12	dV_{CC}/dt	1	V/μs
Fault Input Voltage	8	V_{Fault}	−0.3 to (V_{CC} + 1.25)	V
Fault Input Current	8	I_{Fault}	10	mA
QR Flyback Zero Current Detection Input Voltage	11	V_{QZCD}	−0.9 to (V_{CC} + 1.25)	V
QR Flyback Zero Current Detection Input Current	11	I_{QZCD}	−2/+5	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $V_{PCS/PZCD(MAX)}$ is the maximum voltage of the pin shown in the electrical table. When the voltage on this pin exceeds 5 V, the pin sinks a current equal to ($V_{PCS/PZCD}$ − 5 V) / (2 kΩ). A $V_{PSC/PZCD}$ of 7 V generates a sink current of approximately 1 mA.
2. Maximum driver voltage is limited by the driver clamp voltage, $V_{XDRV(high)}$, when V_{CC} exceeds the driver clamp voltage. Otherwise, the maximum driver voltage is V_{CC}.
3. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum−rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
4. This device contains Latch−Up protection and exceeds ± 100 mA per JEDEC Standard JESD78.
5. Low Conductivity Board. As mounted on 80 x 100 x 1.5 mm FR4 substrate with a single layer of 50 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC51−1 conductivity test PCB. Test conditions were under natural convection of zero air flow.
6. Pins 1, 3, and 20 are rated to the maximum voltage of the part, or 700 V.

Table 3. MAXIMUM RATINGS (Notes 1 – 6)

Rating	Pin	Symbol	Value	Unit
QR Feedback Input Voltage	7	V_{QCT}	−0.3 to 10	V
QR Feedback Input Current	7	I_{QCT}	10	mA
QR Flyback Current Sense Input Voltage	13	V_{QCS}	−0.3 to 10	V
QR Flyback Current Sense Input Current	13	I_{QCS}	10	mA
QR Flyback Feedback Input Voltage	10	V_{QFB}	−0.3 to 10	V
QR Flyback Feedback Input Current	10	I_{QFB}	10	mA
PSTimer Input Voltage	9	$V_{PSTimer}$	−0.3 to 10	V
PSTimer Input Current	9	$I_{PSTimer}$	10	mA
PFC Driver Maximum Voltage (Note 2)	15	V_{PDRV}	−0.3 to $V_{PDRV(high)}$	V
PFC Driver Maximum Current	15	$I_{PDRV(SRC)}$ $I_{PDRV(SNK)}$	500 800	mA
Flyback Driver Maximum Voltage (Note 2)	14	V_{QDRV}	−0.3 to $V_{QDRV(high)}$	V
Flyback Driver Maximum Current	14	$I_{QDRV(SRC)}$ $I_{QDRV(SNK)}$	500 800	mA
PFC ON/OFF Threshold Adjust Input Voltage	6	V_{PONOFF}	−0.3 to 10	V
PFC ON/OFF Threshold Adjust Input Current	6	I_{PONOFF}	10	mA
Operating Junction Temperature Range	N/A	T_J	−40 to 125	°C
Maximum Junction Temperature	N/A	$T_{J(MAX)}$	150	°C
Storage Temperature Range	N/A	T_{STG}	−60 to 150	°C
Power Dissipation (T_A = 75°C, 1 Oz Cu, 0.155 Sq Inch Printed Circuit Copper Clad) Plastic Package SOIC−20NB		P_D	0.62	W
Thermal Resistance, Junction−to−Ambient (1 oz. Cu Printed Circuit Copper Clad) Plastic Package SOIC−20NB		$R_{\theta JA}$	121	°C/W
Thermal Resistance, Junction−to−Case		$R_{\theta JC}$	77	°C/W
ESD Capability (Note 6) Human Body Model per JEDEC Standard JESD22−A114F. Machine Model per JEDEC Standard JESD22−A115−A. Charge Device Model per JEDEC Standard JESD22−C101E.		 HBM MM CDM	 3000 200 750	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $V_{PCS/PZCD(MAX)}$ is the maximum voltage of the pin shown in the electrical table. When the voltage on this pin exceeds 5 V, the pin sinks a current equal to ($V_{PCS/PZCD}$ − 5 V) / (2 kΩ). A $V_{PSC/PZCD}$ of 7 V generates a sink current of approximately 1 mA.
2. Maximum driver voltage is limited by the driver clamp voltage, $V_{XDRV(high)}$, when V_{CC} exceeds the driver clamp voltage. Otherwise, the maximum driver voltage is V_{CC}.
3. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum−rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
4. This device contains Latch−Up protection and exceeds ± 100 mA per JEDEC Standard JESD78.
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6. Pins 1, 3, and 20 are rated to the maximum voltage of the part, or 700 V.

Table 4. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, $V_{BO/X2}$ = 120 V, $V_{HV/X2}$ = 120 V, V_{Fault} = open, V_{RPFBHV} = 20 V, V_{PFBLV} = 2.4 V, $V_{PControl}$ = 4 V, $V_{PCS/PZCD}$ = 0 V, V_{QFB} = 3 V, V_{PONOFF} = 4 V, V_{QCS} = 0 V, V_{QZCD} = 0 V, $V_{PSTimer}$ = 0 V, R_{PFBHV} = 200 kΩ, C_{VCC} = 100 nF , C_{QCT} = 220 pF, C_{PDRV} = 1 nF, C_{QDRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is − 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Pin	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS							
Supply Voltage							V
Startup Threshold	V_{CC} increasing	12	$V_{CC(on)}$	16	17	18	
Regulation Level in PSM	V_{QFB} = 0, $V_{PSTimer}$ = 3 V		$V_{CC(PS\_on)}$	–	11	–	
Minimum Operating Voltage	V_{CC} decreasing		$V_{CC(off)}$	8.2	8.8	9.4	
Operating Hysteresis	$V_{CC(on)} - V_{CC(off)}$		$V_{CC(HYS)}$	7.7	–	–	
Delta Between PSM and $V_{CC(off)}$ Levels	$V_{CC(PS\_on)} - V_{CC(off)}$		$V_{CC(\Delta PS\_off)}$	1.65	2.20	2.75	
Internal Latch / Logic Reset Level	V_{CC} decreasing		$V_{CC(reset)}$	4.5	5.5	7.5	
Transition from I_{start1} to I_{start2}	V_{CC} increasing, $I_{HV/X2}$ = 650 μA		$V_{CC(inhibit)}$	0.3	0.7	0.95	
Startup Current in Inhibit Mode	V_{CC} = 0 V, $V_{BO/X2}$ = 0 V	12	$I_{start1A}$	0.20	0.50	0.65	mA
	V_{CC} = 0 V, $V_{HV/X2}$ = 0 V	12	$I_{start1B}$	0.20	0.50	0.65	
Startup Current	$V_{CC} = V_{CC(on)} - 0.5$ V						mA
Operating Mode	$V_{HV/X2}$ = 100 V, $V_{BO/X2} = V_{CC}$	12	$I_{start2A}$	2.5		5	
	$V_{BO/X2}$ = 100 V, $V_{HV/X2} = V_{CC}$		$I_{start2B}$	2.5		5	
PSM Mode	$V_{HV/X2}$ = 100 V, $V_{BO/X2}$ = 0 V	12	$I_{start2A\_PSM}$	9	15	20	
	$V_{BO/X2}$ = 100 V, $V_{HV/X2}$ = 0 V		$I_{start2B\_PSM}$	9	15	20	
Startup Circuit Off−State Leakage Current	$V_{HV/X2}$ = 500 V	1	$I_{HV/X2\ (off)}$	–	–	3	μA
Minimum Startup Voltage	$I_{start2A}$ = 1 mA, $V_{CC} = V_{CC(on)} - 0.5$ V	1	$V_{HV/X2(MIN)}$	–	–	40	V
	$I_{start2B}$ = 1 mA, $V_{CC} = V_{CC(on)} - 0.5$ V	3	$V_{BO/X2(MIN)}$	–	–	40	
Minimum Startup Voltage in PSM	I_{start} = 9 mA, $V_{CC} = V_{CC(PS\_on)} - 0.5$ V	1	$V_{HV/X2(MIN)}$	–	–	60	V
	I_{start} = 9 mA, $V_{CC} = V_{CC(PS\_on)} - 0.5$ V	3	$V_{BO/X2(MIN)}$	–	–	60	
V_{CC} Overvoltage Protection Threshold		12	$V_{CC(OVP)}$	27	28	29	V
V_{CC} Overvoltage Protection Delay		12	$t_{delay(VCC\_OVP)}$		30.0		μs
Supply Current		12					mA
In Power Savings Mode			I_{CC1a}	–	–	0.07	
Before Startup, Fault or Latch	$V_{CC} = V_{CC(on)} - 0.5$ V		I_{CC2}		0.15	0.25	
Flyback in Skip, PFC Disabled	V_{QFB} = 0.35 V		I_{CC3a}		0.3	0.4	
Flyback in Skip, PFC in Skip	V_{QFB} = 0.35 V, $V_{PControl} < V_{PSKIP}$		I_{CC3b}		0.5	1.0	
Flyback Enabled, QDRV Low, PFC Disabled	V_{QZCD} = 1 V,		I_{CC4}		0.85	1.35	
Flyback Enabled, QDRV Low, PFC in Skip	V_{QZCD} = 1 V, $V_{PControl} < V_{PSKIP}$		I_{CC5}		1.1	1.8	
PFC and Flyback switching at 70 kHz	$C_{QDRV} = C_{PDRV}$ = open		I_{CC6}		1.5	4.0	
PFC and Flyback switching at 70 kHz			I_{CC7}		2.8	5.2	
INPUT FILTER DISCHARGE							
Current Consumption in Discharge Mode	$V_{CC} = V_{CC(off)}$ + 200 mV	12	$I_{CC(discharge)}$	8.0	11.5	15.0	mA
Line Voltage Removal Detection Threshold	$V_{BO/X2}$ decreasing	3	$V_{lineremoval}$	20	30	40	V
Line Voltage Removal Detection Delay	$V_{BO/X2}$ stays above $V_{lineremoval}$	3	$t_{lineremoval}$	130	200	270	ms

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Characteristics	Conditions	Pin	Symbol	Min	Typ	Max	Unit
BROWN–OUT DETECTION							
System Brown–out Thresholds (See Table 2 for device options)	$V_{BO/X2}$ increasing $V_{BO/X2}$ decreasing	3	$V_{BO(start)}$ $V_{BO(stop)}$	102 86	111 101	120 116	V
System Brown–out Thresholds (See Table 2 for device options) (B51, C61)	$V_{BO/X2}$ increasing $V_{BO/X2}$ decreasing	3	$V_{BO(start)}$ $V_{BO(stop)}$	83 79	97 87	111 95	V
Brown–out Hysteresis	$V_{BO/X2}$ increasing	3	$V_{BO(hys)}$	4		16	V
Brown–out Detection Blanking Time	$V_{BO/X2}$ decreasing, duration below $V_{BO(stop)}$ for a Brown–out fault	3	$t_{BO(stop)}$	43	54	65	ms
Brown–out Drive Disable Threshold	$V_{BO/X2}$ decreasing, threshold to disable switching	3	$V_{BO(DRV\_disable)}$	20	30	40	V
Line Level Detection Threshold Line Level Detection Threshold (B51, C61)	$V_{BO/X2}$ increasing	3	$V_{BO(lineselect)}$	216 199	240 221	264 243	V
High to Low Line Mode Selector Timer	$V_{BO/X2}$ decreasing	3	$t_{high\ to\ low\ line}$	43	54	65	ms
Low to High Line Mode Selector Timer	$V_{BO/X2}$ increasing	3	$t_{low\ to\ high\ line}$	200	350	450	μs
Brownout Pin Off State Leakage Current	$V_{BO/X2}$ = 500 V	3	$I_{BO/X2(off)}$	–	–	42	μA
PFC MAXIMUM OFF TIME TIMER							
Maximum Off Time	$V_{PCS/PZCD} > V_{PILIM2}$	15	$t_{PFC(off1)}$ $t_{PFC(off2)}$	100 700	200 1000	300 1300	μs
PFC CURRENT SENSE							
Cycle by Cycle Current Sense Threshold		16	V_{PILIM1}	0.45	0.50	0.55	V
Cycle by Cycle Leading Edge Blanking Duration		16	$t_{PCS(LEB1)}$	250	325	400	ns
Cycle by Cycle Current Sense Propagation Delay		16	$t_{PCS(delay1)}$		100	200	ns
Abnormal Overcurrent Fault Threshold		16	V_{PILIM2}	1.12	1.25	1.38	V
Abnormal Overcurrent Fault Leading Edge Blanking Duration		16	$t_{PCS(LEB2)}$	100	175	250	ns
Abnormal Overcurrent Fault Propagation Delay		16	$t_{PCS(delay2)}$		100	200	ns
Number of Consecutive Abnormal Overcurrent Faults to Enter Latch Mode		15	n_{PILIM2}	–	4	–	
Pull–up Current Source	$V_{PCS/PZCD}$ = 1.5 V	16	$I_{PCS/PZCD}$	0.7	1.0	1.3	μA
PFC REGULATION BLOCK							
Reference Voltage	$V_{BO/X2} > V_{BO(lineselect)}$ $V_{BO/X2} < V_{BO(lineselect)}$	18	$V_{PREF(HL)}$ $V_{PREF(LL)}$	3.92 2.45	4.00 2.50	4.08 2.55	V
Error Amplifier Current	PFC Enabled						μA
Source	V_{PFBLV} = 0.96 x $V_{PREF(HL)}$	5	$I_{EA(SRCHL)}$	16	32	48	
Sink	V_{PFBLV} = 1.04 x $V_{PREF(HL)}$		$I_{EA(SNKHL)}$	16	32	48	
Source	V_{PFBLV} = 0.96 x $V_{PREF(LL)}$		$I_{EA(SRCLL)}$	10	20	30	
Sink	V_{PFBLV} = 1.04 x $V_{PREF(LL)}$		$I_{EA(SNKLL)}$	10	20	30	
Open Loop Error Amplifier Transconductance	$V_{PFBLV} = V_{PREF(LL)} \pm 4\%$ $V_{PFBLV} = V_{PREF(HL)} \pm 4\%$	5	g_m g_{m_HL}	100 100	200 200	300 300	μS
Maximum Control Voltage	V_{PFBLV} * $K_{LOW(PFCxL)}$, $C_{PControl}$ = 10 nF	5	$V_{PControl(MAX)}$	–	4.5	–	V
Minimum Control Voltage (PWM Offset)	V_{PFBLV} * $K_{POVP(xL)}$, $C_{PControl}$ = 10 nF	5	$V_{PControl(MIN)}$	–	0.5	–	V

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Characteristics	Conditions	Pin	Symbol	Min	Typ	Max	Unit
PFC REGULATION BLOCK							
EA Output Control Voltage Range	$V_{PControl(MAX)}$ - $V_{PControl(MIN)}$	5	$\Delta V_{PControl}$	3.8	4.0	4.2	V
Delta Between Minimum Control Voltage and Lower Clamp PControl Voltages	$V_{PControl(MIN)}$ − $V_{PClamp(lower)}$	5	$\Delta V_{PClamp(lower)}$	−125	−100	−75	mV
Ratio between the V_{out} Low Detect Threshold and the Regulation Level	V_{PFBLV} decreasing, V_{BOOST} / $V_{PREF(HL)}$ V_{PFBLV} decreasing, V_{BOOST} / $V_{PREF(LL)}$	18	$K_{LOW(PFCHL)}$ $K_{LOW(PFCLL)}$	0.940 0.940	0.945 0.945	0.950 0.950	
Ratio between the V_{out} Low Exit Threshold and the Regulation Level	V_{PFBLV} increasing	18	$K_{LOW(HYSHL)}$ $K_{LOW(HYSLL)}$	0.950 0.950	0.960 0.960	0.965 0.965	
Source Current During V_{out} Low Detect		5	$I_{PControl(boost)}$	190	240	290	μA
PFC In Regulation Threshold	$V_{PControl}$ increasing	5	$I_{In\_Regulation}$	−6.5	–	0	μA
Resistance of Internal Pull Down Switch	$I_{PControl}$ = 5 mA	5	$R_{PControl}$	4	25	50	Ω
PFC SKIP MODE							
Delta Between Skip Level and Lower Clamp PControl Voltages	$V_{PControl}$ decreasing, measured from $V_{PClamp(lower)}$	5	ΔV_{PSKIP}	5	25	50	mV
PFC Skip Hysteresis	$V_{PControl}$ increasing	5	$V_{PSKIP(HYS)}$	25	50	75	mV
Delay Exiting Skip Mode	Apply 1 V step from $V_{PClamp(lower)}$	5	$t_{delay(PSKIP)}$	–	50	60	μs
PFC FAULT PROTECTION							
Ratio between the Hard Overvoltage Protection Threshold and Regulation Level	V_{PFBLV} increasing $K_{POVP(LL)}$ = $V_{PFBLV}/V_{PREF(LL)}$ $K_{POVP(HL)}$ = $V_{PFBLV}/V_{PREF(HL)}$	18	$K_{POVP(LL)}$ $K_{POVP(HL)}$	1.06 1.05	1.08 1.06	1.10 1.08	
Soft Overvoltage Protection Threshold	$V_{PSOVP(LL)}$ = soft overvoltage level $\Delta_{POVP(LL)} = K_{POVP} * V_{PREF(LL)} - V_{PSOVP(LL)}$ $\Delta_{POVP(HL)} = K_{POVP} * V_{PREF(HL)} - V_{PSOVP(HL)}$	18	$\Delta_{POVP(LL)}$ $\Delta_{POVP(HL)}$	20 20	– –	55 55	mV
PFC Feedback Pin Disable Threshold	V_{PFBLV} decreasing	18	$V_{PFB(disable)}$	0.225	0.30	0.35	V
PFC Feedback Pin Enable Threshold	V_{PFBLV} increasing	18	$V_{PFB(enable)}$	0.275	0.35	0.40	V
PFC Feedback Pin Hysteresis	V_{PFBLV} increasing	18	$V_{PFB(HYS)}$	25	50		mV
PFC Feedback Disable Delay		18	$t_{delay(PFB)}$		30		μs
PFC ON TIME CONTROL							
PFC Maximum On Time	$V_{PControl}$ = $V_{PControl(MAX)}$, $V_{BO/X2}$ = 163 V $V_{BO/X2}$ = 325 V	15	t_{on1a} t_{on1b}	12.5 4.25	15 5.00	17.5 5.75	μs
Minimum On−Time	$V_{PControl}$ = $V_{PControl(MIN)}$	15	$t_{P(on-time)}$	–	–	200	ns
PFC Frequency Clamp (See Table 2 for device options)		15	$f_{clamp(PFC)}$	112 215	131 250	150 285	kHz

Table 4. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, $V_{BO/X2}$ = 120 V, $V_{HV/X2}$ = 120 V, V_{Fault} = open, V_{RPFBHV} = 20 V, V_{PFBLV} = 2.4 V, $V_{PControl}$ = 4 V, $V_{PCS/PZCD}$ = 0 V, V_{QFB} = 3 V, V_{PONOFF} = 4 V, V_{QCS} = 0 V, V_{QZCD} = 0 V, $V_{PSTimer}$ = 0 V, R_{PFBHV} = 200 kΩ, C_{VCC} = 100 nF , C_{QCT} = 220 pF, C_{PDRV} = 1 nF, C_{QDRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is − 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Pin	Symbol	Min	Typ	Max	Unit
PFC DISABLE							
Voltage to Current Conversion Ratio	V_{QFB} = 3 V, Low Line V_{QFB} = 3 V, High Line	6	$I_{ratio1(QFB/PON)}$ $I_{ratio2(QFB/PON)}$	14 14	15 15	16 16	μA
PFC Disable Threshold	V_{PONOFF} decreasing	6	V_{POFF}	1.9	2.0	2.1	V
PFC Enable Hysteresis	V_{PONOFF} = increasing	6	V_{PONHYS}	0.135	0.160	0.185	V
PONOFF Operating Mode Voltage	t_{demag}/T = 70%, R_{PONOFF} = 191 kΩ, C_{PONOFF} = 1 nF V_{QFB} = 1.8 V (decreasing) V_{QFB} = 3 V (decreasing)	6	$V_{PONOFF1}$ $V_{PONOFF2}$	1.08 1.8	1.20 2.0	1.32 2.2	V
PFC Disable Timer (See Table 2 for device options)	Disable Timer	6	$t_{Pdisable}$	0.45 3.6 11.7	0.50 4 13	0.55 4.4 14.3	s
PFC Enable Filter Delay		6	$t_{Penable(filter)}$	50	100	150	μs
PFC Enable Timer	PONOFF Increasing	6	$t_{Penable}$	200	–	500	μs
PFC Off−State Leakage Current	V_{PONOFF} = 1 V, V_{PFBHV} = 500 V	20	$I_{PFBHV(off)}$	–	0.1	3	μA
PFC Feedback Switch On Resistance	V_{PFBHV} = 4.25 V, I_{PFBHV} = 100 μA	20	$R_{PFBswitch(on)}$	–	–	10	kΩ
PFC GATE DRIVE							
Rise Time (10−90%)	V_{PDRV} from 10 to 90% of V_{CC}	15	$t_{PDRV(rise)}$	–	40	80	ns
Fall Time (90−10%)	90 to 10% of V_{PDRV}	15	$t_{PDRV(fall)}$	–	20	40	ns
Driver Resistance Source Sink		15	$R_{PDRV(SRC)}$ $R_{PDRV(SNK)}$		13 7		Ω
Current Capability Source Sink	V_{PDRV} = 2 V V_{PDRV} = 10 V	15	$I_{PDRV(SRC)}$ $I_{PDRV(SNK)}$	– –	500 800	– –	mA
High State Voltage	V_{CC} = $V_{CC(off)}$ + 0.2 V, R_{PDRV} = 10 kΩ V_{CC} = 26 V, R_{PDRV} = 10 kΩ	15	$V_{PDRV(high)}$	8 10	– 12	– 14	V
Low Stage Voltage	V_{Fault} = 4 V	15	$V_{PDRV(low)}$	–	–	0.25	V
PFC ZERO CURRENT DETECTION							
Zero Current Detection Threshold	$V_{PCS/PZCD}$ rising $V_{PCS/PZCD}$ falling	16	$V_{PZCD(rising)}$ $V_{PZCD(falling)}$	675 200	750 250	825 300	mV
Hysteresis on Voltage Threshold	$V_{PZCD(rising)}$ − $V_{PZCD(falling)}$	16	$V_{PZCD(HYS)}$	375	500	625	mV
Propagation Delay		16	t_{PZCD}	50	100	170	ns
Input Voltage Excursion Upper Clamp Negative Clamp	$I_{PCS/PZCD}$ = 1 mA $I_{PCS/PZCD}$ = −2 mA	16	$V_{PCS/PZCD(MAX)}$ $V_{PCS/PZCD(MIN)}$	6.5 −0.9	7 −0.7	7.5 0	V
Minimum detectable ZCD Pulse Width		16	t_{SYNC}	–	70	200	ns
Missing Valley Timeout Timer	Measured after last ZCD transition	16	$t_{P(tout)}$	8	10	12	μs

Table 4. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, $V_{BO/X2}$ = 120 V, $V_{HV/X2}$ = 120 V, V_{Fault} = open, V_{RPFBHV} = 20 V, V_{PFBLV} = 2.4 V, $V_{PControl}$ = 4 V, $V_{PCS/PZCD}$ = 0 V, V_{QFB} = 3 V, V_{PONOFF} = 4 V, V_{QCS} = 0 V, V_{QZCD} = 0 V, $V_{PSTimer}$ = 0 V, R_{PFBHV} = 200 kΩ, C_{VCC} = 100 nF , C_{QCT} = 220 pF, C_{PDRV} = 1 nF, C_{QDRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Pin	Symbol	Min	Typ	Max	Unit
QR FLYBACK GATE DRIVE							
Rise Time (10–90%)	V_{QDRV} from 10 to 90%	14	$t_{QDRV(rise)}$	–	40	80	ns
Fall Time (90–10%)	90 to 10% of V_{QDRV}	14	$t_{QDRV(fall)}$	–	20	40	ns
Driver Resistance Source Sink		14	$R_{QDRV(SRC)}$ $R_{QDRV(SNK)}$		13 7		Ω
Current Capability Source Sink	V_{QDRV} = 2 V V_{QDRV} = 10 V	14	$I_{QDRV(SRC)}$ $I_{QDRV(SNK)}$	– –	500 800	– –	mA
High State Voltage	$V_{CC} = V_{CC(off)}$ + 0.2 V, R_{QDRV} = 10 kΩ V_{CC} = 26 V, R_{QDRV} = 10 kΩ	14	$V_{QDRV(high)}$	8 10	– 12	– 14	V
Low Stage Voltage	V_{Fault} = 4 V	14	$V_{QDRV(low)}$	–	–	0.25	V
QR FLYBACK FEEDBACK							
Internal Pull–Up Current Source		10	I_{QFB}	48	50	52	μA
Feedback Input Open Voltage		10	$V_{QFB(open)}$	4.8	5.0	5.2	V
V_{QFB} to Internal Current Setpoint Division Ratio		10	K_{QFB}	3.95	4.0	4.15	–
QFB Pull Up Resistor	$V_{PSTimer}$ = 3 V; V_{QFB} = 0.4 V	10	R_{QFB}	365	400	435	kΩ
Valley Thresholds		10					V
Transition from 1st to 2nd valley	V_{QFB} decreasing		V_{H2D}	1.316	1.400	1.484	
Transition from 2nd to 3rd valley	V_{QFB} decreasing		V_{H3D}	1.128	1.200	1.272	
Transition from 3rd to 4th valley	V_{QFB} decreasing		V_{H4D}	0.846	0.900	0.954	
Transition from 4th valley to VCO	V_{QFB} decreasing		V_{HVCOD}	0.752	0.800	0.848	
Transition from VCO to 4th valley	V_{QFB} increasing		V_{HVCOI}	1.316	1.400	1.484	
Transition from 4th to 3rd valley	V_{QFB} increasing		V_{H4I}	1.504	1.600	1.696	
Transition from 3rd to 2nd valley	V_{QFB} increasing		V_{H3I}	1.692	1.800	1.908	
Transition from 2nd to 1st valley	V_{QFB} increasing		V_{H2I}	1.880	2.000	2.120	
Skip Threshold	V_{QFB} decreasing	10	V_{QSKIP}	0.35	0.40	0.45	V
Skip Hysteresis	V_{QFB} increasing	10	$V_{QSKIP(HYS)}$	25	50	75	mV
Delay Exiting Skip Mode to 1st QDRV Pulse	Apply 1 V step from V_{QSKIP}	10	$t_{delay(QSKIP)}$	–	–	10	μs
Maximum On Time		14	$t_{onQR(MAX)}$	26	32	38	μs
QR FLYBACK TIMING CAPACITOR							
QCT Operating Voltage Range	V_{QFB} = 0.5 V	7	$V_{QCT(peak)}$	3.815	4.000	4.185	V
On Time Control Source Current	V_{QCT} = 0 V	7	I_{QCT}	18	20	22	μA
Minimum voltage on QCT Input		7	$V_{QCT(min)}$	–	–	90	mV
Minimum Operating Frequency in VCO Mode	$V_{QCT} = V_{QCT(peak)}$ + 100 mV	7	$f_{VCO(MIN)}$	23.5	27	30.5	kHz

Table 4. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, $V_{BO/X2}$ = 120 V, $V_{HV/X2}$ = 120 V, V_{Fault} = open, V_{RPFBHV} = 20 V, V_{PFBLV} = 2.4 V, $V_{PControl}$ = 4 V, $V_{PCS/PZCD}$ = 0 V, V_{QFB} = 3 V, V_{PONOFF} = 4 V, V_{QCS} = 0 V, V_{QZCD} = 0 V, $V_{PSTimer}$ = 0 V, R_{PFBHV} = 200 kΩ, C_{VCC} = 100 nF , C_{QCT} = 220 pF, C_{PDRV} = 1 nF, C_{QDRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Pin	Symbol	Min	Typ	Max	Unit
QR FLYBACK DEMAGNETIZATION INPUT							
QZCD threshold voltage	V_{QZCD} decreasing	11	$V_{QZCD(th)}$	35	55	90	mV
QZCD hysteresis	V_{QZCD} increasing	11	$V_{QZCD(HYS)}$	15	35	55	mV
Demagnetization Propagation Delay	V_{QZCD} step from 4.0 V to –0.3 V	11	t_{DEM}	–	150	250	ns
Input Voltage Excursion Upper Clamp Negative Clamp	I_{QZCD} = 5.0 mA I_{QZCD} = –2.0 mA	11	$V_{QZCD(MAX)}$ $V_{QZCD(MIN)}$	12.4 –0.9	12.7 –0.7	13.25 0	V
Blanking Delay After Turn–Off		11	$t_{ZCD(blank)}$	2	3	4	μs
Timeout After Last Demagnetization Detection	During soft–start After soft–start	14	$t_{Q(tout1)}$ $t_{Q(tout2)}$	80 5.1	100 6	120 6.9	μs
QR FLYBACK CURRENT SENSE							
Current Sense Voltage Threshold	V_{QCS} increasing V_{QCS} increasing, V_{QZCD} = 1 V	13	$V_{QILIM1a}$ $V_{QILIM1b}$	0.760 0.760	0.800 0.800	0.840 0.840	V
Cycle by Cycle Leading Edge Blanking Duration		13	$t_{QCS(LEB1)}$	220	275	350	ns
Cycle by Cycle Current Sense Propagation Delay		13	$t_{QCS(delay1)}$	–	125	175	ns
Immediate Fault Protection Threshold	V_{QCS} increasing, V_{QFB} = 4 V	13	V_{QILIM2}	1.125	1.200	1.275	V
Abnormal Overcurrent Fault Leading Edge Blanking Duration		13	$t_{QCS(LEB2)}$	90	120	150	ns
Abnormal Overcurrent Fault Propagation Delay		13	$t_{QCS(delay2)}$	–	125	175	ns
Number of Consecutive Abnormal Overcurrent Faults to Enter Latch Mode		13	n_{QILIM2}	–	4	–	
Minimum Peak Current Level in VCO Mode	V_{QFB} = 0.4 V, V_{QCS} increasing	13	$I_{peak(VCO)}$	11	12.5	14	%
Set point decrease for V_{QZCD} = – 250 mV	V_{QCS} Increasing, V_{QFB} = 4 V	13	$V_{OPP(MAX)}$	28	31.25	33	%
Overpower Protection Delay		11	$t_{QOPP(delay)}$	–	125	175	ns
Pull–up Current Source	V_{QCS} = 1.5 V	13	I_{QCS}	0.7	1.0	1.3	μA
QR FLYBACK FAULT PROTECTION							
Soft–Start Period		13	t_{SSTART}	2.8	4.0	5.0	ms
Flyback Overload Fault Timer	V_{QCS} = V_{QILIM1}	13	t_{QOVLD}	60	80	100	ms

Table 4. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, $V_{BO/X2}$ = 120 V, $V_{HV/X2}$ = 120 V, V_{Fault} = open, V_{RPFBHV} = 20 V, V_{PFBLV} = 2.4 V, $V_{PControl}$ = 4 V, $V_{PCS/PZCD}$ = 0 V, V_{QFB} = 3 V, V_{PONOFF} = 4 V, V_{QCS} = 0 V, V_{QZCD} = 0 V, $V_{PSTimer}$ = 0 V, R_{PFBHV} = 200 kΩ, C_{VCC} = 100 nF , C_{QCT} = 220 pF, C_{PDRV} = 1 nF, C_{QDRV} = 1 nF, for typical values T_J = 25°C, for min/max values, T_J is − 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Pin	Symbol	Min	Typ	Max	Unit
COMMON FAULT PROTECTION							
Overvoltage Protection (OVP) Threshold	V_{Fault} increasing	8	$V_{Fault(OVP)}$	2.79	3.00	3.21	V
Delay Before Fault Confirmation Used for OVP Detection Used for OTP Detection	 V_{Fault} increasing V_{Fault} decreasing	8	 $t_{delay(Fault\_OVP)}$ $t_{delay(Fault\_OTP)}$	 22.5 22.5	 30.0 30.0	 37.5 37.5	µs
Overtemperature Protection (OTP) Threshold (Note 7)	V_{Fault} decreasing	8	$V_{Fault(OTP\_in)}$	0.38	0.40	0.42	V
Overtemperature Protection (OTP) Exiting Threshold (Note 7)	V_{Fault} increasing, Options B and D	8	$V_{Fault(OTP\_out)}$	0.874	0.920	0.966	V
OTP Pull−up Current Source (Note 7)	V_{Fault} = $V_{Fault(OTP\_in)}$ + 0.2 V T_J = 110°C	8	$I_{Fault(OTP)}$ $I_{Fault(OTP\_110)}$	42.5 −	45.5 45.5	48.5 −	µA
Fault Input Clamp Voltage	V_{Fault} = open	8	$V_{Fault(clamp)}$	1.5	1.75	2.0	V
Fault Input Clamp Series Resistor			$R_{Fault(clamp)}$	1.32	1.55	1.82	kΩ
POWER SAVINGS MODE							
PSM Enable Threshold	$V_{PSTimer}$ increasing	9	V_{PS_in}	3.325	3.500	3.675	V
PSM Disable Threshold	$V_{PSTimer}$ decreasing	9	V_{PS_out}	0.45	0.50	0.55	V
PSTimer Pull Up Current Sources	$V_{PSTimer}$ = 0.9 V $V_{PSTimer}$ = 3.4 V	9	$I_{PSTimer1}$ $I_{PSTimer2}$	9 800	10 1000	11 1200	µA
$I_{PSTimer2}$ Enable Threshold		9	$V_{PSTimer2}$	0.95	1.0	1.05	V
Filter Delay Before Entering PSM		9	$t_{delay(PS\_in)}$		40		µs
Startup Circuits Turn−on Thresholds in PSM	V_{HV_X2} increasing V_{BO_X2} increasing	1 3	$V_{HV\_X2(PS)}$ $V_{BO\_X2(PS)}$	20 20	30 30	40 40	V
PSTimer Discharge Current	$V_{PSTimer}$ = $V_{PSTimer(off)}$ + 10 mV	9	$I_{PSTimer(DIS)}$	200	−	−	µA
PSTimer Discharge Turn Off Threshold	$V_{PSTimer}$ decreasing	9	$V_{PSTimer(off)}$	50	100	150	mV
THERMAL PROTECTION							
Thermal Shutdown	Temperature increasing	N/A	T_{SHDN}		150		°C
Thermal Shutdown Hysteresis	Temperature decreasing	N/A	$T_{SHDN(HYS)}$		40		°C

7. NTC with R_{110} = 8.8 kΩ (TTC03−474)

DETAILED OPERATING DESCRIPTION

Introduction

The NCP1937 is a combination critical mode (CrM) power factor correction (PFC) and quasi−resonant (QR) flyback controller optimized for off−line adapter applications. This device includes all the features needed to implement a highly efficient adapter with extremely low input power in no−load conditions.

This device reduces standby input power by integrating an active input filter capacitor discharge circuit and disconnecting the PFC feedback resistor divider when the PFC is disabled.

High Voltage Startup Circuit

The NCP1937 integrates two high voltage startup circuits accessible by the HV_X2 and BO_X2 pins. The startup circuits are also used for input filter capacitor discharge. The BO_X2 input is also used for monitoring the ac line voltage and detecting brown−out faults. The startup circuits are rated at a maximum voltage of 700 V.

A startup regulator consists of a constant current source that supplies current from the ac input terminals (V_{in}) to the supply capacitor on the V_{CC} pin (C_{CC}). The startup circuit currents ($I_{start2A/B}$) are typically 3.75 mA. $I_{start2A/B}$ are disabled if the VCC pin is below $V_{CC(inhibit)}$. In this condition the startup current is reduced to $I_{start1A/B}$, typically 0.5 mA. The internal high voltage startup circuits eliminate the need for external startup components. In addition, these regulators reduce no load power and increase the system efficiency as they use negligible power in the normal operation mode.

Once C_{CC} is charged to the startup threshold, $V_{CC(on)}$, typically 17 V, the startup regulators are disabled and the controller is enabled. The startup regulators remain disabled until V_{CC} falls below the minimum operating voltage threshold, $V_{CC(off)}$, typically 8.8 V. Once reached, the PFC and flyback controllers are disabled reducing the bias current consumption of the IC. Both startup circuits are then enabled allowing V_{CC} to charge back up.

In power savings mode V_{CC} is regulated by enabling the startup circuits once the supply voltage decays below $V_{CC(PS\_on)}$, typically 11 V. The startup circuit is disabled once V_{CC} exceeds $V_{CC(PS\_on)}$. This provides enough headroom from $V_{CC(off)}$ to maintain a supply voltage and allow the controller to detect the line voltage removal in order to discharge the input filter capacitor(s). In this mode, the supply capacitor is charged by the startup circuit on the HV_X2 and BO_X2 pins once the voltage on these pin exceeds 30 V, typically. This reduces the average voltage during which the startup circuit is enabled reducing power consumption. Both startup circuits are enabled once the controller exits power savings mode in order to quickly charge V_{CC}. A new startup sequence commences once V_{CC} reaches $V_{CC(on)}$.

A dedicated comparator monitors V_{CC} when the QR stage is enabled and latches off the controller if V_{CC} exceeds $V_{CC(OVP)}$, typically 28 V.

The controller is disabled once a fault is detected. The controller will restart the next time V_{CC} reaches $V_{CC(on)}$ and all non−latching faults have been removed.

The supply capacitor provides power to the controller during power up. The capacitor must be sized such that a V_{CC} voltage greater than $V_{CC(off)}$ is maintained while the auxiliary supply voltage is building up. Otherwise, V_{CC} will collapse and the controller will turn off. The operating IC bias current, I_{CC4}, and gate charge load at the drive outputs must be considered to correctly size C_{CC}. The increase in current consumption due to external gate charge is calculated using Equation 1.

$$I_{CC(gate\ charge)} = f \cdot Q_G \qquad \text{(eq. 1)}$$

where f is the operating frequency and Q_G is the gate charge of the external MOSFETs.

Line Voltage Sense

The BO/X2 pin provides access to the brown−out and line voltage detectors. It also provides access to the input filter capacitor discharge circuit. The brown−out detector detects mains interruptions and the line voltage detector determines the presence of either 110 V or 220 V ac mains. Depending on the detected input voltage range device parameters are internally adjusted to optimize the system performance.

This pin connects to either line or neutral to achieve half−wave rectification as shown in Figure 3. A diode is used to prevent the pin from going below ground. A resistor in series with the BO/X2 pin can be used for protection, but a low value (< 3 kΩ) resistor should be used to reduce the voltage offset while sensing the line voltage.

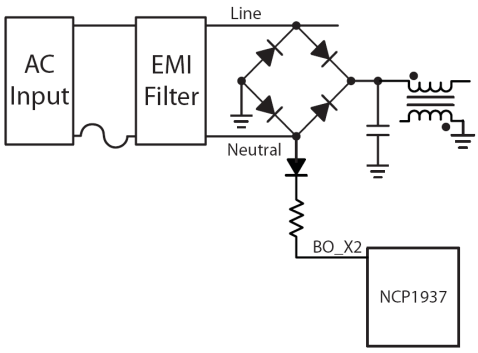

Figure 3. Brown−out and Line Voltage Detectors Configuration

The flyback stage is enabled once V_{BO_X2} is above the brown−out threshold, $V_{BO(start)}$, and V_{CC} reaches $V_{CC(on)}$. The high voltage startups are immediately enabled when the voltage on V_{BO_X2} crosses over the brown−out start threshold, $V_{BO(start)}$, to ensure that device is enabled quickly upon exiting a brown−out state. Figure 4 shows typical power up waveforms.

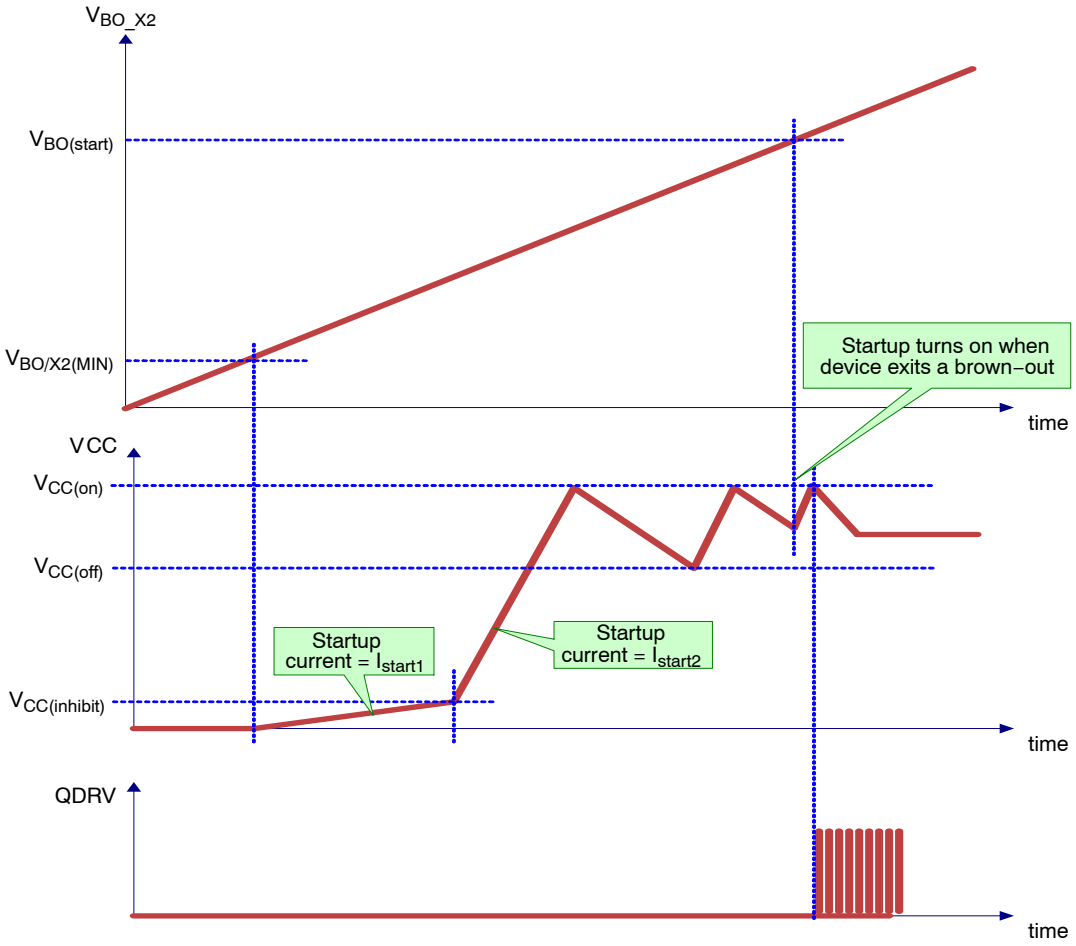

Figure 4. Startup Timing Diagram

A timer is enabled once V_{BO_X2} drops below its stop threshold, $V_{BO(stop)}$. If the timer, t_{BO}, expires the device will begin monitoring the voltage on V_{BO_X2} and disable the PFC and flyback stages when that voltage is below the Brown−out Drive Disable threshold, $V_{BO(DRV\_disable)}$, typically 30 V. This ensures that device switching is stopped in a low energy state which minimizes inductive voltage kick from the EMI components and ac mains. The timer, t_{BO}, typically 54 ms, is set long enough to ignore a single cycle drop−out.

Line Voltage Detector

The input voltage range is detected based on the peak voltage measured at the BO_X2 pin. Discrete values are selected for the PFC stage gain (feedforward) depending on the input voltage range. The controller compares V_{BO_X2} to an internal line select threshold, $V_{BO(lineselect)}$. Once V_{BO_X2} exceeds $V_{BO(lineselect)}$, the PFC stage operates in "high line" (Europe/Asia) or "220 Vac" mode. In high line mode the maximum on time is reduced by a factor of 3, resulting in a maximum output power independent of input voltage.

Figure 5 shows typical operation for the line voltage detector. The default power−up mode of the controller is low line. The controller switches to "high line" mode if V_{BO_X2} exceeds the line select threshold for longer than the low to high line timer, $t_{(low\ to\ high\ line)}$, typically 300 μs, as long as it was not previously in high line mode. If the controller has switched from "high line" to "low line" mode, the low to high line timer, $t_{(low\ to\ high\ line)}$, is inhibited until $V_{BO/X2}$ falls below $V_{BO(stop)}$. This prevents the controller from toggling back to "high line" until at least one $V_{BO(stop)}$ transition has occurred. The timer and logic is included to prevent unwanted noise from toggling the operating line level.

In "high line" mode the high to low line timer, $t_{(high\ to\ low\ line)}$, (typically 54 ms) is enabled once V_{BO_X2} falls below $V_{BO(lineselect)}$. It is reset once V_{BO_X2} exceeds $V_{BO(lineselect)}$. The controller switches back to "low line" mode if the high to low line timer expires.

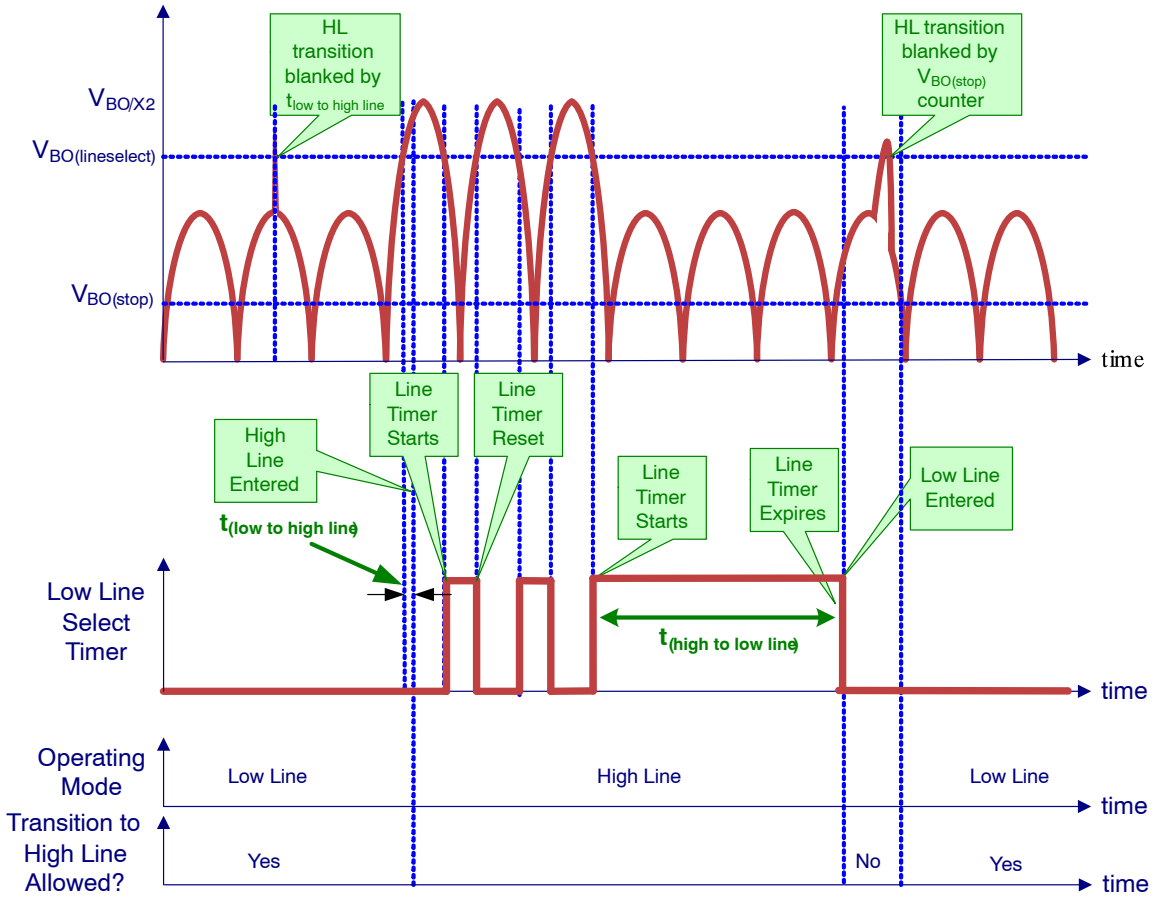

Figure 5. Line Detector Waveforms

Input Filter Capacitor Discharge

Safety agency standards require the input filter capacitors to be discharged once the ac line voltage is removed. A resistor network is the most common method to meet this requirement. Unfortunately, the resistor network consumes power across all operating modes and is a major contributor to the total input power dissipation during light−load and no−load conditions.

The NCP1937 eliminates the need for external discharge resistors by integrating active input filter capacitor discharge circuitry. A novel approach is used to reconfigure the high voltage startup circuits to discharge the input filter capacitors upon removal of the ac line voltage.

Once the controller detects the absence of the ac line voltage, the controller is disabled and V_{CC} is discharged by a current source, $I_{CC(discharge)}$, typically 11.5 mA. This will cause V_{CC} to fall down to $V_{CC(off)}$. Upon reaching $V_{CC(off)}$, both startup circuits are enabled. The startup circuits will then source current from the BO_X2 and HV_X2 inputs to the VCC pin and discharge the input filter capacitors by transferring its charge to the V_{CC} capacitor(s). The input filter capacitor(s) are typically discharged once the startup circuit turns on the 1st time because the energy stored in the input filter capacitor(s) is significantly lower than the energy needed to charge the V_{CC} capacitor from $V_{CC(off)}$ to $V_{CC(on)}$. After the initial discharge the controller enters a low current mode (I_{CC2}) once V_{CC} drops to $V_{CC(off)}$.

In the event that the input filter capacitor is not fully discharged, a larger V_{CC} capacitor should be used. But, this is not a concern for most applications because the supply capacitor value will be large enough to maintain V_{CC} during skip operation. Figure 6 shows typical behavior of the filter capacitor discharge when the ac line is removed.

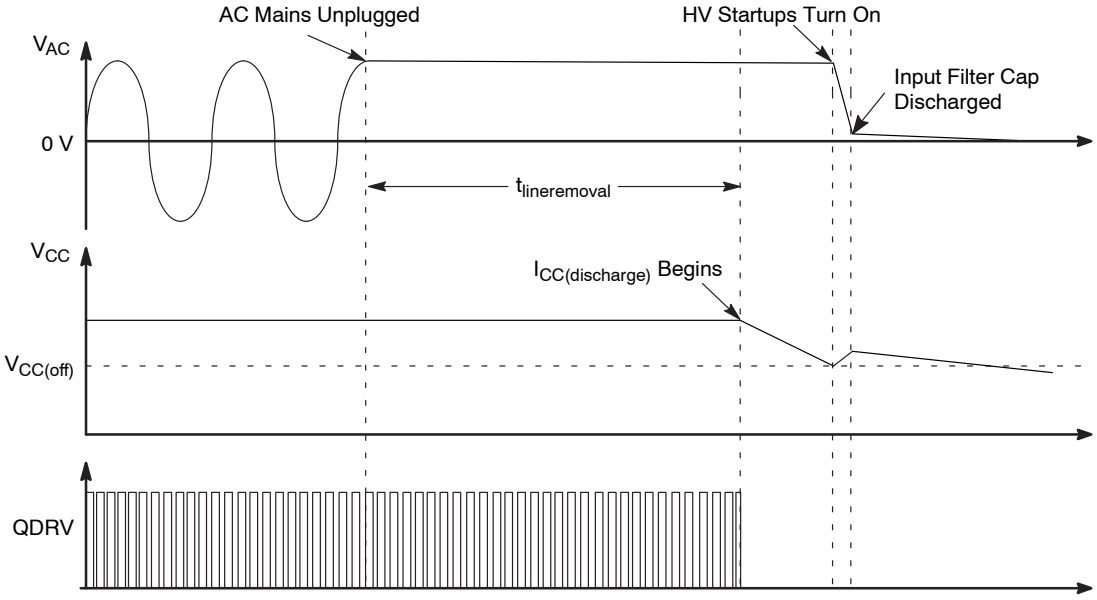

Figure 6. Input Filter Capacitor Discharge Waveforms

The diode connecting the AC line to the BO_X2 pin should be placed after the system fuse. A resistor in series with the BO_X2 pin is recommended to limit the current during transient events. A low value resistor (< 3 kΩ) should be used to reduce the voltage drop when the startup circuit is enabled.

Power Savings Mode

The NCP1937 has a low current consumption mode known as power savings mode (PSM). The supply current consumption in this mode is below 70 μA. PSM operation is controlled by an external control signal. This signal is typically generated on the secondary side of the power supply and fed via an optocoupler.

The NCP1937 is configured as active on logic, that is it enters PSM in the absence of the control signal. The control signal is applied to the PSTimer pin. The block diagram for NCP1937 PSTimer pin is shown in Figure 7. Power savings mode operating waveforms for the NCP1937 are shown in Figure 8.

The NCP1937 controller starts once V_{CC} reaches $V_{CC(on)}$ and no faults are present. At this time the current source on the PSTimer pin, $I_{PSTimer1}$, is enabled. $I_{PSTimer1}$ is typically 10 μA. The current source charges the capacitor connected from this pin to ground. Once $V_{PSTimer}$ reaches $V_{PSTimer2}$ a 2nd current source, $I_{PSTimer2}$, is enabled to speed up the charge of C_{PSM}. $V_{PSTimer2}$ and $I_{PSTimer2}$ are typically 1 V and 1 mA, respectively. The controller enters PSM if the voltage on $V_{PSTimer}$ exceeds V_{PS_in}, typically 3.5 V. An external optocoupler or switch needs to pull down on this pin before its voltage reaches V_{PS_in} to prevent entering PSM. Once the controller enters PSM, $I_{PSTimer1/2}$ is disabled. A resistor between this pin and ground discharges the PSTimer capacitor. The controller exits PSM once $V_{PSTimer}$ drops below V_{PS_out}, typically 0.5 V. Once the QR stage is enabled, the capacitor on the PSTimer pin is discharged with an internal pull down transistor. The transistor is disabled once $V_{PSTimer}$ falls below its minimum operating level, $V_{PSTimer(MIN)}$ (maximum of 50 mV). The time to enter PSM mode is calculated using Equations 2 through 4. The time to exit PSM mode is calculated using Equation 5.

$$t_{PSM(in)} = t_{PSM(in1)} + t_{PSM(in2)} \quad \text{(eq. 2)}$$

$$t_{PSM(in1)} = -R_{PSM}C_{PSM} \cdot \ln\left(1 - \frac{V_{PSTimer2}}{I_{PSTimer1} \cdot R_{PSM}}\right) \quad \text{(eq. 3)}$$

$$t_{PSM(in2)} \approx -R_{PSM}C_{PSM} \cdot \ln\left(1 - \frac{V_{PS\_in} - V_{PSTimer2}}{I_{PSTimer2} \cdot R_{PSM}}\right) \quad \text{(eq. 4)}$$

$$t_{PSM(out)} = -R_{PSM}C_{PSM} \cdot \ln\left(\frac{V_{PS\_out}}{V_{PS\_in}}\right) \quad \text{(eq. 5)}$$

In PSM the startup circuits on the HV_X2 and BO_X2 pins work to maintain V_{CC} above $V_{CC(off)}$. The input filter capacitor discharge circuitry continues operation in PSM. The supply voltage is maintained in PSM by enabling one of the startup circuits once V_{CC} falls below $V_{CC(PS\_on)}$ (typically 11 V) and either V_{HV_X2} exceeds $V_{HV\_X2(PS)}$ or V_{BO_X2} exceeds $V_{BO\_X2(PS)}$ (typically 30 V). The startup circuit is disabled once V_{CC} exceeds $V_{CC(PS\_on)}$. A voltage offset is observed on V_{CC} while the startup circuit is enabled due to the capacitor ESR. This will cause the startup circuit to turn off because V_{CC} exceeds $V_{CC(PS\_on)}$. Internal circuitry prevents the startup circuit from turning on multiple times during the same ac line half−cycle. The complementary startup circuit will then turn on during the next half−cycle. Eventually, V_{CC} will be regulated several millivolts below $V_{CC(PS\_on)}$. The offset is dependent on the capacitor ESR.

This architecture enables the startup circuit for the exact amount of time needed to regulate V_{CC}. This results in a significant reduction in power dissipation because the average input voltage is greatly reduced.

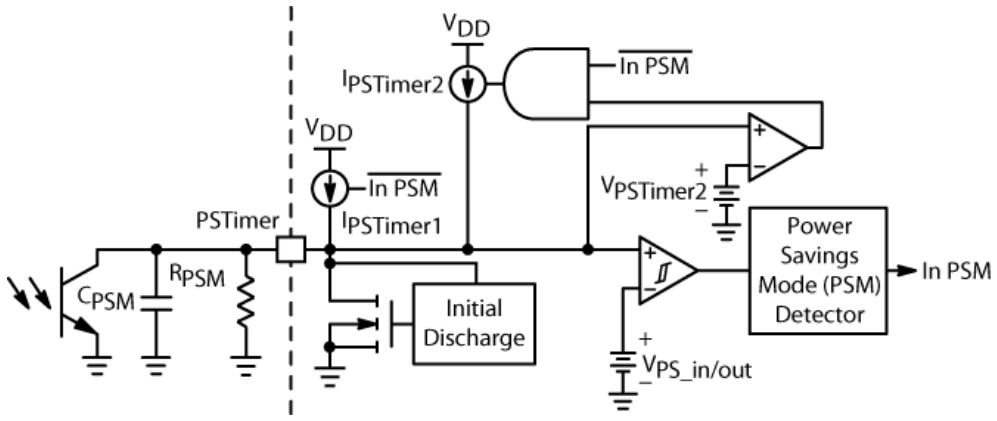

Figure 7. NCP1937 Power Savings Mode Control Block Diagram

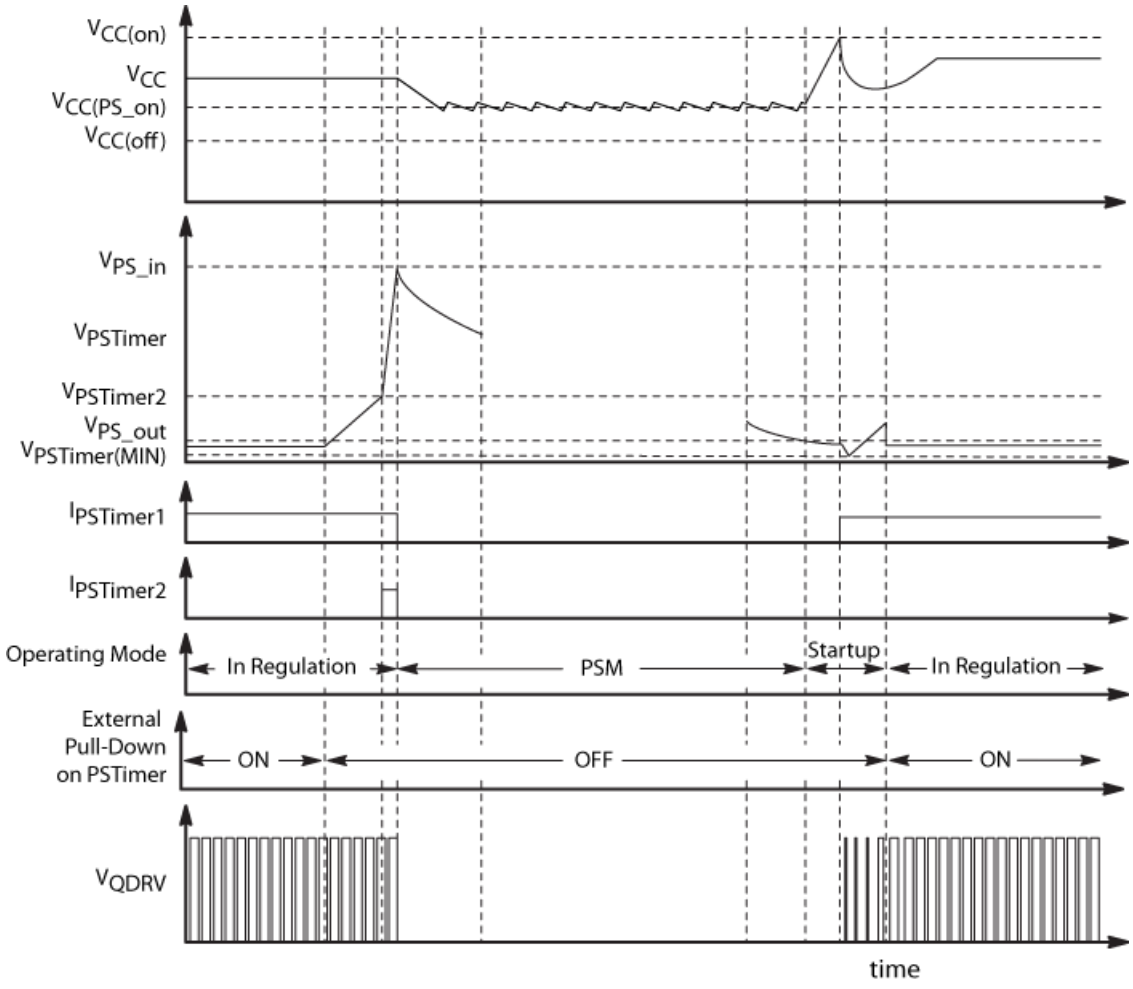

Figure 8. NCP1937 Power Savings Mode Operating Waveforms

Fault Input

The NCP1937 includes a dedicated fault input accessible via the Fault pin. The controller can be latched by pulling the pin above the upper fault threshold, $V_{Fault(OVP)}$, typically 3.0 V. The controller is disabled if the Fault pin voltage, V_{Fault}, is pulled below the lower fault threshold, $V_{Fault(OTP\_in)}$, typically 0.4 V. The lower threshold is normally used for detecting an overtemperature fault. The controller operates normally while the Fault pin voltage is maintained within the upper and lower fault thresholds. Figure 9 shows the architecture of the Fault input.

The lower fault threshold is intended to be used to detect an overtemperature fault using an NTC thermistor. A pull up current source $I_{Fault(OTP)}$, (typically 45.5 μA) generates a voltage drop across the thermistor. The resistance of the NTC thermistor decreases at higher temperatures resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below $V_{Fault(OTP\_in)}$. Options A and C latch−off the controller after an overtemperature fault is detected. In Options B and D the controller is re−enabled once the fault is removed such that V_{Fault} increases above $V_{Fault(OTP\_out)}$ and V_{CC} reaches $V_{CC(on)}$. Figure 10 shows typical waveforms related to the latch option whereas Figure 11 shows waveforms of the auto−recovery option.

An active clamp prevents the Fault pin voltage from reaching the upper latch threshold if the pin is open. To reach the upper threshold, the external pull−up current has to be higher than the pull−down capability of the clamp (set by $R_{Fault(clamp)}$ at $V_{Fault(clamp)}$). The upper fault threshold is intended to be used for an overvoltage fault using a Zener diode and a resistor in series from the auxiliary winding voltage, V_{AUX}. The controller is latched once V_{Fault} exceeds $V_{Fault(OVP)}$.

The Fault input signal is filtered to prevent noise from triggering the fault detectors. Upper and lower fault detector blanking delays, $t_{delay(Fault\_OVP)}$ and $t_{delay(Fault\_OTP)}$ are both typically 30 μs. A fault is detected if the fault condition is asserted for a period longer than the blanking delay.

A bypass capacitor is usually connected between the Fault and GND pins and it will take some time for V_{Fault} to reach its steady state value once $I_{Fault(OTP)}$ is enabled. Therefore, a lower fault (i.e. overtemperature) is ignored during soft−start. In Options B and D, $I_{Fault(OTP)}$ remains enabled while the lower fault is present independent of V_{CC} in order to provide temperature hysteresis. The controller can detect an upper OVP fault once V_{CC} exceeds $V_{CC(reset)}$. The OVP fault detection remains active provided the device is not in PSM.

Once the controller is latched, it is reset if a brown−out condition is detected or if V_{CC} is cycled down to its reset level, $V_{CC(reset)}$. In the typical application these conditions occur only if the ac voltage is removed from the system. Prior to reaching $V_{CC(reset)}$, $V_{fault(clamp)}$ is set at 0 V.

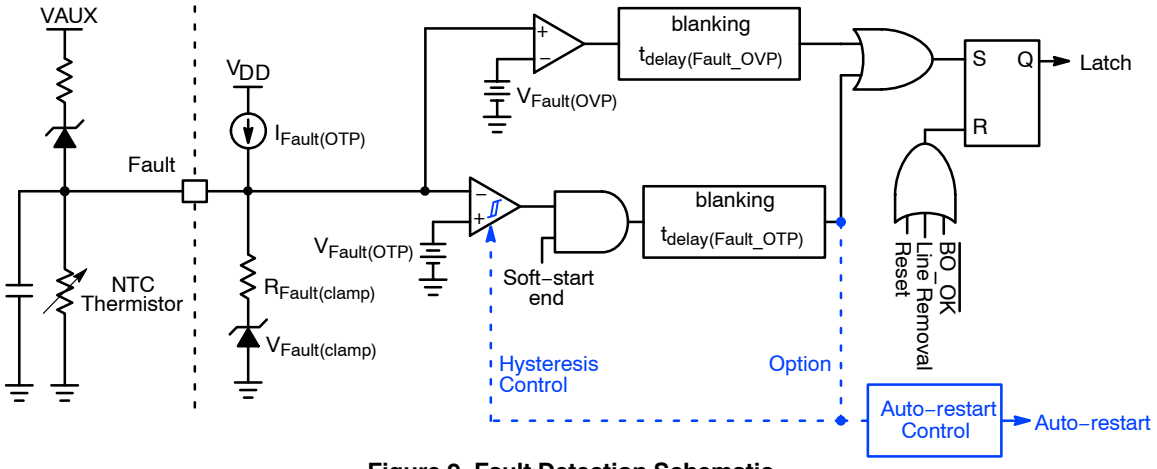

Figure 9. Fault Detection Schematic

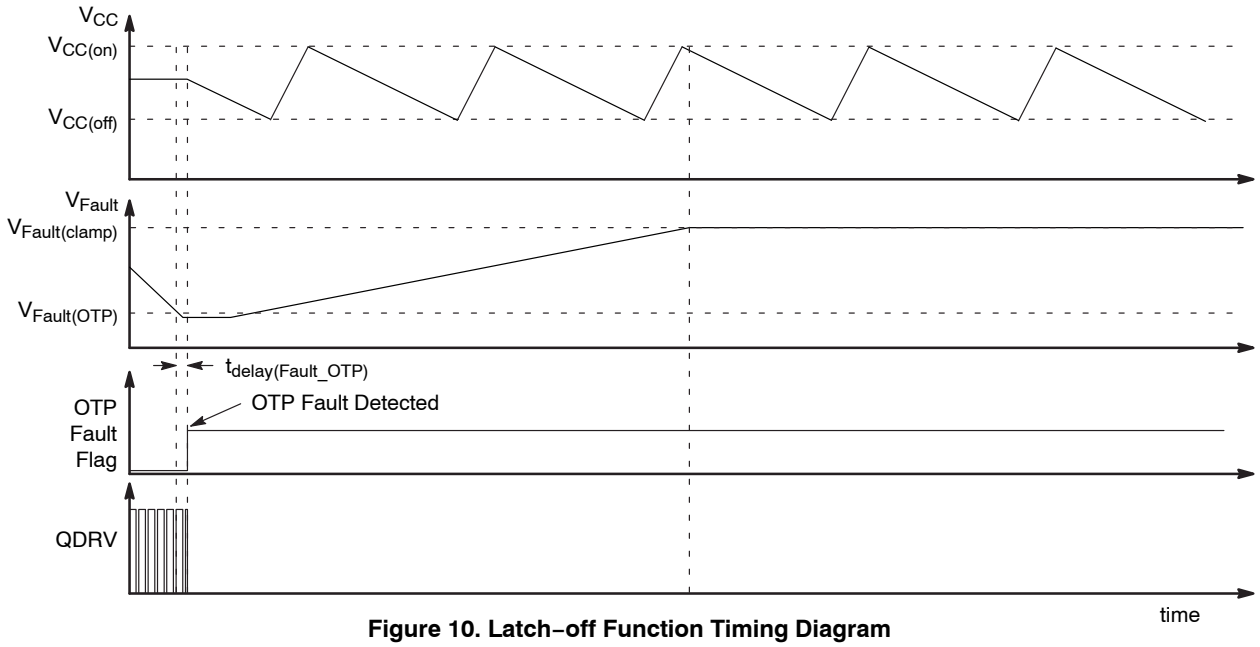

Figure 10. Latch−off Function Timing Diagram

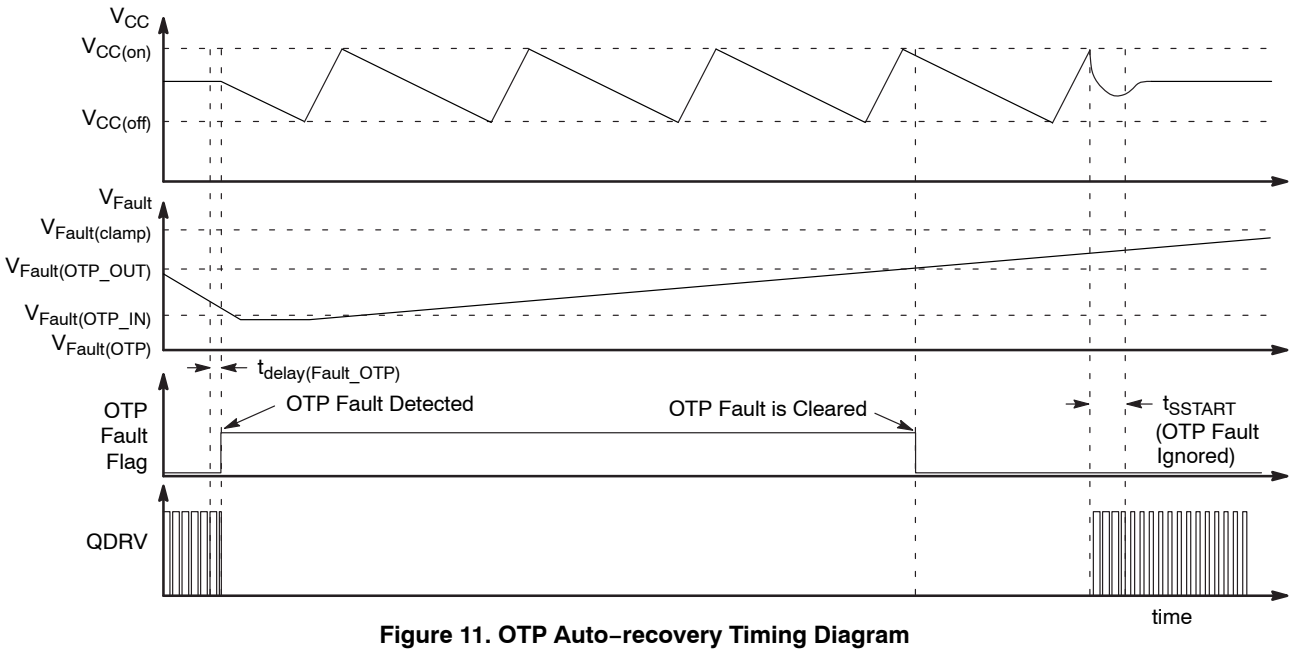

Figure 11. OTP Auto−recovery Timing Diagram

QR Flyback Valley Lockout

The NCP1937 integrates a quasi−resonant (QR) flyback controller. The power switch turn−off of a QR converter is determined by the peak current set by the feedback loop. The switch turn−on is determined by the transformer demagnetization. The demagnetization is detected by monitoring the transformer auxiliary winding voltage.

Turning on the power switch once the transformer is demagnetized or reset reduces switching losses. Once the transformer is demagnetized, the drain voltage starts ringing at a frequency determined by the transformer magnetizing inductance and the drain lump capacitance eventually settling at the input voltage. A QR controller takes advantage of the drain voltage ringing and turns on the power switch at the drain voltage minimum or “valley” to reduce switching losses and electromagnetic interference (EMI).

The operating frequency of a traditional QR flyback controller is inversely proportional to the system load. That is, a load reduction increases the operating frequency. This tradionally requires a maximum frequency clamp to limit the operating frequency. This causes the controller to become unstable and jump (or hesitate) between two valleys generating audible noise. The NCP1937 incorporates a patent pending valley lockout circuitry to eliminate valley jumping. Once a valley is selected, the controller stays locked in this valley until the output power changes significantly. Like a traditional QR flyback controller, the frequency increases when the load decreases. Once a higher valley is selected the frequency decreases very rapidly. It will continue to increase if the load is further reduced. This technique extends QR operation over a wider output power range while maintaining good efficiency and limiting the maximum operating frequency. Figure 12 shows a qualitative frequency vs output power relationship.

Figure 13 shows the internal arrangement of the valley lockout circuitry. The decimal counter increases each time a valley is detected. The operating valley (1^{st}, 2^{nd}, 3^{rd} or 4^{th}) is determined by the QFB voltage. As V_{QFB} decreases or increases, the valley comparators toggle one after another to select the proper valley. The activation of an “n” valley comparator blanks the “n−1” or “n+1” valley comparator output depending if V_{QFB} decreases or increases, respectively.

A valley is detected once V_{QZCD} falls below the QR flyback demagnetization threshold, $V_{QZCD(th)}$, typically 55 mV. The controller will switch once the valley is detected or increment the valley counter depending on QFB voltage.

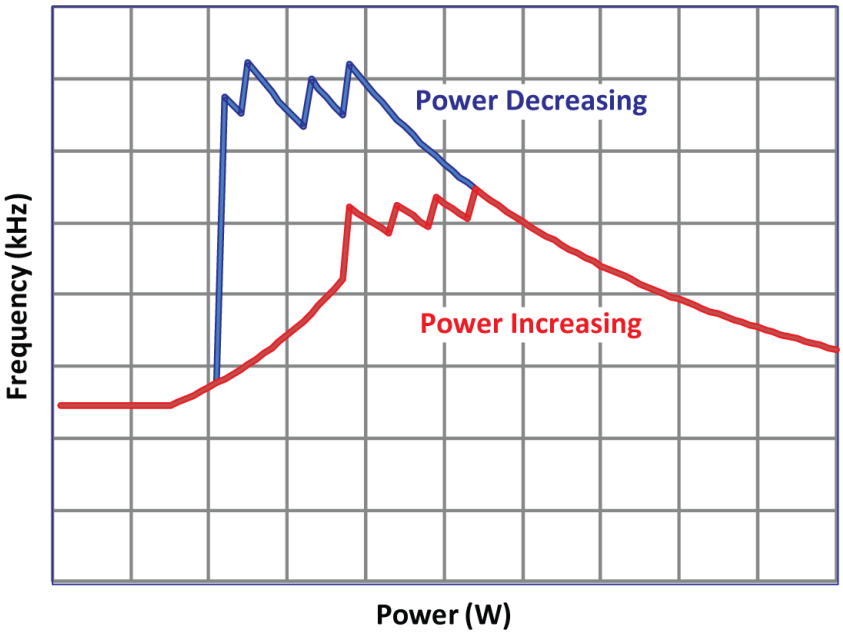

Figure 12. Valley Lockout Frequency vs. Output Power Relationship

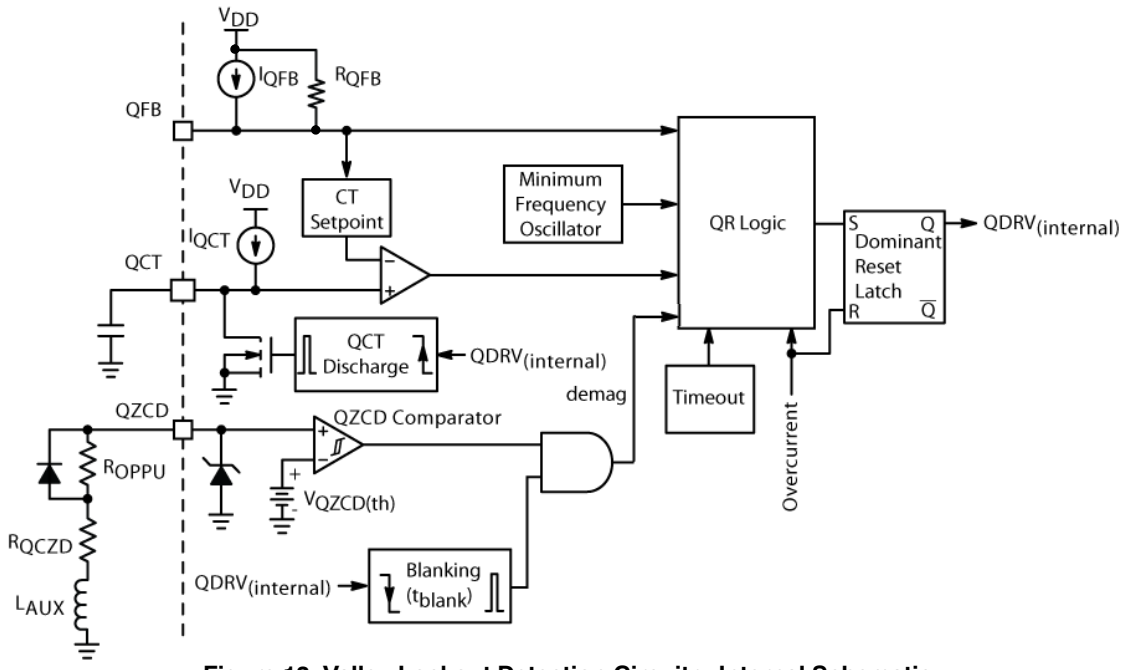

Figure 13. Valley Lockout Detection Circuitry Internal Schematic

Figure 14 shows the operating valley versus V_{QFB}. Once a valley is asserted by the valley selection circuitry, the controller is locked in this valley until V_{QFB} decreases or increases such that V_{QFB} reaches the next valley threshold. A decrease in output power causes the controller to switch from "n" to "n+1" valley until reaching the 4th valley.

A further reduction of output power causes the controller to enter the voltage control oscillator (VCO) mode once V_{QFB} falls below V_{HVCOD}. In VCO mode the peak current is set as shown in Figure 15. The operating frequency in VCO mode is adjusted to deliver the required output power.

A hysteresis between valleys provides noise immunity and helps stabilize the valley selection in case of small perturbations on V_{QFB}.

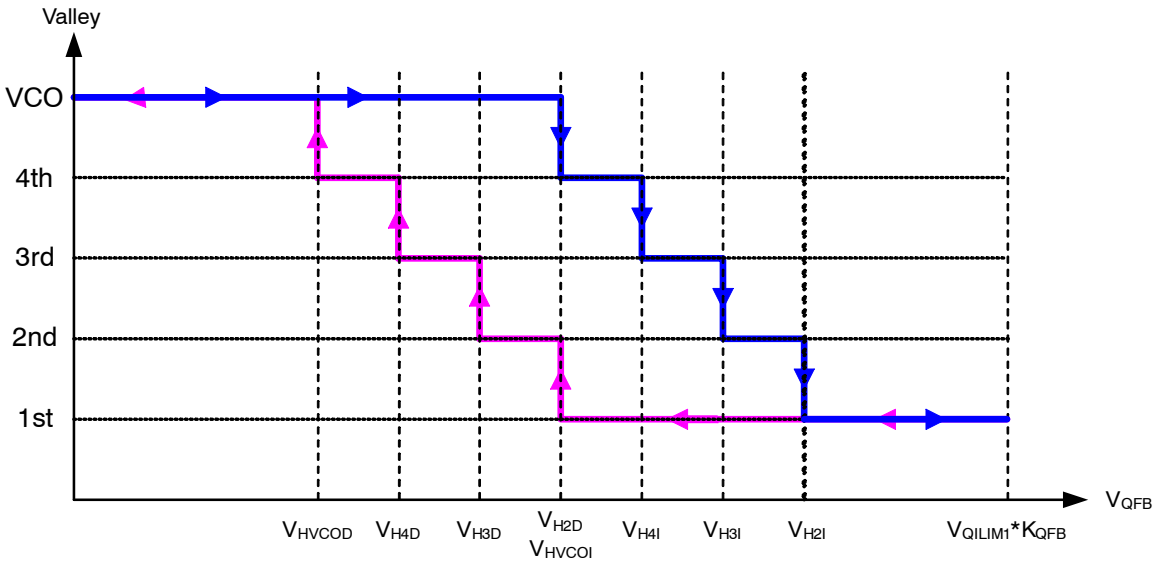

Figure 14. Selected Operating Valley vs. V_{QFB}

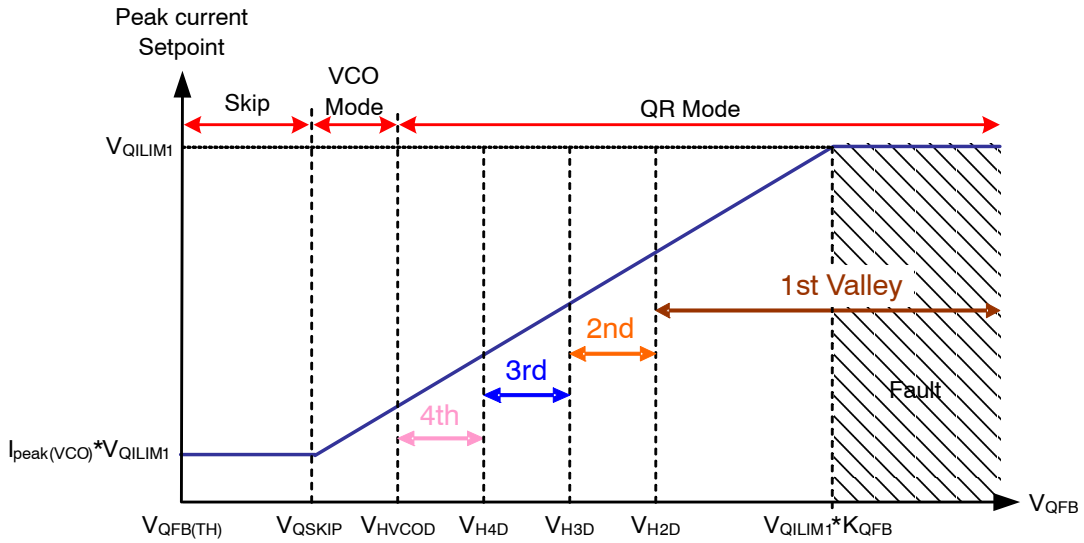

Figure 15. Operating Valley vs. V_{QFB}

Figure 16 through Figure 19 show drain voltage, V_{QFB} and V_{QCT} simulation waveforms for a reduction in output power. The transitions between 2nd to 3rd, 3rd to 4th and 4th valley to VCO mode are observed without any instabilities or valley jumping.

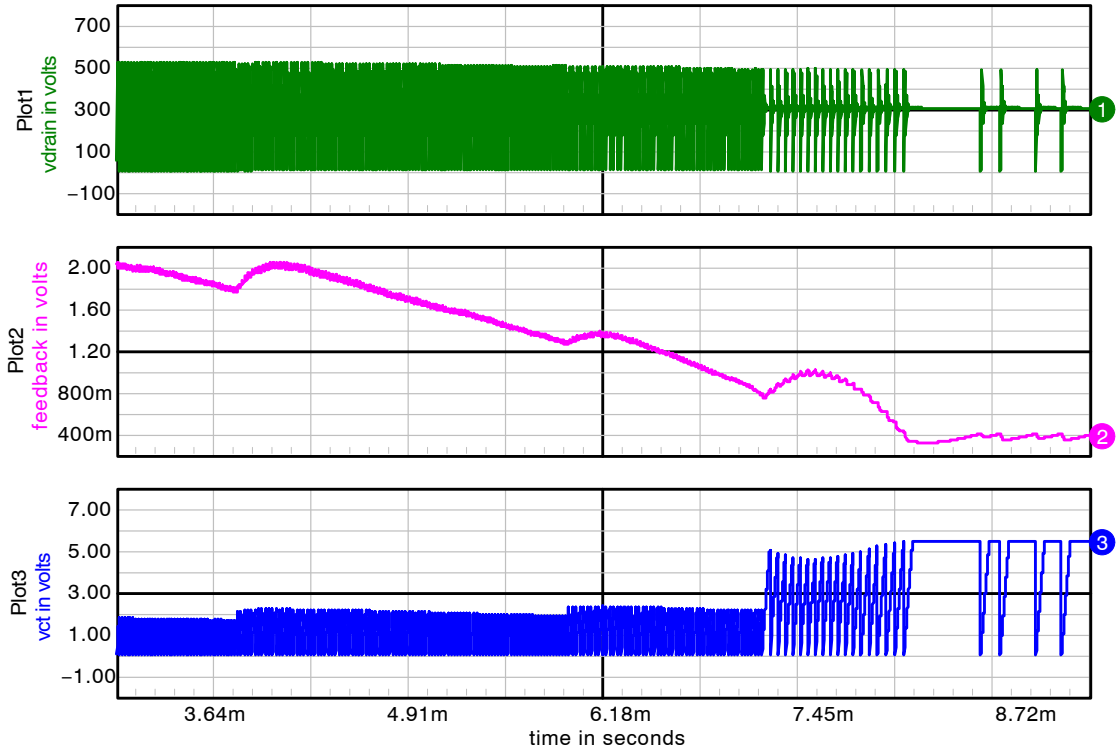

Figure 16. Operating Mode Transitions between 2nd to 3rd, 3rd to 4th and 4th Valley to VCO Mode

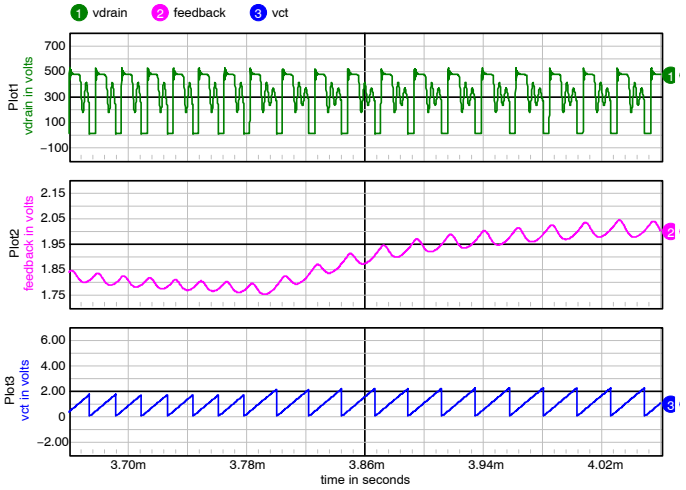

Figure 17. Zoom 1: 2nd to 3rd Valley Transition

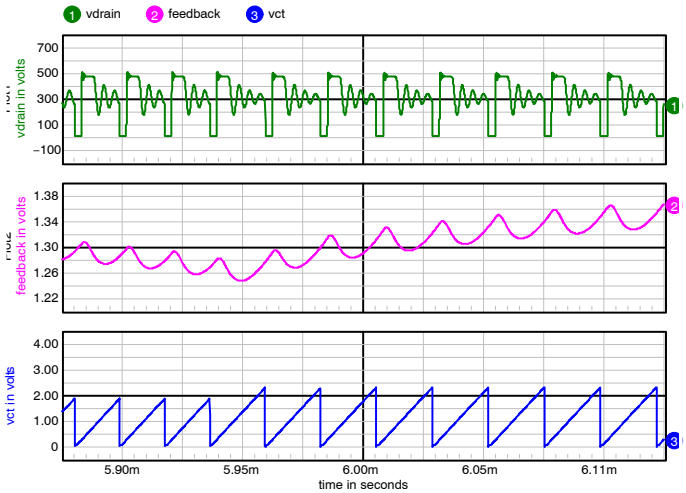

Figure 18. Zoom 2: 3rd to 4th Valley Transition

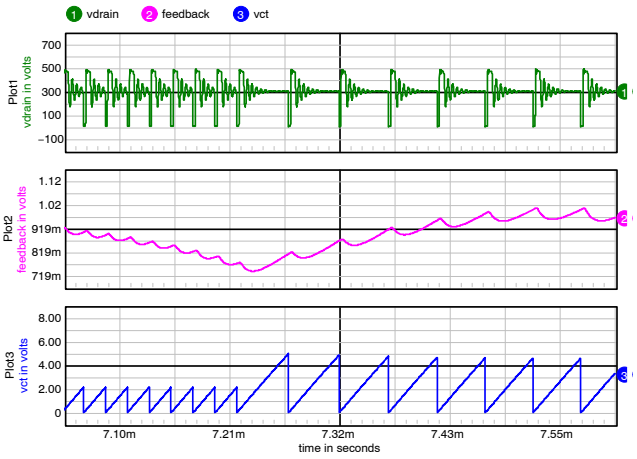

Figure 19. Zoom 3: 4th Valley to VCO Mode Transition

VCO Mode

The controller enters VCO mode once V_{QFB} falls below V_{HVCOD} and remains in VCO until V_{QFB} exceeds V_{HVCOI}. In VCO mode the peak current is set to V_{QILIM1}*$I_{peak(VCO)}$ and the operating frequency is linearly dependent on V_{QFB}. The product of V_{QILIM1}*$I_{peak(VCO)}$ is typically 12.5%. A minimum frequency clamp, $f_{VCO(MIN)}$, typically 27 kHz, prevents operation in the audible range. Further reduction in output power causes the controller to enter skip operation. The minimum frequency clamp is only enabled when operating in VCO mode.

The VCO mode operating frequency is set by the timing capacitor connected between the QCT and GND pins. This capacitor is charged with a constant current source, I_{QCT}, typically 20 μA.

The capacitor voltage, V_{QCT}, is compared to an internal voltage level, $V_{f(QFB)}$, inversely proportional to V_{QFB} The relationship between and $V_{f(QFB)}$ and V_{QFB} is given by Equation 6.

$$V_{f(QFB)} = 5 - 2 \cdot V_{QFB} \qquad \text{(eq. 6)}$$

A drive pulse is generated once V_{QCT} exceeds $V_{f(QFB)}$ followed by the immediate discharge of the timing capacitor. The timing capacitor is also discharged once the minimum frequency clamp is reached.

Figure 20 shows simulation waveforms of $V_{f(QFB)}$, V_{QDRV} and output current while operating in VCO mode.

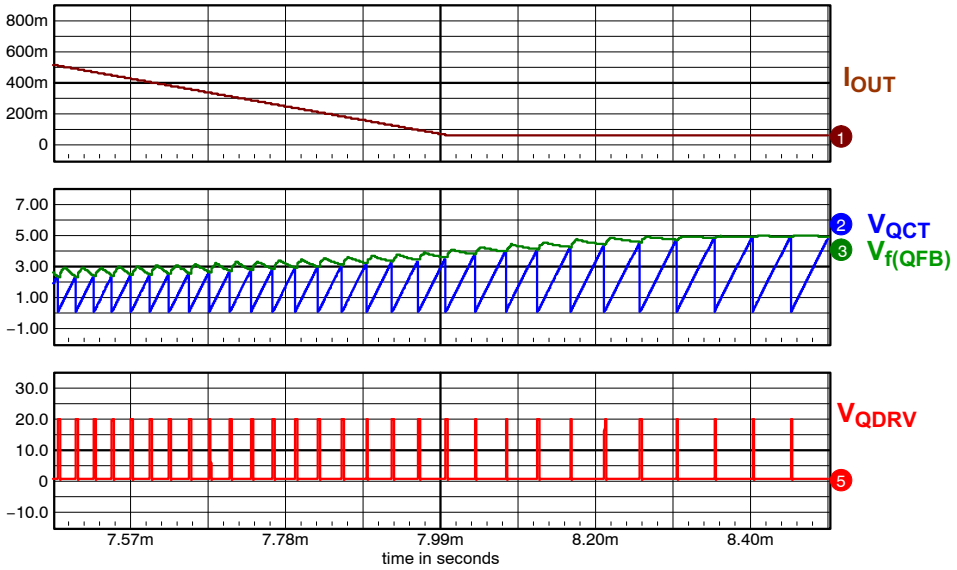

Figure 20. VCO Mode Operating Waveforms

Flyback Timeout

In case of extremely damped oscillations, the QZCD comparator may be unable to detect the valleys. In this condition, drive pulses will stop waiting for the next valley or ZCD event. The NCP1937 ensures continued operation by incorporating a maximum timeout period after the last demagnetization detection. The timeout signal is a substitute for the ZCD signal for the valley counter. Figure 21 shows the timeout period generator circuit schematic. The steady state timeout period, $t_{Q(tout2)}$, is set at 6 μs to limit the frequency step.

During startup, the voltage offset added by the overpower compensation diode, D_{OPP}, prevents the QZCD Comparator from accurately detecting the valleys. In this condition, the steady state timeout period will be shorter than the inductor demagnetization period causing continuous current mode (CCM) operation. CCM operation lasts for a few cycles until the voltage on the QZCD pin is high enough to detect the valleys. A longer timeout period, $t_{Q(tout1)}$, (typically 100 μs) is set during soft−start to limit CCM operation. Figure 22 and Figure 23 show the timeout period generator related waveforms.

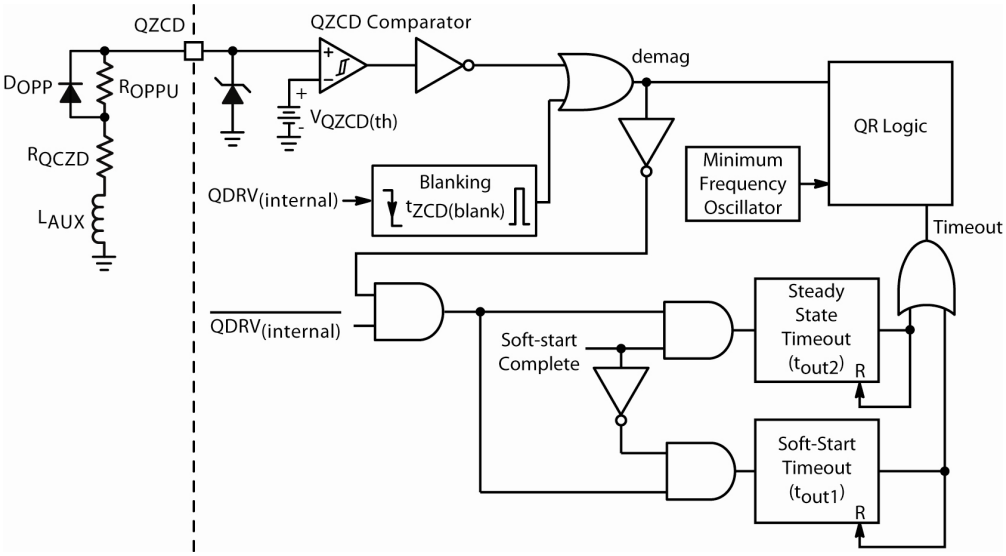

Figure 21. Timeout Period Generator Circuit Schematic

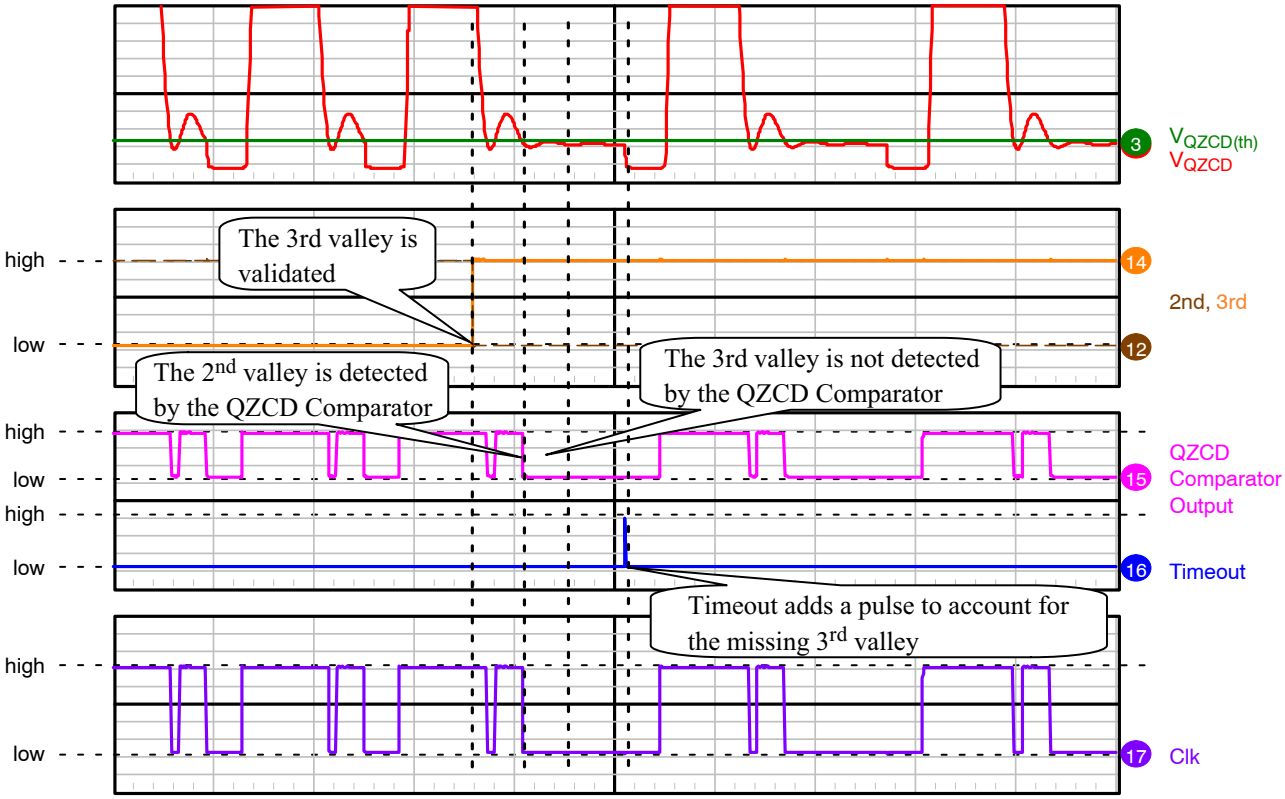

Figure 22. Timeout Operation with a Missing 3rd Valley

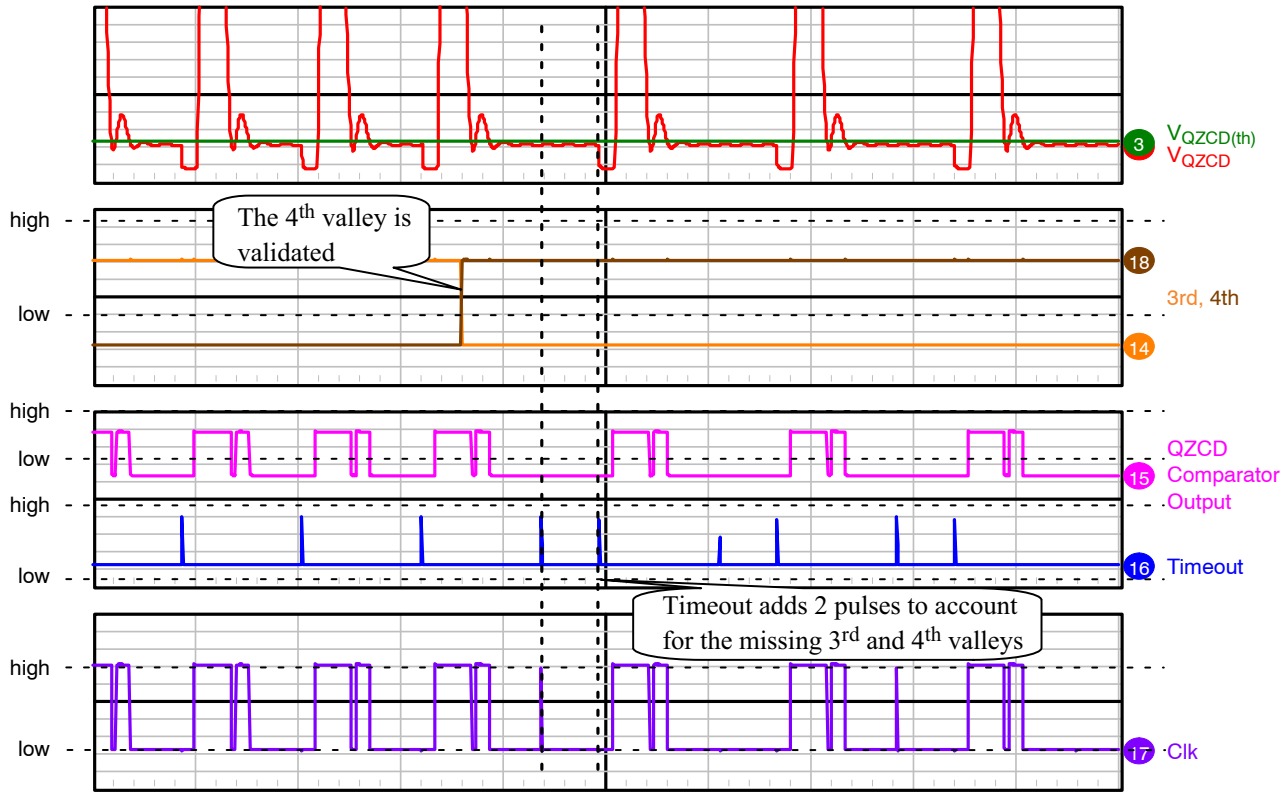

Figure 23. Timeout Operation with Missing 3rd and 4th Valleys

QR Flyback Current Sense and Overload

The power switch on time is modulated by comparing a ramp proportional to the switch current to V_{QFB}/K_{QFB} using the PWM Comparator. The switch current is sensed across a current sense resistor, $R_{SENSE,}$ and the resulting voltage is applied to the QCS pin. The current signal is blanked by a leading edge blanking (LEB) circuit. The blanking period eliminates the leading edge spike and high frequency noise during the switch turn−on event. The LEB period, $t_{QCS(LEB1)}$, is typically 275 ns. The drive pulse terminates once the current sense signal exceeds V_{QFB}/K_{QFB}.

The Maximum Peak Current Comparator compares the current sense signal to a reference voltage to limit the maximum peak current of the system. The maximum peak current reference voltage, V_{QILIM1}, is typically 0.8 V. The maximum peak current setpoint is reduced by the overpower compensation circuitry. An overload condition causes the output of the Maximum Peak Current Comparator to transition high and enable the overload timer. Figure 24 shows the implementation of the current sensing circuitry.

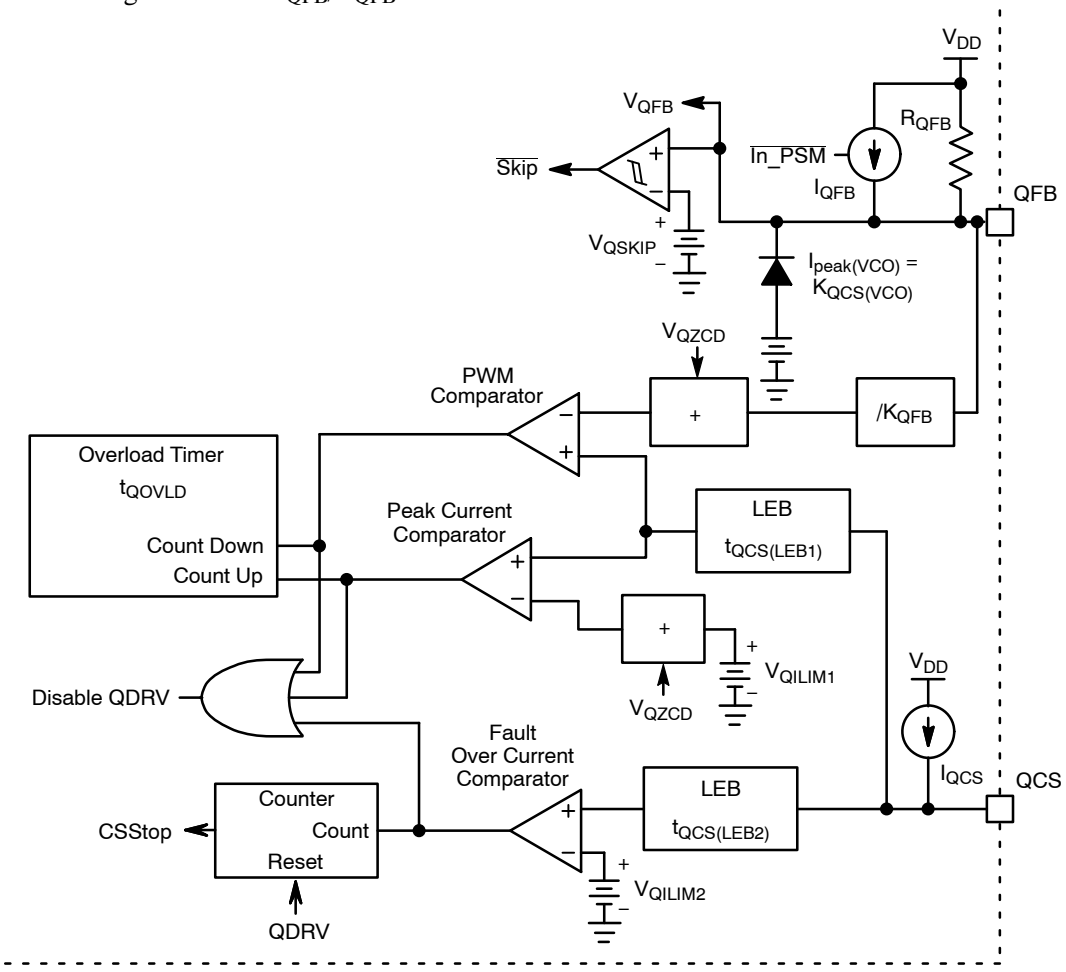

Figure 24. Current Sensing Circuitry Schematic

The overload timer integrates the duration of the overload fault. That is, the timer count increases while the fault is present and reduces its count once it is removed. The overload timer duration, t_{QOVLD}, is typically 80 ms. If both the PWM and Maximum Peak Current Comparators toggle at the same time, the PWM Comparator takes precedence and the overload timer counts down. The controller can latch (options C and D) or allow for auto−recovery (options A and B) once the overload timer expires. Auto−recovery requires a V_{CC} triple hiccup before the controller restarts. Figure 25 and Figure 26 show operating waveforms for latched and auto−recovery overload conditions.

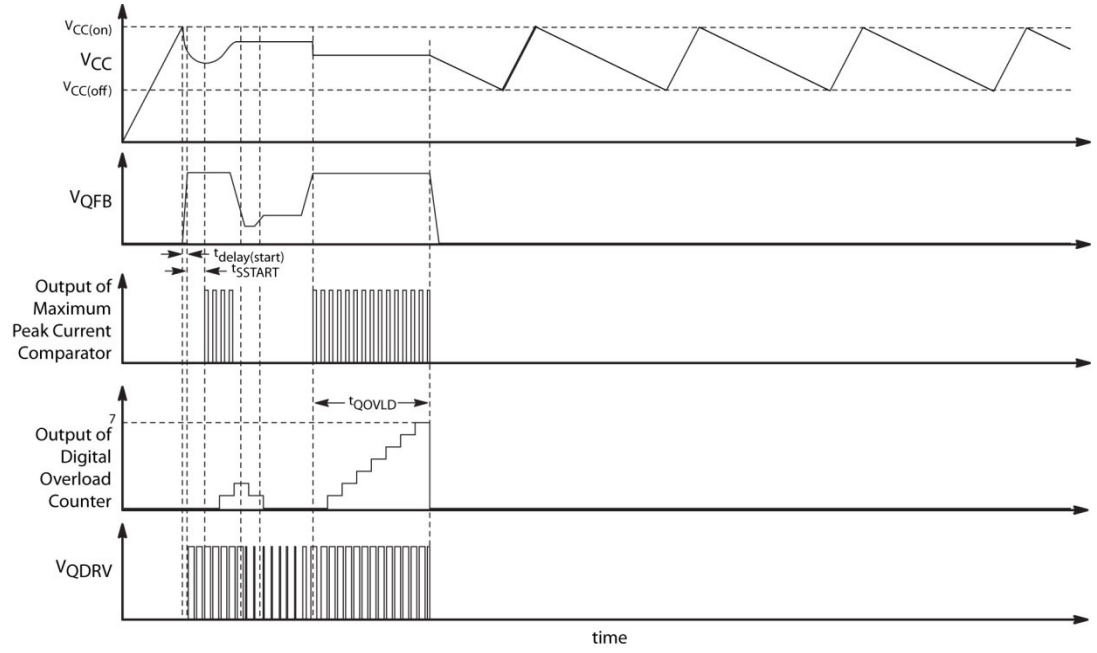

Figure 25. Latched Overload Operation

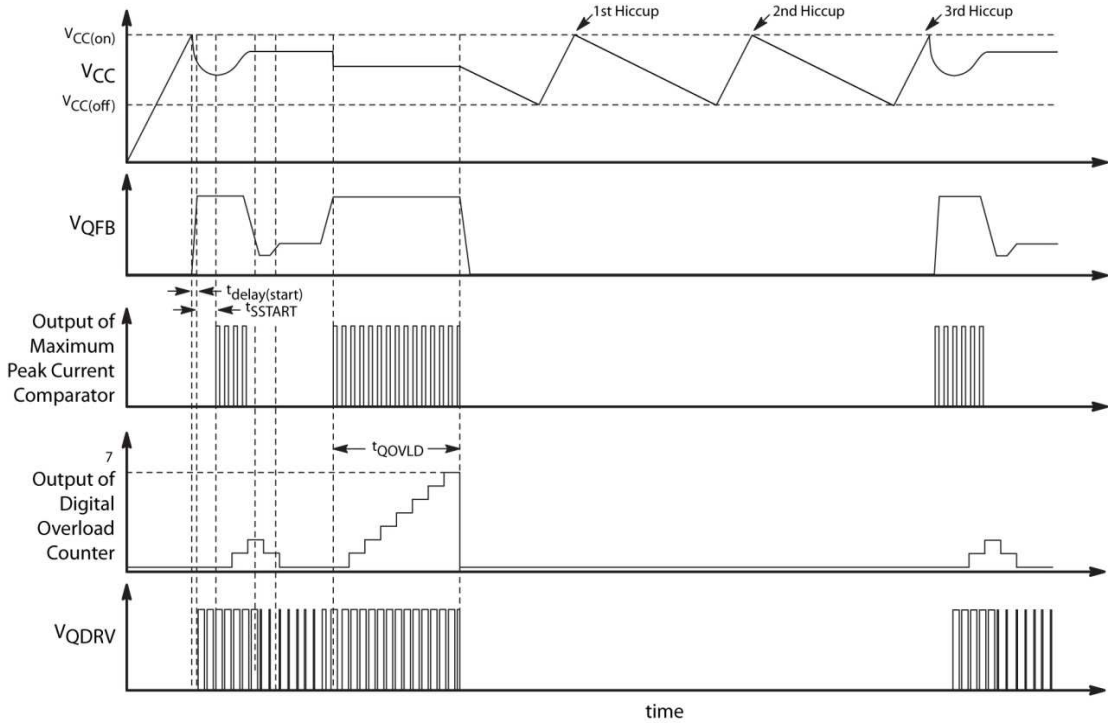

Figure 26. Auto−recovery Overload Operation

A severe overload fault like a secondary side winding short−circuit causes the switch current to increase very rapidly during the on−time. The current sense signal significantly exceeds V_{QILIM1}. But, because the current sense signal is blanked by the LEB circuit during the switch turn on, the system current can get extremely high causing system damage.

The NCP1937 protects against this fault by adding an additional comparator, Fault Overcurrent Comparator. The current sense signal is blanked with a shorter LEB duration, $t_{QCS(LEB2)}$, typically 120 ns, before applying it to the Fault Overcurrent Comparator. The voltage threshold of the comparator, V_{QILIM2}, typically 1.2 V, is set 50% higher than V_{QILIM1}, to avoid interference with normal operation. Four consecutive faults detected by the Fault Overcurrent Comparator causes the controller to enter latch mode. The count to 4 provides noise immunity during surge testing. The counter is reset each time a QDRV pulse occurs without activating the Fault Overcurrent Comparator. A 1 μA (typically) pull−up current source, I_{QCS}, pulls up the QCS pin to disable the controller if the pin is left open.

QR Flyback Soft−Start

Soft−start is achieved by ramping up an internal reference, V_{SSTART}, and comparing it to current sense signal. V_{SSTART} ramps up from 0 V once the controller powers up. The soft−start duration, t_{SSTART}, is typically 4 ms.

During soft−start the timeout duration is extended and the lower latch or OTP Comparator signal (typically for overtemperature) is blanked. Soft−start ends once V_{SSTART} exceeds the peak current sense signal threshold.

QR Flyback Overpower Compensation

The input voltage of the QR flyback stage varies with the line voltage and operating mode of the PFC converter. At low line the PFC bulk voltage is 250 V and at high line it is 400 V. In addition, the PFC can be disabled at light loads to reduce input power at which point the PFC bulk voltage is set by the rectified peak line voltage.

An integrated overpower circuit provides a relative constant output power across PFC bulk voltage, V_{bulk}. It also reduces the variation on V_{QFB} during the PFC stage enable or disable transitions. Figure 27 shows the circuit schematic for the overpower detector.

The auxiliary winding voltage during the power switch on time is a reflection of the input voltage scaled by the primary to auxiliary winding turns ratio, $N_{P,AUX}$, as shown in Figure 28.

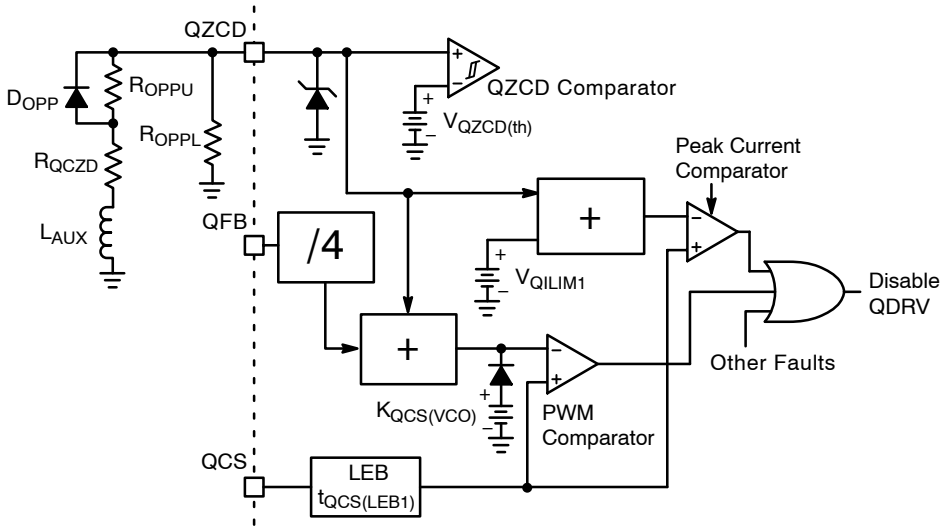

Figure 27. Overpower Compensation Circuit Schematic

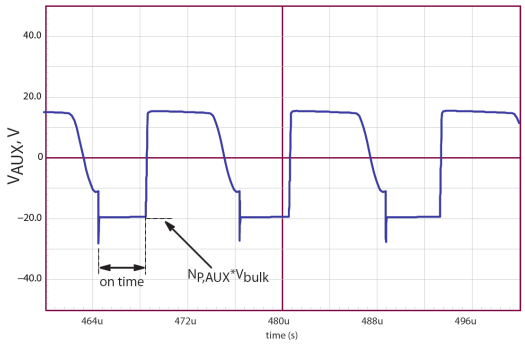

Figure 28. Auxiliary Winding Voltage Waveform

Overpower compensation is achieved by scaling down the on−time reflected voltage and applying it to the QZCD pin. The voltage is scaled down using R_{OPPU} and R_{OPPL}. The negative voltage applied to the pin is referred to as V_{OPP}.

The internal current setpoint is the sum of V_{OPP} and peak current sense threshold, V_{QILIM1}. V_{OPP} is also subtracted from V_{QFB} to compensate for the PWM Comparator delay and improve the PFC on/off accuracy.

The current setpoint is calculated using Equation 7. For example, a V_{OPP} of −0.15 V results in a current setpoint of 0.65 V.

$$\text{Current setpoint} = V_{QILIM1} + V_{OPP} \quad \text{(eq. 7)}$$

To ensure optimal zero−crossing detection, a diode is needed to bypass R_{OPPU} during the off−time. Equation 8 is used to calculate R_{OPPU} and R_{OPPL}.

$$\frac{R_{QZCD} + R_{OPPU}}{R_{OPPL}} = -\frac{N_{P,AUX} \cdot V_{bulk} - V_{OPP}}{V_{OPP}} \quad \text{(eq. 8)}$$

R_{OPPU} is selected once a value is chosen for R_{OPPL}. R_{OPPL} is selected large enough such that enough voltage is available for the zero crossing detection during the off−time. It is recommended to have at least 8 V applied on the QZCD pin for good detection. The maximum voltage is internally clamped to V_{CC}. The off−time voltage on the QZCD is given by Equation 9.

$$V_{QZCD} = \frac{R_{OPPL}}{R_{QZCD} + R_{OPPL}} \cdot (V_{AUX} - V_F) \quad \text{(eq. 9)}$$

Where V_{AUX} is the voltage across the auxiliary winding and V_F is the D_{OPP} forward voltage drop.

The ratio between R_{QZCD} and R_{OPPL} is given by Equation 10. It is obtained combining Equations 8 and 9.

$$\frac{R_{QZCD}}{R_{OPPL}} = \frac{V_{AUX} - V_F - V_{QZCD}}{V_{QZD}} \quad \text{(eq. 10)}$$

A design example is shown below:

System Parameters:

V_{AUX} = 18 V

V_F = 0.6 V

$N_{P,AUX}$ = 0.18

The ratio between R_{QZCD} and R_{OPPL} is calculated using Equation 10 for a minimum V_{QZCD} of 8 V.

$$\frac{R_{QZCD}}{R_{OPPL}} = \frac{18 - 0.6 - 8}{8} \approx 1.2$$

R_{QZCD} is arbitrarily set to 1 kΩ. R_{OPPL} is also set to 1 kΩ because the ratio between the resistors is close to 1.

The NCP1937 maximum overpower compensation or peak current setpoint reduction is 31.25% for a V_{OPP} of −250 mV. We will use this value for the following example:

Substituting values in Equation 8 and solving for R_{OPPU} we obtain,

$$\frac{R_{QZCD} + R_{OPPU}}{R_{OPPL}} = -\frac{0.18 \cdot 370 - (-0.25)}{(-0.25)} = 271$$

$$R_{OPPU} = 271 \cdot R_{OPPL} - R_{QZCD}$$

$$R_{OPPU} = 271 \cdot 1\ k - 1\ k = 270\ k$$

Power Factor Correction

The PFC stage operates in critical conduction mode (CrM). In CrM, the PFC inductor current, $I_L(t)$ reaches zero at the end of each switch cycle. Figure 29 shows the PFC inductor current while operating in CrM. The average input current, $I_{in}(t)$, is in phase with the ac line voltage, $V_{in}(t)$, to achieve power factor correction.

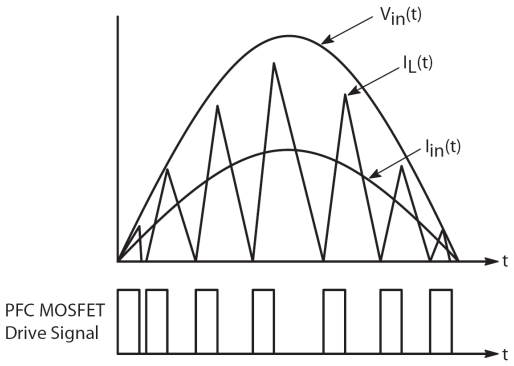

Figure 29. Inductor Current in CrM

High power factor is achieved in CrM by maintaining a constant on time (t_{on}) for a given RMS input voltage ($V_{ac(RMS)}$) and load condition. Equation 11 shows the relationship between on time and system operating conditions.

$$t_{on} = \frac{2 \cdot P_{out} \cdot L}{\eta \cdot V_{ac(RMS)}^2} \quad \text{(eq. 11)}$$

where P_{out} is the output power, L is the PFC choke inductance and η is the system efficiency.

PFC Feedback

The PFC feedback circuitry is shown in Figure 30. A transconductance error amplifier regulates the PFC output voltage, V_{bulk}, by comparing the PFC feedback signal to an internal reference voltage, V_{PREF}. The feedback signal is applied to the inverting input and the reference is connected to the non−inverting input of the error amplifier. A resistor divider consisting of R1 and R2 scales down V_{bulk} to generate the PFC feedback signal. V_{PREF} is trimmed during manufacturing to achieve an accuracy of ± 2%.

The PFC stage is disabled at light loads to reduce input power. The NCP1937 integrates a 700 V switch, PFC FB Switch, between the PFBHV and PFBLV pins. The PFC FB Switch is in series between R1 and R2 to disconnect the resistors and reduce input power when the PFC stage is disabled.

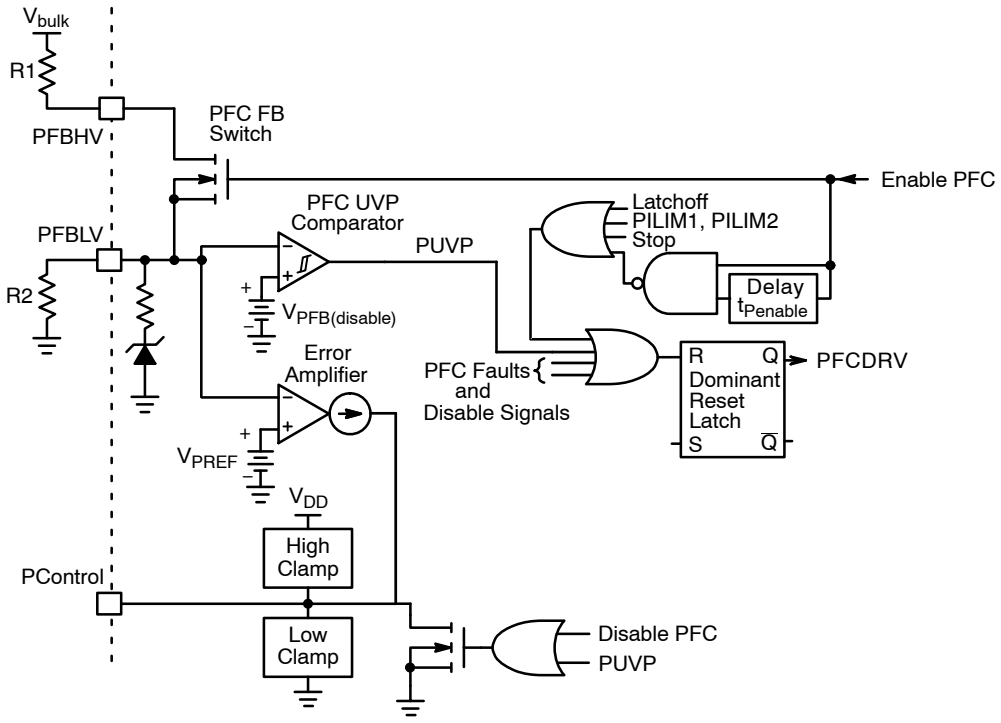

Figure 30. PFC Regulation Circuit Schematic

The maximum on resistance of the PFC FB Switch, $R_{PFBswitch(on)}$, is 10 kΩ. Because the PFC FB Switch is in series with R1 and R1's value is several orders of magnitudes larger, the switch introduces minimum error on the regulation level. The off state leakage current of the PFC FB Switch, $I_{PFBSwitch(off)}$, is less than 3 μA.

The NCP1937 safely disables the controller if the PFBLV pin is grounded. A short pin detector disables the controller if V_{PFBLV} is below the disable threshold, $V_{PFB(disable)}$, typically 0.3 V. If the PFBLV pin is open, the PFC FB Switch will raise V_{PFBLV} above the overvoltage threshold and disable the controller. Equation 12 shows the relationship between the PFC output voltage, the PFC reference threshold, R1 and R2.

$$V_{PFC} = V_{PREF(xL)} \cdot \frac{R1 + R2}{R2} \qquad \text{(eq. 12)}$$

PFC Error Amplifier

A transconductance amplifier has a voltage−to−current gain, g_m. That is, the amplifier's output current is controlled by the differential input voltage. The NCP1937 amplifier has a typical g_m of 200 μS. The PControl pin provides access to the amplifier output for compensation. The compensation network is ground referenced allowing the PFC feedback signal to be used to detect an overvoltage condition.

The compensation network on the PControl pin is selected to filter the bulk voltage ripple such that a constant control voltage is maintained across the ac line cycle. A capacitor between the PControl pin and ground sets a pole. A pole at or below 20 Hz is enough to filter the ripple voltage for a 50 and 60 Hz system. The low frequency pole, f_p, of the system is calculated using Equation 13.

$$f_p = \frac{gm}{2\pi C_{PControl}} \qquad \text{(eq. 13)}$$

where, $C_{PControl}$ is the capacitor on the PControl pin to ground.

The output of the error amplifier is held low when the PFC is disabled by means of an internal pull−down transistor. The pull down transistor is disabled once the PFC stage is enabled. An internal voltage clamp is then enabled to quickly raise $V_{PControl}$ to its minimum voltage, $V_{PClamp(lower)}$.

PFC On−Time

The PFC on time is controlled by $V_{PControl}$. The PFC On−Time Comparator terminates the drive pulse once the PFC on−time ramp voltage plus offset exceeds $V_{PControl}$. The ramp is generated by charging an internal timing capacitor, C_{PCT}, with a constant current source, I_{PCT}. The capacitor ramp is level shifted to achieve 0 duty ratio (stop drive pulses) at the minimum $V_{PControl}$. $V_{PControl}$ is proportional to the output power and it is fixed for a given RMS line voltage and output load, satisfying Equation 11.

Lower and upper voltage clamps limit the excursion of $V_{PControl}$. The maximum on−time, $t_{on(MAX)}$, occurs when $V_{PControl}$ is at its maximum value, $V_{PControl(MAX)}$. The PFC drive pulses are inhibited once $V_{PControl}$ is below its minimum value, $V_{PControl(MIN)}$. The maximum PFC on−time in the NCP1937 is set internally. The maximum on time at low line is typically 15 μs.

PFC Transient Response

The PFC bandwidth is set low enough to achieve good power factor. A low bandwidth system is slow and fast load transients can result in large output voltage excursions. The NCP1937 incorporates dedicated circuitry to help mantain regulation of the output voltage independent of load transients.

An undervoltage detector monitors V_{bulk} and prevents it from dropping below from its regulation level. Once the ratio between V_{PFBLV} and $V_{PREF(xL)}$ exceeds $K_{LOW(PFCxL)}$, typically 5.5%, a pull−up current source on the PControl pin, $I_{PControl(boost)}$, is enabled to speed up the charge of the compensation capacitor(s). This results in an increased on−time and thus output power. $I_{PControl(boost)}$ is typically 240 μA. The boost current source is disabled once the ratio between V_{PFBLV} and $V_{PREF(xL)}$ drops below $K_{LOW(PFCxL)}$, typically 4%.

The boost current source becomes active as soon as the PFC is enabled. Coupled with the lower control clamp, the current provided by the boost current source assists in rapidly bringing $V_{PControl}$ to its set point to allow the bulk voltage to quickly reach regulation. Achieving regulation is detected by monitoring the error amplifier output current. The error amplifier output current drops to zero once the PFC output voltage reaches the target regulation level.

The maximum PFC output voltage is limited by the overvoltage protection circuitry. The NCP1937 incorporates both soft and hard overvoltage protection. The hard overvoltage protection function immediately terminates and prevents further PFC drive pulses when V_{PFBLV} exceeds the hard−OVP level, $V_{PREF(xL)}$ * $K_{POVP(xL)}$. Soft−OVP reduces the on−time proportional to the delta between V_{PFBLV} and the hard−OVP level. Soft−OVP is enabled once the delta, $\Delta_{POVP(xL)}$, between V_{PFBLV} and the hard−OVP level, is between 20 and 55 mV. Figure 31 shows the circuit schematic of the boost and Soft−OVP circuits.

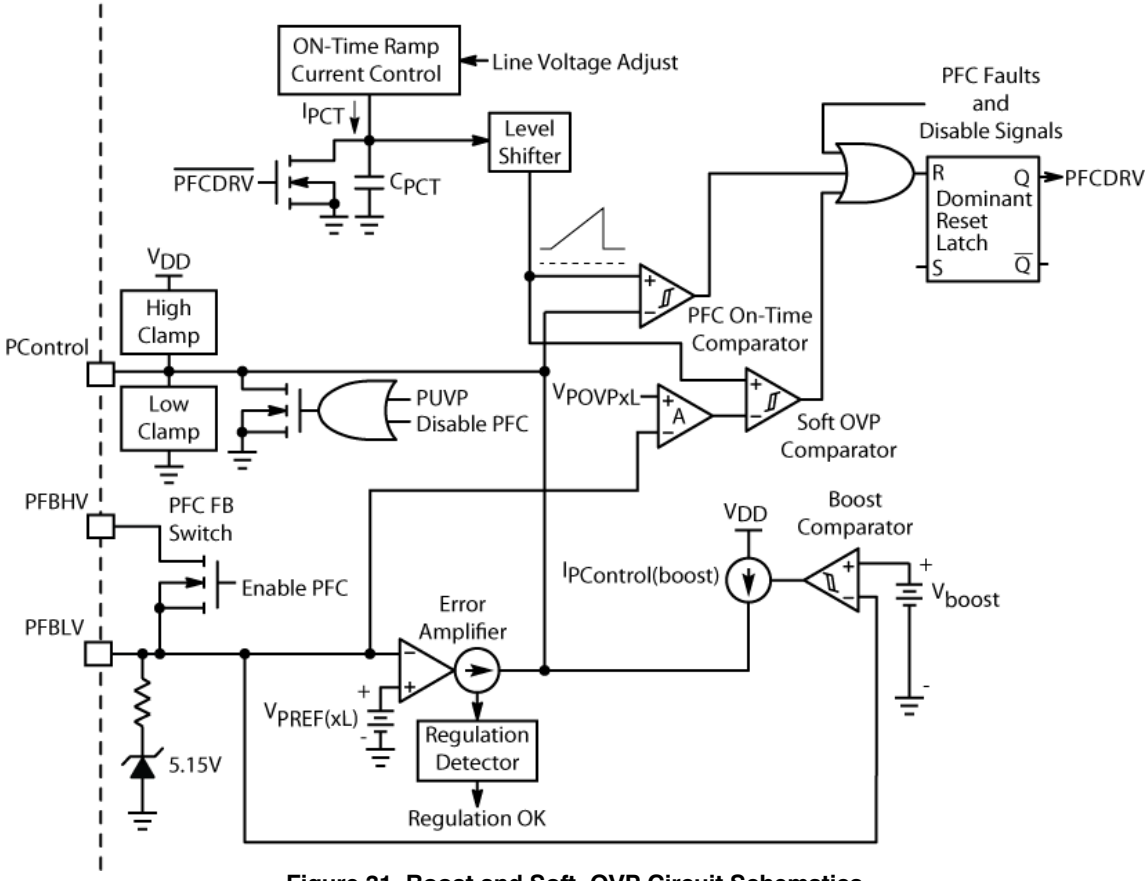

Figure 31. Boost and Soft−OVP Circuit Schematics

During power up, $V_{PControl}$ exceeds the regulation level due to the system's inherently low bandwidth. This causes the bulk voltage to rapidly increase and exceed its regulation. The on time starts to decrease when soft−OVP is activated. Once the bulk voltage decreases to its regulation level the PFC on time is no longer controlled by the soft−OVP circuitry.

PFC Current Sense and Zero Current Detection

The NCP1937 uses a novel architecture combining the PFC current sense and zero current detectors (ZCD) in a single input terminal. Figure 32 shows the circuit schematic of the current sense and ZCD detectors.

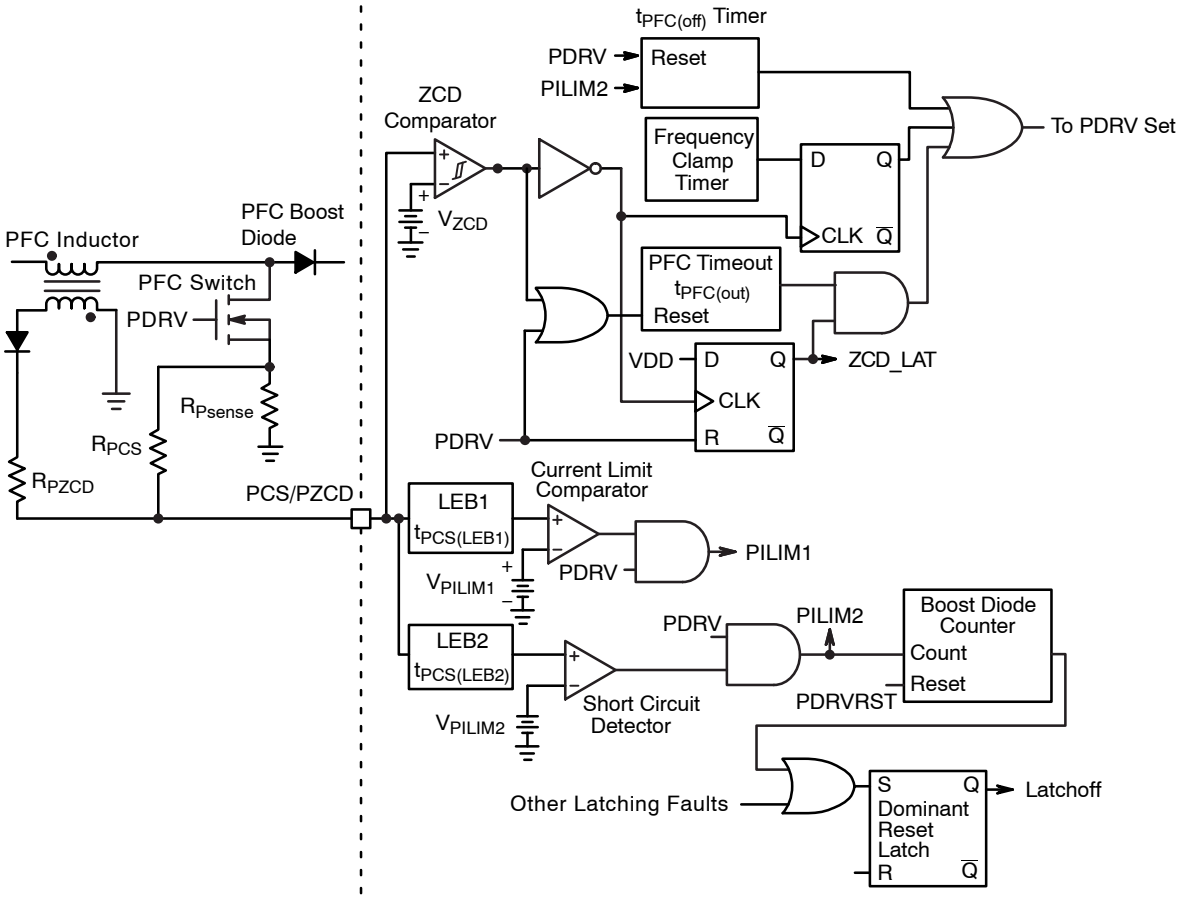

Figure 32. PFC Current Sense and ZCD Detectors Schematic

PFC Current Sense

The PFC Switch current is sensed across a sense resistor, R_{Psense}, and the resulting voltage ramp is applied to the PCS/PZCD pin. The current signal is blanked by a leading edge blanking (LEB) circuit. The blanking period eliminates the leading edge spike and high frequency noise during the switch turn−on event. The LEB period, $t_{PCS(LEB1)}$, is typically 325 ns. The Current Limit Comparator disables the PFC driver once the current sense signal exceeds the PFC current sense reference, V_{PILIM1}, typically 0.5 V.

A severe overload fault like a PFC boost diode short circuit causes the switch current to increase very rapidly during the on−time. The current sense signal significantly exceeds V_{PILIM1}. But, because the current sense signal is blanked by the LEB circuit during the switch turn on, the system current can get extremely high causing system damage.

The NCP1937 protects against this fault by adding an additional comparator, PFC Short Circuit Comparator. The current sense signal is blanked with a shorter LEB duration, $t_{PCS(LEB2)}$, typically 175 ns, before applying it to the PFC Short Circuit Comparator. The voltage threshold of the comparator, V_{PILIM2}, typically 1.25 V, is set 250% higher than V_{PILIM1}, to avoid interference with normal operation. Four consecutive faults detected by the Short Circuit Comparator causes the controller to enter latch mode. The count to 4 provides noise immunity during surge testing. The counter is reset each time a PDRV pulse occurs without activating the Short Circuit Comparator.

The PFC watchdog timer duration increases to $t_{PFC(off2)}$ (typically 1 ms) when a V_{PILIM2} fault is detected independent of the PFC ZCD state.

PFC Zero Current Detection

The off−time in a CrM PFC topology varies with the instantaneous line voltage and is adjusted every switching cycle to allow the inductor current to reach zero before the next switching cycle begins. The inductor is demagnetized once its current reaches zero. Once the inductor is demagnetized the drain voltage of the PFC switch begins to drop. The inductor demagnetization is detected by sensing the voltage across the inductor using an auxiliary winding. This winding is commonly known as a zero crossing detector (ZCD) winding. This winding provides a scaled version of the inductor voltage. Figure 33 shows the ZCD winding arrangement.

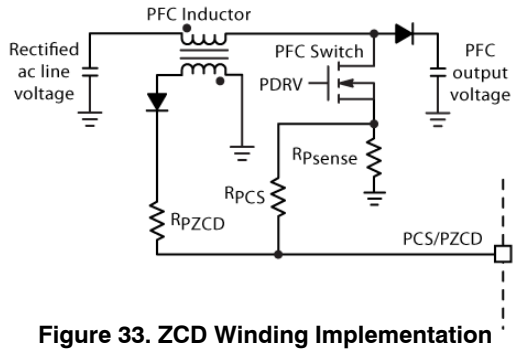

Figure 33. ZCD Winding Implementation

The ZCD voltage, V_{ZCD}, is positive while the PFC Switch is off and current flows through the PFC inductor. V_{ZCD} drops to and rings around zero volts once the inductor is demagnetized. The next switching cycle begins once a negative transition is detected on the PCS/PZCD pin. A positive transition (corresponding to the PFC switch turn off) arms the ZCD detector to prevent false triggering. The arming of the ZCD detector, $V_{PZCD(rising)}$, is typically 0.75 V ($V_{PCS/PZCD}$ increasing). The trigger threshold, $V_{PZCD(falling)}$, is typically 0.25 V ($V_{PCS/PZCD}$ decreasing).

The PCS/PZCD pin is internally clamped to 5 V with a Zener diode and a 2 kΩ resistor. A resistor in series with the PCS/PZCD pin is required to limit the current into pin. The Zener diode also prevents the voltage from going below ground. Figure 34 shows typical ZCD waveforms.

During startup there are no ZCD transitions to set the PFC PWM Latch and generate a PDRV pulse. A watchdog timer, $t_{PFC(off1)}$, starts the drive pulses in the absence of ZCD transitions. Its duration is typically 200 μs. The timer is also useful if the line voltage transitions from low line to high line and while operating at light load because the amplitude of the ZCD signal may be too small to cross the ZCD arming threshold. The watchdog timer is reset at the beginning of a PFC drive pulse. It is disabled during a PFC hard overvoltage and feedback input short circuit condition.

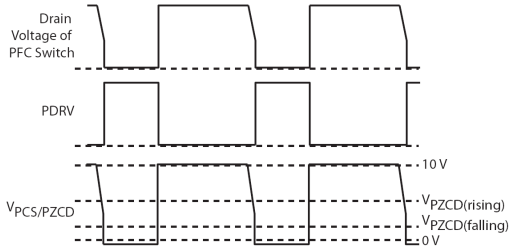

Figure 34. ZCD Winding Waveforms

The watchdog timer duration increases to $t_{PFC(off2)}$, typically 1 ms, when a V_{PILIM2} fault is detected.

PFC Frequency Clamp

The PFC operating frequency naturally increases when the line voltage gets near to zero due to the reduced demagnetization time or when the PFC is operating at light loads. A maximum frequency clamp, $f_{clamp(PFC)}$, limits the PFC frequency to improve efficiency and facilitate compliance with EMI requirements. The NCP1937 has options for PFC frequency clamp values of 131 kHz or 250 kHz.

The PDRV pulse is blanked until the frequency clamp timer expires. Once expired, the controller waits for the next ZCD transition to initiate PDRV. This ensures valley switching to reduce switching losses. A timeout timer, $t_{P(tout)}$, starts the next PDRV pulse in the absence of a ZCD transition. The timeout timer duration is typically 10 μs. The timer is reset at every ZCD event. Figure 35 shows the block diagram of the PFC frequency clamp.

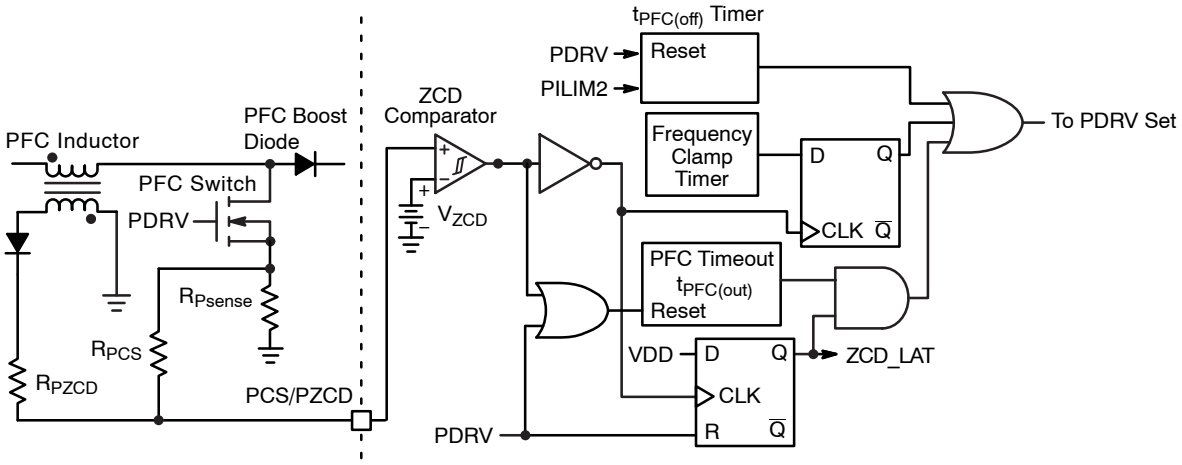

Figure 35. PFC Frequency Clamp Schematic

PFC Enable & Disable

In some applications it is desired to disable the PFC at lighter loads to increase the overall system efficiency. The NCP1937 integrates a novel architecture that allows the user to program the PFC disable threshold based on the percentage of QR output power. The PFC enable circuitry is inactive until the QR flyback soft start period has ended. A voltage to current (V−I) converter generates a current proportional to V_{QFB}. This current is pulse width modulated by the demagnetization time of the flyback controller to generate a current, I_{PONOFF}, proportional to the output power. An external resistor, R_{PONOFF}, between the PONOFF and GND pins generate a voltage proportional to the output power. This resistor is used to scale the output power signal. A capacitor, C_{PONOFF}, in parallel with R_{PONOFF} is required to average the signal on this pin. A good compromise between voltage ripple and speed is achieved by setting the time constant of C_{PONOFF} and R_{PONOFF} to 160 μs.

The PONOFF pin voltage, V_{PONOFF}, is compared to an internal reference, V_{POFF} (typically 2 V) to disable the PFC stage. The PFC disable point is typically set between 25 and 50% or between 50 and 75% of the maximum system load. These setpoints provide the best system efficiency across low line and high line.

Once V_{PONOFF} decreases below V_{POFF}, the PFC disable timer, $t_{Pdisable}$, is enabled. The NCP1937 has options for 500 ms, 4 s, or 13 s PFC disable timer. The PFC stage is disabled once the timer expires. The PFC stage is enabled once V_{PONOFF} exceeds V_{POFF} by V_{PONHYS} for a period longer than the PFC enable filter, $t_{Penable(filter)}$, typically 100 μs. A shorter delay for the PFC enable threshold is used to reduce the bulk capacitor requirements during a step load response. Figure 36 shows the block diagram of the PFC disable circuit.

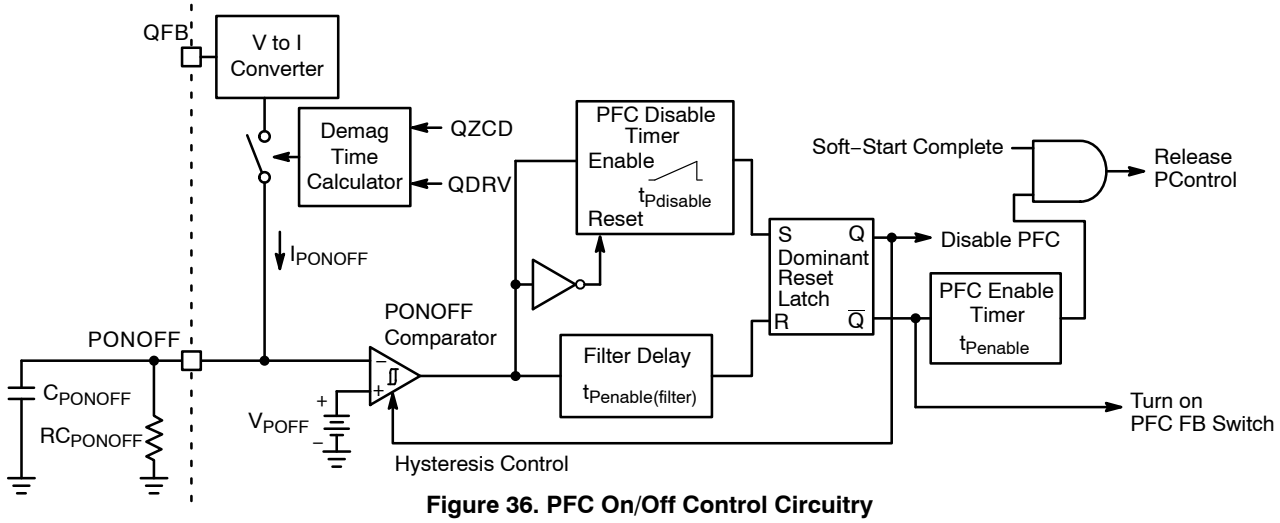

Figure 36. PFC On/Off Control Circuitry

PFC Skip

The PFC stage incorporates skip cycle operation at light loads to reduce input power. Skip operation disables the PFC stage if the PControl voltage decreases below the skip threshold. The skip threshold voltage is typically 25 mV (ΔV_{PSKIP}) above the PControl lower voltage clamp, $V_{clamp(lower)}$. The PFC stage is enabled once $V_{PControl}$ increases above the skip threshold by the skip hysteresis, $V_{PSKIP(HYS)}$. PFC skip is disabled during any initial PFC startup and when the PFC is in a UVP. Skip operation will become active after the PFC has reached regulation.

PFC and Flyback Drivers

The NCP1937 maximum supply voltage, $V_{CC(MAX)}$, is 30 V. Typical high voltage MOSFETs have a maximum gate voltage rating of 20 V. Both the PFC and flyback drivers incorporate an active voltage clamp to limit the gate voltage on the external MOSFETs. The PFC and flyback voltage clamps, $V_{PDRV(high)}$ and $V_{QDRV(high)}$, are typically 12 V with a maximum limit of 14 V.

Auto Recovery

The controller is disabled and enters “triple−hiccup” mode if V_{CC} drops below $V_{CC(off)}$. The controller will also enter “triple−hiccup” mode if an overload fault is detected on the non−latching version. A hiccup consists of V_{CC} falling down to $V_{CC(off)}$ and charging up to $V_{CC(on)}$. The controller needs to complete 3 hiccups before restarting.

Temperature Shutdown

An internal thermal shutdown circuit monitors the junction temperature of the IC. The controller is disabled if the junction temperature exceeds the thermal shutdown threshold, T_{SHDN}, typically 150°C. A continuous V_{CC} hiccup is initiated after a thermal shutdown fault is detected. The controller restarts at the next $V_{CC(on)}$ once the IC temperature drops below below T_{SHDN} by the thermal shutdown hysteresis, $T_{SHDN(HYS)}$, typically 40°C.

The thermal shutdown fault is also cleared if V_{CC} drops below $V_{CC(reset)}$, a brown−out fault is detected or if the line voltage is removed. A new power up sequences commences at the next $V_{CC(on)}$ once all the faults are removed.

PCB Layout Recommendations

In any power converter, the PCB layout and routing require consideration to minimize noise generation and ensure stable operation. As a combo device, the NCP1937 controls two variable switching frequency converters that operate independently of each other and can therefore switch asynchronously. A turn−on or turn−off event of one converter can occur at any point in the other converter's switching cycle possibly disrupting its operation. It is therefore necessary to pay particular attention to the current paths and grounding patterns to avoid interactions between the two converters.

Before laying out a PCB for the NCP1937 it is recommended to identify and annotate the various grounds as shown in Figure 37. Table 5 below includes a description of the different grounds. The grounds are divided into power grounds, denoted as PGNDx, and analog or signal grounds, denoted as AGNDx.

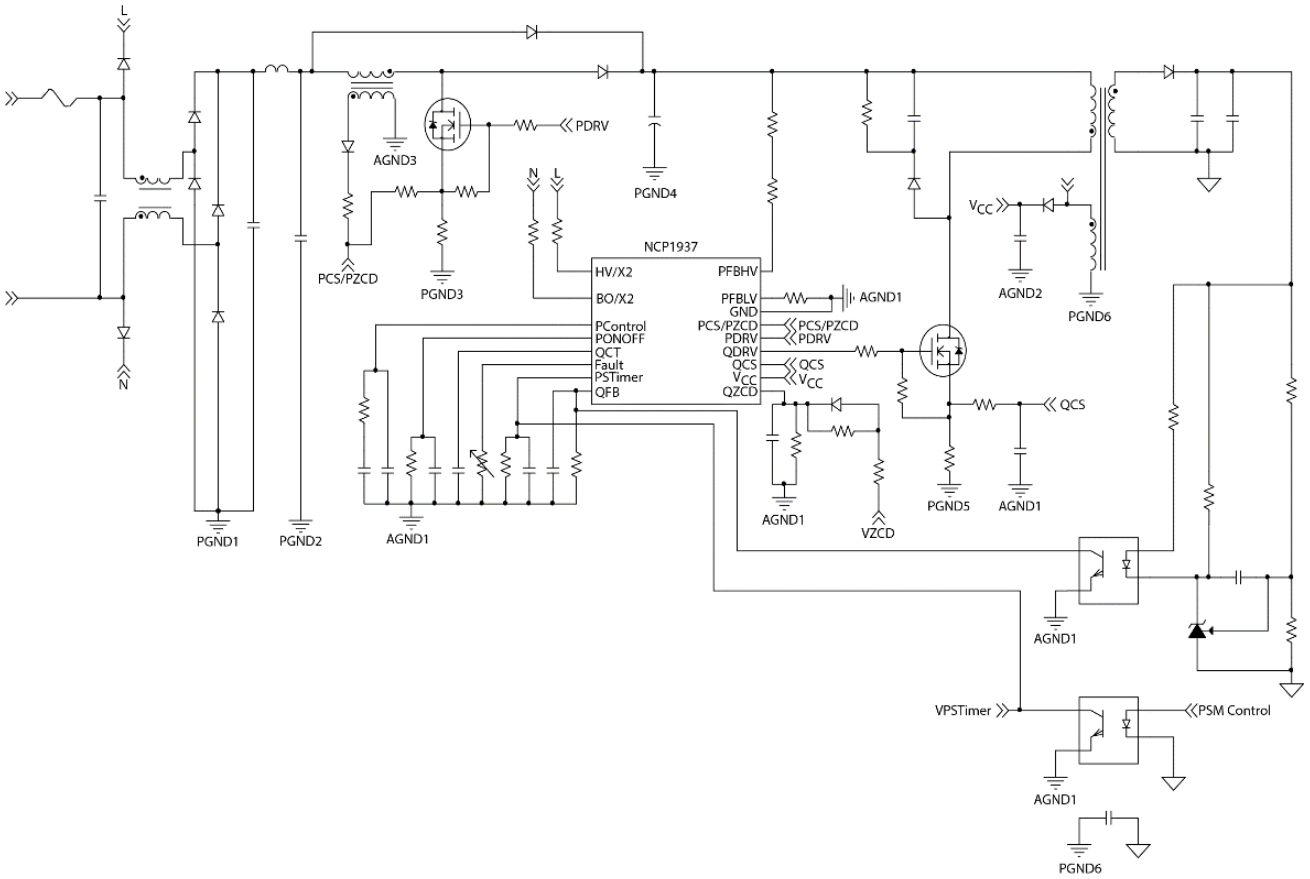

Figure 37. Typical Application with Annotated Grounds

Table 5. DESCRIPTION OF ANNOTATED GROUND NODES IN NCP1937 APPLICATION

Label	Location
PGND1	Diode bridge and input bulk ground
PGND2	PFC pi filter ground
PGND3	PFC current sense resistor ground
PGND4	Negative of PFC bulk cap ground
PGND5	current sense resistor ground of flyback
PGND6	Primary Y−cap and Aux winding ground
AGND1	All programming components of NCP1937
AGND2	Ground of V_{CC} bulk capacitor
AGND3	PFC ZCD auxiliary winding
AGND	GND at the IC

For the NCP1937 the following routing requirements are recommended for the primary side power grounds:

- The current path from PGND3 to PGND4 and the current path from PGND4 to PGND5 are isolated to the greatest extent possible to provide separate paths for the switching currents of the PFC and flyback converter. This will avoid the switching currents and the gate drive currents from the two converters overlapping
- Path between PGND6 and PGND1 is key for improved surge performance. It is necessary to use a separate, isolated trace to connect PGND6 back to PGND1. Make this trace as wide as possible.
- The connection between PGND4 and PGND5 should be as short as possible with as wide of a trace as possible.

- PGND4 will be the center point of a star connection for the analog signal grounds. The trace connection between PGND4 and AGND should be as short and wide as possible.
- The path between PGND1 and PGND2 and PGND3 can be sequential paths, i.e., it is not necessary to isolate these paths.

Routing requirements for the primary side analog grounds:

- AGND is the NCP1937 IC ground and will be the center point of the analog star configuration. The three other analog grounds should intersect at this point. The trace between AGND and PGND4 (bulk capacitor ground) should be as short and wide as possible.
- AGND3 which originates from the PFC choke auxiliary winding should have its own isolated trace back to AGND. To the greatest extent possible AGND1 & AGND3 should not overlap except for their intersection point at the AGND star.
- AGND2 should its own trace back to the AGND star intersection point and try to avoid overlap with the other analog grounds.
- Star ground connections are well known in the industry and a good practice for optimal layouts. Figure 38 is an example star grounding configuration for the primary grounds

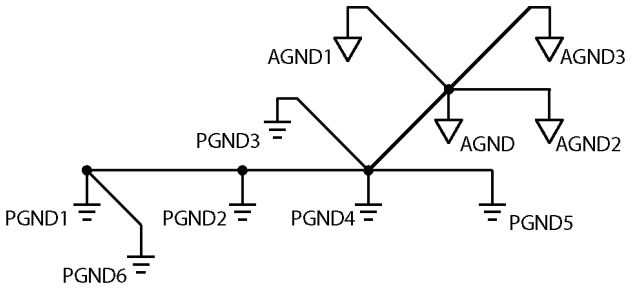

Figure 38. Example Star Ground Configuration for NCP1937

The above recommendations are meant to serve as a general guideline for most applications. If the above recommendations are not followed, it is possible that the switching events from one converter can interrupt operation of the other converter. One particular sensitivity that may occur is that the PFC switching and gate drive currents can interfere with QR current sense signal resulting in erratic drive pulses. The QR current sense signal is particularly critical for stable operation of the QR and RC filtering decoupled to the appropriate ground should be employed.

In summary:

- Layout is a critical consideration for power converter operation. This is especially true with a combination controller operating two power converters asynchronously
- Follow the suggested grounding recommendation outlined above. These recommendations are intended to mitigate noise from one converter coupling onto the sensitive control signals of the other converter
- An RC filter with a time constant of ≥ 100 ns should be placed close to the QCS pin of the IC, with the capacitor decoupled to AGND1 as shown above
- If any erratic drive operation of the OR is observed, it is recommended to increase the time constant of the RC filter. Time constants up to 250 – 300 ns are reasonable

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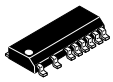
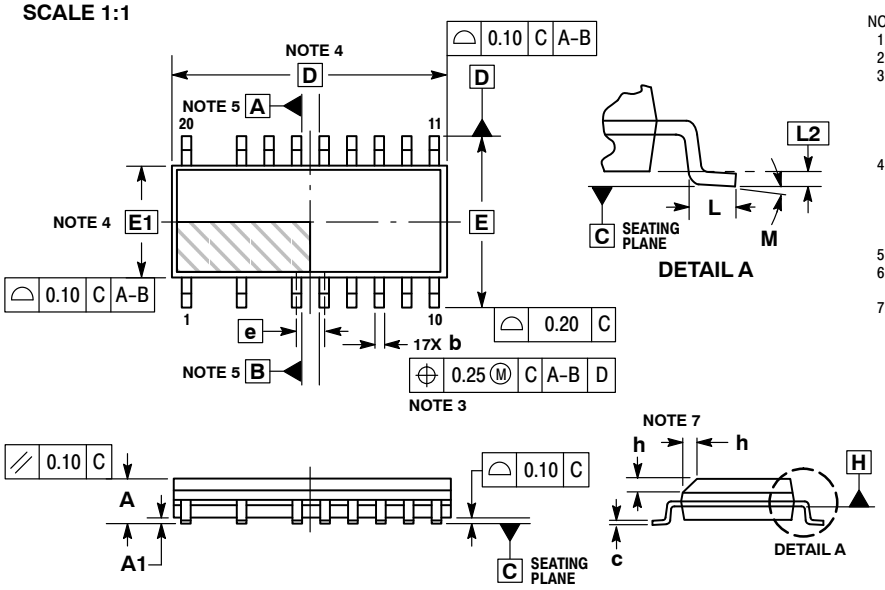
DATE 28 APR 2011



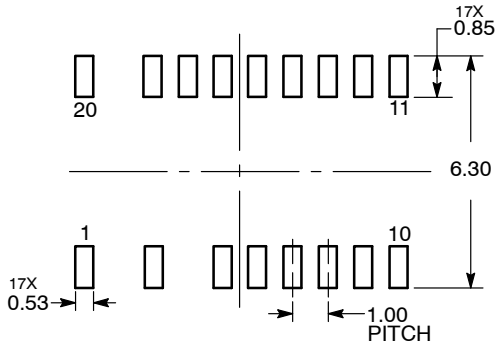
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 TOTAL IN EXCESS OF THE b DIMENSION. DIMENSION b APPLIES TO THE FLAT PORTION OF THE LEAD AND SHALL BE MEASURED BETWEEN 0.13 AND 0.25 FROM THE TIP.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS BUT DO INCLUDE MOLD MISMATCH. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. CHAMFER FEATURE IS OPTIONAL. IF NOT PRESENT, THEN A PIN ONE IDENTIFIER MUST BE LOCATED IN THIS AREA.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.70
A1	0.00	0.20
b	0.31	0.51
c	0.10	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.00 BSC	
h	0.25	0.50
L	0.40	0.85
L2	0.25 BSC	
M	0°	8°

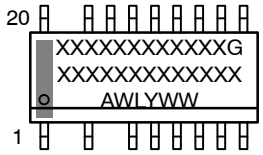
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**SOIC20 NB LESS PINS 2, 4 & 19**	**PAGE 1 OF 1**

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