NCP110

Linear Regulator, Low V_{IN}, Low Noise and High PSRR, 200 mA

The NCP110 is a linear regulator capable of supplying 200 mA output current from 1.1 V input voltage. The device provides wide output range from 0.6 V up to 4.0 V, very low noise and high PSRR. Due to low quiescent current the NCP110 is suitable for battery powered devices such as smartphones and tablets. The device is designed to work with a 1 μF input and a 1 μF output ceramic capacitor. It is available in ultra−small 0.35P, 0.65 mm x 0.65 mm Chip Scale Package (CSP) and XDFN4 0.65P, 1 mm x 1 mm.

Features

- Operating Input Voltage Range: 1.1 V to 5.5 V
- Available in Fixed Voltage Option: 0.6 V to 4.0 V
- ±2% Accuracy Over Load/Temperature
- Ultra Low Quiescent Current Typ. 20 μA
- Standby Current: Typ. 0.1 μA
- Very Low Dropout: 70 mV for 1.05 V @ 100 mA
- High PSRR: Typ. 95 dB at 20 mA, f = 1 kHz
- Ultra Low Noise: 8.8 μV_{RMS}
- Stable with a 1 μF Small Case Size Ceramic Capacitors
- Available in −WLCSP4 0.65mm x 0.65mm x 0.33mm − Case 567VS
  −XDFN4 1mm x 1mm x 0.4mm − Case 711AJ
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery−powered Equipment
- Smartphone, Tablets
- Digital Cameras
- Smoke Detectors
- Portable Medical Equipment
- RF, PLL, VCO and Clock Power Supplies
- Battery Powered Wireless IoT Modules

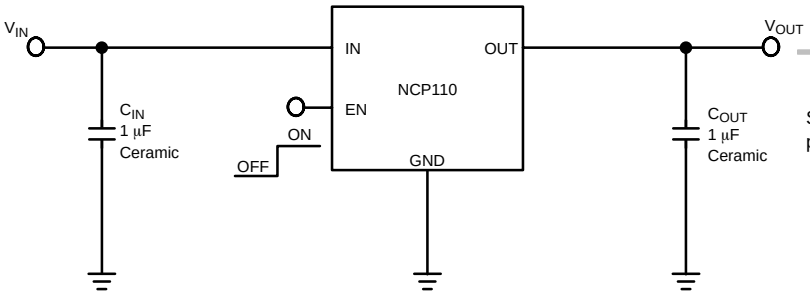

Figure 1. Typical Application Schematics

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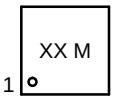
MARKING DIAGRAMS

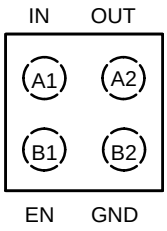
WLCSP4
CASE 567VS

XDFN4
CASE 711AJ

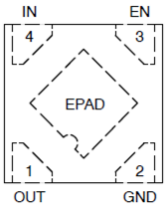


X or XX = Specific Device Code
M = Date Code

PIN CONNECTIONS



(Top View)



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 14 of this data sheet.

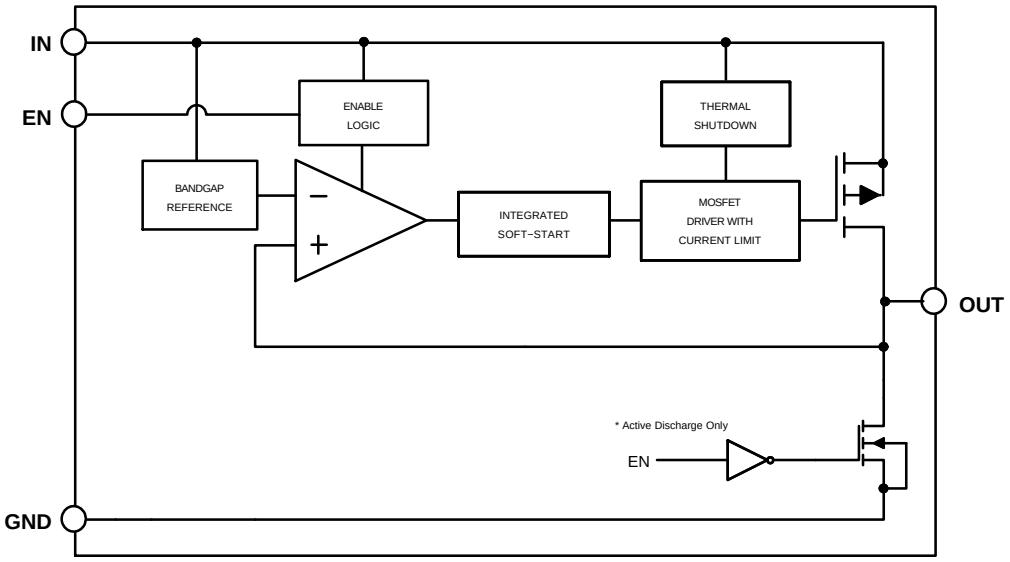


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. CSP4	Pin No. XDFN4	Pin Name	Description
A1	4	IN	Input voltage supply pin
A2	1	OUT	Regulated output voltage. The output should be bypassed with small 1 μF ceramic capacitor.
B1	3	EN	Chip enable: Applying V_{EN} < 0.2 V disables the regulator, Pulling V_{EN} > 0.7 V enables the LDO.
B2	2	GND	Common ground connection
−	EPAD	EPAD	Expose pad can be tied to ground plane for better power dissipation

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3, max. 6 V	V
Chip Enable Input	V_{CE}	−0.3 to 6 V	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, CSP4 (Note 3) Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	108	°C/W
Thermal Characteristics, XDFN4 (Note 3) Thermal Resistance, Junction−to−Air		208	

3. Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7

ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 125°C$; $V_{IN} = V_{OUT(NOM)} + 0.3$ V or 1.1 V, whichever is greater; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1 μF, unless otherwise noted. V_{EN} = 1.0 V. Typical values are at T_J = +25°C (Note 4).

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.1		5.5	V
Output Voltage Accuracy	$V_{IN} = V_{OUT(NOM)} + 0.3$ V ($V_{IN} \ge 1.1$ V)	$V_{OUT(NOM)} \le 1.5$ V	V_{OUT}	−30		+30	mV
		$V_{OUT(NOM)} > 1.5$ V		−2		+2	%
Line Regulation	$V_{OUT(NOM)} + 0.5$ V ≤ V_{IN} ≤ 5.5 V, ($V_{IN} \ge 1.1$ V)		$Line_{Reg}$		0.02		%/V
Load Regulation	I_{OUT} = 1 mA to 200 mA		$Load_{Reg}$		0.001		%/mA
Dropout Voltage (Note 5)	$V_{OUT(NOM)}$ = 1.05 V	I_{OUT} = 50 mA	V_{DO}		40	70	mV
		I_{OUT} = 100 mA			70	130	
	$V_{OUT(NOM)}$ = 1.20 V	I_{OUT} = 110 mA			60	140	
		I_{OUT} = 200 mA			110	190	
	$V_{OUT(NOM)}$ = 1.80 V	I_{OUT} = 200 mA			65	120	
	$V_{OUT(NOM)}$ = 2.80 V	I_{OUT} = 200 mA			45	100	
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$		I_{CL}	225	300		mA
Short Circuit Current	V_{OUT} = 0 V		I_{SC}		300		
Quiescent Current	I_{OUT} = 0 mA		I_Q		20	25	μA
Shutdown Current	$V_{EN} \le 0.2$ V, V_{IN} = 1.1 V		I_{DIS}		0.01	1.0	μA
EN Pin Threshold Voltage	EN Input Voltage “H”		V_{ENH}	0.7			V
	EN Input Voltage “L”		V_{ENL}			0.2	
EN Pull Down Current	V_{EN} = 1.1 V		I_{EN}		0.2	0.5	μA
Turn−On Time	C_{OUT} = 1 μF, From assertion of V_{EN} to V_{OUT} = 95% $V_{OUT(NOM)}$		t_{ON}		120		μs
Power Supply Rejection Ratio	I_{OUT} = 20 mA, $V_{IN} = V_{OUT} + 0.3$ V	f = 100 Hz f = 1 kHz f = 10 kHz f = 100 kHz	PSRR		90 95 85 55		dB
Output Voltage Noise	f = 10 Hz to 100 kHz		V_N		8.8		μV_{RMS}
Thermal Shutdown Threshold	Temperature rising		T_{SDH}		160		°C
	Temperature falling		T_{SDL}		140		°C
Active Output Discharge Resistance	V_{EN} < 0.2 V, Version A only		R_{DIS}		280		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 0.02 x $V_{OUT(NOM)}$ below $V_{OUT(NOM)}$.
6. Guaranteed by design.

TYPICAL CHARACTERISTICS

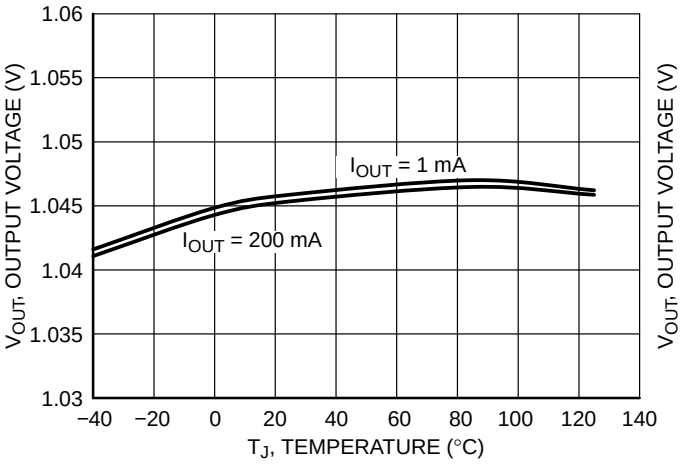


Figure 3. Output Voltage vs. Temperature − $V_{OUT,nom}$ = 1.05 V − CSP4

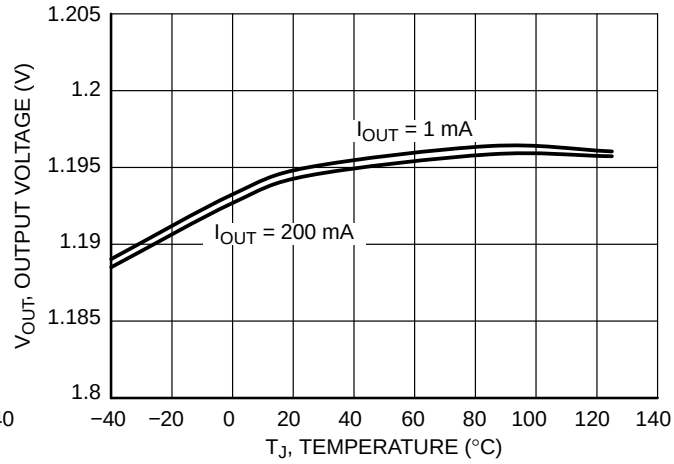


Figure 4. Output Voltage vs. Temperature − $V_{OUT,nom}$ = 1.2 V − CSP4

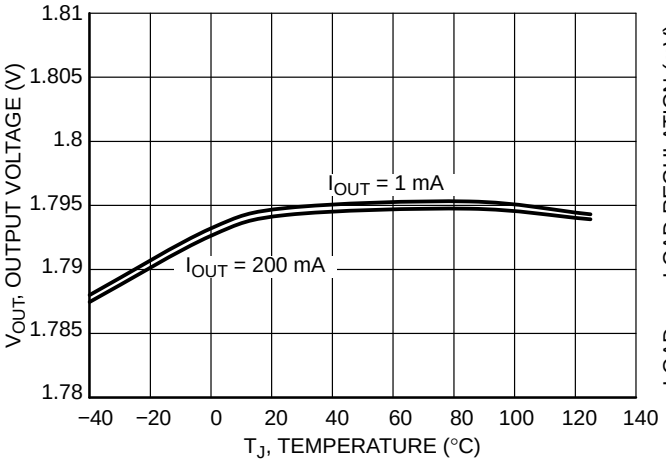


Figure 5. Output Voltage vs. Temperature − $V_{OUT,nom}$ = 1.8 V − CSP4

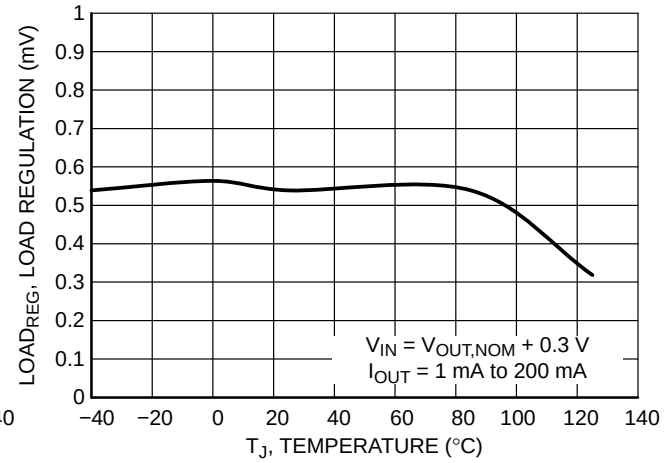


Figure 6. Load Regulation vs. Temperature

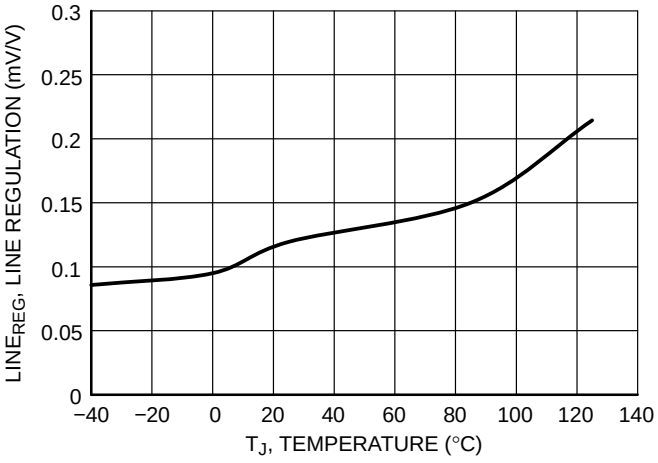


Figure 7. Line Regulation vs. Temperature

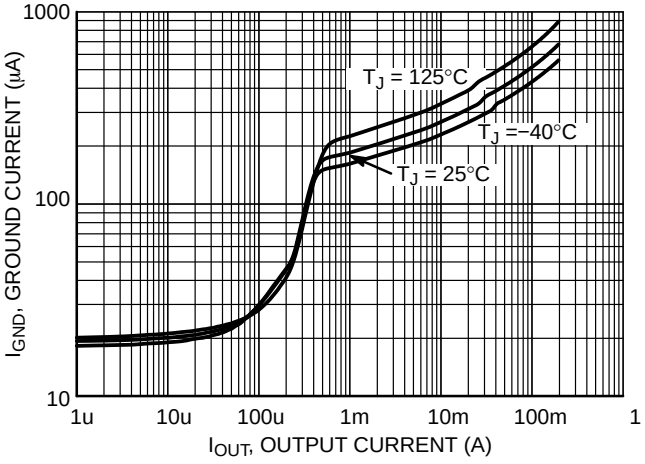


Figure 8. Ground Current vs. Output Current − $V_{OUT,nom}$ = 1.2 V

TYPICAL CHARACTERISTICS

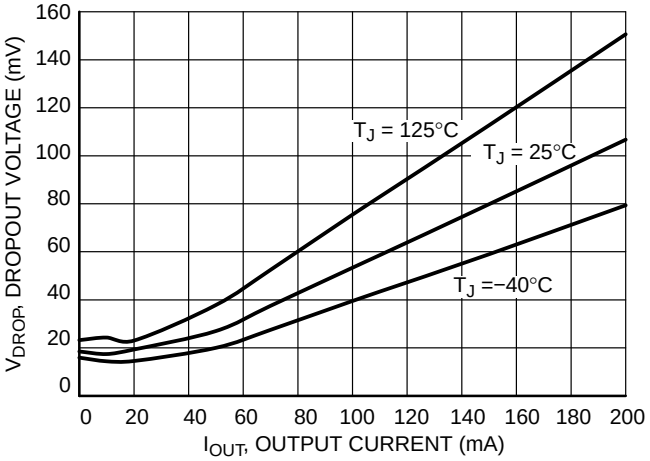


Figure 9. Dropout Voltage vs. Output Current − V_{OUT},nom = 1.2 V − CSP4 Package

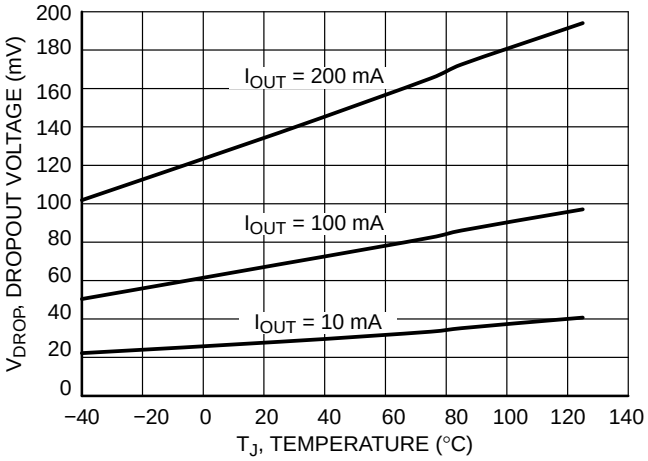


Figure 10. Dropout Voltage vs. Temperature − V_{OUT},nom = 1.05 V − CSP4 Package

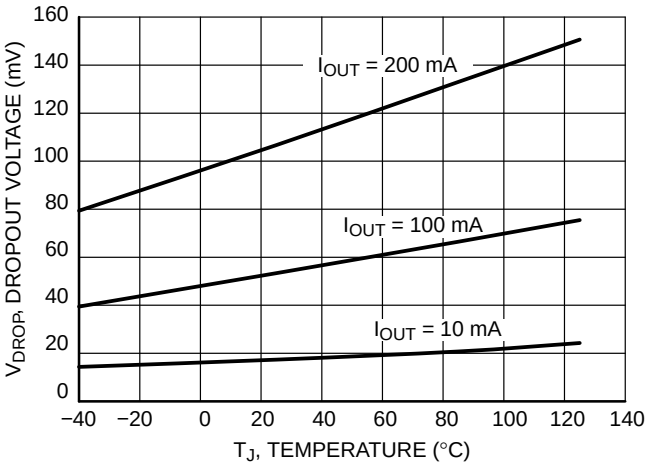


Figure 11. Dropout Voltage vs. Temperature − V_{OUT},nom = 1.2 V − CSP4 Package

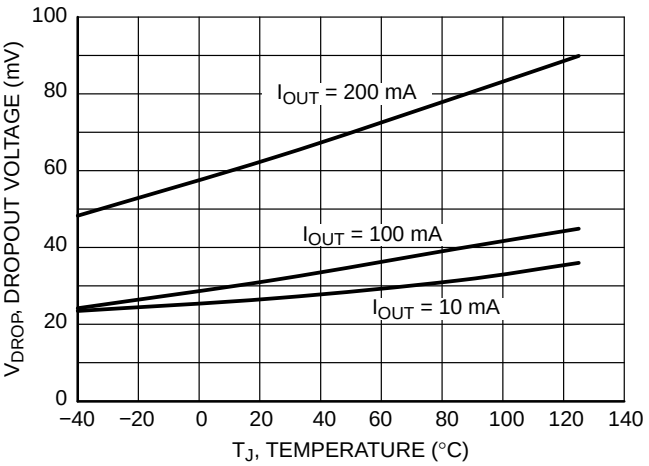


Figure 12. Dropout Voltage vs. Temperature − V_{OUT},nom = 1.8 V − CSP4 Package

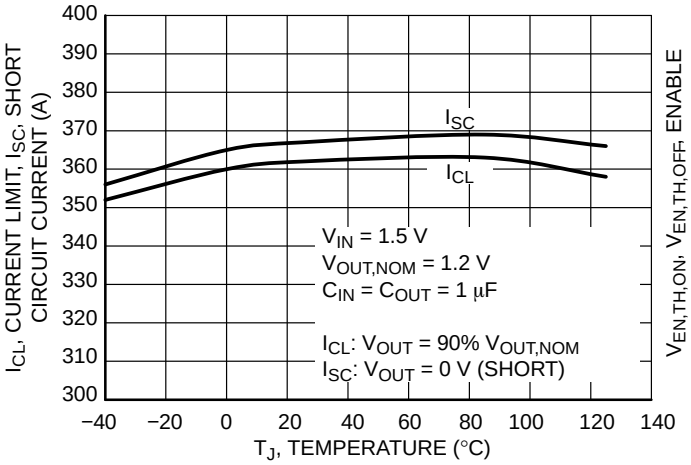


Figure 13. Short−circuit Current vs. Temperature

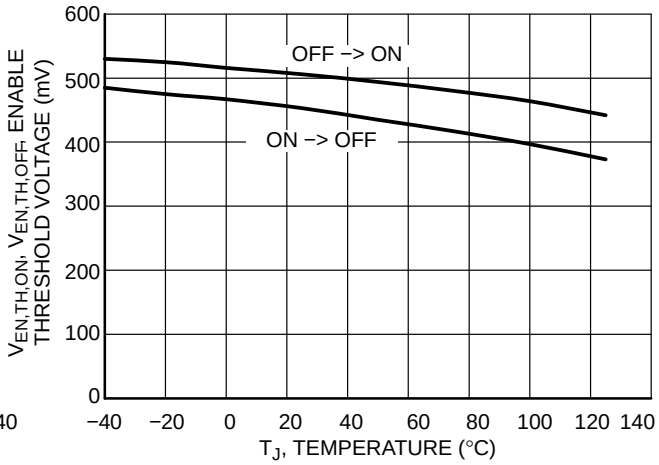


Figure 14. Enable thresholds voltage vs. Temperature

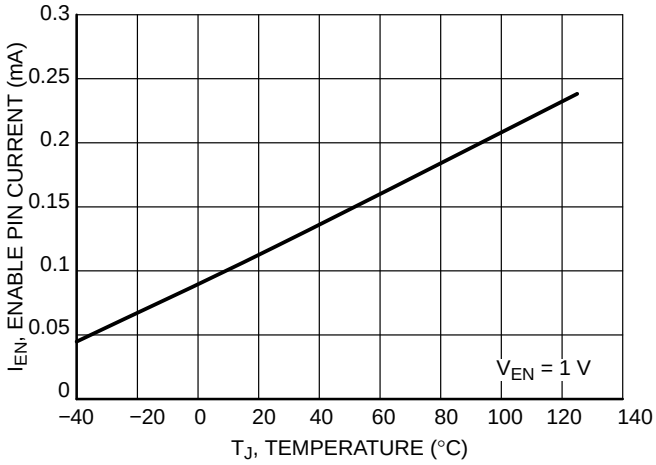


Figure 15. Enable Pin Current vs. Temperature

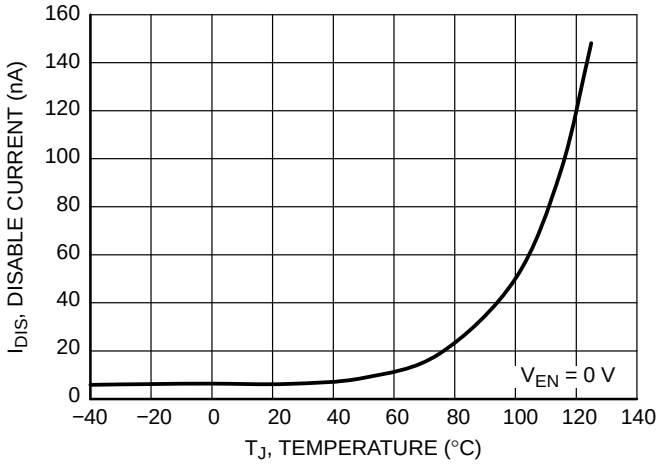


Figure 16. Disable Current vs. Temperature

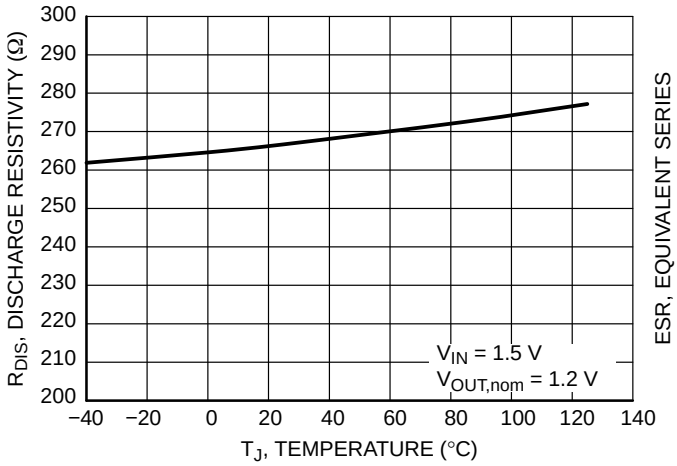


Figure 17. Discharge Resistivity vs. Temperature

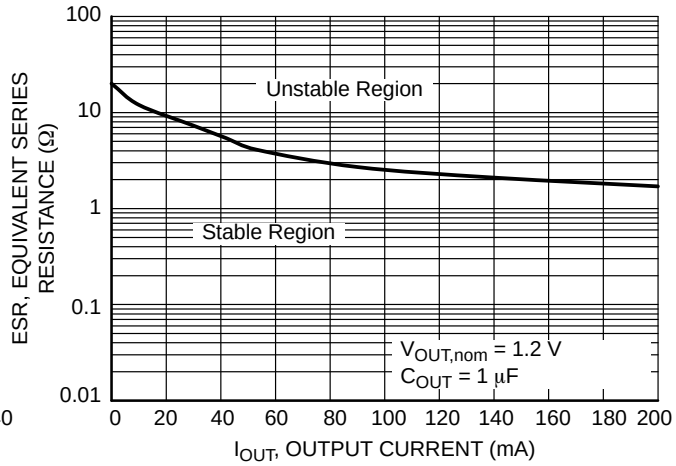


Figure 18. Maximum C_{OUT} ESR Value vs. Output Current

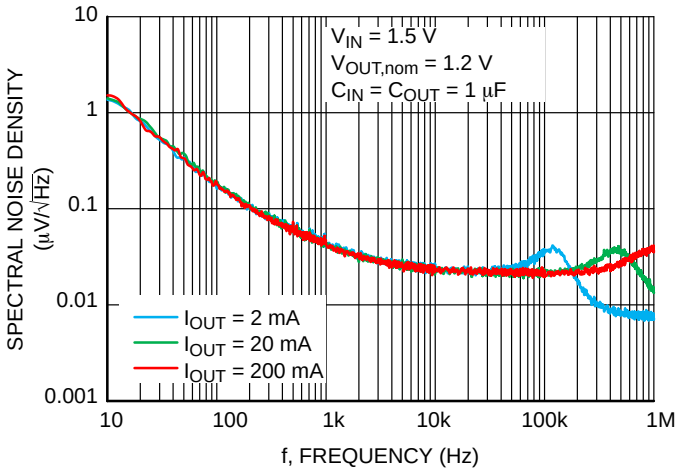


Figure 19. Output Voltage Spectral Noise Density vs. Frequency

I_{OUT} (mA)	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
2	10.01	8.79
20	8.78	7.39
200	8.77	7.44

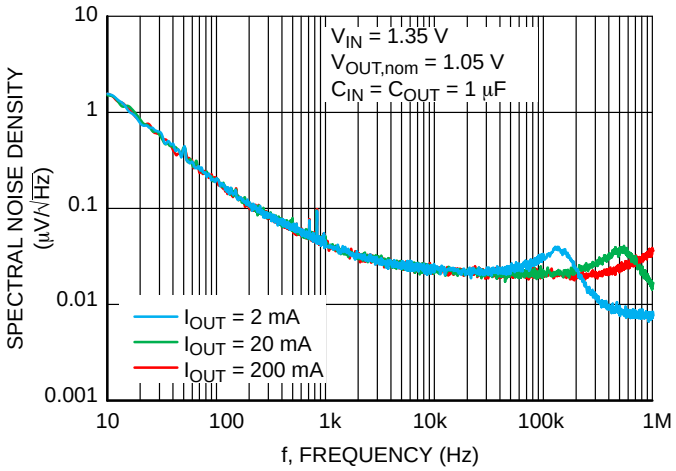


Figure 20. Output Voltage Spectral Noise Density vs. Frequency

I_{OUT} (mA)	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
2	10.01	8.79
20	8.78	7.39
200	8.77	7.44

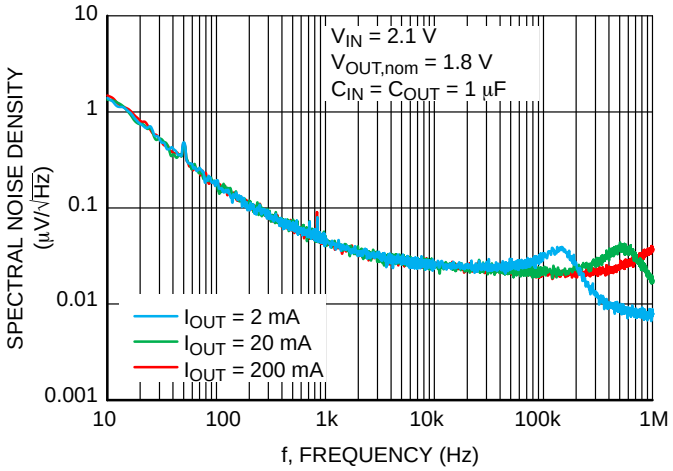


Figure 21. Output Voltage Spectral Noise Density vs. Frequency

I_{OUT} (mA)	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
2	9.88	8.71
20	9.01	7.73
200	9.08	7.70

TYPICAL CHARACTERISTICS

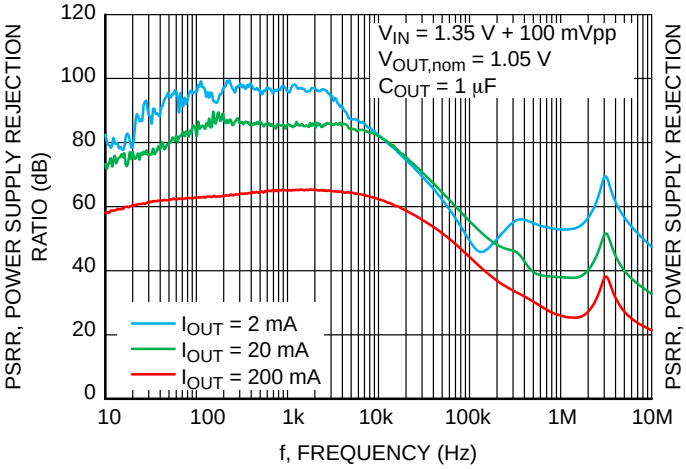


Figure 22. PSRR vs. Frequency

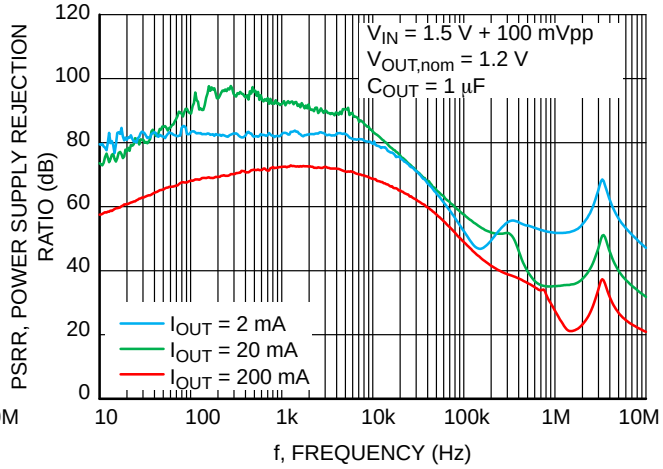


Figure 23. PSRR vs. Frequency

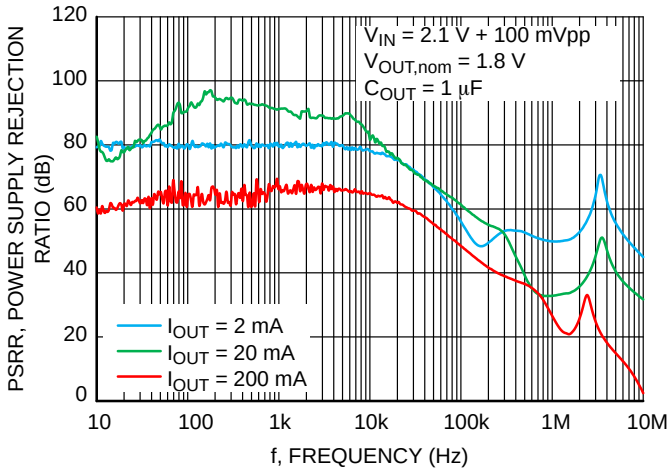


Figure 24. PSRR vs. Frequency

TYPICAL CHARACTERISTICS

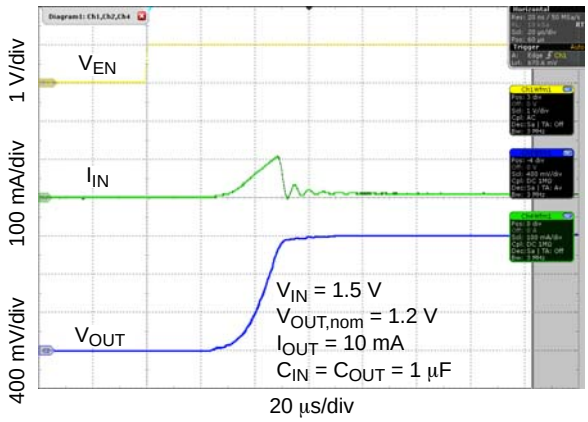


Figure 25. Enable Turn−on Response, C_{OUT} = 1 μF, I_{OUT} = 10 mA

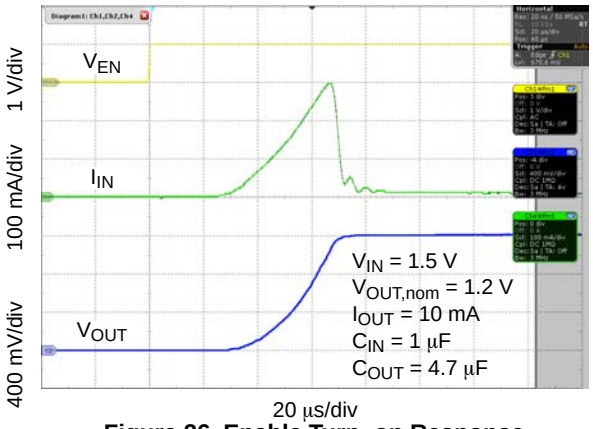


Figure 26. Enable Turn−on Response, C_{OUT} = 4.7 μF, I_{OUT} = 10 mA

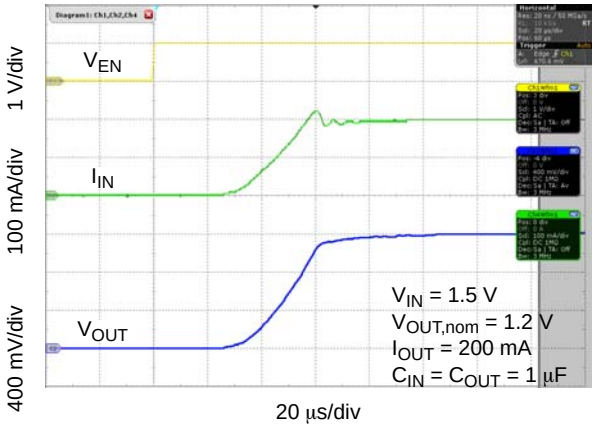


Figure 27. Enable Turn−on Response, C_{OUT} = 1 μF, I_{OUT} = 200 mA

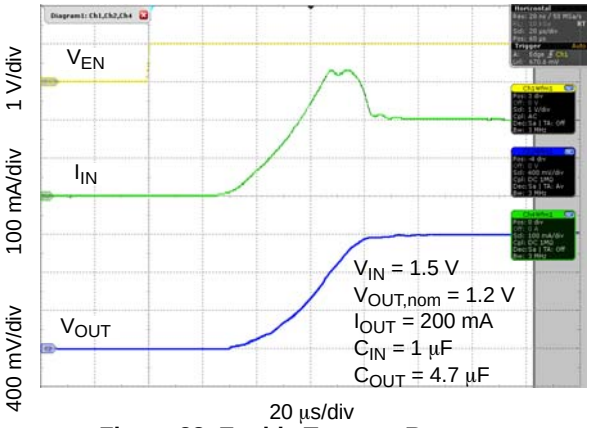


Figure 28. Enable Turn−on Response, C_{OUT} = 4.7 μF, I_{OUT} = 200 mA

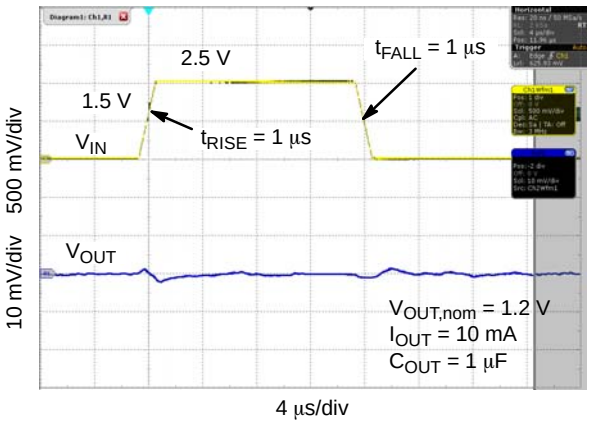


Figure 29. Line Transient Response, I_{OUT} = 10 mA

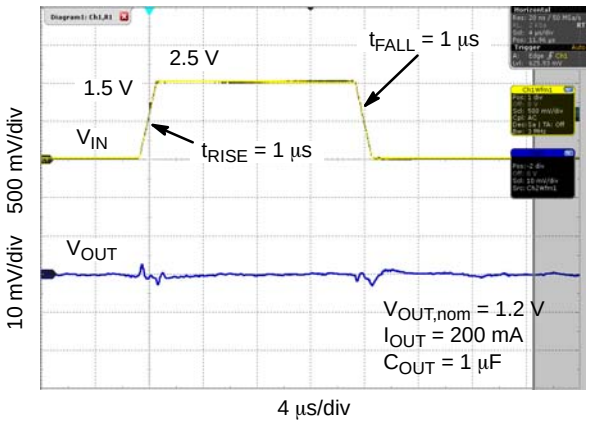


Figure 30. Line Transient Response, I_{OUT} = 200 mA

TYPICAL CHARACTERISTICS

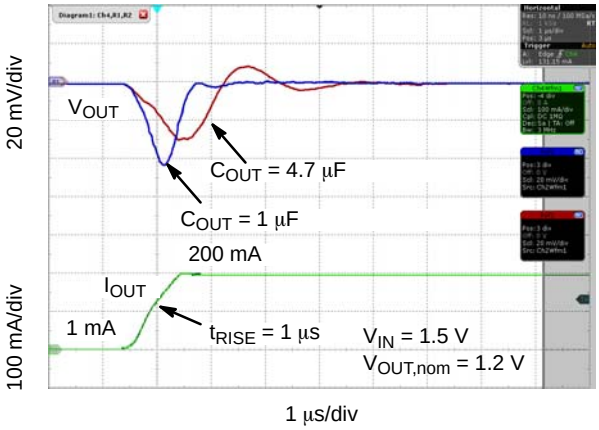


Figure 31. Load Transient Response, I_{OUT} = 1 mA to 200 mA

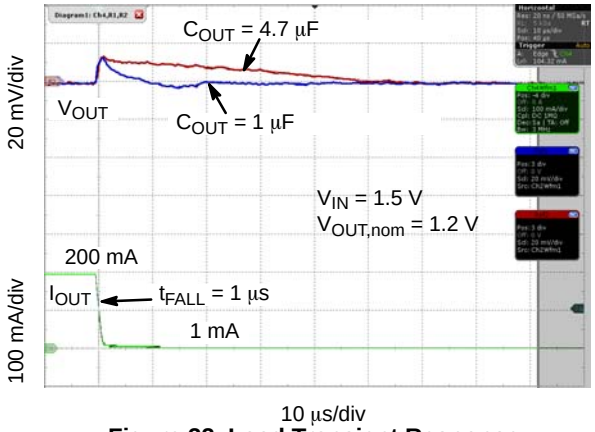


Figure 32. Load Transient Response, I_{OUT} = 1 mA to 200 mA

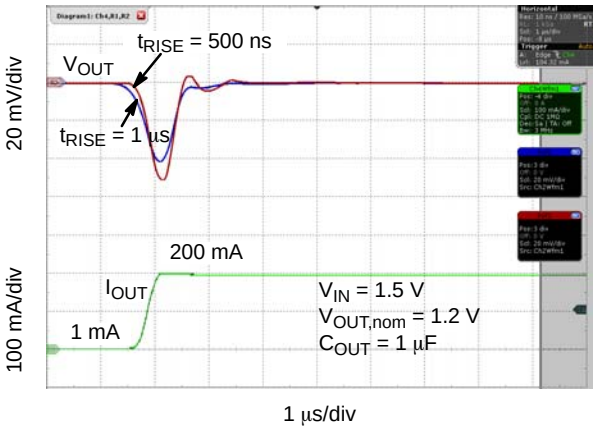


Figure 33. Load Transient Response, I_{OUT} = 1 mA to 200 mA

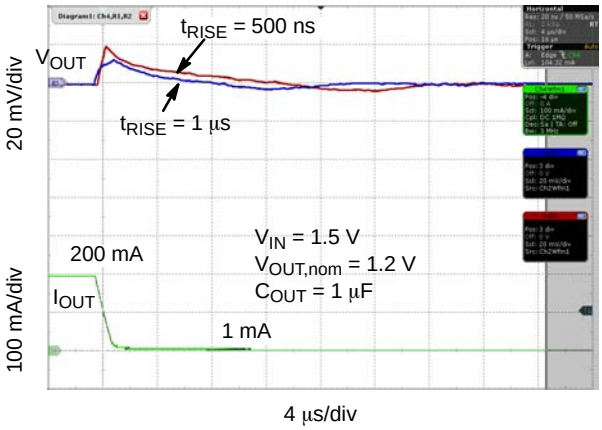


Figure 34. Load Transient Response, I_{OUT} = 1 mA to 200 mA

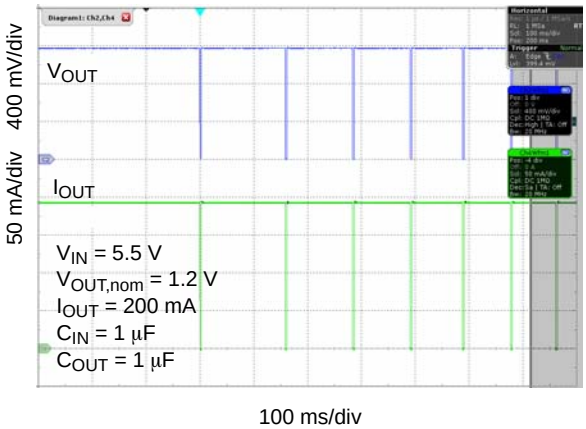


Figure 35. Overheating Protection − TSD

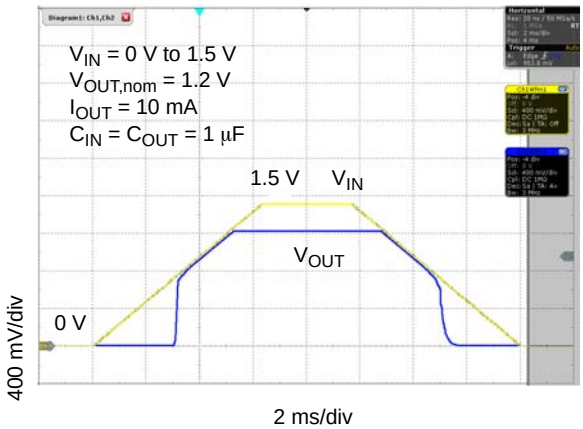


Figure 36. Turn On/Off, Slow Rising V_{IN}

TYPICAL CHARACTERISTICS

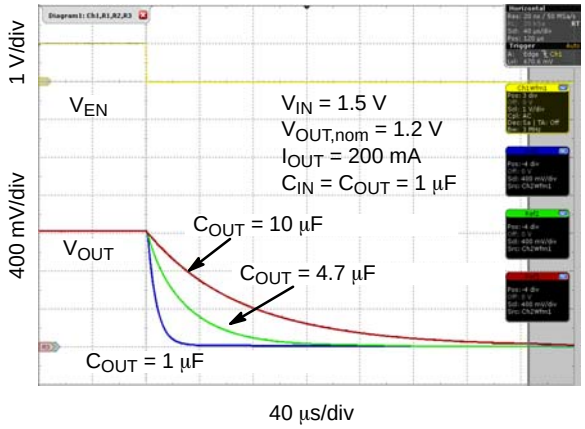


Figure 37. Enable Turn−off Response, Various Output Capacitors

APPLICATIONS INFORMATION

General

The NCP110 is an ultra−low input voltage, ultra−low noise 200 mA low dropout regulator designed to meet the requirements of low voltage RF applications and high performance analog circuits. The NCP110 device provides very high PSRR and excellent dynamic response. In connection with low quiescent current this device is well suitable for battery powered application such as cell phones, tablets and other. The NCP110 is fully protected in case of current overload, output short circuit and overheating.

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary for ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μF or greater to ensure the best dynamic performance. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Output decoupling

The NCP110 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCP110 is designed to remain stable with minimum effective capacitance of 0.6μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias. Please refer to Figure 38.

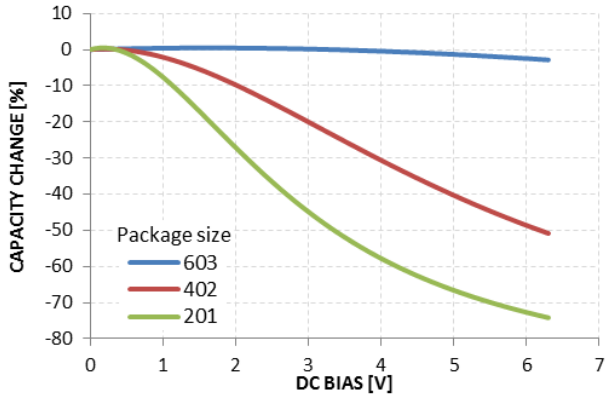


Figure 38. Capacity vs DC Bias Voltage

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 1.6 Ω. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature.

Enable Operation

The NCP110 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function. If the EN pin voltage is <0.2 V the device is guaranteed to be disabled. The pass transistor is turned−off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 280 Ω resistor. In the disable state the device consumes as low as typ. 10 nA from the V_{IN}. If the EN pin voltage >0.7 V the device is guaranteed to be enabled. The NCP110 regulates the output voltage and the active discharge transistor is turned−off. The EN pin has internal pull−down current source with typ. value of 200 nA which assures that the device is turned−off when the EN pin is not connected. In the case where the EN function isn't required the EN should be tied directly to IN.

Output Current Limit

Output Current is internally limited within the IC to a typical 350 mA. The NCP110 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 360 mA (typ). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (TSD − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (TSDU − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCP110 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature

rise for the part. The maximum power dissipation the NCP110 can handle is given by:

$$P_{D(MAX)} = \frac{[125^{\circ}C - T_A]}{\theta_{JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCP110 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN} \cdot I_{GND} + I_{OUT}(V_{IN} - V_{OUT}) \quad \text{(eq. 2)}$$

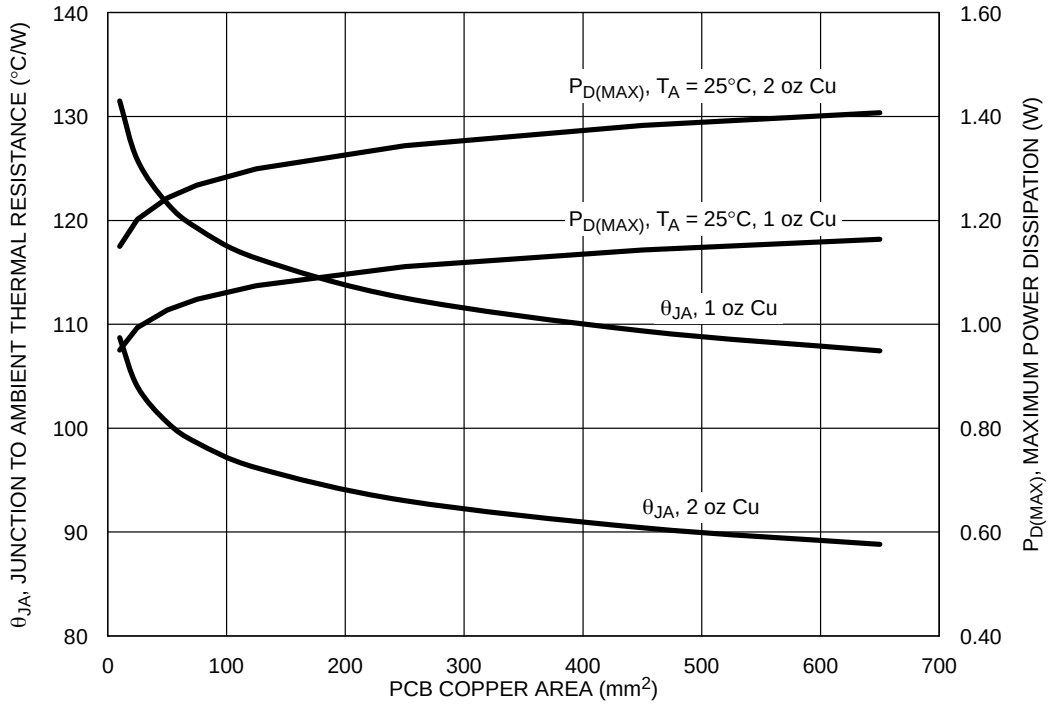


Figure 39. θ_{JA} and $P_{D\ (MAX)}$ vs. Copper Area (CSP4)

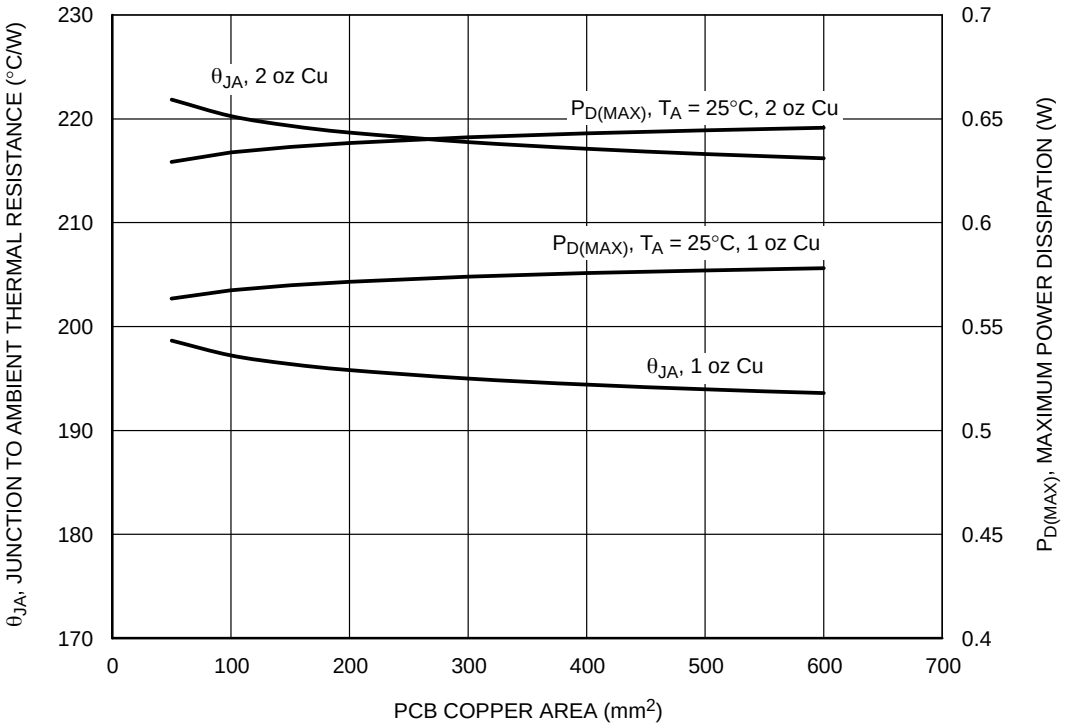


Figure 40. θ_{JA} and $P_{D\ (MAX)}$ vs. Copper Area (XDFN4)

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Rotation	Description	Package	Shipping†
NCP110AFCT060T2G	0.60 V	C	0°	200 mA, Active Discharge	WLCSP4 CASE 567VS (Pb-Free)	5000 / Tape & Reel
NCP110AFCT080T2G	0.80 V	J	0°			
NCP110AFCT085T2G	0.85 V	2	0°			
NCP110AFCT105T2G	1.05 V	A	0°			
NCP110AFCT110T2G	1.10 V	G	0°			
NCP110AFCT120T2G	1.20 V	F	0°			
NCP110AFCT180T2G	1.80 V	D	0°			
NCP110AFCT280T2G	2.80 V	E	0°			

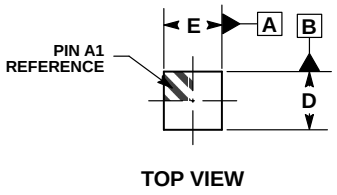
ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Description	Package	Shipping
NCP110AMX060TBG	0.60 V	FC	200 mA, Active Discharge	XDFN4 CASE 711AJ (Pb-Free)	3000 / Tape & Reel
NCP110AMX075TBG	0.75 V	F3			
NCP110AMX080TBG	0.80 V	FJ			
NCP110AMX085TBG	0.85 V	F2			
NCP110AMX105TBG	1.05 V	FA			
NCP110AMX110TBG	1.10 V	FH			
NCP110AMX120TBG	1.20 V	FF			
NCP110AMX180TBG	1.80 V	FD			
NCP110AMX280TBG	2.80 V	FE			

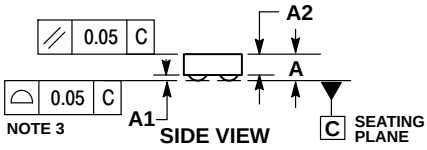
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

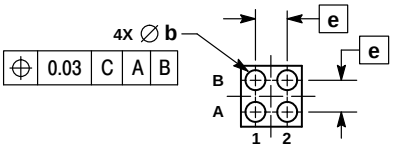
WLCSP4, 0.64x0.64x0.33
CASE 567VS
ISSUE O



TOP VIEW



SIDE VIEW

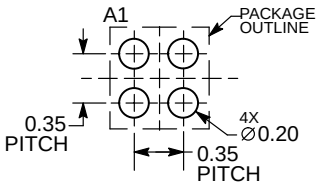


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	---	---	0.33
A1	0.04	0.06	0.08
A2	0.23 REF		
b	0.180	0.200	0.220
D	0.610	0.640	0.670
E	0.610	0.640	0.670
e	0.35 BSC		

RECOMMENDED SOLDERING FOOTPRINT*

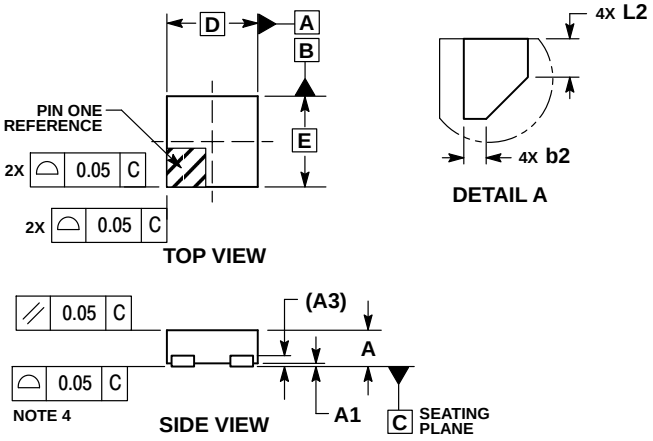


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

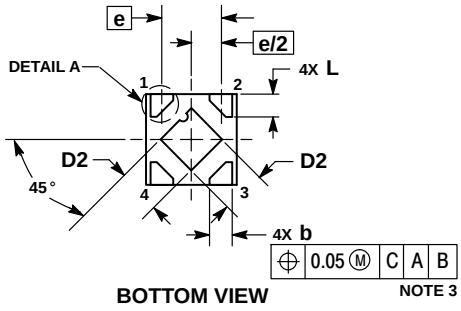
PACKAGE DIMENSIONS

XDFN4 1.0x1.0, 0.65P
CASE 711AJ
ISSUE A

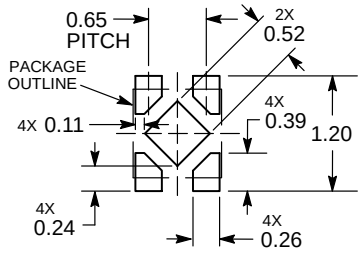


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.33	0.43
A1	0.00	0.05
A3	0.10 REF	
b	0.15	0.25
b2	0.02	0.12
D	1.00 BSC	
D2	0.43	0.53
E	1.00 BSC	
e	0.65 BSC	
L	0.20	0.30
L2	0.07	0.17



RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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