NBSG16M

2.5 V/3.3 V Multilevel Input to CML Clock/Data Receiver/Driver/Translator Buffer

ON Semiconductor®

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QFN−16
MN SUFFIX
CASE 485G

Description

The NBSG16M is a differential current mode logic (CML) receiver/driver/translator buffer. The device is functionally equivalent to the EP16, LVEP16, or SG16 devices with CML output structure and lower EMI capabilities.

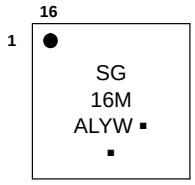
Inputs incorporate internal 50 Ω termination resistors and accept LVNECL (Negative ECL), LVPECL (Positive ECL), LVTTL, LVCMOS, CML, or LVDS. The CML output structure contains internal 50 Ω source termination resistor to V_{CC}. The device generates 400 mV output amplitude with 50 Ω receiver resistor to V_{CC}.

The V_{BB} pin is internally generated voltage supply available to this device only. For all single-ended input conditions, the unused complementary differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} output should be left open.

Features

- Maximum Input Clock Frequency > 10 GHz Typical
- Maximum Input Data Rate > 10 Gb/s Typical
- 120 ps Typical Propagation Delay
- 35 ps Typical Rise and Fall Times
- Positive CML Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- Negative CML Output with RSNECL or NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.465 V
- CML Output Level; 400 mV Peak-to-Peak Output with 50 Ω Receiver Resistor to V_{CC}
- 50 Ω Internal Input and Output Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, LVEL and SG Devices
- V_{BB} Reference Voltage Output
- These are Pb-Free Devices

MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

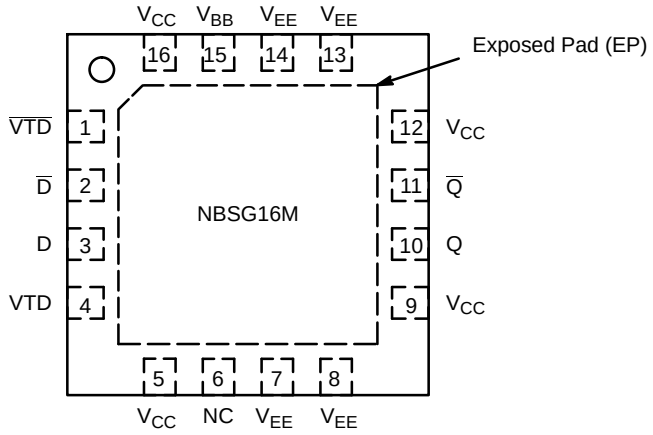


Figure 1. QFN−16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	$\overline{V_{TD}}$	−	Internal 50 Ω Termination Pin. See Table 2. (Note 2)
2	$\overline{D}$	LVDS, CML, ECL, LVTTL, LVCMOS Input	Inverted Differential Input (Note 2)
3	D	LVDS, CML, ECL, LVTTL, LVCMOS Input	Noninverted Differential Input. (Note 2)
4	V_{TD}	−	Internal 50 Ω Termination Pin. See Table 2. (Note 2)
5	V_{CC}	−	Positive Supply Voltage. All V_{CC} pins must be externally connected to Power Supply to guarantee proper operation.
6	NC	−	No Connect
7	V_{EE}	−	Negative Supply Voltage. All V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.
8	V_{EE}	−	Negative Supply Voltage. All V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.
9	V_{CC}	−	Positive Supply Voltage. All V_{CC} pins must be externally connected to Power Supply to guarantee proper operation.
10	Q	CML Output	Noninverted CML Differential Output with Internal 50 Ω Source Termination Resistor. (Note 1)
11	$\overline{Q}$	CML Output	Inverted CML Differential Output with Internal 50 Ω Source Termination Resistor. (Note 1)
12	V_{CC}	−	Positive Supply Voltage. All V_{CC} pins must be externally connected to Power Supply to guarantee proper operation.
13	V_{EE}	−	Negative Supply Voltage. All V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.
14	V_{EE}	−	Negative Supply Voltage. All V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.
15	V_{BB}	−	Internally Generated ECL Reference Output Voltage
16	V_{CC}	−	Positive Supply Voltage. All V_{CC} pins must be externally connected to Power Supply to guarantee proper operation.
−	EP	−	The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die but may be electrically and thermally connected to V_{EE} on the PC board.

1. CML outputs require 50 Ω receiver termination resistor to V_{CC} for proper operation.
2. In the differential configuration when the input termination pin (V_{TD}, $\overline{V_{TD}}$) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self-oscillation.

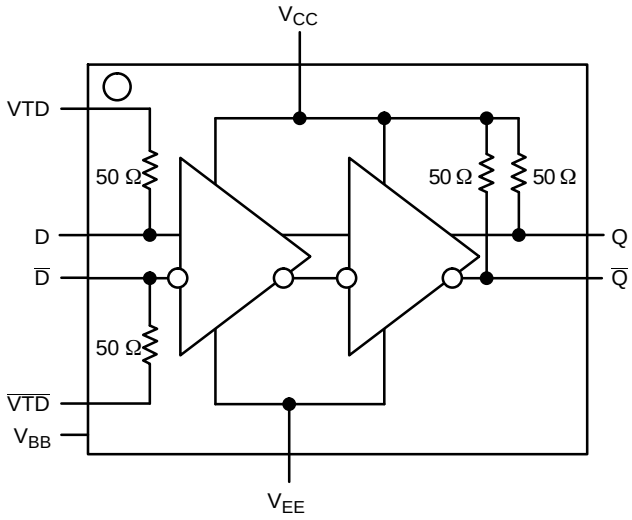


Figure 2. Logic Diagram

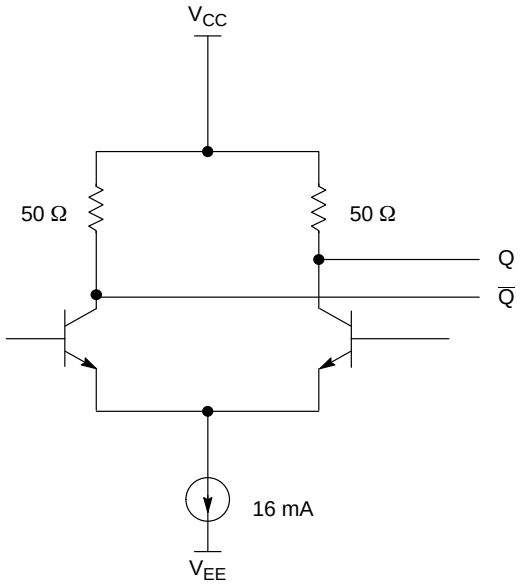


Figure 3. CML Output Structure

Table 2. Interfacing Options

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD and $\overline{VTD}$ to V_{CC}
LVDS	Connect VTD and $\overline{VTD}$ together
AC−COUPLED	Bias VTD and $\overline{VTD}$ Inputs within (V_{IHCMR}) Common Mode Range
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL, LVCMOS	An external voltage should be applied to the unused complementary differential input. Nominal voltage 1.5 V for LVTTL and V_{CC}/2 for LVCMOS inputs.

Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model Charged Device Model	> 1 kV > 100 V > 4 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 3)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		145
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		−3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 −3.6	V
V_{INPP}	Differential Input Voltage |D − $\overline{D}$|	$V_{CC} - V_{EE} \ge 2.8$ V $V_{CC} - V_{EE} < 2.8$ V		2.8 $\|V_{CC} - V_{EE}\|$	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA
I_{out}	Output Current	Continuous Surge		25 50	mA
I_{BB}	V_{BB} Sink/Source			1.0	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 4)	0 lfpm 500 lfpm		42 35	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	1S2P (Note 4)		4.0	°C/W
T_{sol}	Wave Solder Pb-Free	<2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. JEDEC standard multilayer board − 1S2P (1 signal, 2 power)

Table 5. DC CHARACTERISTICS, POSITIVE CML OUTPUT
(V_{CC} = 2.5 V; V_{EE} = 0 V) (Note 5)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
POWER SUPPLY CURRENT											
I_{CC}	Positive Power Supply Current	37	43	51	37	43	51	37	43	51	mA
CML OUTPUTS (Note 6)											
V_{OH}	Output HIGH Voltage	V_{CC} − 40	V_{CC} − 10	V_{CC}	V_{CC} − 40	V_{CC} − 10	V_{CC}	V_{CC} − 40	V_{CC} − 10	V_{CC}	mV
V_{OL}	Output LOW Voltage		V_{CC} − 400	V_{CC} − 330		V_{CC} − 400	V_{CC} − 330		V_{CC} − 400	V_{CC} − 330	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 8 & 10) (Note 7)											
V_{IH}	Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Input LOW Voltage	0		V_{IH} − 150	0		V_{IH} − 150	0		V_{IH} − 150	mV
V_{th}	Input Threshold Voltage Range (Note 8)	950		V_{CC} − 75	950		V_{CC} − 75	950		V_{CC} − 75	mV
V_{ISE}	Single-Ended Input Voltage (V_{IH} − V_{IL})	150		2600	150		2600	150		260	mV
V_{BB}	ECL Reference Output Voltage	1075	1170	1265	1075	1170	1265	1075	1170	1265	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 9 & 11) (Note 9)											
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	0		V_{IHD} − 75	0		V_{IHD} − 75	0		V_{IHD} − 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 10) (Figure 12)	1200		2500	1200		2500	1200		2500	mV
I_{IH}	Input HIGH Current (@V_{IH})		60	100		60	100		60	100	μA
I_{IL}	Input LOW Current (@V_{IL})		25	50		25	50		25	50	μA
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with V_{CC}.
6. All loading with 50 Ω to V_{CC} − 2.0 V.
7. V_{th}, V_{IH}, $V_{IL,}$ and V_{ISE} parameters must be complied with simultaneously.
8. V_{th} is applied to the complementary input when operating in single-ended mode. V_{th} = (V_{IH} − V_{IL}) / 2.
9. V_{IHD}, $V_{ILD,}$ V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
10. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. DC CHARACTERISTICS, POSITIVE CML OUTPUT
(V_{CC} = 3.3 V; V_{EE} = 0 V) (Note 11)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY CURRENT											
I_{CC}	Positive Power Supply Current	37	43	51	37	43	51	37	43	51	mA
CML OUTPUTS (Note 12)											
V_{OH}	Output HIGH Voltage	V_{CC} − 40	V_{CC} − 10	V_{CC}	V_{CC} − 40	V_{CC} − 10	V_{CC}	V_{CC} − 40	V_{CC} − 10	V_{CC}	mV
V_{OL}	Output LOW Voltage		V_{CC} − 400	V_{CC} − 330		V_{CC} − 400	V_{CC} − 330		V_{CC} − 400	V_{CC} − 330	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 8 & 10) (Note 13)											
V_{IH}	Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Input LOW Voltage	0		V_{IH} − 150	0		V_{IH} − 150	0		V_{IH} − 150	mV
V_{th}	Input Threshold Voltage Range (Note 14)	950		V_{CC} − 75	950		V_{CC} − 75	950		V_{CC} − 75	mV
V_{ISE}	Single-Ended Input Voltage (V_{IH} − V_{IL})	150		2600	150		2600	150		260	mV
V_{BB}	ECL Reference Voltage Output	1875	1970	2065	1875	1970	2065	1875	1970	2065	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 9 & 11) (Note 15)											
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	0		V_{IHD} − 75	0		V_{IHD} − 75	0		V_{IHD} − 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 16) (Figure 12)	1200		3300	1200		3300	1200		3300	mV
I_{IH}	Input HIGH Current (@V_{IH})		60	100		60	100		60	100	μA
I_{IL}	Input LOW Current (@V_{IL})		25	50		25	50		25	50	μA
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Input and output parameters vary 1:1 with V_{CC}.
12. All loading with 50 Ω to V_{CC} − 2.0 V.
13. V_{th}, V_{IH}, $V_{IL,}$ and V_{ISE} parameters must be complied with simultaneously.
14. V_{th} is applied to the complementary input when operating in single-ended mode. V_{th} = (V_{IH} − V_{IL}) / 2.
15. V_{IHD}, $V_{ILD,}$ V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
16. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. DC CHARACTERISTICS, NEGATIVE CML OUTPUT
(V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V) (Note 17)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
POWER SUPPLY CURRENT											
I_{CC}	Positive Power Supply Current	37	43	51	37	43	51	37	43	51	mA
CML OUTPUTS (Note 18)											
V_{OH}	Output HIGH Voltage	V_{CC} − 40	V_{CC} − 10	V_{CC}	V_{CC} − 40	V_{CC} − 10	V_{CC}	V_{CC} − 40	V_{CC} − 10	V_{CC}	mV
V_{OL}	Output LOW Voltage		V_{CC} − 400	V_{CC} − 330		V_{CC} − 400	V_{CC} − 330		V_{CC} − 400	V_{CC} − 330	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 8 & 10) (Note 19)											
V_{IH}	Input HIGH Voltage	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	mV
V_{IL}	Input LOW Voltage	V_{EE}		V_{IH} − 150	V_{EE}		V_{IH} − 150	V_{EE}		V_{IH} − 150	mV
V_{th}	Input Threshold Voltage Range (Note 20)	V_{EE} + 950		V_{CC} − 75	V_{EE} + 950		V_{CC} − 75	V_{EE} + 950		V_{CC} − 75	mV
V_{ISE}	Single-Ended Input Voltage (V_{IH} − V_{IL})	150		2600	150		2600	150		260	mV
V_{BB}	ECL Reference Voltage Output	−1425	−1330	−1235	−1425	−1330	−1235	−1425	−1330	−1235	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 9 & 11) (Note 21)											
V_{IHD}	Differential Input HIGH Voltage	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{IHD} − 75	V_{EE}		V_{IHD} − 75	V_{EE}		V_{IHD} − 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 22) (Figure 12)	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	mV
I_{IH}	Input HIGH Current (@V_{IH})		60	100		60	100		60	100	μA
I_{IL}	Input LOW Current (@V_{IL})		25	50		25	50		25	50	μA
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

17. Input and output parameters vary 1:1 with V_{CC}.
18. All loading with 50 Ω to V_{CC} − 2.0 V.
19. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
20. V_{th} is applied to the complementary input when operating in single-ended mode. V_{th} = (V_{IH} − V_{IL}) / 2.
21. V_{IHD}, V_{ILD}, V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
22. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 8. AC CHARACTERISTICS

(V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude (f_{in} < 7 GHz) (See Figure 4) (Note 23) (f_{in} < 10 GHz)	300 200	400 250		300 200	400 250		300 100	400 150		mV
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	90	110	150	100	120	150	100	125	155	ps
t_{SKEW}	Duty Cycle Skew (Note 24)		3	15		3	15		3	15	ps
t_{JITTER}	RMS Random Clock Jitter (Note 26) f_{in} < 10 GHz Peak-to-Peak Data Dependent Jitter (Note 27) f_{in} < 10 Gb/s		0.2 8	1 15		0.2 8	1 15		0.2 8	1.0 15	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 25)	75		2500	75		2500	75		2500	mV
t_r t_f	Output Rise/Fall Times @ 1 GHz (20% − 80%) Q, $\overline{Q}$	21	35	53	21	35	53	21	35	53	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

23. Measured using a 400 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}. Input edge rates 40 ps (20% − 80%).
24. See Figure 13 $t_{skew} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform.
25. $V_{INPP(max)}$ cannot exceed $V_{CC} - V_{EE}$. (Applicable only when $V_{CC} - V_{EE}$ < 2500 mV). Input voltage swing is a single-ended measurement operating in differential mode.
26. Additive RMS jitter with 50% duty cycle clock signal at 10GHz.
27. Additive Peak-to-Peak data dependent jitter with NRZ PRBS2^{31}–1 data rate at 10 Gb/s.

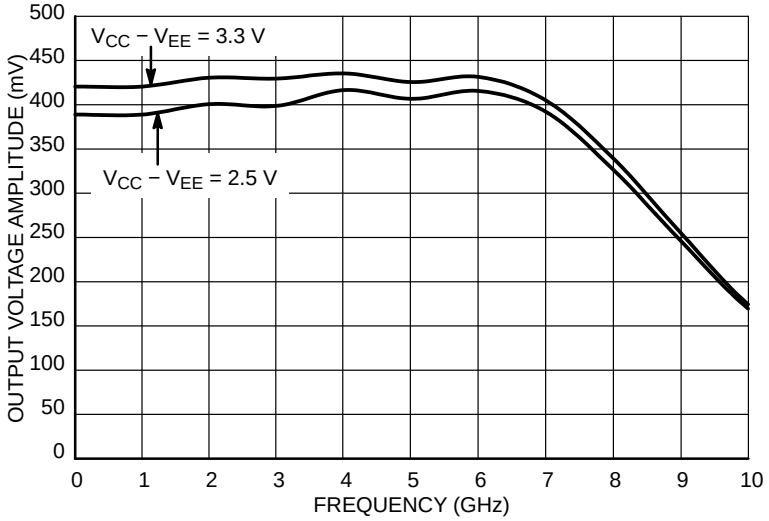


Figure 4. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{in}) at Ambient Temperature (Typical)

Application Information

All inputs can accept PECL, CML, and LVDS signal levels. The input voltage can range from V_{CC} to 1.2 V. Examples interfaces are illustrated below in a 50 Ω environment (Z = 50 Ω).

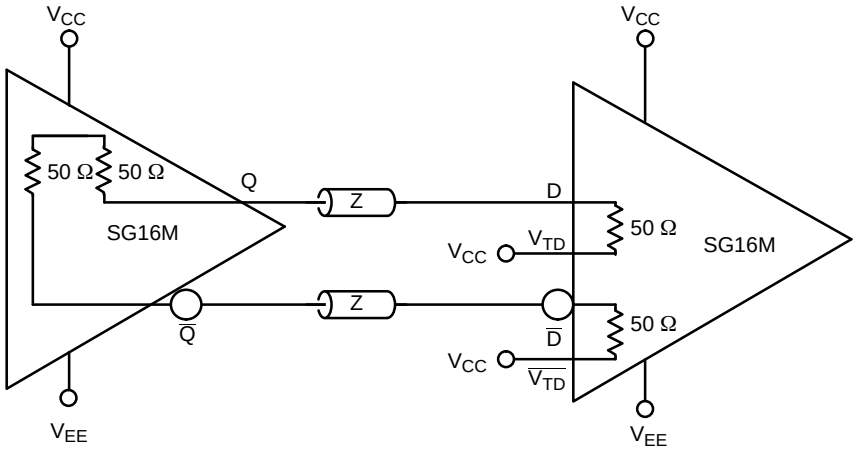
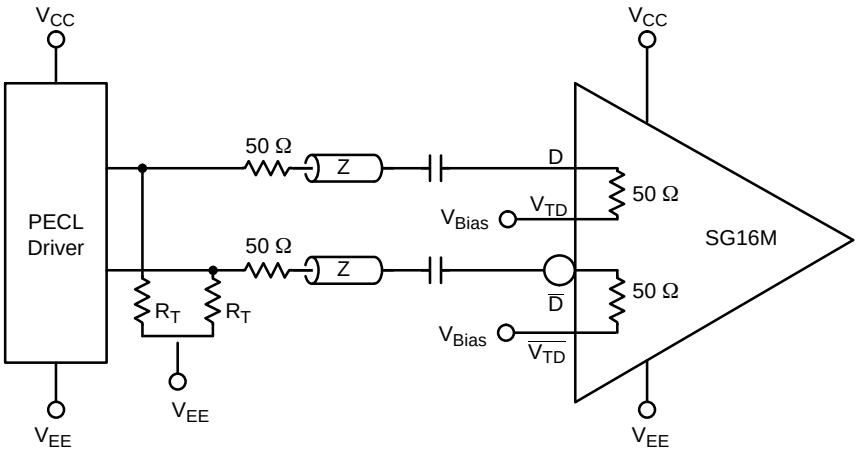


Figure 5. CML to CML Interface



Recommended R_T Values

V_{CC}	R_T
5.0 V	290 Ω
3.3 V	150 Ω
2.5 V	80 Ω

Figure 7. PECL to CML Receiver Interface

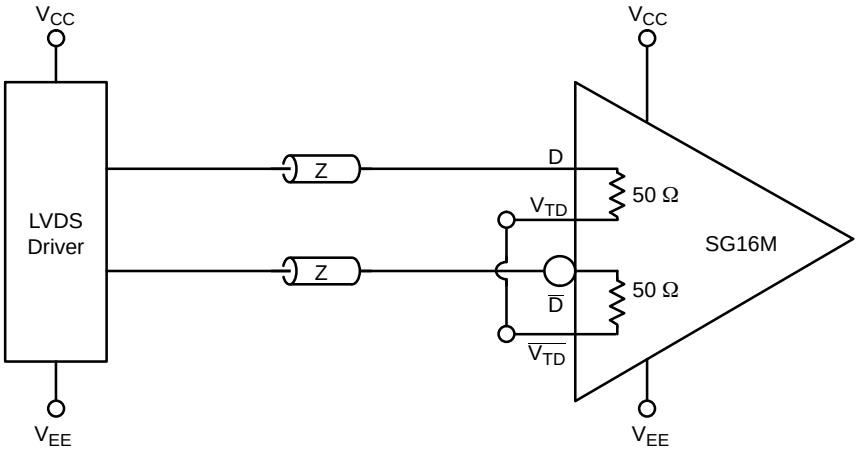


Figure 6. LVDS to CML Receiver Interface

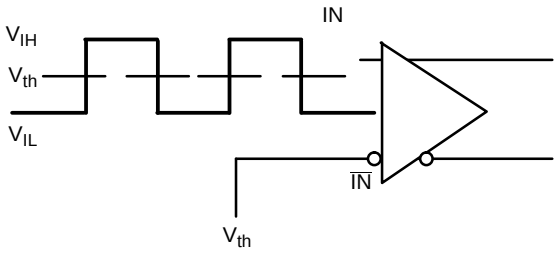


Figure 8. Differential Input Driven Single-Ended

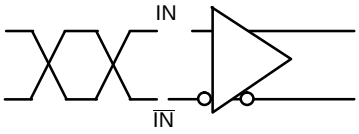


Figure 9. Differential Inputs Driven Differentially

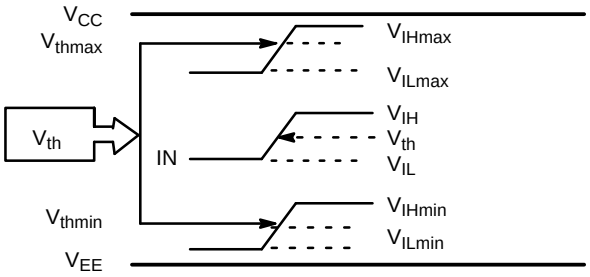


Figure 10. V_{th} Diagram

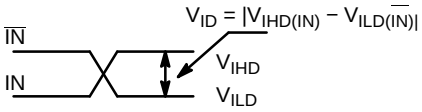


Figure 11. Differential Inputs Driven Differentially

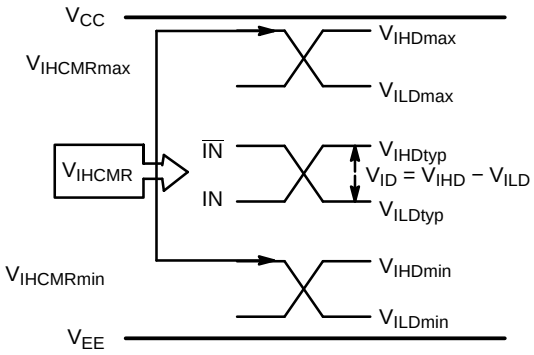


Figure 12. V_{IHCMR} Diagram

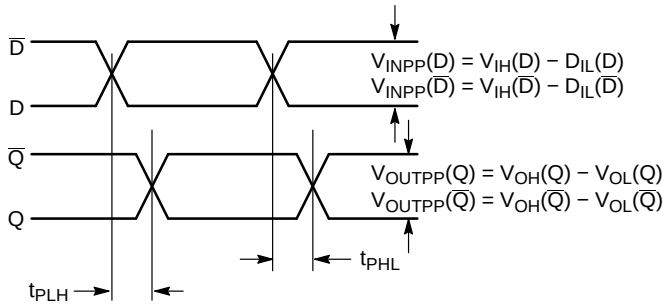


Figure 13. AC Reference Measurement

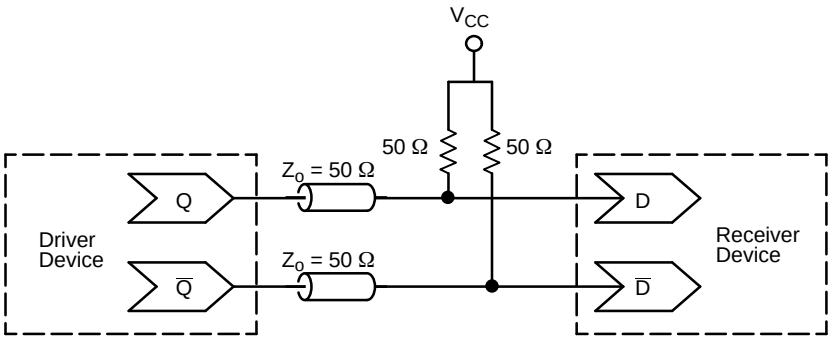


Figure 14. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 − Termination of ECL Logic Devices)

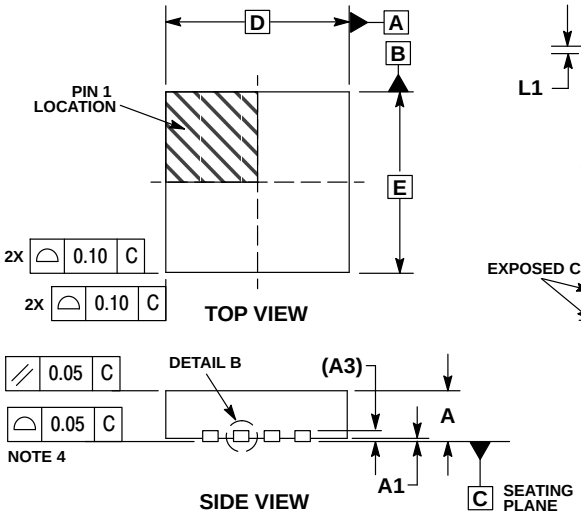
ORDERING INFORMATION

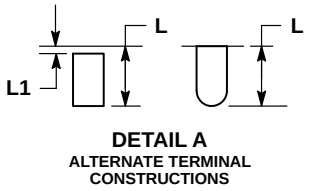
Device	Package	Shipping†
NBSG16MMNG	QFN-16 (Pb-Free / Halide-Free)	123 Units / Tube
NBSG16MMNR2G	QFN-16 (Pb-Free / Halide-Free)	3000 / Tape & Reel

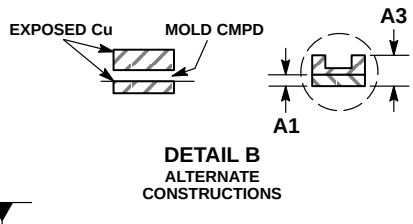
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485G
ISSUE F

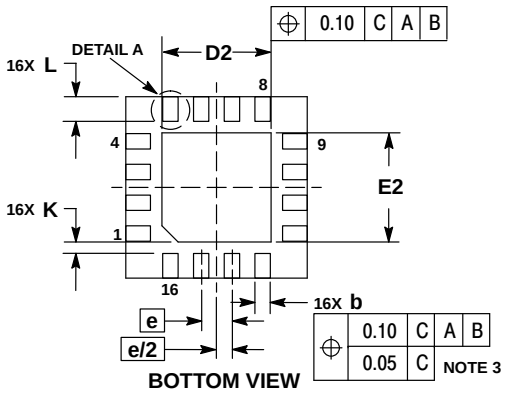




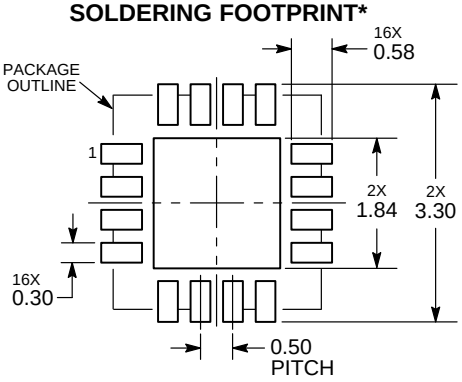


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.24	0.30
D		3.00 BSC	
D2	1.65	1.75	1.85
E		3.00 BSC	
E2	1.65	1.75	1.85
e		0.50 BSC	
K		0.18 TYP	
L	0.30	0.40	0.50
L1	0.00	0.08	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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