NAT9914

Pin compatible with TI TMS9914A Software compatible with NEC µPD7210 or TI TMS9914A controller chips Low power consumption Meets all IEEE 488.2 requirements Bus line monitoring Preferred implementation of requesting service Will not send messages when there are no Listeners Performs all IEEE 488.1 interface functions Programmable data transfer rate (T1 delays of 350 ns, 500 ns, 1.1 µs, and 2 µs) Automatic EOS and/or NL message detection Direct memory access (DMA) Automatically processes IEEE 488 commands and reads undefined commands

TTL-compatible CMOS device Programmable clock rate 20 MHz maximum Reduces driver overhead Does not lose a data byte if ATN is asserted while transmitting data



Description

The NAT9914 IEEE 488.2 controller chip can perform all the interface functions defined by the IEEE Standard 488.1-1987, and also meets the additional requirements and recommendations of the IEEE Standard 488.2-1987. Connected between the processor and the IEEE 488 bus, the NAT9914 provides highlevel management of the IEEE 488 bus, significantly increases the throughput of driver software, and simplifies both the hardware and software design. The NAT9914 performs complete IEEE 488 Talker, Listener, and Controller functions. In addition to its numerous improvements, the NAT9914 is also completely pin compatible with the TI TMS 9914A and software compatible with the NEC µPD7210 and TI TMS9914A controller chips.

IEEE 488.2 Overview

The IEEE 488.2 standard removes the ambiguities of IEEE 488.1 by standardizing the way instruments and controllers operate. It defines data formats, status reporting, error handling, and common configuration commands to which all IEEE 488.2 instruments must respond in a precise manner. It also defines a set of controller requirements. With IEEE 488.2, you gain the benefits of reduced development time and cost because systems are more compatible and reliable. The NAT9914 brings the full power of IEEE 488.2 to the design engineer along with numerous other design and performance benefits, while retaining the 40-pin and 44-pin hardware configurations of the TI TMS 9914A.

NATIONAL INSTRUMENTS

General

The NAT9914 manages the IEEE 488 bus. You program the IEEE 488 bus by writing control words into the appropriate registers. CPU-readable status registers supply operational feedback. The NAT9914 mode determines the function of these registers. On power up or reset, the NAT9914 registers resemble those of the TMS9914A set, with additional registers that supply extra functionality and IEEE 488.2 compatibility. In this mode, the NAT9914 is completely pin compatible with the TI TMS9914A. If you enable the 7210 mode, the registers resemble those of the NEC µPD7210 set, with additional registers that supply extra functionality and IEEE 488.2 compatibility. This mode is not pin compatible with the NECµPD7210. Figure 4 shows the key components of the NAT9914.



Figure 1. NAT9914BPD Pin Configuration



Figure 2. NAT9914BPL Pin Configuration



Figure 3. NAT9914BPQ Pin Configuration

Pin Identification

| PLCC DIP OFP Mnemonic Type Description 11, 12, 13, 10, 11, 12, 16, 17, 18, 17, 18, 17, 19, 16, 17, 18, 19, 20, 21, 17, 19, 16, 17, 12, 2, 24 D/7-0) D/0 Bidirectional 3-state data bus transfers commands, data, and status between the NAT9914 and the CPU. D0 is the most significant bit. 4 3 9 CE* I Chip Enable gives access to the register selected by a read or write operation, and the register selected by a read or write operation. 6 5 11 DBIN I With the Data Bus Input, you can place the contents of the register selected by RS(2-0) and CE* or to the data bus D(7-0). The polari of DBIN is reversed for DMA operation. 5 4 10 WE* I The Write input Lackes the contents of the register selected by RS(2-0) and CE* onto the data bus D(7-0). The polari of DBIN is reversed for DMA operation. 5 4 10 WE* I The Access Grant signal selects the DIR or CDOR for the current read or write cycle. 20 18 25 CLK I' The Access Request output asserts to request a DMA Acknowledge cycle. 21 19 26 RESET* I' Asserting the estate. NAT9914 in an initial (is state. 10 9 <th>riii luei</th> <th>Pin Number</th> <th></th> <th></th> <th colspan="2"></th> | riii luei | Pin Number | | | | |
|--|-------------|-------------|-------------|-------------|---------------------|--|
| 11, 12, 13, 14, 15, 16, 17, 19 10, 11, 12, 13, 14, 15, 16, 17 16, 17, 18, 22, 24 D(7-0) 100 Bidirectional 3-state data bus transfers commands, data, and status between the NAT9914 and the CPU. 4 3 9 CE* I Chip Enable gives access to the register selected by a read or write operation, and the register selects RS(2-0). 6 5 11 DBIN I' With the Data Bus Input, you can place the contents of the register selected by RS(2-0) and CE* onto the data bus D(7-0). The polari of DBIN is reversed for DMA operation. 5 4 10 WE* I The Write input latches the contents of the data bus D(7-0) into the register selected by RS(2-0). 3 2 8 ACCGR* I' The Access Grant signal selects the DIR or CDOR for the current read or write cycle. 20 18 25 CLK I' The Access Request output asserts twhen one of the data bus D(7-0) into the register selected by RS(2-0). 10 9 15 INT* 0 The Access Request output asserts when one of the unmasked interrupt conditions is true. The NAT9914 does not drive INT* high. The INT* pin must be pulled up by an extremal resistor. 24 22 29 REN* I/0.0' Bidirectional control line initializes the UO 31 28 3 | PLCC | | OFP | Mnemonic | Type | Description |
| 14, 15, 16, 17, 1913, 14, 15, 16, 1719, 20, 21, 22, 24Commands, data, and status between the NAT9914 and the CPU. D0 is the most significant bit.439CE*IChip Enable gives access to the register selected by a read or write operation, and the register selects RS(2-0).6511DBINI'With the Data Bus input, you can place the contents of the register selects QP(2-0).6511DBINI'With the Data Bus input, you can place the contents of the register selected by RS(2-0).5410WE*IThe Write input latches the contents of the rada bus D(7-0). The polari of DBIN is reversed for DMA operation.5410WE*IThe Access Request output asserts to reque a DMA Acknowledge cycle.217ACCRQ*0The Access Request output asserts to reque a DMA Acknowledge cycle.201825CLKI'The CLK input can be up to 20 MHz.211926RESET*I'Asserting the RESET* input places the NAT9914 does not dive. INT* injb. The INT* pin must be pulled up by an external resistor.9, 8, 78, 7, 614, 13, 12RS(2-0)I''The Register functional.242229REN*10''Bidirectional control line initiates whether data on the DI line initiates whether data control line initiates whether data on the DI lines is an interface or device deependent message.< | | | | | | |
| 17, 1916, 1722, 24Image: Constraint of the data bus D(7-0) into the register selected by RS(2-0), and CE* onto the data bus D(7-0) into the register selected by RS(2-0).5410WE*IThe Access Carnt signal selects the DIR or constraint of the data bus D(7-0) into the register selected by RS(2-0).328ACCRO*0The Access Carnt signal selects the DIR or constraint on write copel.21825CLKI'The CLK input can be up to 20 MHz.211926RESET*I'Asserting the RESET* input places the NAT9914 in an initial, ide state.10915INT*0The Interrupt output asserts when one of the unmasked interrupt conditions is true. The NAT9914 does not drive INT* high. The INT* pin must be pulled up by an external resistor.9,8,78,7,614,13,12RS(2-0)I''Recess during a read or write operation.242229REN*I/O''Bidirectional control line initializes the pravisor.332.836ATN*I/OBidirectional control line initializes whether data on the DIO lines | | | | D(7 0) | 1/0 | |
| Image: section of the section of th | | | | | | |
| 439CE*IChip Enable gives access to the register selected by a read or write operation, and the register selects RS(2-0).6511DBINI'With the Data Bus Input, you can place the contents of the register selected by RS(2-0) and CE* ont the data bus D(7-0). The polari of DBIN is reversed for DMA operation.5410WE*IThe Write input latches the contents of the data bus D(7-0) into the register selected by RS(2-0).328ACCGR*I'The Access Grant signal selects the DIR or CDDR for the current read or write cycle.217ACCRO*0The Access Request output asserts to reque: a DMA Acknowledge cycle.201825CLKI'The Access Request output asserts to reque: a DMA Acknowledge cycle.201825CLKI'Access the number of the unmasked interrupt conditions is true.10915INT*0The Interrupt output asserts when one of the unmasked interrupt conditions is true. The NAT9914 in an initial, idle state.9, 8, 78, 7, 614, 13, 12RS(2-0)I'''The Register Selects determine which register to access during a read or write operation.242229REN*1/0Bidirectional control line initializes the (CC)EEE 488 interface functions.312836ATN*1/0Bidirectional control line initializes the ted at on the DIO lines is an interface or device dependent message.322937SRQ*1/0Bi | 17, 17 | 10, 17 | 22,27 | | | |
| Image: Selected by a read or write operation, and the register selects RS(2-0).6511DBINI'With the Data Bus Input, you can place the contents of the register selected by RS(2-0).6511DBINI'With the Data Bus Input, you can place the contents of the register selected by RS(2-0).5410WE*IThe Write input latches the contents of the data bus D(7-0). The polar of DBIN is reversed for DMA operation.5410WE*IThe Write input latches the contents of the data bus D(7-0) into the register selected by RS(2-0).328ACCGR*I'The Access Grant signal selects the DIR or CDOR for the current read or write cycle.217ACCRQ*0The Access Request output asserts to request a DMA Acknowledge cycle.201825CLKI'The CLK input can be up to 20 MHz.211926RESET*I'Asserting the RESET* input places the NAT9914 in an initial, idle state.10915INT*0The Interrupt output asserts when one of the unmasked interrupt conditions is true. The NAT9914 does not drive INT* high. The INT* pin must be pulled up by an external resistor.282330IFC*I/0'."Bidirectional control line initializes the (COC)242229REN*I/0Bidirectional control line indicates whether data on the DO lines is an interface or device dependent message.312836ATN*I/0Bidirectional control line indicates service fro the controller.34 | Λ | 2 | 0 | CE * | | _ |
| Image: select | 4 | 5 | 7 | 0L | ' | |
| 6511DBINI'With the Data Bus Input, you can place the contents of the register selected by RS(2-0) and CE* onto the data bus D(7-0). The polari of DBIN is reversed for DMA operation.5410WE*IThe Write input latches the contents of the register selected by RS(2-0) and CE* onto the data bus D(7-0). The polari of DBIN is reversed for DMA operation.5410WE*IThe Write input latches the contents of the data bus D(7-0) into the register selected by RS(2-0).328ACCGR*I'The Access Grant signal selects the DIR or CDOR for the current read or write cycle.217ACCRQ*0The Access Request output asserts to request a DMA Acknowledge cycle.201825CLKI'The Access Request output asserts to request a DMA Acknowledge cycle.211926RESET*I'Asserting the RESET* input places the UNATION on NAT9914 in an initial, idle state.10915INT*0The Interrupt output asserts when one of the unmasked interrupt conditions is true. The NAT9914 does not drive INT* high. The INT* pin must be pulled up by an external resistor.9, 8, 78, 7, 614, 13, 12RS(2-0)I'''Bidirectional control line indicates whether data an the DIO line selects either remote or local control of devices.242229REN*1/0Bidirectional control line requests service for or local control of devices.312836ATN*1/0Bidirectional control line requests service for the controller.34, 35, 3631, 32, 33 <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> | | | | | | |
| Image: Section of the sectin sectin the sectin section of the sec | 6 | 5 | 11 | DBIN | T. | - |
| Image: series of the series | Ū | 5 | | DDIN | | |
| 111 | | | | | | |
| 5410WE*IThe Write input latches the contents of the data bus D(7-0) into the register selected by RS(2-0).328ACCGR*I'The Access Grant signal selects the DIR or CDOR for the current read or write cycle.217ACCRQ*0The Access Request output asserts to request a DMA Acknowledge cycle.201825CLKI'The CLK input can be up to 20 MHz.211926RESET*I'Asserting the RESET* input places the NAT9914 in an initial, idle state.10915INT*0The Interrupt output asserts when one of the unmasked interrupt conditions is true. The NAT9914 does not drive INT* high. The INT* pin must be pulled up by an external resistor.9, 8, 78, 7, 614, 13, 12RS(2-0)I''The Register Selects determine which register to access during a read or write operation.252330IFC*I/O.''Bidirectional control line initializes the IEEE 488 interface functions.242229REN*I/OBidirectional control line selects either remote data on the DIO lines is an interface or device dependent message.312836ATN*I/OBidirectional control line requests service fro the controller.34, 35, 36, 37, 38, 39, 34, 35, 3639, 40, 41, 2, 37, 38DIO(8-1)*I/OBidirectional control line requests service fro the controller. | | | | | | |
| Image: Section of the section of th | 5 | 4 | 10 | W/F* | 1 | - |
| Image: Section of the section of th | Ŭ | | 10 | | | |
| 328ACCGR*I'The Access Grant signal selects the DIR or CDOR for the current read or write cycle.217ACCRQ*0The Access Request output asserts to request a DMA Acknowledge cycle.201825CLKI'The CLK input can be up to 20 MHz.211926RESET*I'Asserting the RESET* input places the NAT9914 in an initial, idle state.10915INT* (OC)0The Interrupt output asserts when one of the unmasked interrupt conditions is true. The NAT9914 does not drive INT* high. The INT* pin must be pulled up by an external resistor.9, 8, 78, 7, 614, 13, 12RS(2-0)I'''The Register Selects determine which register to access during a read or write operation.252330IFC*I/O'.''Bidirectional control line initializes the IEEE 488 interface functions.242229REN*I/OBidirectional control line indicates whether data on the DIO lines is an interface or device dependent message.312836ATN*I/OBidirectional control line requests service fro the controller.34, 35, 36, (31, 32, 33, (34, 35, 36, (31, 32, 33,< | | | | | | |
| Image: Constraint of the current of the cur | 3 | 2 | 8 | ACCGR* | I, | |
| 217ACCRO*0The Access Request output asserts to request a DMA Acknowledge cycle.201825CLKI'The CLK input can be up to 20 MHz.211926RESET*I'Asserting the RESET* input places the NAT9914 in an initial, idle state.10915INT*0The Interrupt output asserts when one of the unmasked interrupt conditions is true. The NAT9914 does not drive INT* high. The INT* pin must be pulled up by an external resistor.9, 8, 78, 7, 614, 13, 12RS(2-0)I'''The Register Selects determine which register to access during a read or write operation.252330IFC*I/O''Bidirectional control line initializes the (OC)IEEE 488 interface functions.242229REN*I/OBidirectional control line selects either remote data on the DIO lines is an interface or device dependent message.312836ATN*I/O'Bidirectional control line requests service from the controller.34, 35, 36, 41, 41, 4237, 382, 3OIO(8-1)*I/O'Bidirectional control line requests service from the controller. | Ū | - | Ū | 100011 | | - |
| Image: Constraint of the constra | 2 | 1 | 7 | ACCRO* | 0 | _ |
| 201825CLKI'The CLK input can be up to 20 MHz.211926RESET*I'Asserting the RESET* input places the NAT9914 in an initial, idle state.10915INT*0The Interrupt output asserts when one of the unmasked interrupt conditions is true. The NAT9914 does not drive INT* high. The INT* pin must be pulled up by an external resistor.9, 8, 78, 7, 614, 13, 12RS(2-0)I'''The Register Selects determine which register to access during a read or write operation.252330IFC*I/O'.''Bidirectional control line initializes the (OC)IEEE 488 interface functions.242229REN*I/O'Bidirectional control line indicates whether data on the DIO lines is an interface or device dependent message.312836ATN*I/O'Bidirectional control line requests service fro the controller.34, 35, 36,31, 32, 33,39, 40, 41, 2, 37DIO(8-1)*I/O'Bidirectional line requests service fro the controller.34, 41, 4237, 382, 3InterventI/O'Bidirectional control line requests service fro the controller. | - | · | | 71001112 | Ű | |
| 211926RESET*I'Asserting the RESET* input places the NAT9914 in an initial, idle state.10915INT*0The Interrupt output asserts when one of the unmasked interrupt conditions is true. The NAT9914 does not drive INT* high. The INT* pin must be pulled up by an external resistor.9, 8, 78, 7, 614, 13, 12RS(2-0)I'''The Register Selects determine which register to access during a read or write operation.252330IFC*I/O'.''Bidirectional control line initializes the (OC)IEEE 488 interface functions.242229REN*I/O'Bidirectional control line indicates whether data on the DIO lines is an interface or device dependent message.312836ATN*I/O'Bidirectional control line requests service fro the controller.34, 35, 36, 37, 38, 39, 34, 35, 3639, 40, 41, 2, 37, 38DIO(8-1)*I/O'Bidirectional line requests service fro the controller. | 20 | 18 | 25 | CL K | I, | |
| Image: Constraint of the state of the sta | | | | | | |
| 10915INT* (OC)0The Interrupt output asserts when one of the unmasked interrupt conditions is true. The NAT9914 does not drive INT* high. The INT* pin must be pulled up by an external resistor.9, 8, 78, 7, 614, 13, 12RS(2-0)I"The Register Selects determine which register to access during a read or write operation.252330IFC*I/O."Bidirectional control line initializes the (OC)IEEE 488 interface functions.242229REN*I/O.Bidirectional control line selects either remote (OC)Bidirectional control line indicates whether data on the DIO lines is an interface or device.312836ATN*I/O.Bidirectional control line requests service from the controller.34, 35, 36,31, 32, 33,39, 40, 41, 41, 42DIO(8-1)*I/O.Bidirectional LEEE 488 data bus37, 38, 39,34, 35, 3642, 43, 44, 41, 42J7, 382, 3 | 2. | ., | 20 | | | . |
| Image: Section of the section of th | 10 | 9 | 15 | INT* | 0 | |
| NAT9914 does not drive INT* high. The INT* pin must be pulled up by an external resistor.9, 8, 78, 7, 614, 13, 12RS(2-0)I"The Register Selects determine which register to access during a read or write operation.252330IFC*I/0."Bidirectional control line initializes the (OC)IEEE 488 interface functions.242229REN*I/OBidirectional control line selects either remote (OC)312836ATN*I/OBidirectional control line indicates whether data on the DIO lines is an interface or devices.322937SRQ*I/OBidirectional control line requests service from the controller.34, 35, 36, 37, 38, 39, 41, 4237, 382, 3DIO(8-1)*I/OBidirectional IEEE 488 data bus | | , | | | Ŭ | |
| 9, 8, 78, 7, 614, 13, 12RS(2-0)I"fin must be pulled up by an external resistor.252330IFC*I/0."Bidirectional control line initializes the (OC)IEEE 488 interface functions.242229REN*I/OBidirectional control line selects either remote (OC)312836ATN*I/OBidirectional control line initializes the (OC)322937SRQ*I/OBidirectional control line indicates whether data on the DIO lines is an interface or devices.322937SRQ*I/OBidirectional control line requests service fro the controller.34, 35, 36, 41, 4237, 382, 3DIO(8-1)*I/OBidirectional IEEE 488 data bus | | | | () | | |
| 9, 8, 78, 7, 614, 13, 12RS(2-0)I"The Register Selects determine which register to access during a read or write operation.252330IFC*I/0."Bidirectional control line initializes the IEEE 488 interface functions.242229REN*I/0'Bidirectional control line selects either remote or local control of devices.312836ATN*I/0'Bidirectional control line indicates whether data on the DIO lines is an interface or device dependent message.322937SRQ*I/0'Bidirectional control line requests service from the controller.34, 35, 36, 37, 38, 39, 41, 4237, 382, 3DIO(8-1)*I/0'Bidirectional IEEE 488 data bus | | | | | | Ũ |
| 1000000000000000000000000000000000000 | 9, 8, 7 | 8, 7, 6 | 14, 13, 12 | RS(2-0) | | |
| 252330IFC*I/O:"Bidirectional control line initializes the IEEE 488 interface functions.242229REN*I/O: (OC)Bidirectional control line selects either remote or local control of devices.312836ATN*I/O: (OC)Bidirectional control line indicates whether data on the DIO lines is an interface or devices322937SRQ*I/O: (OC)Bidirectional control line requests service from the controller.34, 35, 36, 37, 38, 39, 41, 4237, 382, 3DIO(8-1)*I/O: (OC)Bidirectional IEEE 488 data bus | | -, , , - | ., ., | | | |
| 1242229REN*1/0'IEEE 488 interface functions.242229REN*1/0'Bidirectional control line selects either remote or local control of devices.312836ATN*I/O'Bidirectional control line indicates whether data on the DIO lines is an interface or devices dependent message.322937SRQ*I/O'Bidirectional control line requests service from the controller.34, 35, 3631, 32, 33, 34, 35, 3639, 40, 41, 42, 37, 38DIO(8-1)*I/O'Bidirectional IEEE 488 data bus | 25 | 23 | 30 | IFC* | I/O ^{†,††} | |
| 242229REN*I/O'Bidirectional control line selects either remote or local control of devices.312836ATN*I/O'Bidirectional control line indicates whether data on the DIO lines is an interface or device dependent message.322937SRQ*I/O'Bidirectional control line requests service from the controller.34, 35, 36,31, 32, 33, 34, 35, 3639, 40, 41, 42, 37, 38DIO(8-1)*I/O'Bidirectional IEEE 488 data bus | | | | | (OC) | IEEE 488 interface functions. |
| 312836ATN*I/O'Bidirectional control line indicates whether data on the DIO lines is an interface or device dependent message.322937SRQ*I/O'Bidirectional control line requests service from the controller.34, 35, 36, 37, 38, 39, 41, 4237, 3839, 40, 41, 2, 3DIO(8-1)*I/O'Bidirectional IEEE 488 data bus | 24 | 22 | 29 | REN* | | Bidirectional control line selects either remote |
| Alton | | | | | (OC) | or local control of devices. |
| 111 | 31 | 28 | 36 | ATN* | I/O⁺ | Bidirectional control line indicates whether |
| 32 29 37 SRQ* I/O' Bidirectional control line requests service from the controller. 34, 35, 36, 31, 32, 33, 39, 40, 41, DIO(8-1)* I/O' 8-bit bidirectional IEEE 488 data bus 37, 38, 39, 34, 35, 36 42, 43, 44, DIO(8-1)* I/O' 8-bit bidirectional IEEE 488 data bus | | | | | | data on the DIO lines is an interface or device- |
| Image: Note of the controller. Image: Note of the controller. Image: Note of the controller. 34, 35, 36, 31, 32, 33, 39, 40, 41, 37, 38, 39, 34, 35, 36 39, 40, 41, 42 DIO(8-1)* I/O* B-bit bidirectional IEEE 488 data bus 41, 42 37, 38 2, 3 Image: Note of the controller. Image: Note of the controller. | | | | | | dependent message. |
| 34, 35, 36, 31, 32, 33, 39, 40, 41, DIO(8-1)* I/O' 8-bit bidirectional IEEE 488 data bus 37, 38, 39, 34, 35, 36 42, 43, 44, I/O' 1/O' 8-bit bidirectional IEEE 488 data bus 41, 42 37, 38 2, 3 I/O' I/O' 1/O' | 32 | 29 | 37 | SRQ* | I/O [↑] | Bidirectional control line requests service from |
| 37, 38, 39, 34, 35, 36 42, 43, 44, 41, 42 37, 38 2, 3 | | | | | | the controller. |
| 41, 42 37, 38 2, 3 | 34, 35, 36, | 31, 32, 33, | 39, 40, 41, | DIO(8-1)* | I/O⁺ | 8-bit bidirectional IEEE 488 data bus |
| | 37, 38, 39, | 34, 35, 36 | 42, 43, 44, | | | |
| 29 26 34 DAV* I/O' Handshake line indicates that the data on the | 41, 42 | 37, 38 | 2, 3 | | | |
| | 29 | 26 | 34 | DAV* | I/O⁺ | Handshake line indicates that the data on the |
| DIO(8-1)* lines is valid. | | | | | | |
| 27 25 32 NRFD* I/O' Handshake line indicates that the device is | 27 | 25 | 32 | NRFD* | I/O⁺ | Handshake line indicates that the device is |
| ready for data. | | | | | | ready for data. |
| 26 24 31 NDAC* I/O' Handshake line indicates the completion of a | 26 | 24 | 31 | NDAC* | I/O⁺ | Handshake line indicates the completion of a |
| message reception. | | | | | | message reception. |
| | 30 | 27 | 35 | EOI* | I/O [†] | Bidirectional control line indicates the last byte |
| | | | | | | of a data message or executes a parallel poll. |
| 23 21 28 TE O' Talk Enable controls the direction of the | 23 | 21 | 28 | TE | O [†] | Talk Enable controls the direction of the |
| IEEE 488 data transceiver. | | | | | | IEEE 488 data transceiver. |

2 National Instruments -

Tel: (512) 794-0100 • Fax: (512) 683-9300 • info@ni.com • ni.com/gpib

| Pin Number | | | | | |
|------------|-----|--------|----------|----------------|--|
| PLCC | DIP | QFP | Mnemonic | Туре | Description |
| 43 | 39 | 4 | TR | 0' | Trigger asserts when one of the trigger conditions is satisfied. |
| 33 | 30 | 38 | CONT* | O [†] | Controller asserts when the NAT9914 is Controller-In-Charge. |
| 44 | 40 | 5 | VDD | - | Power pin – +5 V (±5%) |
| 22 | 20 | 27 | VSS | - | Ground pin – 0 V |
| 1, 18, | - | 1, 6, | NC | - | No connect |
| 28,40 | | 23, 33 | | | |

OC= Open collector.

[†] The pin contains an internal pull-up resistor of 25 k Ω to 100 k Ω .

* Active low.

" In controller applications where the CLK signal frequency is > 8 MHz, IFC* should be pulled up with a 4.7 k Ω resistor.

^{III} RS0 and RS1 contain an internal pull-up resistor of 25 kΩ to 100 kΩ. RS2 does not contain an internal pull-up or pull-down resistor.



Figure 4. NAT9914 Block Diagram

9914 Mode Registers

In 9914 mode, the NAT9914 registers consist of all the TI TMS9914A registers and two types of additional registers – newly defined registers and paged-in registers. The NAT9914 maps the newly defined registers into the unused portion of the 9914 address space. Each paged-in register appears at Offset 2 immediately after you issue an auxiliary page-in command, and it remains there until you page another register into the same space or you issue a reset. The table below lists all the registers in the 9914 register set. See the NAT9914 Reference Manual available at **ni.com** for more information.

9914 Register Set

| Register | PAGE-IN | R | S(2-0 |)) | WE* | DBIN | CE* | ACCGR* |
|----------------------|---------|---|-------|----|-----|------|-----|--------|
| Interrupt Status 0 | U | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| Interrupt Mask 0 | U | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Interrupt Status 1 | U | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| Interrupt Mask 1 | U | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| Address Status | U | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| Interrupt Mask 2' | Р | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| End-of-String | Р | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Bus Control | Р | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Accessory | Р | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Bus Status | U | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| Auxiliary Command | U | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Interrupt Status 2' | Р | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| Address | U | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| Serial Poll Status' | Р | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| Serial Poll Mode | U | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| Command Pass Through | U | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| Parallel Poll | U | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| Data-In | U | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| Data-In | U | Х | Х | Х | Х | 0 | Х | 0 |
| Command/Data Out | U | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| Command/Data Out | U | Х | Х | Х | 0 | 1 | Х | 0 |

The " symbol denotes features (such as registers and auxiliary commands) that are not available in the TMS9914A.

Notes for the PAGE-IN column:

- U = Page-in auxiliary commands do not affect the register offset.
- P = The register offset is valid only after a page-in auxiliary command.

7210 Mode Registers

The NAT9914 registers include all the NEC μ PD7210 registers plus two types of additional registers – extra auxiliary registers and paged-in registers. You write the extra auxiliary registers the same as standard μ PD7210 auxiliary registers. On issuing an auxiliary page-in command, the paged-in registers appear at the same offsets as existing μ PD7210 registers. At the end of the next CPU access, the chip pages out the paged-in registers. The following table lists all the registers in the 7210 mode register set. See the NAT9914 Reference Manual available at **ni.com** for more information.

7210 Register Set

| Register | PAGE-IN | l | 4(2-0 |) | WE* | DBIN | CE* | ACCGR* |
|---------------------------------|---------|---|-------|---|-----|------|-----|--------|
| Data-In | U | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| Data-In | Х | Х | Х | Х | Х | 0 | Х | 0 |
| Command/Data Out | U | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Command/Data Out | Х | Х | Х | Х | 0 | 1 | Х | 0 |
| Interrupt Status 1 | U | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| Interrupt Mask 1 | U | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| Interrupt Status 2 | U | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| Interrupt Mask 2 | U | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Serial Poll Status | N | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| Serial Poll Mode | N | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Version | Р | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| Internal Counter 2 | Р | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Address Status | U | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| Address Mode | U | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| Command Pass Through | N | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| Auxiliary Mode | U | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| Source/Acceptor Statust | Р | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| Address 0 | Ν | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| Address | N | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| Interrupt Status 0 ^t | Р | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| Interrupt Mask 0 ⁺ | Р | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| Address 1 | N | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| End-of-String | N | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| Bus Status' | Р | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| Bus Control | Р | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

The " symbol denotes features (such as registers and auxiliary commands) that are not available in the NEC7210.

Notes for the PAGE-IN column:

- U = The page-in auxiliary command does not affect the register.
- N = The register offset is always valid except for immediately after a page-in auxiliary command.
- P = The register is valid only immediately after a page-in auxiliary command.

Preliminary DC Characteristics

 $T_A 0$ to 70 °C; $V_{CC} = 5 V \pm 5\%$

| | | Limits | | | Test |
|-----------------------|-----------------|--------|-----------------|------|-------------------------|
| Parameter | Symbol | Min | Max | Unit | Condition |
| Voltage input low | VIL | -0.5 | +0.8 | V | - |
| Voltage input high | V _{IH} | +2.0 | V _{CC} | V | - |
| Voltage output low | V _{OL} | 0 | 0.4 | V | - |
| Voltage output high | V _{OH} | +2.4 | VCC | V | - |
| Input/output | - | -10 | +10 | μA | without |
| Leakage current | | | | | internal pull-up |
| Input/output | - | -200 | +200 | μA | with internal |
| Leakage current | | | | | pull-up |
| Supply current | - | - | 45 | mA | - |
| Output current low | | | | | |
| All pins except ACCRQ | I _{OL} | 2 | - | mA | 0.4 V @ I _{OL} |
| ACCRQ | I _{OL} | 4 | - | mA | 0.4 V @ I _{OL} |
| Input current low | I _{IL} | - | - 0.5 | mA | - |
| Supply voltage | V _{DD} | 4.75 | 5.25 | V | - |

Capacitance

T_A 0 to 70 °C; V_{CC} = 5 V ±5%

| | | Limits | | | Test |
|----------------------|------------------|--------|-----|------|-----------|
| Parameter | Symbol | Min | Max | Unit | Condition |
| Input capacitance | C _{IN} | - | 10 | pF | - |
| Output capacitance | C _{OUT} | - | 10 | pF | - |
| I/O capacitance | C _{I/O} | - | 10 | pF | - |

Absolute Maximum Ratings

| Property Range | | | | | | |
|---|--|--|--|--|--|--|
| Supply voltage, V _{DD} -0.5 to +7.0 V | | | | | | |
| Input voltage, V ₁ -0.5 to V _{DD} +0.5 V | | | | | | |
| Operating temperature, T _{OPR} 0 to +70° C | | | | | | |
| Storage temperature, T _{STG} -40 to +125° C | | | | | | |
| Comment: Exposing the device to stresses above those listed could cause permanent damage. The | | | | | | |
| device is not meant to be operated under conditions outside the limits described in the operational | | | | | | |
| section. Exposure to absolute maximum ratin | ng conditions for extended periods may affect reliability. | | | | | |

AC Characteristics

T_A 0 to 70 °C; V_{CC} = 5 V ±5%

| | | Lin | nits | | Test |
|---|-----------------|-----|------|------|-----------|
| Parameter | Symbol | Min | Max | Unit | Condition |
| Address hold from CE, WE, and DBIN | t _{AH} | 0 | - | ns | - |
| Address setup to $\overline{\text{CE}}$, $\overline{\text{WE}}$, and DBIN | t _{AS} | 0 | - | ns | - |
| Data float from CE or DBIN | t _{DF} | - | 20 | ns | - |
| Data delay from DBIN \downarrow | t _{DR} | - | 75 | ns | ACCGR=0 |
| ACCRQ unassertion | t _{DU} | - | 20 | ns | - |
| Data delay from $\overline{\text{CE}}\downarrow$ | t _{RD} | - | 80 | ns | ACCGR=1 |
| CE recovery width | t _{RR} | 80 | - | ns | - |
| CE pulse width | t _{RW} | 80 | - | ns | - |
| Data hold from WE↑ | t _{WH} | 0 | - | ns | - |
| Data setup to WE↑ | t _{WS} | 60 | - | ns | - |

Notes:

• tas is the setup time to $\overline{CE}\downarrow$ or $\overline{WE}\downarrow$, whichever is later.

• t_{AH} is the hold time from $\overline{WE}\uparrow$ or $\overline{CE}\uparrow$, whichever is earlier.

Timing Waveforms







Figure 6. DMA Read







Figure 8. DMA Write

Source Handshake

| | | Limits (ns) | | Test |
|--|-----------------|-------------|------|--------------------|
| Parameter | Symbol | Min | Max | Condition |
| NDAC↑ to DAV↑ | t _{ND} | - | 40 | - |
| $\overline{\text{NDAC}}$ to $\overline{\text{INT}}\downarrow$ or $\overline{\text{ACCRQ}}\downarrow$ | t _{NI} | - | 40 | INT(DOIE Bit=1) |
| | | | | ACCGR (DMAO Bit=1) |
| \overline{WE} \uparrow to $\overline{DAV}\downarrow$ | t _{WD} | 2000 | 2180 | 2 µs T1, 5MHz |
| \overline{WE} \uparrow to $\overline{DAV}\downarrow$ | t _{WD} | 1200 | 1380 | 1.1 µs T1, 5MHz |
| WE ↑ to DAV↓ | t _{WD} | 600 | 780 | 500 ns T1, 5MHz |
| $\overline{WE} \uparrow to \overline{DAV} \downarrow$ | t _{WD} | 400 | 580 | 350 ns T1, 5MHz |



Figure 9. Source Handshake Timing

Acceptor Handshake

| | | Limi | ts (ns) | Test |
|---|-----------------|------|---------|--|
| Parameter | Symbol | Min | Max | Condition |
| DAV↓ to NDAC↑ | t _{DD} | | 35+3T | |
| DAV↑ to NDAC↓ | t _{DF} | | 25 | |
| $\overline{\text{DAV}}\downarrow$ to $\overline{\text{INT}}\downarrow$ or $\overline{\text{ACCRQ}}\downarrow$ | t _{DI} | | 50+2T | INT(DIIE Bit=1), ACCGR (DMAI Bit=1) |
| $\overline{\text{DAV}}\downarrow$ to $\overline{\text{NRFD}}\downarrow$ | t _{DR} | | 20 | |
| DBIN↑ to NRFD↑ | t _{NR} | | 35 | Read of DIR, not in Holdoff state |

Note: T = one clock period



Figure 10. Acceptor Handshake Timing

Response to ATN

| | | Limits (ns) | | Test |
|---|-----------------|-------------|-----|-------------------------------|
| Parameter | Symbol | Min | Max | Condition |
| ATN↑ to NRFD↓ | t _{AF} | | 35 | Acceptor handshake holdoff |
| $\overline{\text{ATN}}\downarrow$ to $\overline{\text{NDAC}}\downarrow$ | t _{AN} | | 35 | $AIDS \to ANRS$ |
| $\overline{\text{ATN}}\downarrow$ to $\overline{\text{TE}}\downarrow$ | t _{AT} | | 30 | $TACS \to TADS$ |



Figure 11. ATN Response Timing

Parallel Poll

| | | Limits (ns) | | Test |
|--|-----------------|-------------|-----|-------------------------|
| Parameter | Symbol | Min | Max | Condition |
| $\overline{EOI}\downarrow$ to $\overline{DIO}\downarrow$ valid | t _{ED} | | 90 | $PPSS \rightarrow PPAS$ |
| EOI↓ to TE↑ | t _{ET} | | 30 | $PPSS \rightarrow PPAS$ |
| \overline{EOI} to $\overline{TE}\downarrow$ | t _{TE} | | 30 | $PPAS\toPPSS$ |



Figure 12. Parallel Poll Response Timing



Figure 13. Typical CPU Systems with NAT9914



Figure 14. Mechanical Data 40-Pin Plastic DIP



Figure 15. Mechanical Data 44-Pin PLCC



Figure 16. Mechanical 44-pin QFP.

| Dimensions | Tolerance Value (in mm) | | |
|----------------|-------------------------|-----------|--|
| A | max. | 2.35 | |
| A ₁ | – 0.25 max. | | |
| A ₂ | + 0.10/-0.05 | 2.00 | |
| D | ± 0.25 | 17.20 | |
| D ₁ | ± 0.10 | 14.00 | |
| E | ± 0.25 | 17.20 | |
| E ₁ | ± 0.10 | 14.00 | |
| L | + 0.15/- 0.10 | 0.88 | |
| е | basic | 1.00 | |
| b | ± 0.05 | 0.35 | |
| θ | - | 0 to 7° | |
| ddd | - | 0.20 nom. | |
| ССС | max. | 0.10 | |

Ordering Information

NAT9914BPD NAT9914BPL NAT9914BPQ

Part Number Legend

| а | b | С | d | е |
|-----|------|---|---|---|
| NAT | 9914 | В | Р | D |

- a. Family name NAT = 8-bit GPIB Talker/Listener/Controller interface
- b. Device number 9914 = TI TMS9914A pin-compatible part
- c. Revision
- d. Package material P = plastic
- Package type D = Dual Inline Package (DIP)
 L = Plastic Leaded Chip Carrier (PLCC)
 Q = Quad Flatpack (QFP)

NAT9914 Programmer Reference Manual.....visit ni.com

Technical Support

National Instruments strives to provide you with quality technical assistance worldwide. We currently offer electronic technical support along with our technical support centers staffed by applications engineers.

Access information from our Web site at **ni.com** Our FTP site is dedicated to 24-hour support, with a collection of files and documents to answer your questions. Log on to our Internet host at **ftp.ni.com** You can fax questions to our applications engineers anytime at (800) 328-2203 or (512) 683-5678. Or, you can call from 8:00 a.m. to 6:00 p.m. (central time) at (512) 795-8248. Internationally, contact your local office. National Instruments sponsors a wide variety of group activities, such as user group meetings at trade shows and at large industrial sites. Our users also receive our quarterly newsletters Instrumentation Newsletter[®] and AutomationView[®] to get the latest information on new products, product updates, application tips, and current events. In addition, sign up for NI News, our electronic news service at **ni.com/news**

Warranty

All National Instruments data acquisition, computer-based instrument, VXIbus, and MXI⁻bus products are covered by a oneyear warranty. GPIB hardware products are covered by a two-year warranty from the date of shipment. The warranty covers board failures, components, cables, connectors, and switches, but does not cover faults caused by misuse. The owner may return a failed assembly to National Instruments for repair during the warranty period. Extended warranties are available at an additional charge.

Information furnished by National Instruments is believed to be accurate and reliable. National Instruments reserves the right to change product specifications without notice.

Seminars/Training

Free and fee-paid seminars are presented several times a year in cities around the world. Comprehensive, fee-paid training courses are available at National Instruments offices or at customer sites. Call for training schedules.





ni.com/gpi (512) 794-0100

U.S. Corporate Headquarters • Fax: (512) 683-9300 • info@ni.com

Branch Offices: Australia 03 9879 5166 • Austria 0662 45 79 90 0 • Belgium 02 757 00 20 • Brazil 000817 947 8791 • Canada 514 694 8521 • China 021 6555 7838 Czech Republic 420 2 2423 5774 • Denmark 45 76 26 00 • Finland 09 725 725 11 • France 01 48 14 24 24 • Germany 089 741 31 30 • Greece 30 1 42 96 427 Hong Kong 2645 3186 • India 91 80 535 5406 • Israel 03 6393737 • Italy 02 413091 • Japan 03 5472 2970 • Korea 02 596 7456 • Malaysia 603 9596711 Mexico 001 800 010 0793 • Netherlands 0348 433466 • New Zealand 09 914 0488 • Norway 32 27 73 00 • Poland 48 22 528 94 06 • Portugal 351 210 311 210 Russia 095 238 7139 • Singapore 2265886 • Slovenia 386 3 425 4200 • South Africa 082 877 8530 • Spain 91 640 0085 • Sweden 08 587 895 00 Switzerland 056 200 51 51 • Taiwan 02 2528 727 • U.K. 01635 523545 • Venezuela 800 1 4466 • Convidu 2001 National Instruments Corooration. All rights reserved. Product and company mames listed are trademarks of their respective companies.