Darlington Amplifier Transistors

NPN Silicon

Features

- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector - Emitter Voltage	V _{CES}	30	Vdc
Collector - Base Voltage	V _{CBO}	30	Vdc
Emitter – Base Voltage	V _{EBO}	10	Vdc
Collector Current - Continuous	Ic	300	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 1) T _A = 25°C Derate above 25°C	P _D	225 1.8	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (Note 2) T _A = 25°C Derate above 25°C	P _D	300 2.4	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T _J , T _{stg}	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. FR-5 = $1.0 \times 0.75 \times 0.062$ in.
- 2. Alumina = $0.4 \times 0.3 \times 0.024$ in. 99.5% alumina.



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SOT-23 (TO-236) CASE 318 STYLE 6

COLLECTOR 3



MARKING DIAGRAM



1x = Device Code

x = M for MMBTA13LT1G, SMMBTA13LT1G x = N for MMBTA14LT1G,

T = N for MMBTA14LT1G, SMMBTA14LT1G, T3G

M = Date Code*

= Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping [†]
MMBTA13LT1G, SMMBTA13LT1G	SOT-23 (Pb-Free)	3,000 / Tape & Reel
MMBTA14LT1G, SMMBTA14LT1G	SOT-23 (Pb-Free)	3,000 / Tape & Reel
SMMBTA14LT3G	SOT-23 (Pb-Free)	10,000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	<u>.</u>			•
Collector – Emitter Breakdown Voltage ($I_C = 100 \mu Adc, V_{BE} = 0$)	V _(BR) CES	30	-	Vdc
Collector Cutoff Current (V _{CB} = 30 Vdc, I _E = 0)	I _{CBO}	-	100	nAdc
Emitter Cutoff Current (V _{EB} = 10 Vdc, I _C = 0)	I _{EBO}	-	100	nAdc
ON CHARACTERISTICS (Note 3)				
DC Current Gain $ \begin{aligned} &(I_C=10 \text{ mAdc, V}_{CE}=5.0 \text{ Vdc}) \\ &\text{MMBTA13, SMMBTA13} \\ &\text{MMBTA14, SMMBTA14} \end{aligned} $ $ &(I_C=100 \text{ mAdc, V}_{CE}=5.0 \text{ Vdc}) \\ &\text{MMBTA13, SMMBTA13} \\ &\text{MMBTA14, SMMBTA13} \end{aligned} $	h _{FE}	5000 10,000 10,000 20,000	- - -	-
Collector – Emitter Saturation Voltage (I _C = 100 mAdc, I _B = 0.1 mAdc)	V _{CE(sat)}	-	1.5	Vdc
Base – Emitter On Voltage (I _C = 100 mAdc, V _{CE} = 5.0 Vdc)	V _{BE}	-	2.0	Vdc
SMALL-SIGNAL CHARACTERISTICS	<u>.</u>	•	•	•
Current – Gain – Bandwidth Product (Note 4) (I _C = 10 mAdc, V _{CE} = 5.0 Vdc, f = 100 MHz)	f _T	125	-	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 3. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

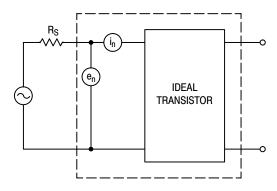


Figure 1. Transistor Noise Model

^{4.} $f_T = |h_{fe}| \bullet f_{test}$.

NOISE CHARACTERISTICS

 $(V_{CE} = 5.0 \text{ Vdc}, T_A = 25^{\circ}C)$

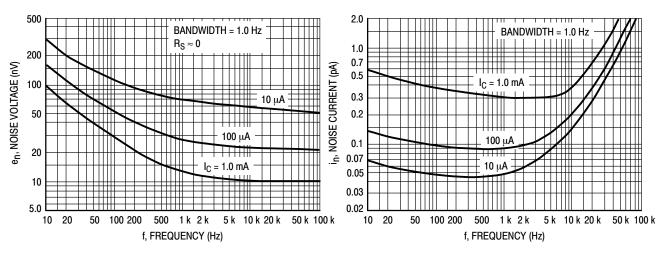


Figure 2. Noise Voltage

Figure 3. Noise Current

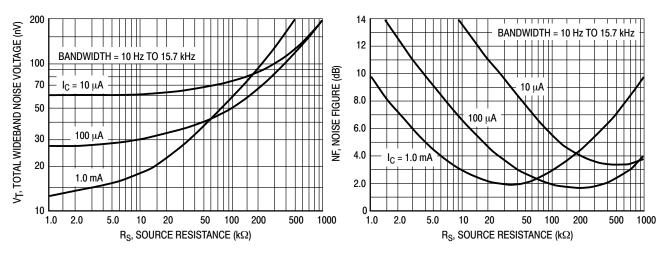


Figure 4. Total Wideband Noise Voltage

Figure 5. Wideband Noise Figure

SMALL-SIGNAL CHARACTERISTICS

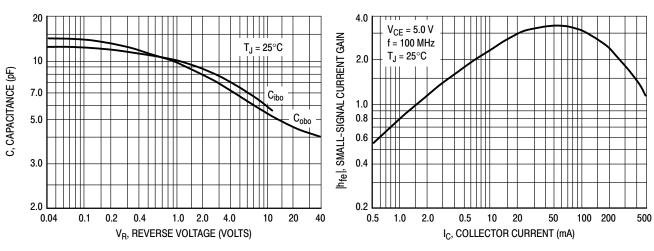


Figure 6. Capacitance

Figure 7. High Frequency Current Gain

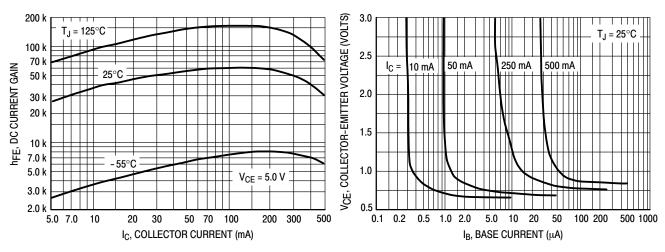


Figure 8. DC Current Gain

Figure 9. Collector Saturation Region

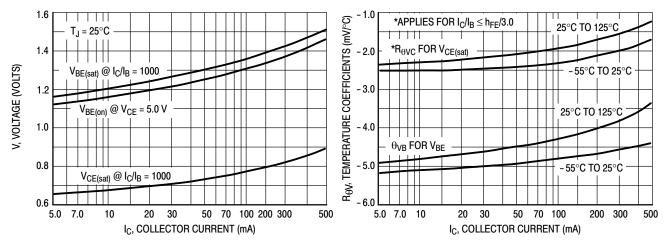


Figure 10. "On" Voltages

Figure 11. Temperature Coefficients

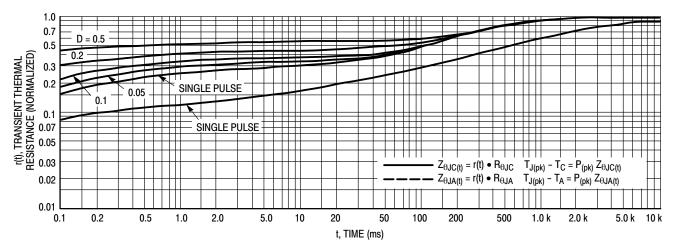


Figure 12. Thermal Response

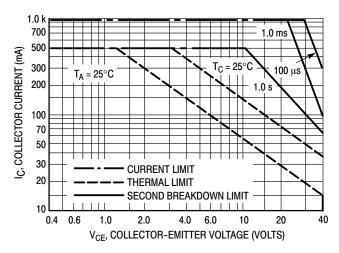
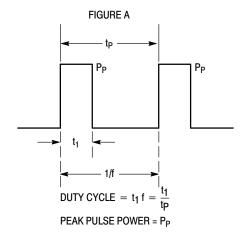


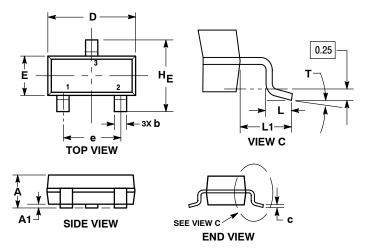
Figure 13. Active Region Safe Operating Area



Design Note: Use of Transient Thermal Resistance Data

PACKAGE DIMENSIONS

SOT-23 (TO-236) CASE 318-08 **ISSUE AR**

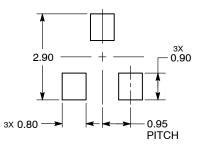


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 MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH.
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 DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH,
- PROTRUSIONS, OR GATE BURRS

	MILLIMETERS INCHES					
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
С	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
Е	1.20	1.30	1.40	0.047	0.051	0.055
е	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
HE	2.10	2.40	2.64	0.083	0.094	0.104
Т	٥°		10 °	0 °		10 °

STYLE 6: PIN 1. BASE 2. EMITTER COLLECTOR

RECOMMENDED SOLDERING FOOTPRINT*



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^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.