# MMBF5457LT1

**Preferred Device**

# JFET - General Purpose Transistor

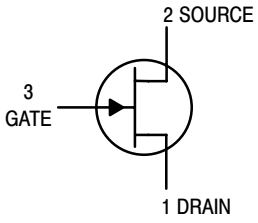
## N−Channel

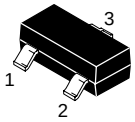
**ON Semiconductor®**

**http://onsemi.com**

### Features

- Pb−Free Package is Available




**SOT−23 (TO−236)**
**CASE 318**
**STYLE 10**

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain−Source Voltage | $V_{DS}$ | 25 | Vdc |
| Drain−Gate Voltage | $V_{DG}$ | 25 | Vdc |
| Reverse Gate−Source Voltage | $V_{GS(r)}$ | −25 | Vdc |
| Gate Current | $I_G$ | 10 | mAdc |

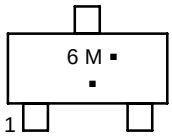
### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Total Device Dissipation FR−5 Board (Note 1) ($T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 225<br><br>1.8 | mW<br><br>mW/°C |
| Thermal Resistance, Junction−to−Ambient | $R_{\theta JA}$ | 556 | °C/W |
| Junction and Storage Temperature | $T_J$, $T_{stg}$ | −55 to +150 | °C |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR−5 = 1.0 × 0.75 × 0.062 in.

### MARKING DIAGRAM




6 = Specific Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MMBF5457LT1 | SOT−23 | 3000/Tape & Reel |
| MMBF5457LT1G | SOT−23 (Pb−Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**Preferred** devices are recommended choices for future use and best overall value.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Gate−Source Breakdown Voltage ($I_G$ = 10 μAdc, $V_{DS}$ = 0) | $V_{(BR)GSS}$ | −25 | − | − | Vdc |
| Gate Reverse Current ($V_{GS}$ = 15 Vdc, $V_{DS}$ = 0)<br>($V_{GS}$ = 15 Vdc, $V_{DS}$ = 0, $T_A$ = 100°C) | $I_{GSS}$ | −<br>− | −<br>− | −1.0<br>−200 | nAdc |
| Gate Source Cutoff Voltage ($V_{DS}$ = 15 Vdc, $I_D$ = 10 nAdc) | $V_{GS(off)}$ | −0.5 | − | −6.0 | Vdc |
| Gate Source Voltage ($V_{DS}$ = 15 Vdc, $I_D$ = 100 μAdc) | $V_{GS}$ | − | −2.5 | − | Vdc |
| **ON CHARACTERISTICS** | | | | | |
| Zero−Gate−Voltage Drain Current (Note 2) ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0) | $I_{DSS}$ | 1.0 | − | 5.0 | mAdc |
| **SMALL−SIGNAL CHARACTERISTICS** | | | | | |
| Forward Transfer Admittance (Note 2) ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0, f = 1.0 kHz) | $\|Y_{fs}\|$ | 1000 | − | 5000 | μmhos |
| Output Common Source Admittance ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0, f = 1.0 kHz) | $\|y_{os}\|$ | − | 10 | 50 | μmhos |
| Input Capacitance ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | − | 4.5 | 7.0 | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{rss}$ | − | 1.5 | 3.0 | pF |

2. Pulse Test: Pulse Width ≤ 630 ms, Duty Cycle ≤ 10%.

## TYPICAL CHARACTERISTICS

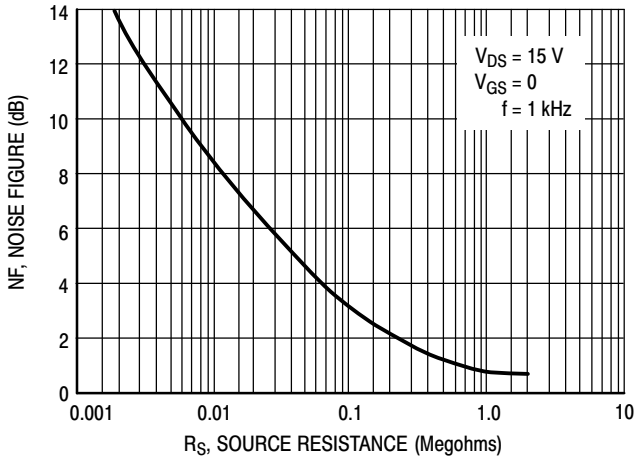



**Figure 1. Noise Figure versus Source Resistance**

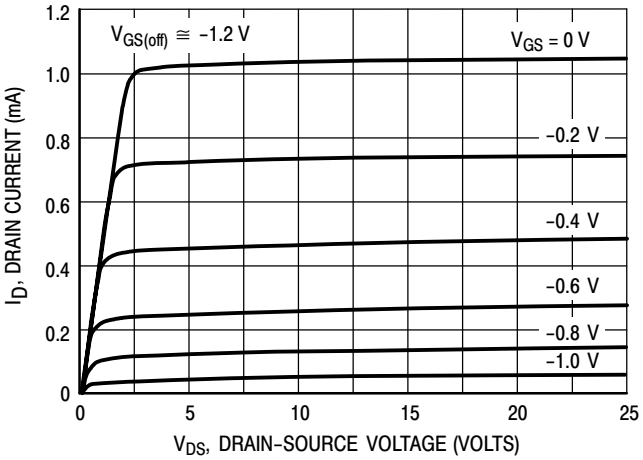



**Figure 2. Typical Drain Characteristics**

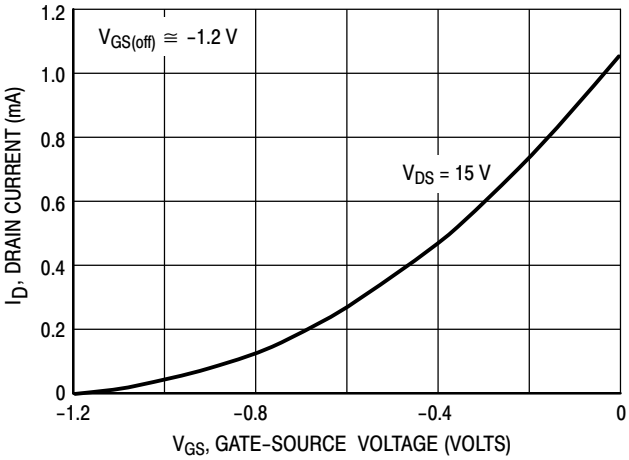



**Figure 3. Common Source Transfer Characteristics**

## TYPICAL CHARACTERISTICS

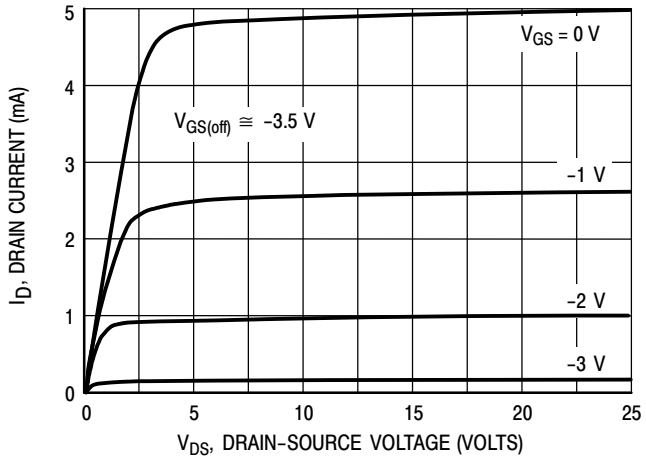



**Figure 4. Typical Drain Characteristics**

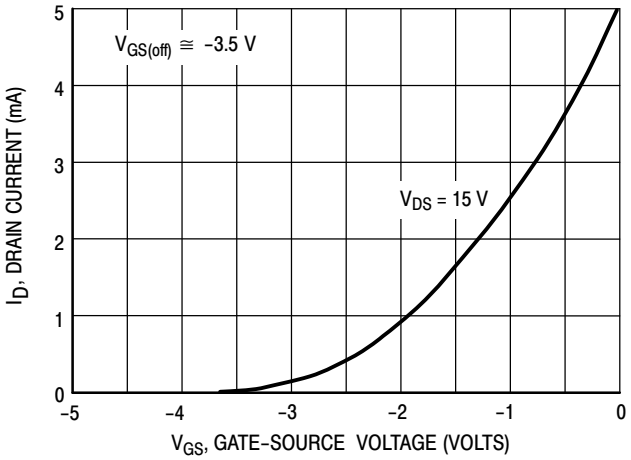



**Figure 5. Common Source Transfer Characteristics**

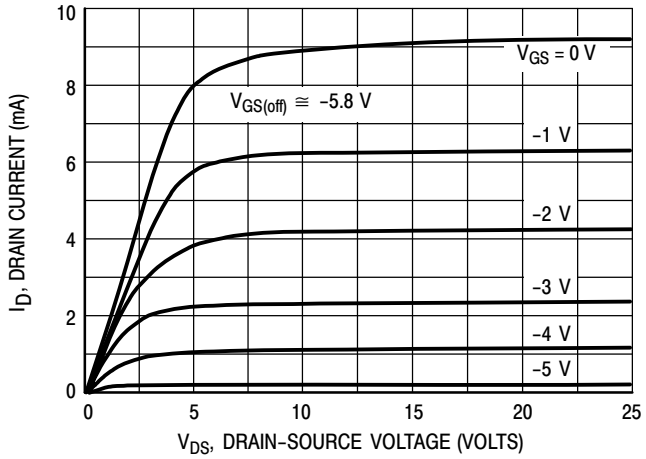



**Figure 6. Typical Drain Characteristics**

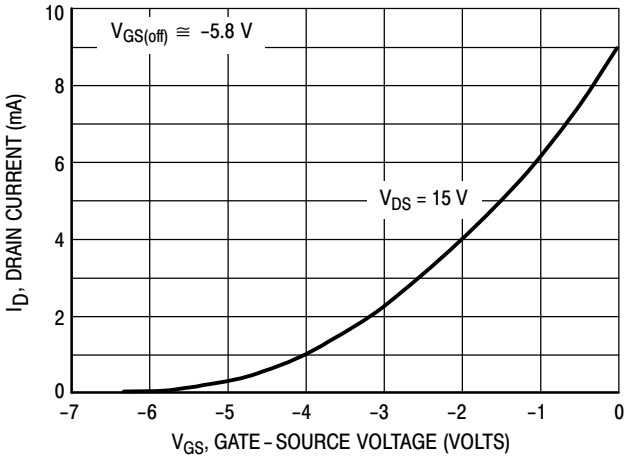
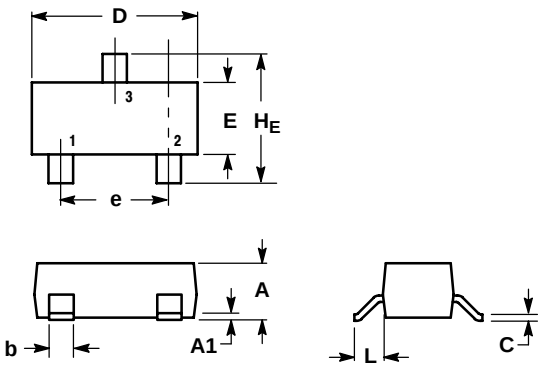



**Figure 7. Common Source Transfer Characteristics**

Note: Graphical data is presented for dc conditions. Tabular data is given for pulsed conditions (Pulse Width = 630 ms, Duty Cycle = 10%). Under dc conditions, self heating in higher $I_{DSS}$ units reduces $I_{DSS}$.

## PACKAGE DIMENSIONS

**SOT−23 (TO−236)**
CASE 318−08
ISSUE AL

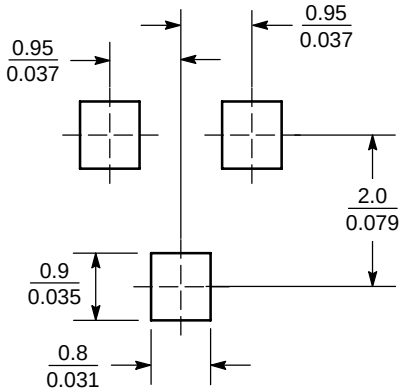



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.89 | 1.00 | 1.11 | 0.035 | 0.040 | 0.044 |
| A1 | 0.01 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.37 | 0.44 | 0.50 | 0.015 | 0.018 | 0.020 |
| c | 0.09 | 0.13 | 0.18 | 0.003 | 0.005 | 0.007 |
| D | 2.80 | 2.90 | 3.04 | 0.110 | 0.114 | 0.120 |
| E | 1.20 | 1.30 | 1.40 | 0.047 | 0.051 | 0.055 |
| e | 1.78 | 1.90 | 2.04 | 0.070 | 0.075 | 0.081 |
| L | 0.35 | 0.54 | 0.69 | 0.014 | 0.021 | 0.029 |
| $H_E$ | 2.10 | 2.40 | 2.64 | 0.083 | 0.094 | 0.104 |

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

## SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
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**Phone**: 81−3−5773−3850

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