MIC5162

Dual Regulator Controller for DDR3 GDDR3/4/5 Memory and High-Speed Bus Termination

General Description

The MIC5162 is a dual regulator controller designed for high speed bus termination. It offers a simple, low-cost JEDEC compliant solution for terminating high-speed, low-voltage digital buses (i.e. DDR, DDR2, DDR3, SCSI, GTL, SSTL, HSTL, LV-TTL, Rambus, LV-PECL, LV-ECL, etc).

The MIC5162 controls two external N-Channel MOSFETs to form two separate regulators. It operates by switching between either the high-side MOSFET or the low-side MOSFET depending upon whether the current is being sourced to the load or sunk by the regulator.

Designed to provide a universal solution for bus termination regardless of input voltage, output voltage, or load current. The desired MIC5162 output voltage can be programmed by forcing the reference voltage externally to desired voltage.

The MIC5162 operates from an input of 1.35V to 6V, with a second bias supply input required for operation. It is available in a tiny MSOP-10 package with operating junction temperature range of -40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

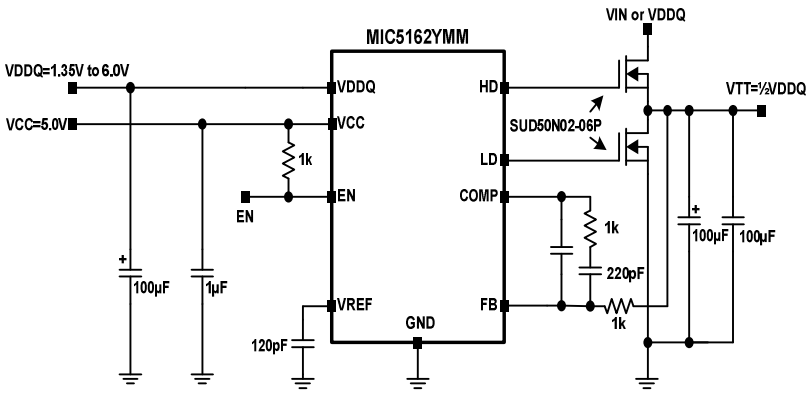
Features

- Input voltage range: 1.35V to 6V
- Up to 7A V_{TT} Current
- Tracking programmable output
- Wide bandwidth
- Logic controlled enable input
- Requires minimal external components
- DDR, DDR2, DDR3, memory termination
- -40°C < T_J < +125°C
- JEDEC Compliant Bus Termination for SCSI, GTL, SSTL, HSTL, LV-TTL, Rambus, LV-PECL, LV-ECL, etc
- Tiny MSOP-10 package

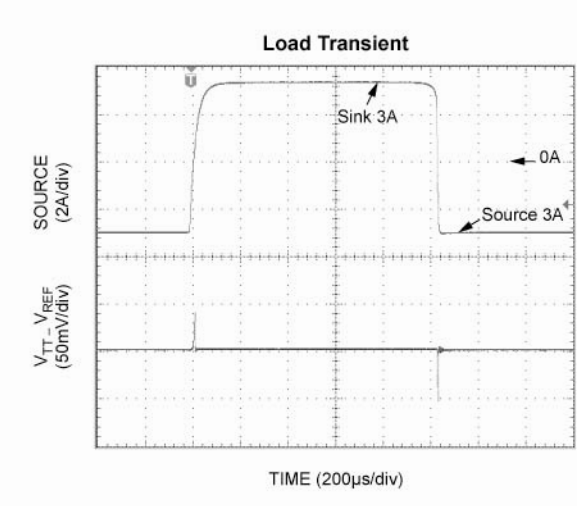
Applications

- Desktop Computers
- Notebook computers
- Communication systems
- Video cards
- DDR/DDR2/DDR3 memory termination

Typical Application



Typical SSTL-2 Application
(Two MOSFETs Support a 3.5A Application)

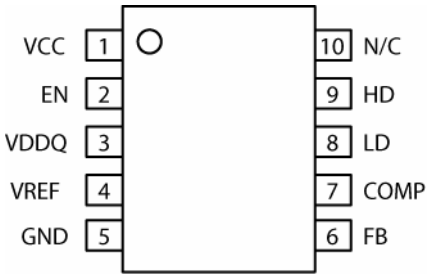


Ordering Information

Part Number	Temperature Range	Package	Lead Finish
MIC5162YMM	–40° to +125°C	10-Pin MSOP	Pb-Free

Note: MSOP is a Green RoHS compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Pin Configuration



10-Pin MSOP (MM)

Pin Description

Pin Number	Pin Name	Pin Function
1	VCC	Bias Supply Input. Apply 3V-6V to this input for internal bias to the controller.
2	EN	Enable (Input): CMOS compatible input. Logic high = enable, logic low = shutdown. The enable pin can be tied directly to V_{DDQ} or V_{CC} for functionality. Do not float the enable pin. Floating this pin causes the enable to be in an undetermined state.
3	VDDQ	Input Supply Voltage.
4	VREF	Reference voltage equal to half of VDDQ. **For internal use only.**
5	GND	Ground.
6	FB	Feedback input to the internal error amplifier.
7	COMP	Compensation (Output): Connect a capacitor and resistor from COMP pin to feedback pin for compensation of the internal control loop.
8	LD	Low-side drive: Connects to the Gate of the external low-side MOSFET.
9	HD	High-side drive: Connects to the Gate of the external high-side MOSFET.
10	NC	Not internally connected.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.3V to +7V
Supply Voltage (V_{DDQ}) ..... –0.3V to +7V
Enable Input Voltage (V_{EN}) ..... –0.3V to (V_{IN}+0.3V)
Junction Temperature Range (T_J) ..... –40°C < T_J < +125°C
Lead Temperature (Soldering 10sec.) ..... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C
ESD Rating[3] ..... +2kV

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... 3V to 6V
Supply Voltage (V_{DDQ}) ..... 1.35V to 6V
Enable Input Voltage (V_{EN}) ..... 0V to V_{IN}
Junction Thermal Resistance
MSOP-10 (θ_{JA}) ..... 130.5°C/W
MSOP-10 (θ_{JC}) ..... 42.6°C/W

Electrical Characteristics[4]

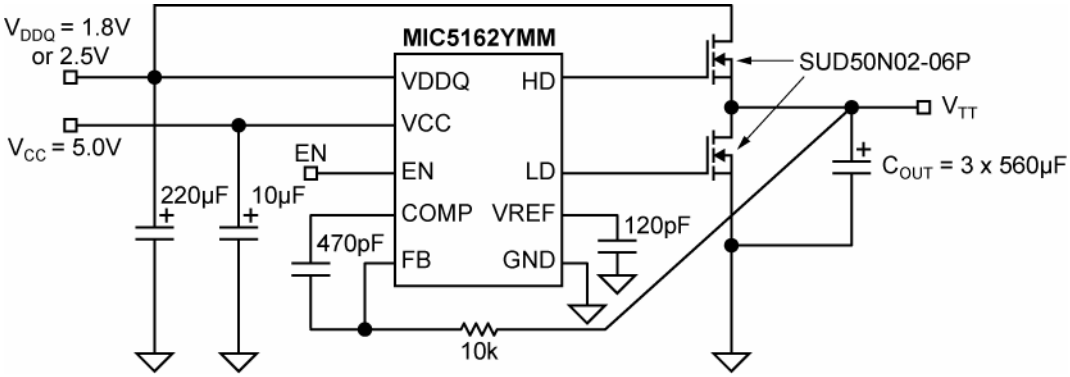
T_A = 25°C with V_{DDQ} = 2.5V; V_{CC} = 5V, V_{EN} = V_{CC}, **bold** values indicate –40°C ≤ T_J ≤ +125°C, unless otherwise specified.
See test circuit 1 for test circuit configuration.

Parameter	Condition	Min	Typ	Max	Units
V_{REF} Voltage Accuracy		-1%	0.5V_{DDQ}	+1%	V
V_{TT} Voltage Accuracy (**Note 5**)	Sourcing; 100mA to 3A	-5 **-10**	0.4	+5 **+10**	mV mV
	Sinking; -100mA to -3A	-5 **-10**	0.6	+5 **+10**	mV mV
Supply Current (I_{DDQ})	V_{EN} = 1.2V (controller ON) No Load		120	140 **200**	µA µA
Supply Current (I_{CC})	No Load		15	20 **25**	mA mA
I_{CC} Shutdown Current (**Note 6**)	V_{EN} = 0.2V (controller OFF)		10	**35**	µA
Start-up Time (**Note 7**)	V_{CC} = 5V external bias; V_{EN} = V_{IN}		8	15 **30**	µs µs
Enable Input					
Enable Input Threshold	Regulator Enable	**1.2**			V
	Regulator Shutdown			**0.3**	V
Enable Hysteresis			40		mV
Enable Pin Input Current	V_{IL} < 0.2V (controller shutdown)		0.01		µA
	V_{IH} > 1.2V (controller enable)		5.5		µA
Driver					
High Side Gate Drive Voltage	High Side MOSFET Fully ON	**4.8**	4.97		V
	High Side MOSFET Fully OFF		0.03	**0.2**	V
Low Side Gate Drive Voltage	Low Side MOSFET Fully ON	**4.8**	4.97		V
	Low Side MOSFET Fully OFF		0.03	**0.2**	V

Notes:

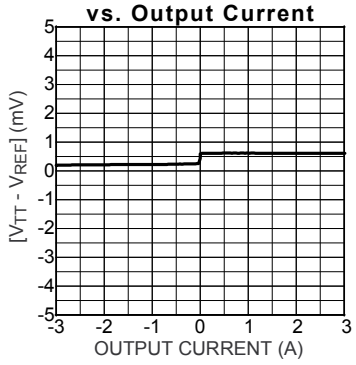
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model 1.5kΩ in series with 100pF.
4. Specification for packaged product only.
5. The V_{TT} voltage accuracy is measured as a delta voltage from the reference output (V_{TT} - V_{REF}).
6. Shutdown current is measured only on the V_{CC} pin. The V_{DDQ} pin will always draw a minimum amount of current when voltage is applied.
7. Start-up time is defined as the amount of time from EN = V_{CC} to HSD = 90% of V_{CC}.

Test Circuit

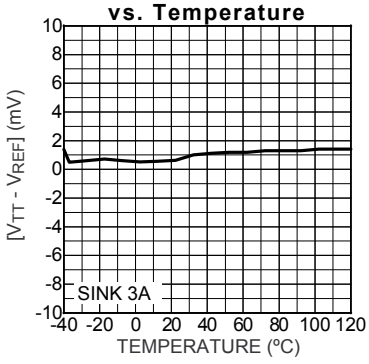


Typical Characteristics

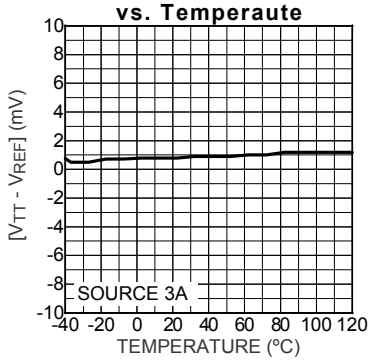
[V_{TT} - V_{REF}] vs. Output Current



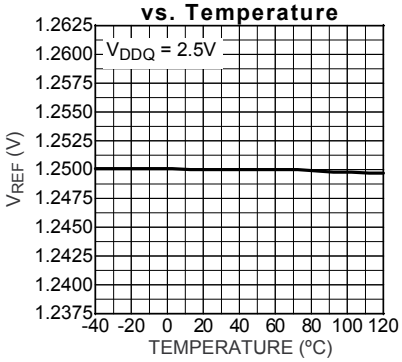
[V_{TT} - V_{REF}] vs. Temperature



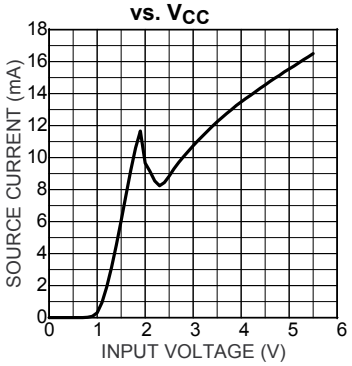
[V_{TT} - V_{REF}] vs. Temperaute



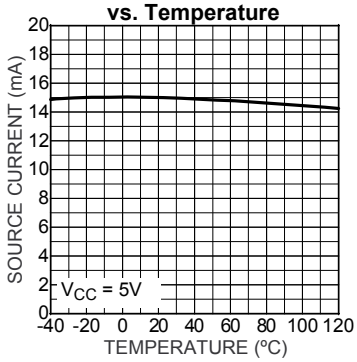
V_{REF} vs. Temperature



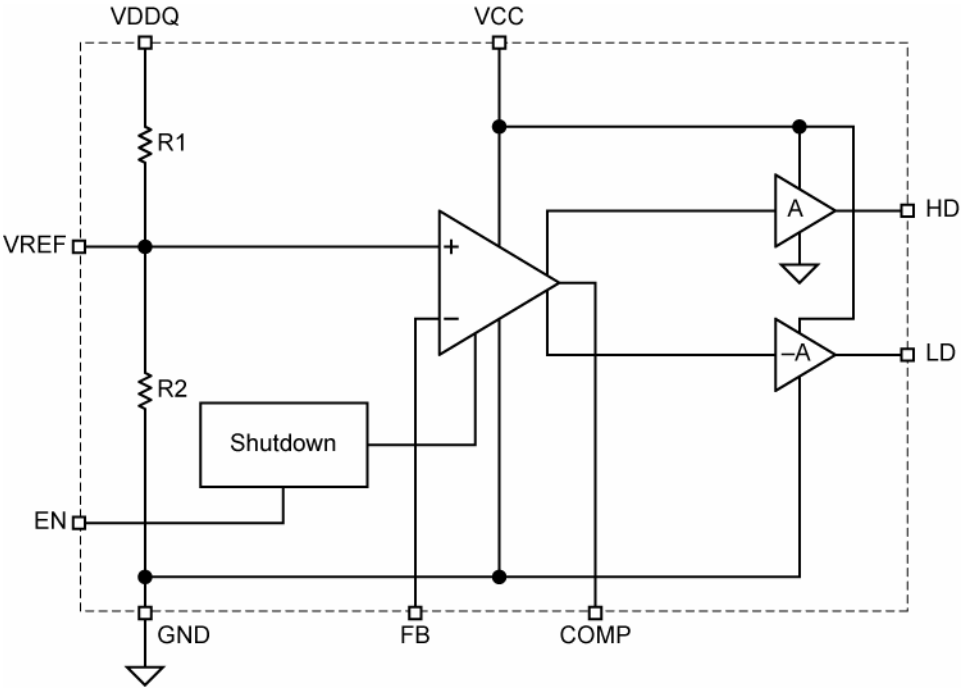
I_{CC} Current vs. V_{CC}



I_{CC} Current vs. Temperature



Functional Diagram



Application Information

High performance memory requires high speed signaling. This means special attention must be paid to maintain signal integrity. Bus termination provides a means to increase signaling speed while maintaining good signal integrity. An example of bus termination is the Series Stub Termination Logic or SSTL. Figure 1 is an example of an SSTL 2 single ended series parallel terminated output. SSTL 2 is a JEDEC signaling standard operating off a 2.5V supply. It consists of a series resistor (R_S) and a terminating resistor (R_T). Values of R_S range between 10Ω to 30Ω with a typical of 22Ω, while R_T ranges from 22Ω to 28Ω with a typical value of 25Ω. V_{REF} must maintain 1/2 VDD with a ±1% tolerance, while V_{TT} will dynamically sink and source current to maintain a termination voltage of ±40mV from the V_{REF} line under all conditions. This method of bus termination reduces common mode noise, settling time, voltage swings, EMI/RFI and improves slew rates.

The MIC5162 is a high performance linear controller, utilizing scalable N-Channel MOSFETs to provide JEDEC-compliant bus termination. Termination is achieved by dividing down the V_{DDQ} voltage by half, providing the reference (V_{REF}) voltage. An internal error amplifier compares the termination voltage (V_{TT}) and V_{REF}, controlling 2 external N-Channel MOSFETs to sink and source current to maintain a termination voltage (V_{TT}) equal to V_{REF}. The N-Channels receive their enhancement voltage from a separate V_{CC} pin on the device.

Although this document focuses mostly on SSTL, the MIC5162 is also capable of providing bus terminations for SCSI, GTL, HSTL, LV-TTL, Rambus, LV-PECL, DDR, DDR2, DDR3 memory termination and other systems.

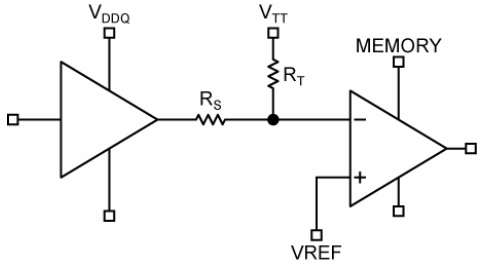


Figure 1. SSTL-2 Termination

V_{DDQ}

The V_{DDQ} pin on the MIC5162 provides the source current through the high-side N-Channel and the reference voltage to the device. The MIC5162 can operate at V_{DDQ} voltages as low as 1.35V. Due to the possibility of large transient currents being sourced from this line, significant bypass capacitance will aid in performance by improving the source impedance at higher frequencies. Since the reference is simply $V_{DDQ}/2$, perturbations on the V_{DDQ} will also appear at half the amplitude on the reference. For this reason, low ESR capacitors such as ceramics or OS-CON are recommended on V_{DDQ}.

V_{TT}

V_{TT} is the actual termination point. V_{TT} is regulated to V_{REF}. Due to high speed signaling, the load current seen by V_{TT} is constantly changing. To maintain adequate large signal transient response, large OS-CON and ceramics are recommended on V_{TT}. The proper combination and placement of the OS-CON and ceramic capacitors is important to reduce both ESR and ESL such that high-current and high-speed transients do not exceed the dynamic voltage tolerance requirement of V_{TT}. The larger OS-CON capacitors provide bulk charge storage while the smaller ceramic capacitors provide current during the fast edges of the bus transition. Using several smaller ceramic capacitors distributed near the termination resistors is typically important to reduce the effects of PCB trace inductance.

V_{REF}

Two resistors dividing down the V_{DDQ} voltage provide V_{REF} (Figure 3). The resistors are valued at around 17kΩ. A minimum capacitor value of 120pF from V_{REF} to ground is required to remove high frequency signals reflected from the source. Large capacitance values (>1500pF) should be avoided. Values greater than 1500pF slow down V_{REF} and detract from the reference voltage's ability to track V_{DDQ} during high speed load transients.

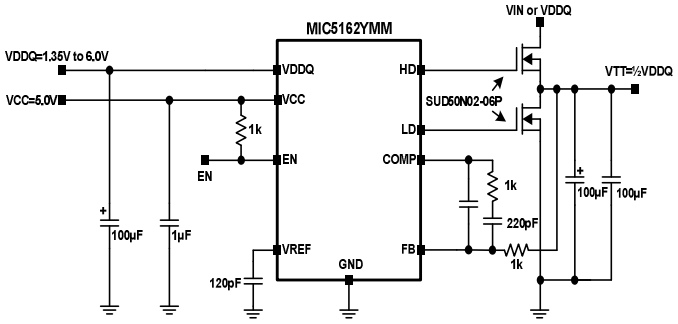


Figure 2. MIC5162 as a DDR Memory Termination for 3.5A Application

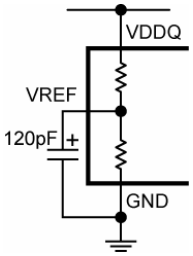


Figure 3. VREF Follows VDDQ

V_{REF} can also be manipulated for different applications. A separate voltage source can be used to externally set the reference point, bypassing the divider network. Also, external resistors can be added from V_{REF}-to-V_{DDQ} or V_{REF}-to-ground to shift the reference point up or down.

V_{CC}

V_{CC} supplies the internal circuitry of the MIC5162 and provides the drive voltage to enhance the external N-Channel MOSFETs. A 1µF ceramic capacitor is recommended for bypassing the V_{CC} pin. The minimum V_{CC} voltage should be a gate-source voltage above V_{TT} or greater than 3V without exceeding 6V. For example, on an SSTL compliant terminator, V_{DDQ} equals 2.5V and V_{TT} equals 1.25V. If the N-Channel MOSFET selected requires a gate source voltage of 2.5V, V_{CC} should be a minimum of 3.75V.

Feedback and Compensation

The feedback provides the path for the error amplifier to regulate V_{TT}. An external resistor must be placed between the feedback and V_{TT}. This allows the error amplifier to be correctly externally compensated.

The COMP pin on the MIC5162 is the output of the internal error amplifier. By placing a capacitor between the COMP pin and the feedback pin, this coupled with the feedback resistor places an external pole on the error amplifier. With a 1kΩ or 510Ω feedback resistor, a minimum 220pF capacitor is recommended for a 3.5A peak termination circuit. Increases in load, multiple N-Channel MOSFETs and/or increase in output capacitance may require feedback and/or compensation capacitor values to be increased to maintain stability. Feedback resistor values should not exceed 10kΩ and compensation capacitors should not be less than 40pF.

Enable

The MIC5162 features an active-high enable (EN) input. In the off-mode state, leakage currents are reduced to microamperes. EN has thresholds compatible with TTL/CMOS for simple logic interfacing. EN can be tied directly to V_{DDQ} or V_{CC} for functionality. Do not float the EN pin. Floating this pin causes the enable circuitry to be in an undetermined state.

Input Capacitance

Although the MIC5162 does not require an input capacitor for stability, using one greatly improves device performance. Due to the high-speed nature of the MIC5162, low ESR capacitors such as OS-CON and ceramics are recommended for bypassing the input. The recommended value of capacitance will depend greatly upon proximity to the bulk capacitance. Although a 10µF ceramic capacitor will suffice for most applications, input capacitance may need to be increased in cases where the termination circuit is greater than 1 inch away from the bulk capacitance.

Output Capacitance

Large, low ESR capacitors are recommended for the output (VTT) of the MIC5162. Although low ESR capacitors are not required for stability, they are recommended to reduce the effects of high-speed current transients on VTT. The change in voltage during the transient condition will be the effect of the peak current multiplied by the output capacitor's ESR. For that reason, OS-CON type capacitors are excellent for this application. They have extremely low ESR and large capacitance-to-size ratio. Ceramic capacitors are also well suited to termination due to their low ESR. These capacitors should have a dielectric rating of X5R or X7R. Y5V and Z5U type capacitors are not recommended, due to their poor performance at high frequencies and over temperature. The minimum recommended capacitance for a 3 Amp peak circuit is 100µF. Output capacitance can be increased to achieve greater transient performance.

MOSFET Selection

The MIC5162 utilizes external N-Channel MOSFETs to sink and source current. MOSFET selection will settle to two main categories: size and gate threshold (V_{GS}).

MOSFET Power Requirements

One of the most important factors is to determine the amount of power the MOSFET required to dissipate. Power dissipation in an SSTL circuit will be identical for both the high-side and low-side MOSFETs. Since the supply voltage is divided by half to supply V_{TT}, both MOSFETs have the same voltage dropped across them. They are also required to be able to sink and source the same amount of current (for either all 0s or all 1s). This equates to each side being able to dissipate the same amount of power. Power dissipation calculation for the high-side driver is as follows:

$$P_D = (V_{DDQ} - V_{TT}) \times I\_SOURCE$$

where I_SOURCE is the average source current. Power dissipation for the low-side MOSFET is as follows:

$$P_D = V_{TT} \times I\_SINK$$

where I_SINK is the average sink current.

In a typical 3A peak SSTL_2 circuit, power considerations for MOSFET selection would occur as follows.

$$P_D = (V_{DDQ} - V_{TT}) \times I\_SOURCE$$

$$P_D = (2.5V - 1.25V) \times 1.6A$$

$$P_D = 2W$$

This typical SSTL_2 application would require both high-side and low-side N-Channel MOSFETs to be able to handle 2 Watts each. In applications where there is excessive power dissipation, multiple N-Channel MOSFETs may be placed in parallel. These MOSFETs will share current, distributing power dissipation across each device.

The maximum MOSFET die (junction) temperature limits maximum power dissipation. The ability of the device to dissipate heat away from the junction is specified by the junction-to-ambient (θ_{JA}) thermal resistance. This is the sum of junction-to-case (θ_{JC}) thermal resistance, case-to-sink (θ_{CS}) thermal resistance and sink-to-ambient (θ_{SA}) thermal resistance;

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

In the example of a 3A peak SSTL_2 termination circuit, a D-pack N-Channel MOSFET that has a maximum junction temperature of 125°C has been selected. The device has a junction-to-case thermal resistance of 1.5°C/Watt. The application has a maximum ambient temperature of 60°C. The required junction-to-ambient thermal resistance can be calculated as follows:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}$$

Where T_J is the maximum junction temperature, T_A is the maximum ambient temperature and P_D is the power dissipation.

In this example:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}$$

$$\theta_{JA} = \frac{125°C - 60°C}{2W}$$

$$\theta_{JA} = 32.5°C / W$$

This shows that our total thermal resistance must be better than 32.5°C/W. Since the total thermal resistance is a combination of all the individual thermal resistances, the amount of heat sink required can be calculated as follows:

$$\theta_{SA} = \theta_{JA} - (\theta_{JC} + \theta_{CS})$$

In this example:

$$\theta_{SA} = 32.5°C / W - (1.5°C / W + 0.5°C)$$

$$\theta_{SA} = 30.5°C / W$$

In most cases, case-to-sink thermal resistance can be assumed to be about 0.5°C/W.

The SSTL termination circuit for this example, using 2 D-pack N-Channel MOSFETs (one high side and one on the low side) will require at least a 30.5°C/W heat sink per MOSFET. This may be accomplished with an external heat sink or even just the copper area that the MOSFET is soldered to. In some cases, airflow may also be required to reduce thermal resistance.

MOSFET Gate Threshold

N-Channel MOSFETs require an enhancement voltage greater than its source voltage. Typical N-Channel MOSFETs have a gate-source threshold (V_{GS}) of 1.8V and higher. Since the source of the high side N-Channel is connected to V_{TT}, the MIC5162 V_{CC} pin requires a voltage greater than the V_{GS} voltage. For example, the SSTL_2 termination circuit has a V_{TT} voltage of 1.25V. For an N-Channel that has a V_{GS} rating of 2.5V, the V_{CC} voltage can be as low as 3.75V, but not less than 3.0V. With an N-Channel that has a 4.5V V_{GS}, the minimum V_{CC} required is 5.75V. Although these N-Channels are driven below their full enhancement threshold, it is recommended that the V_{CC} voltage has enough margin to be able to fully enhance the MOSFETs for large signal transient response. In addition, low gate thresholds MOSFETs are recommended to reduce the V_{CC} requirements.

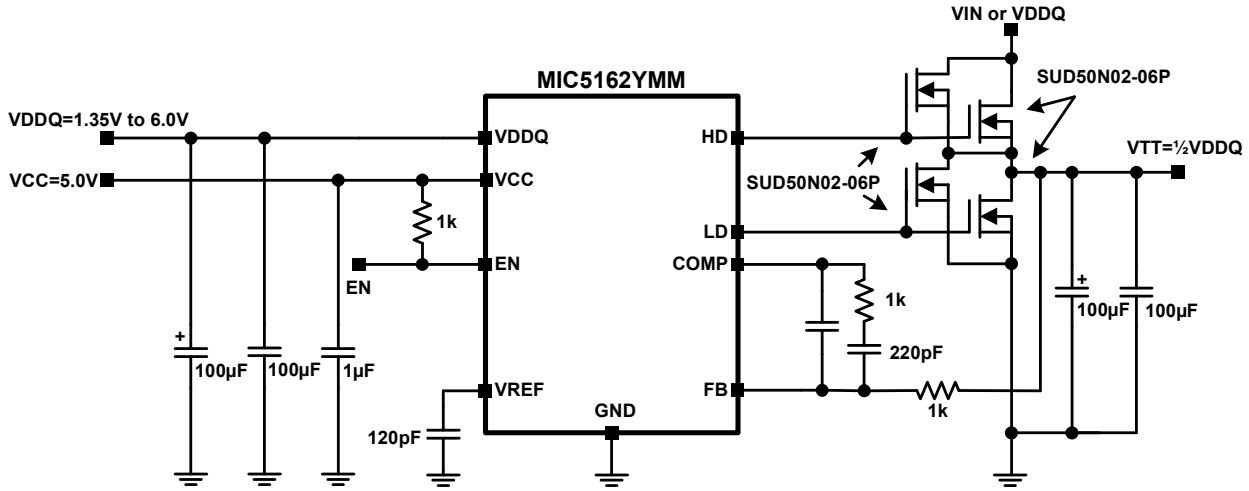
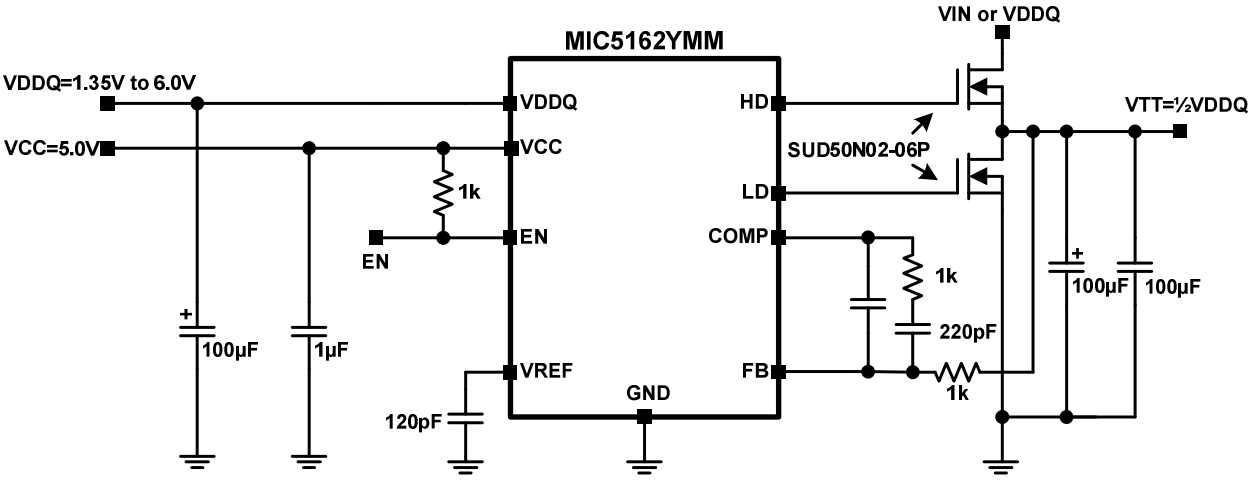
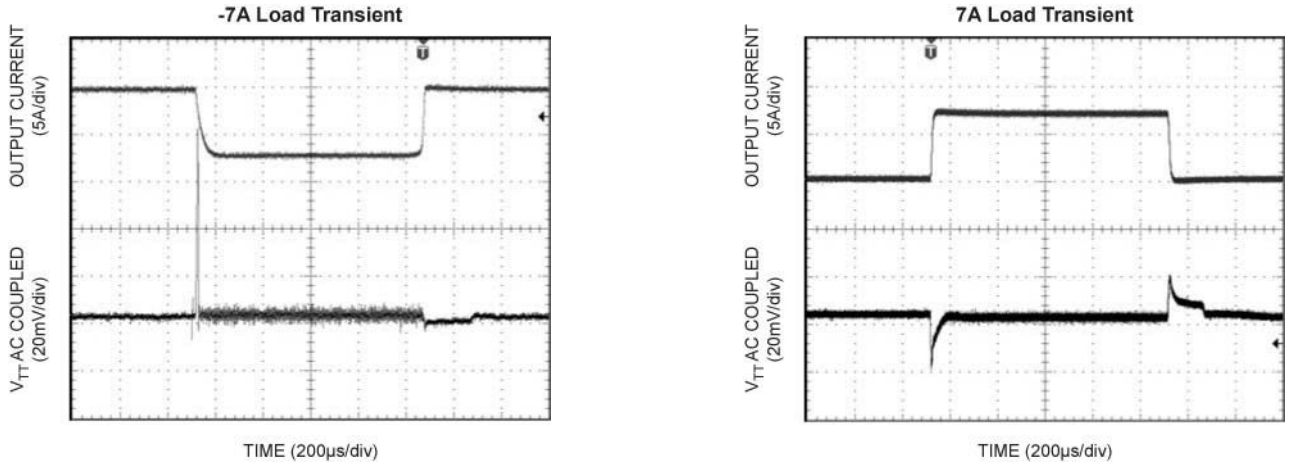


Figure 4. DDR2 Termination (Four MOSFETs Support up to 7A)



SSTL-2 Application
(Two MOSFETs Support up to 3.5A)



Ripple Measurements

To properly measure ripple on either input or output of a switching regulator, a proper ring in tip measurement is required. Standard oscilloscope probes come with a grounding clip, or a long wire with an alligator clip. Unfortunately, for high frequency measurements, this ground clip can pick up high frequency noise and erroneously inject it into the measured output ripple.

The standard evaluation board accommodates a home made version by providing probe points for both the input and output supplies and their respective grounds. This requires the removing of the oscilloscope probe sheath and ground clip from a standard oscilloscope probe and wrapping a non-shielded bus wire around the oscilloscope probe. If there does not happen to be any non-shielded bus wire immediately available, the leads from axial resistors will work. By maintaining the shortest possible ground lengths on the oscilloscope probe, true ripple measurements can be obtained.

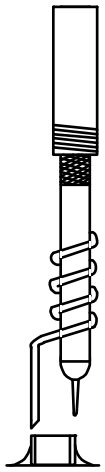


Figure 5. Low Noise Measurement

PCB Layout Guideline

Warning!!! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC5162 controller application.

IC and MOSFET

- Place the IC close to the point of load (POL).
- The trace connecting controller drive pins to MOSFETs gates should be short and wide to avoid oscillations. These oscillations are the result of tank circuit formed by trace inductance and gate capacitance.
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

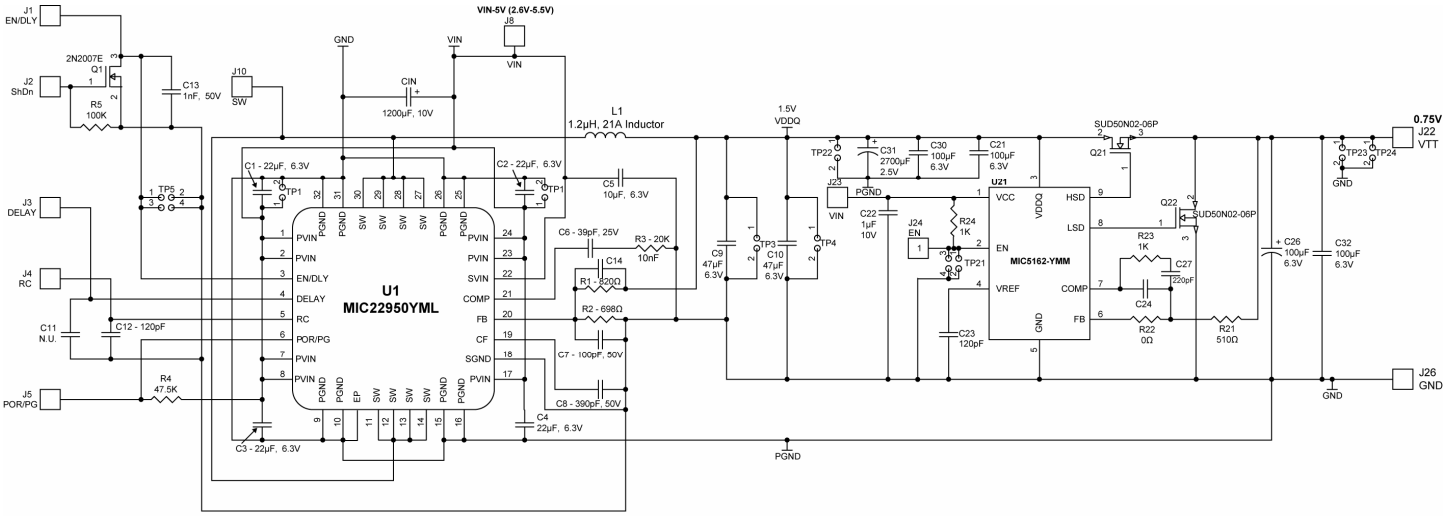
Input Capacitor

- Place the input capacitor next.
- Place the input capacitors on the same side of the board and as close to the MOSFET and IC as possible.
- Place a ceramic bypass capacitor next to MOSFET.
- Keep both the VDDQ and GND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal, but not between the input capacitors and MOSFET.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

Design Example



Micrel's MIC5162 as a DDR3 Memory Termination Device for 3.5A Application (VDDQ and MOSFET Input Tied Together)

Bill of Materials

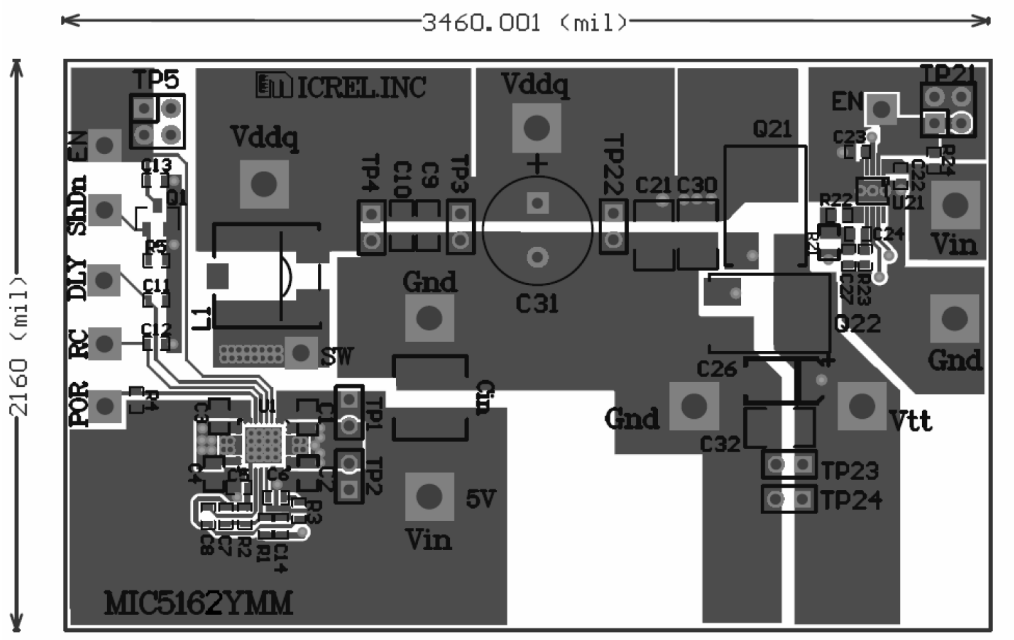
Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C3, C4	GRM21BR60J226ME39L	Murata(1)	22µF, 6.3V, Ceramic capacitor, X5R, 0805	4
	C2012X5R0J226M	TDK(2)		
	08056D226MAT2A	AVX(3)		
C5	GRM188R60J106ME47D	Murata(1)	10µF, 6.3V, Ceramic capacitor, X5R, 0603	1
	C1608X5R0J106M	TDK(2)		
	06036D106MAT2A	AVX(3)		
C6	GRM1885C1H390JA01D	Murata(1)	39pF, 50V, Ceramic capacitor, NPO, 0603	1
	C1608C0G1H390J	TDK(2)	39pF, 25V, Ceramic capacitor, NPO, 0603	
C7	06035C101MAT2A	AVX(3)	100pF, 50V, Ceramic capacitor, X7R, 0603	1
C8	GRM188R71H391KA01D	Murata(1)	390pF, 50V, Ceramic capacitor, X7R, 0603	1
C9, C10	GRM31CR60J476ME19L	Murata(1)	47µF, 6.3V, Ceramic capacitor, X5R, 1206	2
	C3216X5R0J476M	TDK(2)		
	12066D476MAT2A	AVX(3)		
C13	GRM188R71H102KA01D	Murata(1)	1nF, 50V, Ceramic capacitor, X7R, 0603	1
C14	GRM188R71H103KA01D	Murata(1)	10nF, 50V, Ceramic capacitor, X7R, 0603	1
C22	0603ZD105KAT2A	AVX(3)	1µF, 10V, Ceramic capacitor, X5R, 0603	1
	GRM188R61A105K	Murata(1)		
C23, C12	VJ0603A121JXACW1BC	Vishay(4)	120pF, 25V, Ceramic capacitor, NPO, 0603	2
	06033A121JAT2A	AVX(3)		
C27	VJ0603Y221KXACW1BC	Vishay(4)	220pF, 50V, Ceramic capacitor, X7R, 0603	1
	06033C221JAT2A	AVX(3)	220pF, 25V, Ceramic capacitor, X7R, 0603	
C26	TCJB107M006R0070	AVX(3)	100µF, 6.3V, Tantalum capacitor, 1210	1
C24, C11			N.U. 0603 ceramic cap	

Item	Part Number	Manufacturer	Description	Qty.
C30, C32, C21	C4532X5R0J107M	TDK[2]	100µF, 6.3V, Ceramic capacitor, X5R, 1812	3
C31	Open (2SEPC2700M)	Sanyo[5]	2700µF, 2.5V OS-CON Cap	1
CIN	EEE-FPA122UAP	Panasonic[8]	1200µF, 10V, Electrolytic capacitor, SMD, 10x10.2-case	1
L1	CDEP105ME-1R2MC	Sumida[6]	1.2µH, 21A, Inductor, 10.4mmX10.4mm	1
Q1	2N7002E(SOT-23)	Vishay[4]	Signal MOSFET, SOT-23-6	1
Q21, Q22	SUD50N02-06P	Vishay[4]	Low VGS(th) N-Channel 20-V (D-S)	2
R1	CRCW0603820RFRT1	Vishay Dale[4]	820Ω, Resistor, 1%, 0603	1
R2	CRCW0603698RFRT1	Vishay Dale[4]	698Ω, Resistor, 1%, 0603	1
R3	CRCW06032002FRT1	Vishay Dale[4]	20K, Resistor, 1%, 0603	1
R4	CRCW06034752FRT1	Vishay Dale[4]	47.5K, Resistor, 1%, 0603	1
R5	CRCW06031003FRT1	Vishay Dale[4]	100K, Resistor, 1%, 0603	1
R21	CRCW0805510RFKTA	Vishay Dale[4]	510Ω, Resistor, 1%, 0805	1
R23, R24	CRCW06031K00FKTA	Vishay Dale[4]	1K, Resistor, 1%, 0603	2
R22	CRCW06030000FKTA	Vishay Dale[4]	0Ω, Resistor, 1%, 0603	1
U1	**MIC22950YML**	**Micrel[7]**	**Buck Regulator 10A, 0.4MHz-2MHz Synchronous Buck Regulator**	**1**
U21	**MIC5162YMM**	**Micrel[7]**	**Dual Regulator Controller for DDR3**	**1**

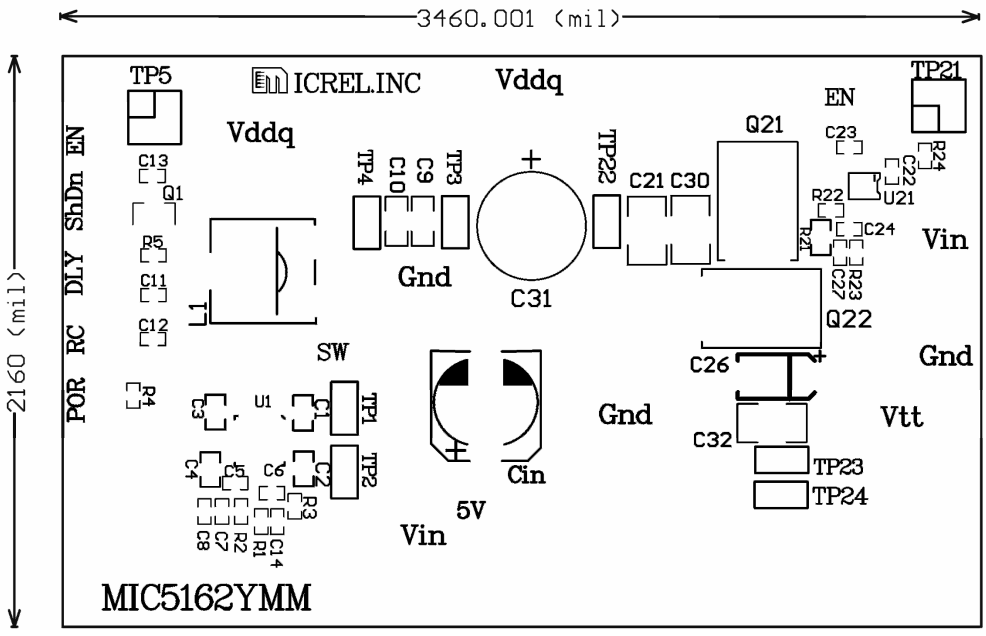
Notes:

1. Murata: www.murata.com.
2. TDK: www.tdk.com.
3. AVX: www.avx.com.
4. Vishay: www.vishay.com.
5. Sanyo: www.sanyo.com
6. Sumida: www.sumida.com
7. **Micrel, Inc.: www.micrel.com.**
8. Panasonic.: www.panasonic.com

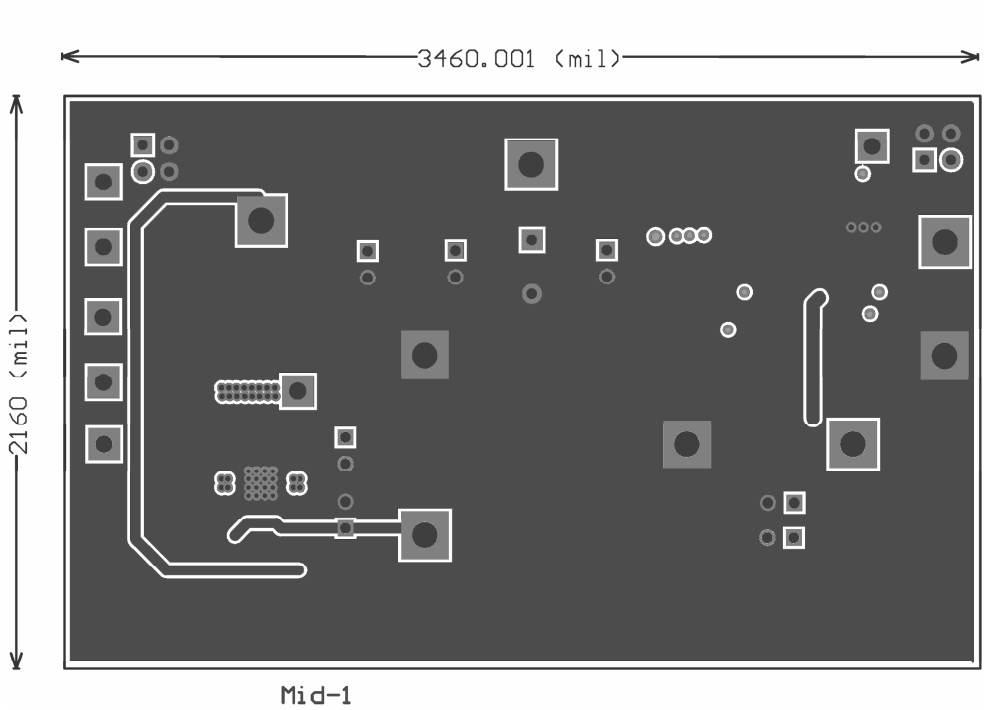
PCB Layout Recommendations (VDDQ and MOSFET Input Tied Together)



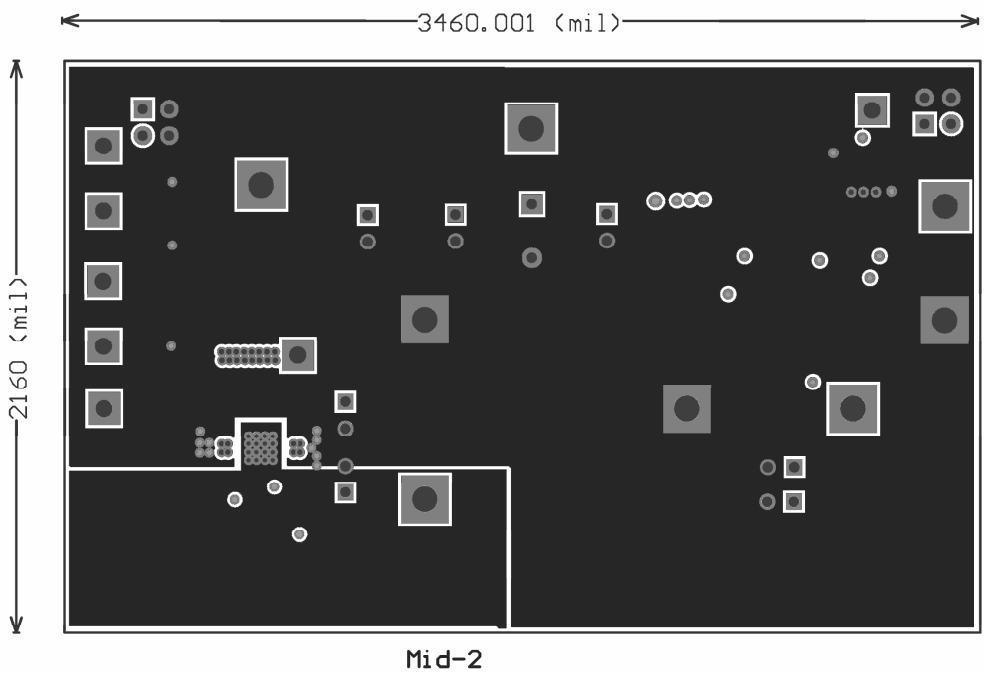
Top Layer



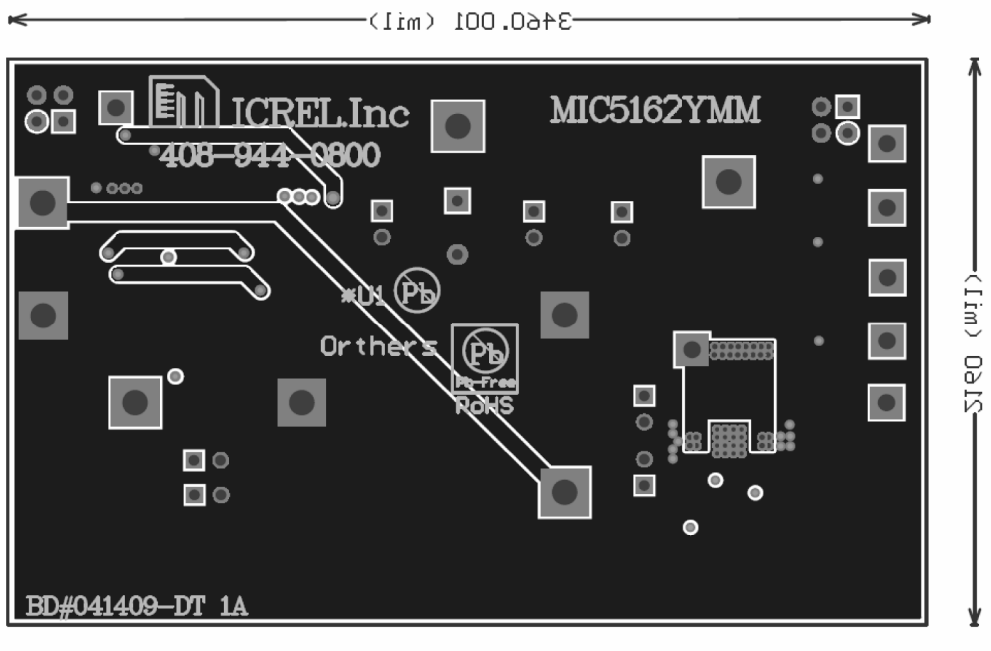
Top Component Layer



Middle Layer 1

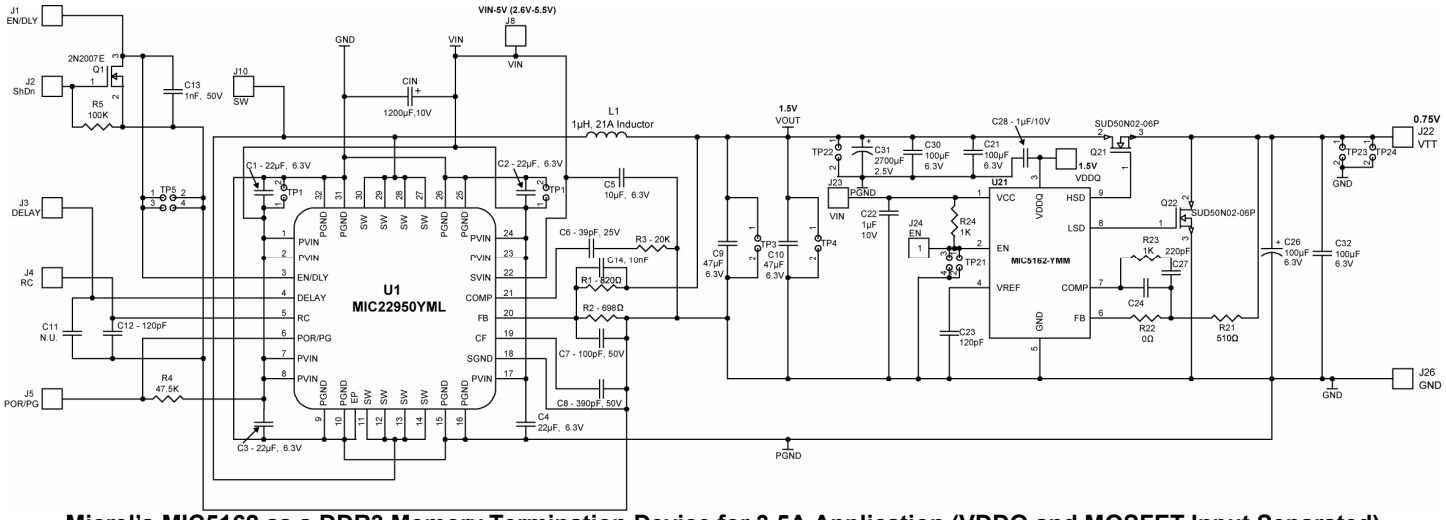


Middle Layer 2



Bottom Layer

Design Example



Micrel's MIC5162 as a DDR3 Memory Termination Device for 3.5A Application (VDDQ and MOSFET Input Separated)

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C3, C4	GRM21BR60J226ME39L	Murata(1)	22µF, 6.3V, Ceramic capacitor, X5R, 0805	4
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	08056D226MAT2A	AVX(3)		
C5	GRM188R60J106ME47D	Murata(1)	10µF, 6.3V, Ceramic capacitor, X5R, 0603	1
	C1608X5R0J106M	TDK(2)		
	06036D106MAT2A	AVX(3)		
C6	GRM1885C1H390JA01D	Murata(1)	39pF, 50V, Ceramic capacitor, NPO, 0603	1
	C1608C0G1H390J	TDK(2)	39pF, 25V, Ceramic capacitor, NPO, 0603	
C7	06035C101MAT2A	AVX(3)	100pF, 50V, Ceramic capacitor, X7R, 0603	1
C8	GRM188R71H391KA01D	Murata(1)	390pF, 50V, Ceramic capacitor, X7R, 0603	1
C9, C10	GRM31CR60J476ME19L	Murata(1)	47µF, 6.3V, Ceramic capacitor, X5R, 1206	2
	C3216X5R0J476M	TDK(2)		
	12066D476MAT2A	AVX(3)		
C13	GRM188R71H102KA01D	Murata(1)	1nF, 50V, Ceramic capacitor, X7R, 0603	1
C14	GRM188R71H103KA01D	Murata(1)	10nF, 50V, Ceramic capacitor, X7R, 0603	1
C22, C28	0603ZD105KAT2A	AVX(3)	1µF, 10V, Ceramic capacitor, X5R, 0603	2
	GRM188R61A105K	Murata(1)		
C23, C12	VJ0603A121JXACW1BC	Vishay(4)	120pF, 25V, Ceramic capacitor, NPO, 0603	2
	06033A121JAT2A	AVX(3)		
C27	VJ0603Y221KXACW1BC	Vishay(4)	220pF, 50V, Ceramic capacitor, X7R, 0603	1
	06033C221JAT2A	AVX(3)	220pF, 25V, Ceramic capacitor, X7R, 0603	
C26	TCJB107M006R0070	AVX(3)	100µF, 6.3V, Tantalum capacitor, 1210	1
C24, C11			N.U. 0603 ceramic cap	

Item	Part Number	Manufacturer	Description	Qty.
C30, C32, C21	C4532X5R0J107M	TDK[2]	100µF, 6.3V, Ceramic capacitor, X5R, 1812	3
C31	Open (2SEPC2700M)	Sanyo[5]	2700µF, 2.5V OS-CON Cap	1
CIN	EEE-FPA122UAP	Panasonic[8]	1200µF, 10V, Electrolytic capacitor, SMD, 10x10.2-case	1
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Q1	2N7002E(SOT-23)	Vishay[4]	Signal MOSFET, SOT-23-6	1
Q21, Q22	SUD50N02-06P	Vishay[4]	Low VGS(th) N-Channel 20-V (D-S)	2
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R2	CRCW0603698RFRT1	Vishay Dale[4]	698Ω, Resistor, 1%, 0603	1
R3	CRCW06032002FRT1	Vishay Dale[4]	20K, Resistor, 1%, 0603	1
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R21	CRCW0805510RFKTA	Vishay Dale[4]	510Ω, Resistor, 1%, 0805	1
R23, R24	CRCW06031K00FKTA	Vishay Dale[4]	1K, Resistor, 1%, 0603	2
R22	CRCW06030000FKTA	Vishay Dale[4]	0Ω, Resistor, 1%, 0603	1
U1	**MIC22950YML**	**Micrel[7]**	**Buck Regulator 10A, 0.4MHz-2MHz Synchronous Buck Regulator**	**1**
U21	**MIC5162YMM**	**Micrel[7]**	**Dual Regulator Controller for DDR3**	**1**

Notes:

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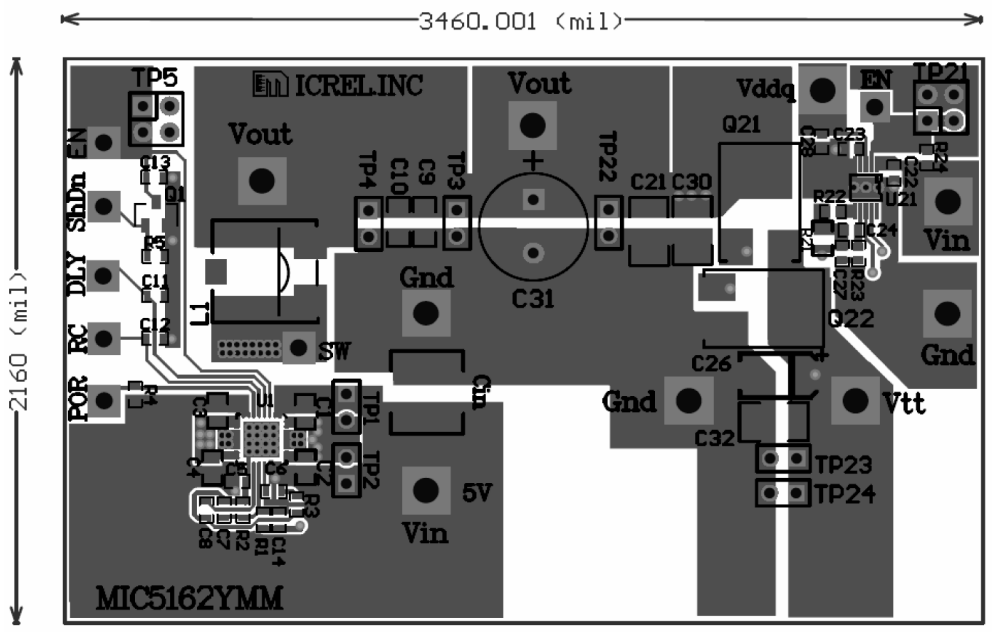
8. Panasonic.: www.panasonic.com

PCB Layout Recommendations (VDDQ and MOSFET Input Separated)



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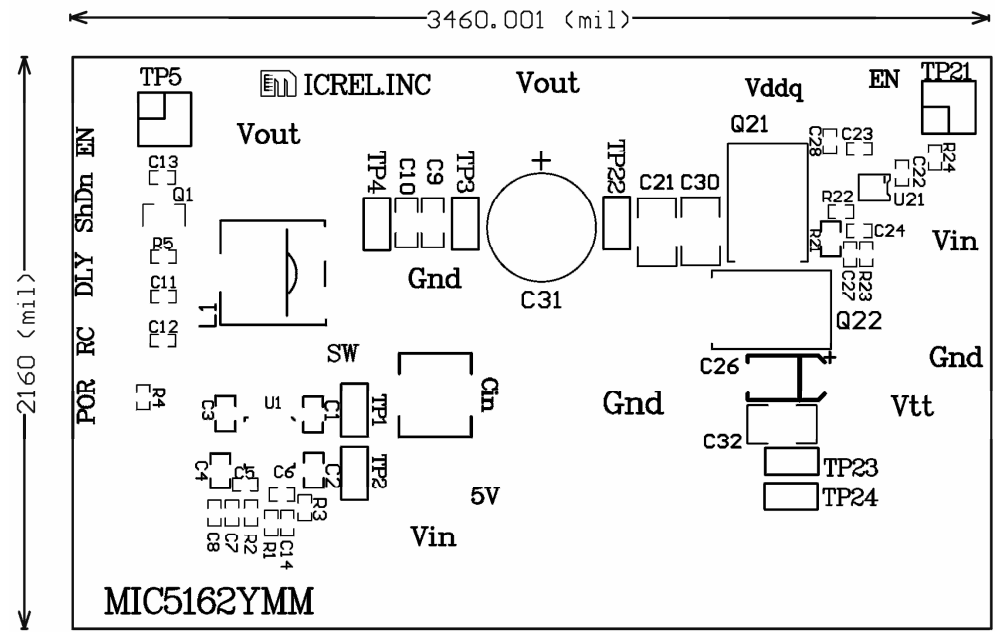

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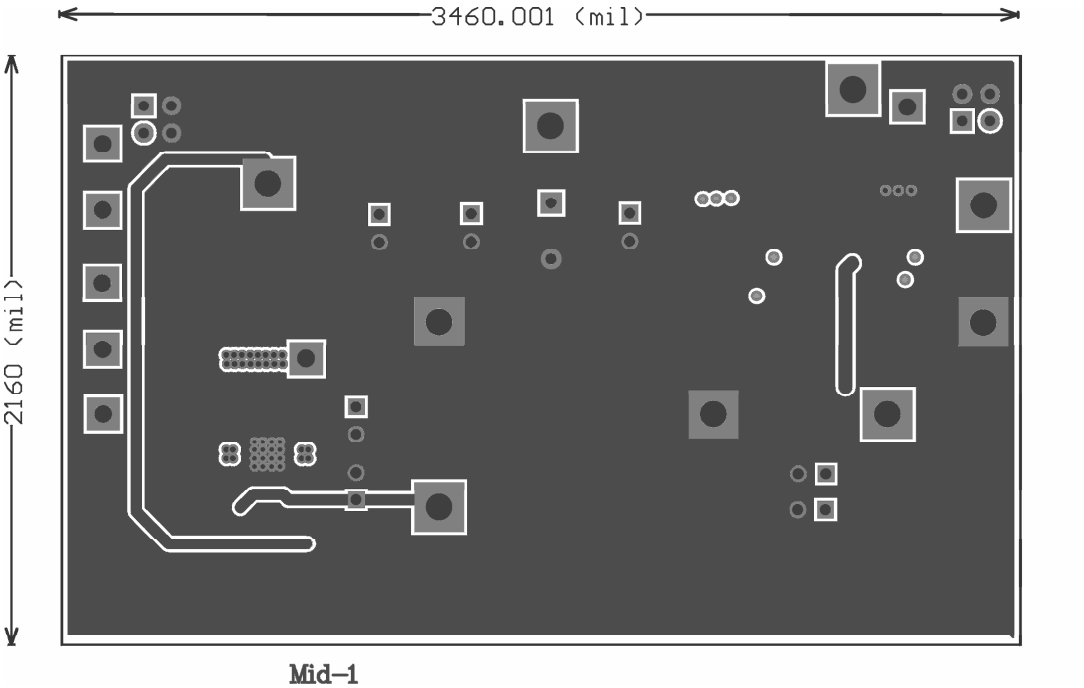
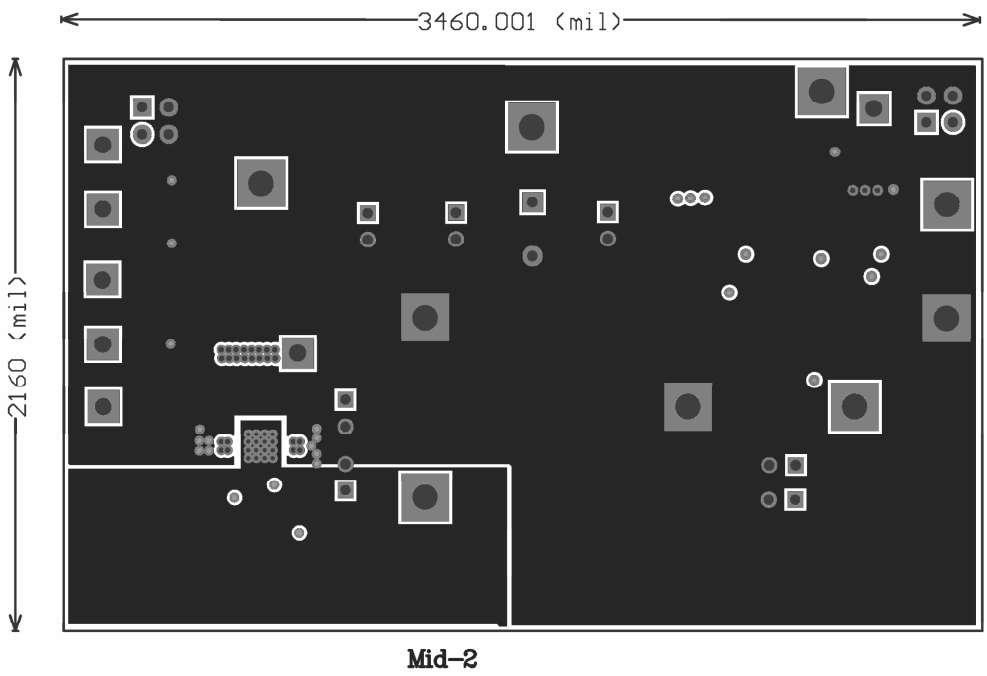
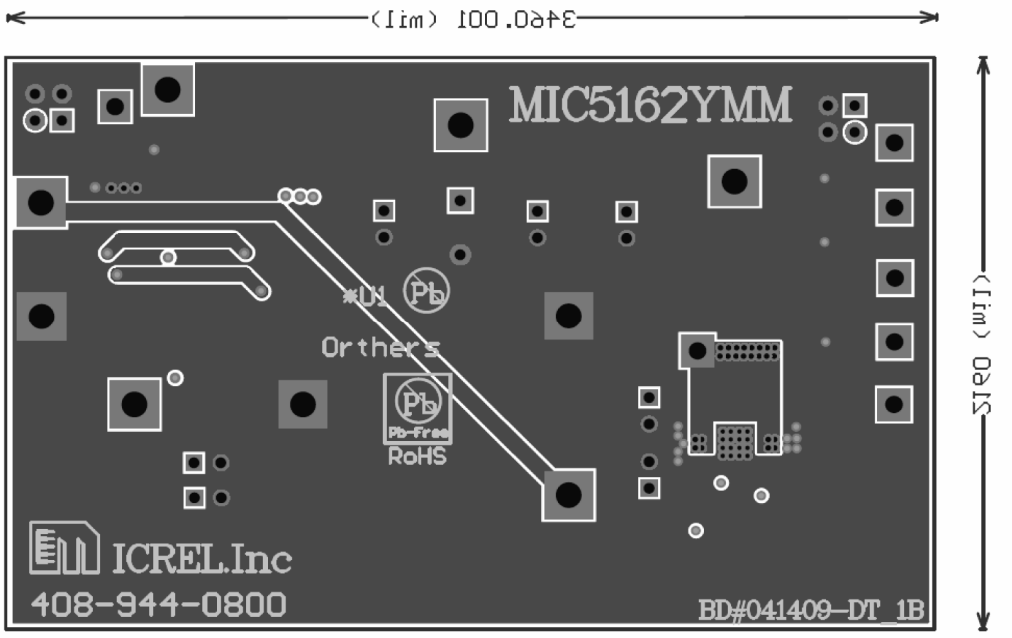


Middle Layer 1

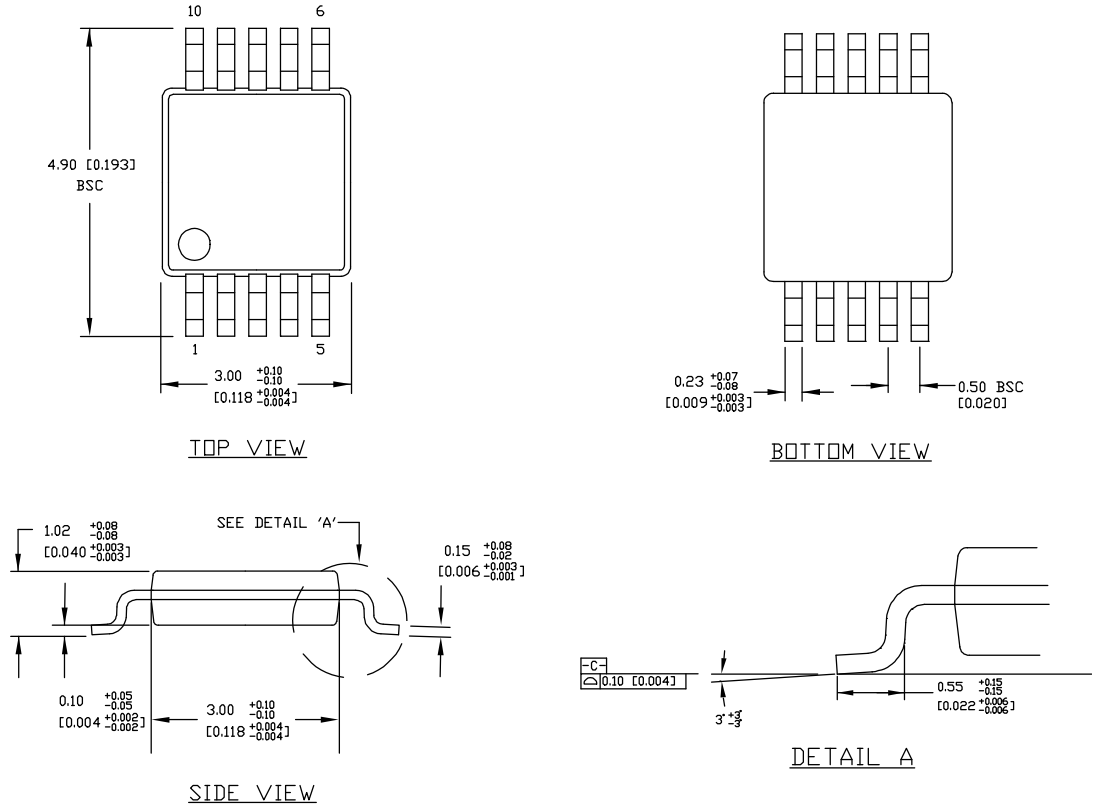


Middle Layer 2



Bottom Layer

Package Information



NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

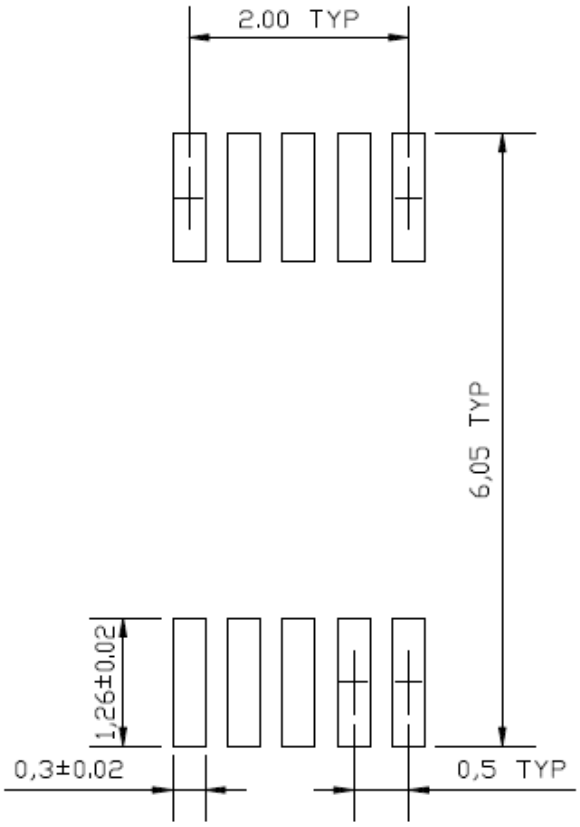
10-Pin MSOP (MM)

Recommended Landing Pattern

FAX# (408) 944-0970

Recommended Land Pattern for MSOP 10 Lead

LP # MSOP-10LD-LP-1
All units are in mm
Tolerance ± 0.05 if not noted



10-Pin MSOP (MM)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com