MCP6D11

Low-Noise, Precision, 90 MHz Differential I/O Amplifier

Features

- Low Power
  - I_Q: 1.4 mA
  - Supply Voltage Range: 2.5V to 5.5V
- Gain-Bandwidth Product: 90 MHz
- Slew Rate: 25V/µs
- Low Noise: 5.0 nV/√Hz, f = 10 kHz
- Low Distortion ($2V_{p-p}$, 10 kHz):
  - HD2: -138 dBc
  - HD3: -137 dBc
- Fast Settling: 200 ns to 0.01%
- Low Offset: 150 µV Max.
- Power-Down Function
- Input Vcm-Range Includes Negative Rail
- Rail-to-Rail Output
- Small Packages: MSOP-8, 3 x 3 mm QFN-16
- Extended Temperature Range: -40°C to +125°C

Typical Applications

- Precision ADC Driver:
  - 14/16/18-bit SAR ADCs
  - Delta-Sigma ADCs
- Single-Ended to Differential Conversion
- Differential Active Filter
- Line Drivers

Design Aids

- Microchip Advanced Part Selector (MAPS)
- Application Notes

Related Parts

- MCP331x1D SAR ADCs

General Description

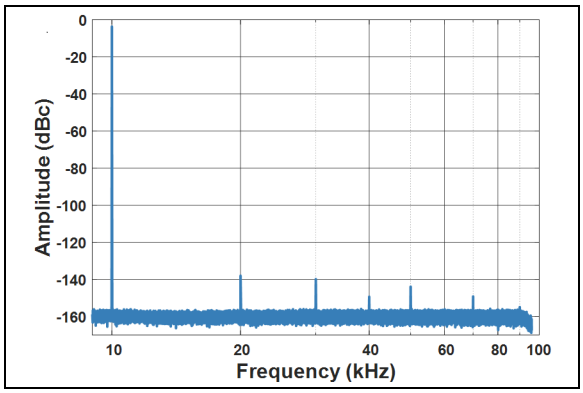
The MCP6D11 from Microchip Technology is a low-noise, low-distortion Differential I/O Amplifier optimized for driving high-performance 14-, and 16-Bit SAR ADCs, such as the MCP331x1D ADC family. Featuring a low 5.0 nV/√Hz input-referred voltage noise and distortion of less than -116 dBc with an input signal of up to 100 kHz (2Vpp), the MCP6D11 consumes only 3.5 mW of quiescent power on a 2.5V supply. For power sensitive applications, a Power-Down function reduces the power consumption to less than 13 µW.

Through its V_{OCM} pin, the MCP6D11 allows easy control of its output common-mode voltage, which can be set independently of the input common-mode voltage. This, coupled with an input common-mode range that extends below the negative supply rail, and a near rail-to-rail output swing capability, results in a simple driver amplifier solution for a variety of ADCs.

The MCP6D11 is the ideal interface solution for converting single-ended, ground-referenced signal sources into a fully differential output signal required to preserve the high performance of today's ultra-low distortion, single-supply ADCs.

The MCP6D11 is specified for the -40°C to +125°C temperature range and is available in QFN-16 (3 x 3 mm) and MSOP-8 package options.

MCP6D11 Harmonic Distortion with a 10 kHz, 2Vpp Signal



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NOTES:

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 6.0V
Supply Voltage Turn-on/off max. dV/dt at +25°C ..... ±0.35V/µs
Supply Voltage Turn-on/off max. dV/dt at +125°C ..... ±0.2V/µs
Current at all Inputs (continuous) ..... ±10 mA
Voltage at all Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD}+0.3V
Differential Input Voltage ..... ±1.0V
Current at Output and Supply Pins (continuous) ..... ±20 mA
Storage Temperature ..... -65°C to +150°C
Maximum Junction Temperature ..... +155°C
ESD protection on all pins (HBM, CDM) ..... ≥ 4 kV, 2 kV

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, **V_{DD} = +2.5V to 5.5V, V_{SS} = 0V**, PD\ = V_{DD}, V_{OCM} = open, V_{ICM} = V_{DD}/2, Single-ended input, G = 1V/V, R_F = R_G = 1 kΩ, R_L = 1 kΩ between differential outputs.

Parameters	Sym.	Min.	Typ.	Max.	Units	Test Level (Note 1)	Conditions
AC Response							
Gain-Bandwidth Product	GBWP	—	90	—	MHz	C	G = 10V/V
Bandwidth (Small-signal, -3 dB)	BW	—	82	—	MHz	C	G = 1V/V, V_{OUT_DM} = 20mVpp, V_{DD} = 5V
		—	80	—			G = 1V/V, V_{OUT_DM} = 20mVpp, V_{DD} = 3V
		—	48	—			G = 2V/V, V_{OUT_DM} = 20mVpp, V_{DD} = 5V
		—	10	—			G = 10V/V, V_{OUT_DM} = 20mVpp, V_{DD} = 5V
Bandwidth (Large-signal, -3 dB)	BW	—	6.4	—	MHz	C	G = 1V/V, V_{OUT_DM} = 2Vpp, V_{DD} = 5V
Bandwidth for 0.1 dB Gain Flatness		—	4	—	MHz	C	G = 1V/V, V_{OUT_DM} = 2Vpp, V_{DD} = 5V
Slew Rate (differential)	SR	—	27	—	V/µs	C	G = 1V/V, V_{OUT_DM} = 2V step, V_{DD} = 5V
		—	26	—			G = 2V/V, V_{OUT_DM} = 2V step, V_{DD} = 5V
		—	24	—			G = 1V/V, V_{OUT_DM} = 2V step, V_{DD} = 3V
		—	23	—			G = 2V/V, V_{OUT_DM} = 2V step, V_{DD} = 3V
Settling Time to 0.1%	t_S	—	160	—	ns	C	G = 1V/V, V_{OUT_DM} = 2V step, V_{DD} = 5V
		—	170	—			G = 1V/V, V_{OUT_DM} = 2V step, V_{DD} = 3V
Settling Time to 0.01%		—	200	—			G = 1V/V, V_{OUT_DM} = 2V step, V_{DD} = 5V
		—	215	—			G = 1V/V, V_{OUT_DM} = 2V step, V_{DD} = 3V
Rise and Fall Times	t_R, t_F	—	34	—	ns	C	V_{OUT_DM} = 1Vpp step
Overdrive Recovery Time	t_{rec}	—	150	—	ns	C	V_{DD} = 5V, 0.5V overdrive
		—	200	—			V_{DD} = 3V, 0.5V overdrive
Closed-Loop Output Impedance	R_{out}	—	0.1	—	Ω	C	f = 1 MHz, differential
Output Balance Error	BAL	—	85	—	dB	C	At DC

Note 1: "Test Level" designation: A = 100% production tested at 25°C; B = not production tested, limits set by characterization and/or simulation, C = values for information only (based on characterization or design).

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AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, **V_{DD} = +2.5V to 5.5V, V_{SS} = 0V**, PD\ = V_{DD}, V_{OCM} = open, V_{ICM} = V_{DD}/2, Single-ended input, G = 1V/V, R_F = R_G = 1 kΩ, R_L = 1 kΩ between differential outputs.

Parameters	Sym.	Min.	Typ.	Max.	Units	Test Level (Note 1)	Conditions
Noise and Distortion							
Input Noise Voltage Density	e_{ni}	—	5.0	—	nV/√Hz	C	at f > 10 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	pA/√Hz	C	at f ≥ 100 kHz
2nd Order Harmonic Distortion	HD2	—	-137	—	dBc	C	f = 10 kHz, 2Vpp, V_{DD} = 3V
		—	-138	—			f = 10 kHz, 2Vpp, V_{DD} = 5V
		—	-118	—			f = 100 kHz, 2Vpp, V_{DD} = 3V
		—	-120	—			f = 100 kHz, 2Vpp, V_{DD} = 5V
3rd Order Harmonic Distortion	HD3	—	-137	—	dBc	C	f = 10 kHz, 2Vpp, V_{DD} = 3V
		—	-137	—			f = 10 kHz, 2Vpp, V_{DD} = 5V
		—	-116	—			f = 100 kHz, 2Vpp, V_{DD} = 3V
		—	-116	—			f = 100 kHz, 2Vpp, V_{DD} = 5V

Note 1: "Test Level" designation: A = 100% production tested at 25°C; B = not production tested, limits set by characterization and/or simulation, C = values for information only (based on characterization or design).

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, **V_{DD} = +2.5V to 5.5V, V_{SS} = 0V**, PD\ = V_{DD}, V_{OCM} = open, V_{ICM} = V_{DD}/2, Single-ended input, G = 1V/V, R_F = R_G = 1 kΩ, R_L = 1 kΩ between differential outputs.

Parameters	Sym.	Min.	Typ.	Max.	Units	Test Level (Note 1)	Conditions
Input Offset							
Input Offset Voltage	V_{OS}	-150	±25	+150	µV	A	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T_A$	-2.0	±0.5	+2.0	µV/°C	B	T_A = -40°C to +125°C (Note 4)
Power Supply Rejection	PSRR	100	117	—	dB	A	
Input Bias Current and Impedance							
Input Bias Current	I_{B+}, I_{B-}	-1.7	-0.7	—	µA	A	(Note 3)
Input Bias Current, across Temperature		-1.9	-0.8	-0.4	µA	B	T_A = +85°C
		-2.1	-1.1	-0.5	µA	B	T_A = +125°C
Input Bias Current Drift	$\Delta I_B/\Delta T_A$	-3.6	±2.75	+3.6	nA/°C	B	T_A = -40°C to +125°C (QFN) (Note 4)
Input Offset Current	I_{OS}	-60	±10	+60	nA	A	
Input Offset Current Drift	$\Delta I_{OS}/\Delta T_A$	-130	±40	+130	pA/°C	B	T_A = -40°C to +125°C (QFN) (Note 4)
Differential Input Impedance	Z_{DIFF}	—	88||1.0	—	kΩ||pF	C	

Note 1: "Test Level" designation: A = 100% production tested at 25°C; B = not production tested, limits set by characterization and/or simulation, C = values for information only (based on characterization or design).

2: The V_{ICM} spec is supported by the CMRR tests.

3: Negative polarity sign indicates current flowing out of node.

4: Based on data taken at the temperature range end-points (-40°C, +125°C) and calculated deltas are divided by the temperature range. The Max./Min. specifications are set using +/-4 standard deviations on the device distribution.

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DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, **V_{DD} = +2.5V to 5.5V, V_{SS} = 0V**, PD\ = V_{DD}, V_{OCM} = open, V_{ICM} = V_{DD}/2, Single-ended input, G = 1V/V, R_F = R_G = 1 kΩ, R_L = 1 kΩ between differential outputs.

Parameters	Sym.	Min.	Typ.	Max.	Units	Test Level (Note 1)	Conditions
Common-Mode							
Common-Mode Input Range, high	V_{ICM_H}	V_{DD} - 1.0	V_{DD} - 0.9	—	V	A	(Note 2)
		V_{DD} - 1.2	V_{DD} - 1.0	—		B	T_A = -40°C to + 125°C
Common-Mode Input Range, low	V_{ICM_L}	—	V_{SS} - 0.25	V_{SS} - 0.15	V	A	(Note 2)
		—	V_{SS} - 0.1	V_{SS}		B	T_A = -40°C to + 125°C
Common-Mode Rejection Ratio	CMRR	95	112	—	dB	A	V_{DD} = 5.5V
		95	110	—		B	V_{DD} = 5.5V T_A = -40°C to + 125°C
		90	107	—		A	V_{DD} = 2.5V
		90	105	—		B	V_{DD} = 2.5V T_A = -40°C to + 125°C
Open Loop Gain							
DC Open Loop Gain	A_{OL}	106	124	—	dB	A	V_{DD} = 5.5V V_{OUT} = 0.4V to V_{DD} – 0.4V
		102	118	—		B	V_{DD} = 5.5V, T_A = -40°C to +125°C
		106	121	—		A	V_{DD} = 2.5V, V_{OUT} = 0.25V to V_{DD} – 0.25V
		102	114	—		B	V_{DD} = 2.5V, T_A = -40°C to +125°C
Internal Feedback Trace Resistance		—	3	—	Ω	C	QFN package only; pins 10-4, 11-1
Internal Feedback Trace Resistance Mismatch		—	0.05	—	Ω	C	QFN package only; pins 10-4, 11-1
Output							
Maximum Output Voltage Swing	V_{OL}	—	V_{SS} + 75	V_{SS} + 100	mV	A	V_{DD} = 5.5V, 0.5V overdrive
		—	V_{SS} + 33	V_{SS} + 50			V_{DD} = 2.5V, 0.5V overdrive
	V_{OH}	V_{DD} - 150	V_{DD} - 100	—			V_{DD} = 5.5V, 0.5V overdrive
		V_{DD} - 75	V_{DD} - 50	—			V_{DD} = 2.5V, 0.5V overdrive
Output Short Circuit Current	I_{SC}	—	±66	—	mA	C	V_{DD} = 2.5V
		—	±75	—			V_{DD} = 5.5V

Note 1: "Test Level" designation: A = 100% production tested at 25°C; B = not production tested, limits set by characterization and/or simulation, C = values for information only (based on characterization or design).

2: The V_{ICM} spec is supported by the CMRR tests.

3: Negative polarity sign indicates current flowing out of node.

4: Based on data taken at the temperature range end-points (-40°C, +125°C) and calculated deltas are divided by the temperature range. The Max./Min. specifications are set using +/-4 standard deviations on the device distribution.

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DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, **V_{DD} = +2.5V to 5.5V, V_{SS} = 0V**, PD\ = V_{DD}, V_{OCM} = open, V_{ICM} = V_{DD}/2, Single-ended input, G = 1V/V, R_F = R_G = 1 kΩ, R_L = 1 kΩ between differential outputs.

Parameters	Sym.	Min.	Typ.	Max.	Units	Test Level (Note 1)	Conditions
Output Common-Mode Voltage Control (V_{OCM})							
Input Voltage Range	V_{CM}	1.0	0.9 to V_{DD} - 1.0	V_{DD} - 1.1	V	A	
Gain	G_{OCM}	0.99	1	1.01	V/V	B	
Input Offset Voltage	V_{OS}	-5	±0.8	+5	mV	A	V_{OCM} pin driven to (V_{DD}/2)
		-10	±2	+10			V_{OCM} pin floating
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T_A$	-45	±15	+30	µV/°C	B	T_A = -40°C to +125°C, V_{DD} = 2.5V (QFN) (Note 4)
		-25	±6.9	+25		B	T_A = -40°C to +125°C, V_{DD} = 5.5V (QFN) (Note 4)
Input Bias Current	I_B	—	±0.01	+1.5	µA	B	
Input Impedance	Z_{CM}	—	46k||2	—	Ω||pF	B	For internal V_{DD}/2 reference
Bandwidth (Small-Signal, -3 dB)	BWss	—	45	—	MHz	C	V_{OCM} = 100mVpp
Slew Rate	SR	—	14	—	V/µs	C	1V step
Power Supply							
Supply Voltage	V_{DD}	2.5	—	5.5	V	A	V_{SS} = 0V
Quiescent Current	I_Q	1.0	1.49	1.8	mA	A	V_{DD} = 5.5V, I_O = 0
		0.9	—	2.1		B	V_{DD} = 5.5V, T_A = -40°C to +125°C
		1.0	1.4	1.8		A	V_{DD} = 2.5V, I_O = 0
		0.8	—	2.0		B	V_{DD} = 2.5V, T_A = -40°C to +125°C
Quiescent Current Drift	$\Delta I_Q/T_A$	—	3.8	—	µA/°C	C	T_A = -40°C to +125°C (Note 4)
Power-Up Time	t_{up}	—	30	—	µs	C	
Power-Down (PD\)							
Quiescent Current	I_{Q_PD}	—	5	7	µA	A	PD\ = V_{SS}
Input Voltage, Logic High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	A	
Input Voltage, Logic Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	A	
Input Current, Logic High	I_{IH}	—	+5	—	nA	B	PD\ = V_{DD}
Input Current, Logic Low	I_{IL}	—	-5	—	nA	B	PD\ = V_{SS}
Turn-on Time	t_{on}	—	1.0	1.5	µs	B	V_{DD} = 5.5V, Vout = 90% of final value
		—	2.5	3			V_{DD} = 2.5V, Vout = 90% of final value
Turn-off Time	t_{off}	—	0.04	0.05	µs	B	V_{DD} = 5.5V, Vout = 10% of final value
		—	0.05	0.06			V_{DD} = 2.5V, Vout = 10% of final value

Note 1: "Test Level" designation: A = 100% production tested at 25°C; B = not production tested, limits set by characterization and/or simulation, C = values for information only (based on characterization or design).

2: The V_{ICM} spec is supported by the CMRR tests.

3: Negative polarity sign indicates current flowing out of node.

4: Based on data taken at the temperature range end-points (-40°C, +125°C) and calculated deltas are divided by the temperature range. The Max./Min. specifications are set using +/-4 standard deviations on the device distribution.

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TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for V_{DD} - V_{SS} = 2.5V to 5.5V						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-MSOP	θ_{JA}	—	170	—	°C/W	
Thermal Resistance, 16L-QFN	θ_{JA}	—	60	—	°C/W	

Note 1: The MCP6D11 operates over this temperature range, but the Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +155°C.

NOTES:

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2.0 PIN DESCRIPTIONS

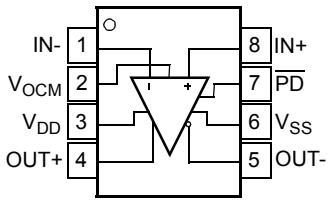
TABLE 2-1: PIN FUNCTION TABLE

MCP6D11		Symbol	Description
MSOP-8	QFN-16		
1	3	IN-	Negative input (Summing Junction)
2	9	V_{OCM}	Output common-mode voltage; a high impedance input
3	5,6,7,8	V_{DD}	Positive Power Supply
4	10	OUT+	Positive output
5	11	OUT-	Negative output
6	13,14,15,16	V_{SS}	Negative Power Supply
7	12	PD\	Power-Down (Low = V_{SS} = Low Power mode; High = V_{DD} = normal operation)
8	2	IN+	Positive Input (Summing Junction)
--	1	FB-	Negative feedback; same signal as negative output (OUT-)
--	4	FB+	Positive feedback; same signal as positive output (OUT+)
--	17	EP	'Exposed Thermal Pad' on bottom side of QFN package only (Note 1)

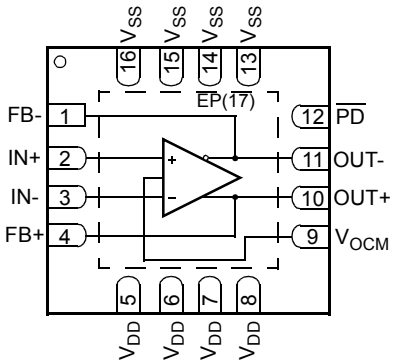
Note 1: The exposed thermal pad should be soldered to a low-noise ground or power plane. This pad is electrically isolated from the die (using non-conductive die attach), however the pad must be connected to a power or ground and can not be left floating.

Package Types

MCP6D11,
MSOP-8



MCP6D11,
QFN-16



NOTES:

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3.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} - V_{SS} = 2.5V to 5.5V, V_{OCM} = open, V_{ICM} = mid-supply, PD\ = V_{DD}, single-ended input, 50Ω input match, G = 1V/V, R_F = R_G = 1 kΩ, C_L = 0 pF and R_L = 1 kΩ between the differential outputs.

3.1 Frequency Response

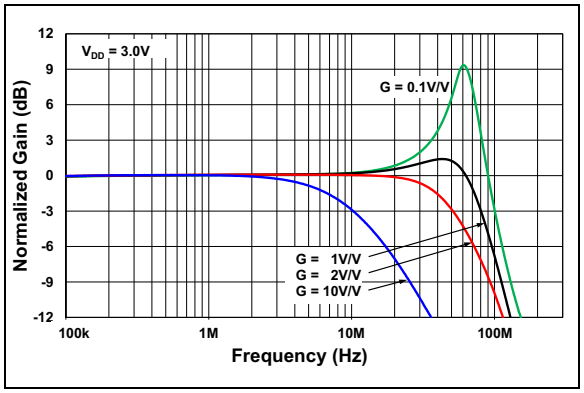

FIGURE 3-1: *Small-Signal Frequency Response vs. Gain, V_{OUTDM} = 20mVpp.*

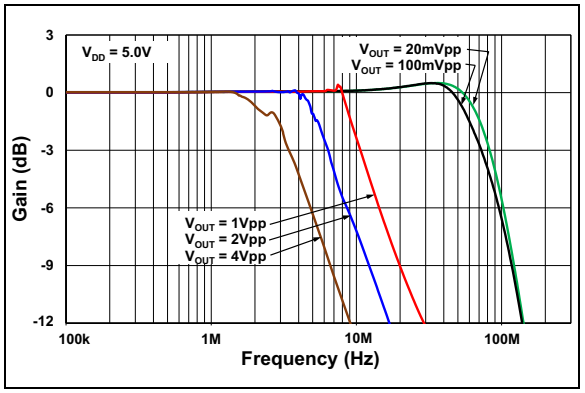

FIGURE 3-4: *Small-Signal Frequency Response vs. V_{OUTDM} (Gain = 1V/V).*

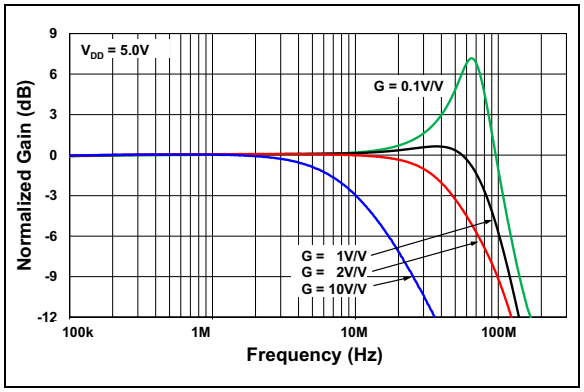

FIGURE 3-2: *Small-Signal Frequency Response vs. Gain, V_{OUTDM} = 20mVpp.*

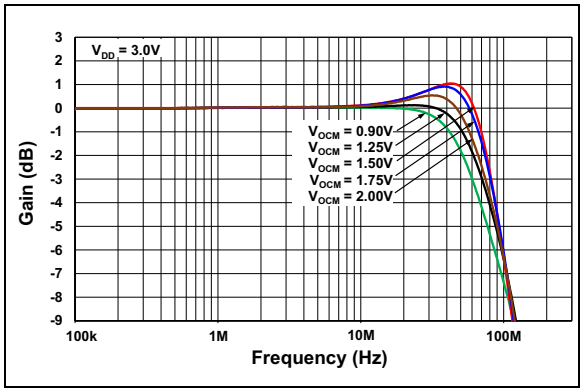

FIGURE 3-5: *Small-Signal Frequency Response vs V_{OCM}, Gain = 1V/V.*

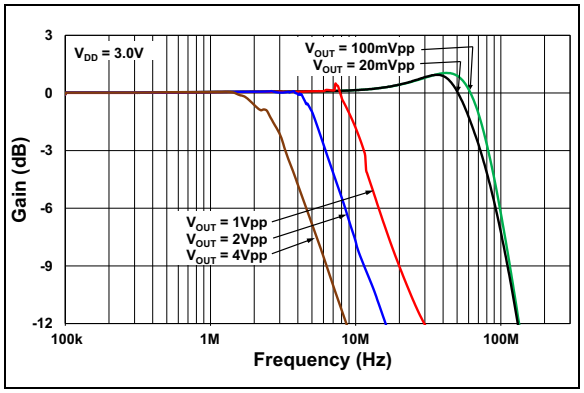

FIGURE 3-3: *Small-Signal Frequency Response vs. V_{OUTDM} (Gain = 1V/V).*

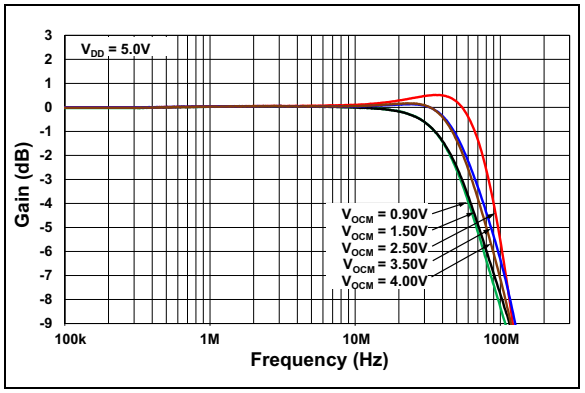

FIGURE 3-6: *Small-Signal Frequency Response vs V_{OCM}, Gain = 1V/V.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} - V_{SS} = 2.5V to 5.5V, V_{OCM} = open, V_{ICM} = mid-supply, PD\ = V_{DD}, single-ended input, 50Ω input match, G = 1V/V, R_F = R_G = 1 kΩ, C_L = 0 pF and R_L = 1 kΩ between the differential outputs.

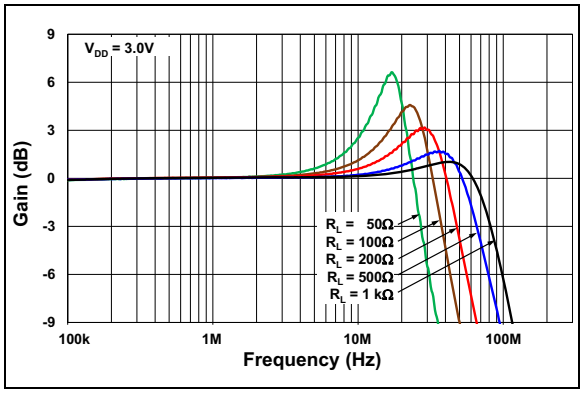

FIGURE 3-7: *Small-Signal Frequency Response vs. R-Loads, Gain = 1V/V.*

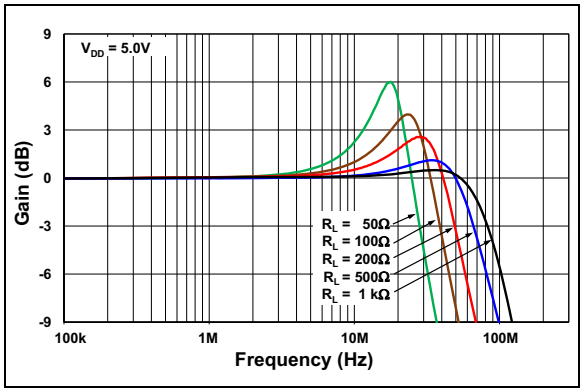

FIGURE 3-8: *Small-Signal Frequency Response vs R-Loads, Gain = 1V/V.*

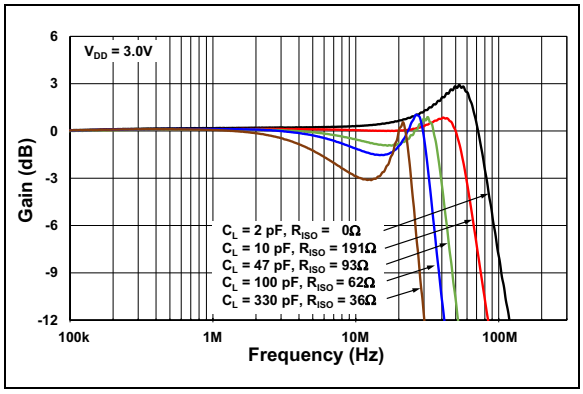

FIGURE 3-9: *Small-Signal Frequency Response vs C-Loads.*

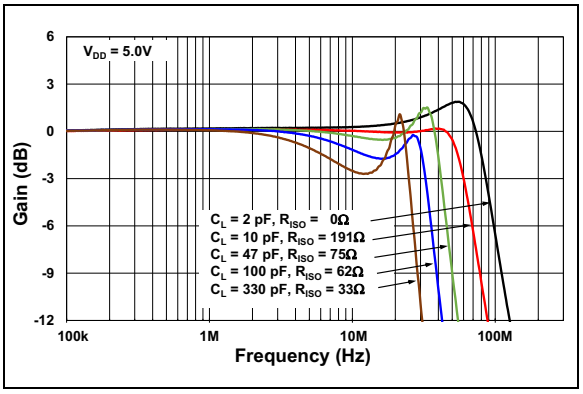

FIGURE 3-10: *Small-Signal Frequency Response vs. C-Loads.*

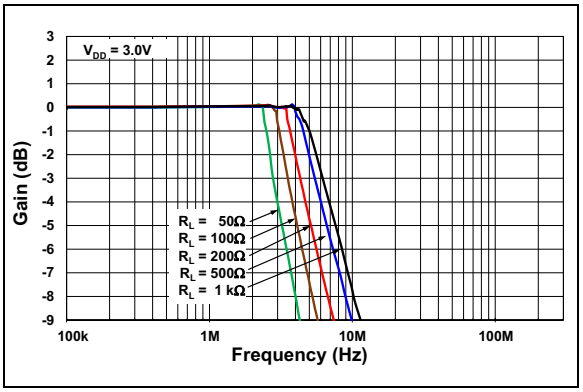

FIGURE 3-11: *Large-Signal Frequency Response vs. R-Loads, V_{OUTDM} = 2Vpp.*

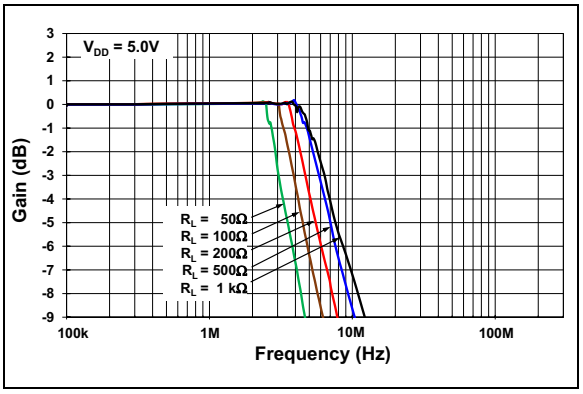

FIGURE 3-12: *Large-Signal Frequency Response vs. R-Loads, V_{OUTDM} = 2Vpp.*

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Note: Unless otherwise indicated, T_A = 25°C, V_{DD} - V_{SS} = 2.5V to 5.5V, V_{OCM} = open, V_{ICM} = mid-supply, PD\ = V_{DD}, single-ended input, 50Ω input match, G = 1V/V, R_F = R_G = 1 kΩ, C_L = 0 pF and R_L = 1 kΩ between the differential outputs.

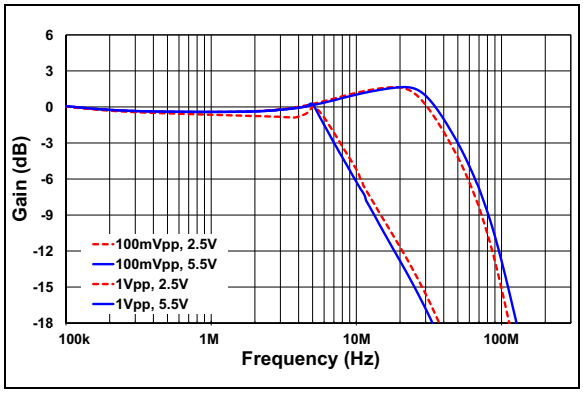

FIGURE 3-13: *V_{OCM} Small- and Large-Signal Frequency Response, Gain = 1V/V.*

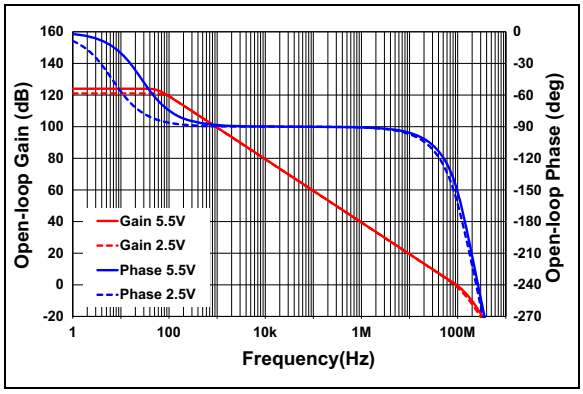

FIGURE 3-16: *Differential Open-Loop Gain and Phase vs. Frequency (Simulation).*

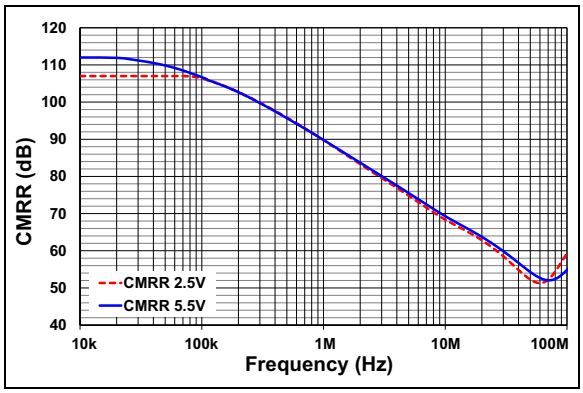

FIGURE 3-14: *CMRR vs. Frequency (Simulation).*

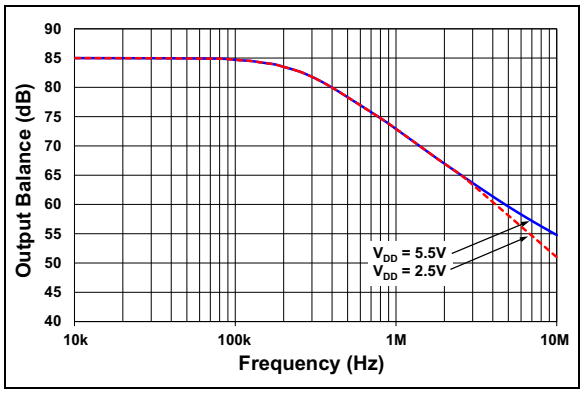

FIGURE 3-17: *Output Balance vs. Frequency, V_{OUTDM} = 100mVpp, Gain = 1V/V (Simulation).*

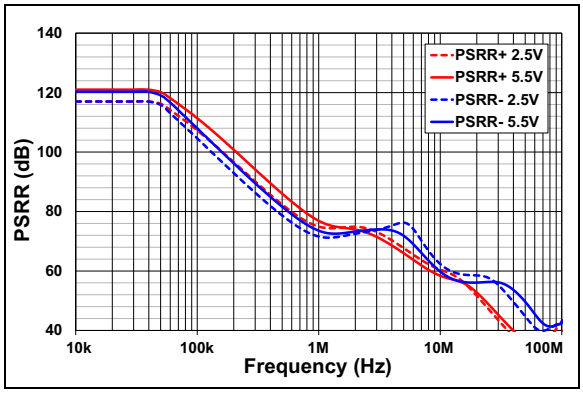

FIGURE 3-15: *+PSRR, -PSRR vs. Frequency, (Simulation).*

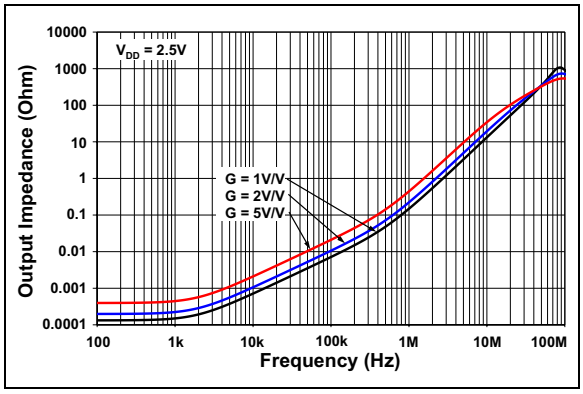

FIGURE 3-18: *Closed-Loop, Differential Output Impedance vs. Frequency (Simulation).*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} - V_{SS} = 2.5V to 5.5V, V_{OCM} = open, V_{ICM} = mid-supply, PD\ = V_{DD}, single-ended input, 50Ω input match, G = 1V/V, R_F = R_G = 1 kΩ, C_L = 0 pF and R_L = 1 kΩ between the differential outputs.

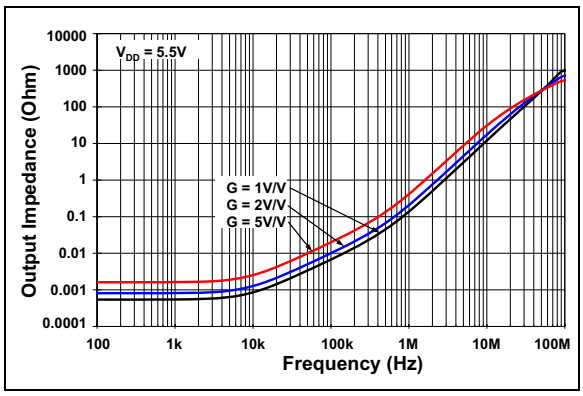

FIGURE 3-19: *Closed-Loop, Differential Output Impedance vs. Frequency (Simulation).*

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Note: Unless otherwise indicated, T_A = 25°C, V_{DD} - V_{SS} = 2.5V to 5.5V, V_{OCM} = open, V_{ICM} = mid-supply, PD\ = V_{DD}, single-ended input, 50Ω input match, G = 1V/V, R_F = R_G = 1 kΩ, C_L = 0 pF and R_L = 1 kΩ between the differential outputs.

3.2 Input Noise and Distortion

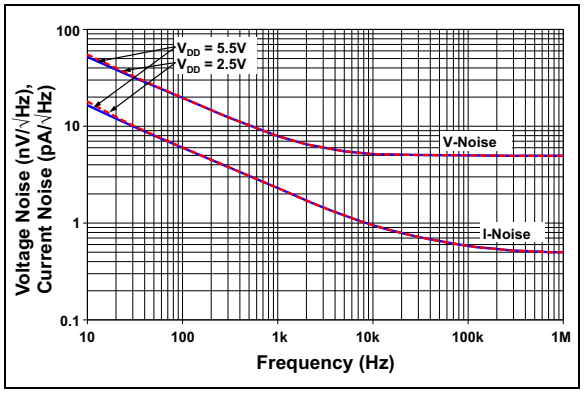

FIGURE 3-20: *Input Noise Voltage and Current Density vs. Frequency.*

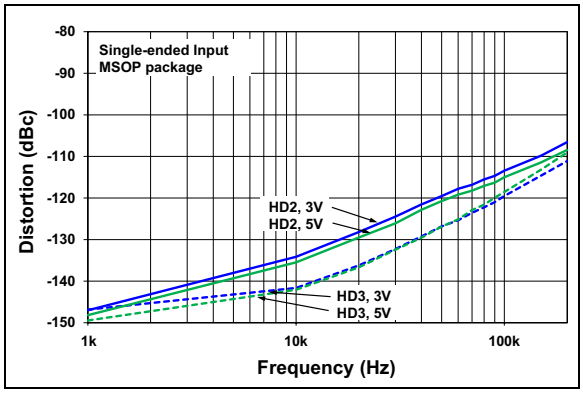

FIGURE 3-23: *HD2 and HD3 vs. Frequency, V_{OUTDM} = 2Vpp.*

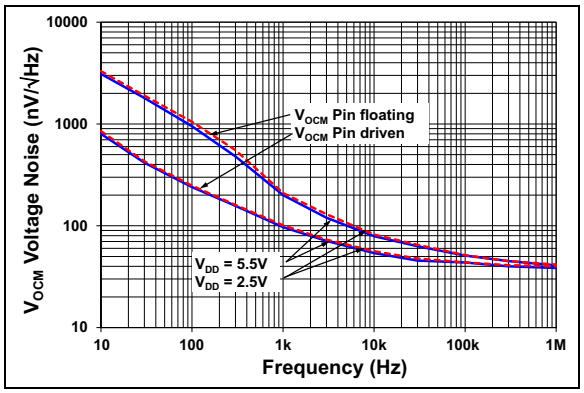

FIGURE 3-21: *V_{OCM} Noise Voltage Density vs. Frequency,; a) Pin Floating, b) Pin Driven.*

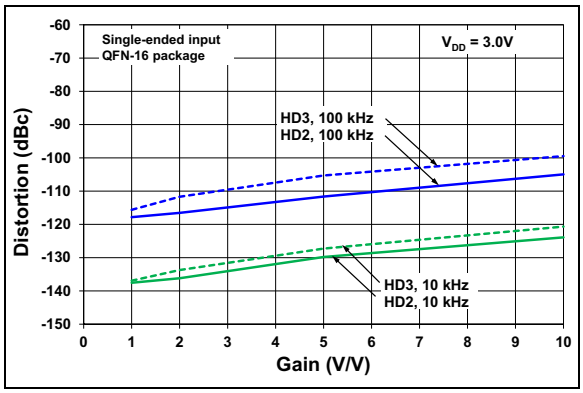

FIGURE 3-24: *HD2, HD3 vs Gain, V_{OUTDM} = 2Vpp.*

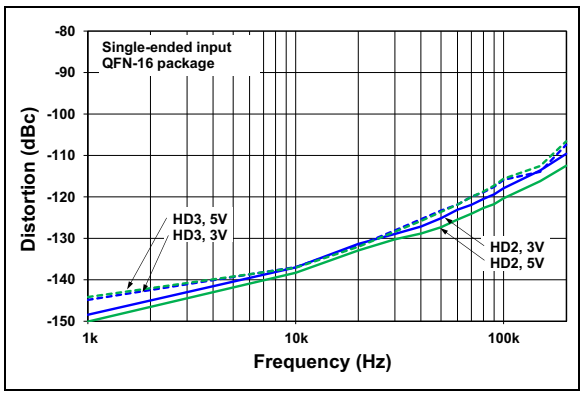

FIGURE 3-22: *HD2, HD3 vs Frequency, V_{OUTDM} = 2Vpp.*

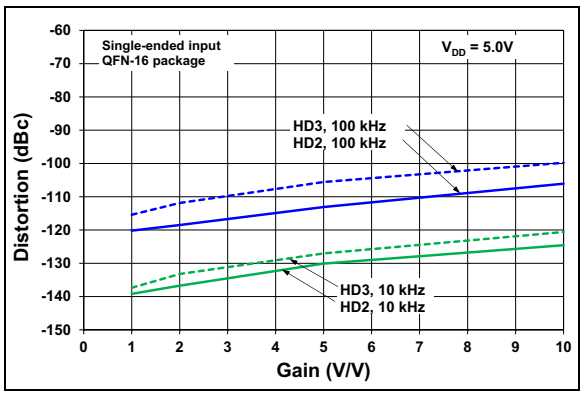

FIGURE 3-25: *HD2, HD3 vs Gain, V_{OUTDM} = 2Vpp.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} - V_{SS} = 2.5V to 5.5V, V_{OCM} = open, V_{ICM} = mid-supply, PD\ = V_{DD}, single-ended input, 50Ω input match, G = 1V/V, R_F = R_G = 1 kΩ, C_L = 0 pF and R_L = 1 kΩ between the differential outputs.

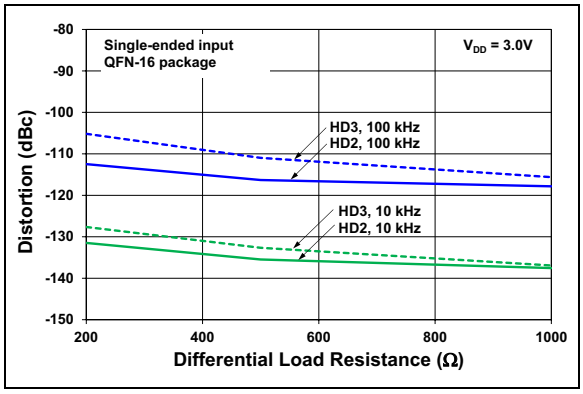

FIGURE 3-26: *HD2, HD3 vs R_L, V_{OUTDM} = 2Vpp.*

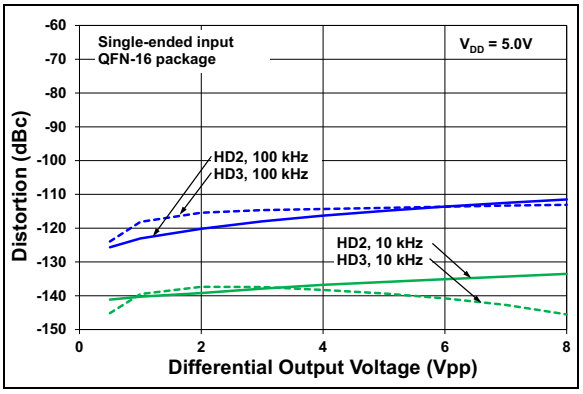

FIGURE 3-29: *HD2, HD3 vs V_{OUTDM}, G = 1V/V.*

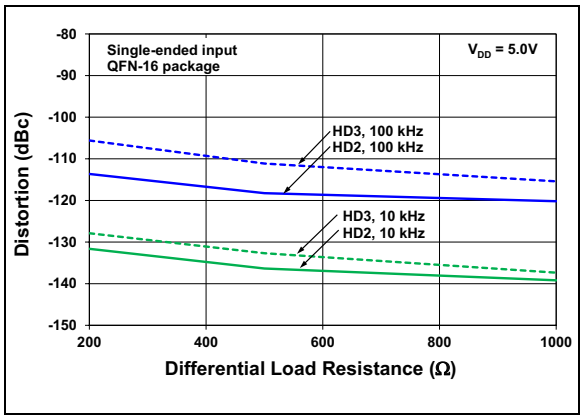

FIGURE 3-27: *HD2, HD3 vs R_L, V_{OUTDM} = 2Vpp.*

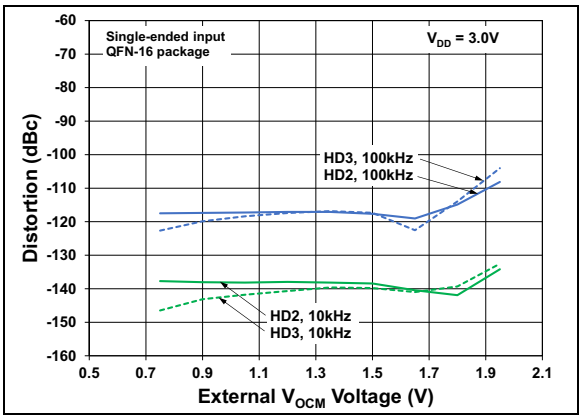

FIGURE 3-30: *HD2, HD3 vs V_{OCM}, V_{OUTDM} = 2Vpp, Gain = 1V/V.*

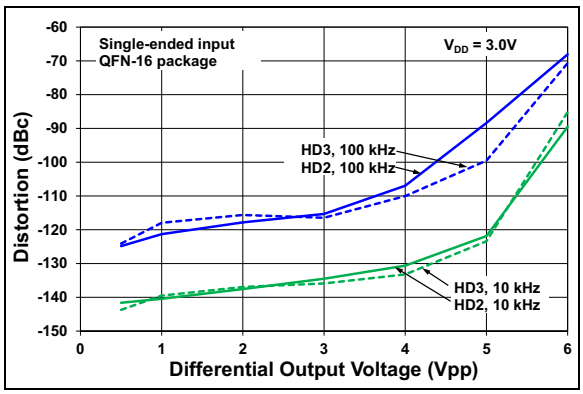

FIGURE 3-28: *HD2, HD3 vs V_{OUTDM}, G = 1V/V.*

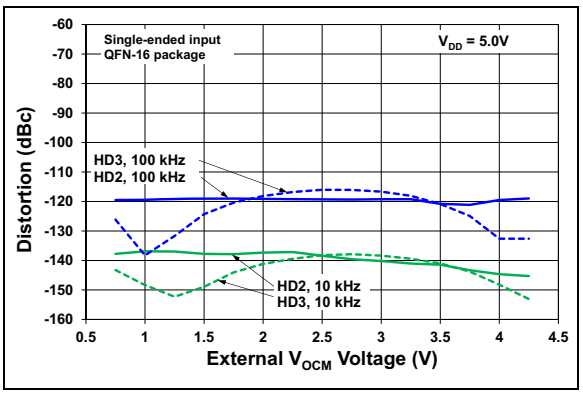

FIGURE 3-31: *HD2, HD3 vs V_{OCM}, V_{OUTDM} = 2Vpp, Gain = 1V/V.*

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Note: Unless otherwise indicated, T_A = 25°C, V_{DD} - V_{SS} = 2.5V to 5.5V, V_{OCM} = open, V_{ICM} = mid-supply, PD\ = V_{DD}, single-ended input, 50Ω input match, G = 1V/V, R_F = R_G = 1 kΩ, C_L = 0 pF and R_L = 1 kΩ between the differential outputs.

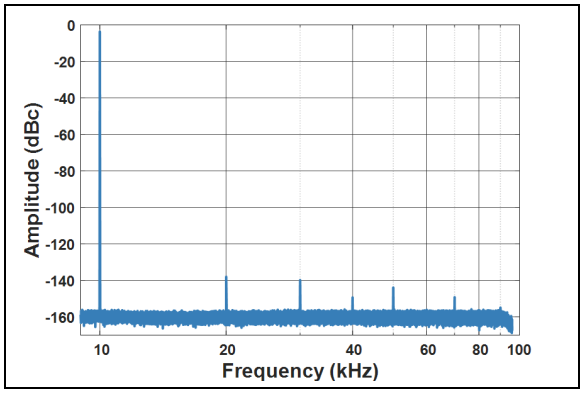

FIGURE 3-32: *10 kHz FFT, V_{OUTDM} = 2Vpp, G = 1V/V, V_{DD} = 3V.*

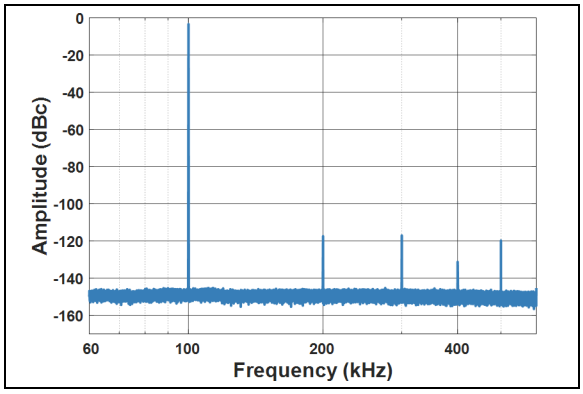

FIGURE 3-34: *100 kHz FFT, V_{OUTDM} = 2Vpp, G = 1V/V, V_{DD} = 3V.*

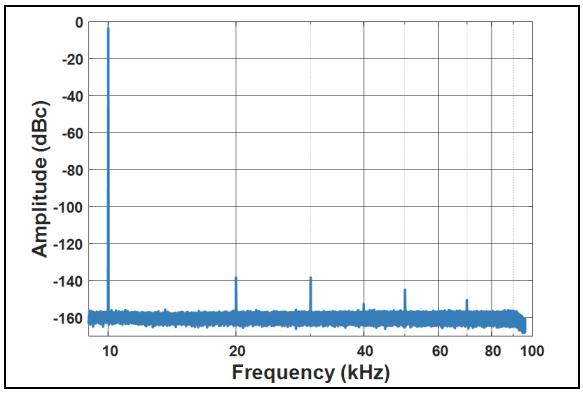

FIGURE 3-33: *10 kHz FFT, V_{OUTDM} = 2Vpp, G = 1V/V, V_{DD} = 5V.*

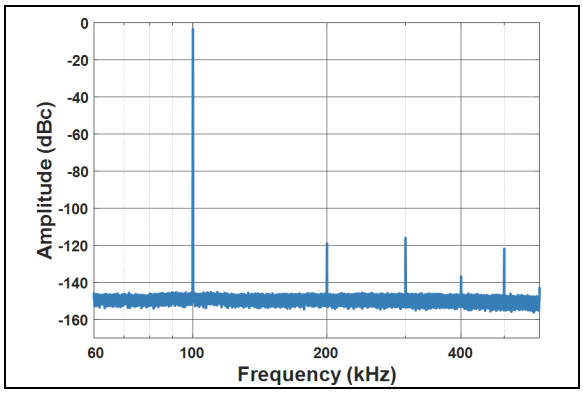

FIGURE 3-35: *100 kHz FFT, V_{OUTDM} = 2Vpp, G = 1V/V, V_{DD} = 5V.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} - V_{SS} = 2.5V to 5.5V, V_{OCM} = open, V_{ICM} = mid-supply, PD\ = V_{DD}, single-ended input, 50Ω input match, G = 1V/V, R_F = R_G = 1 kΩ, C_L = 0 pF and R_L = 1 kΩ between the differential outputs.

3.3 Time Response

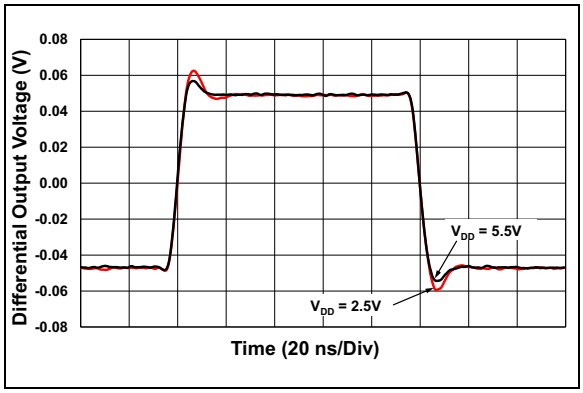

FIGURE 3-36: *Small Signal Step Response, V_{OUTDM} = 100mVpp, G = 1V/V.*

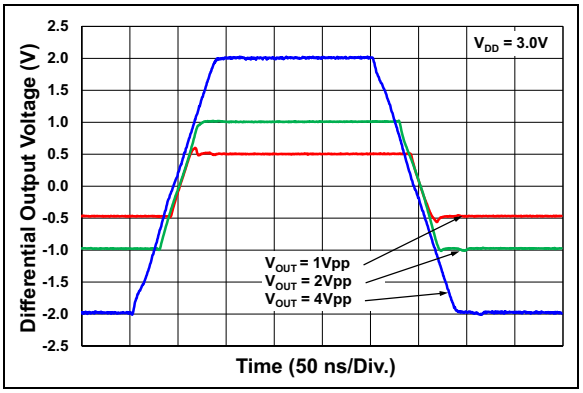

FIGURE 3-39: *Large Signal Step Response, G = 1V/V.*

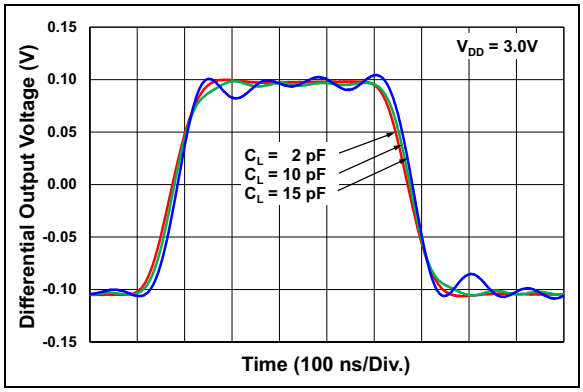

FIGURE 3-37: *Small Signal Step Response vs. C-Load, V_{OUTDM} = 200mVpp, G = 1V/V.*

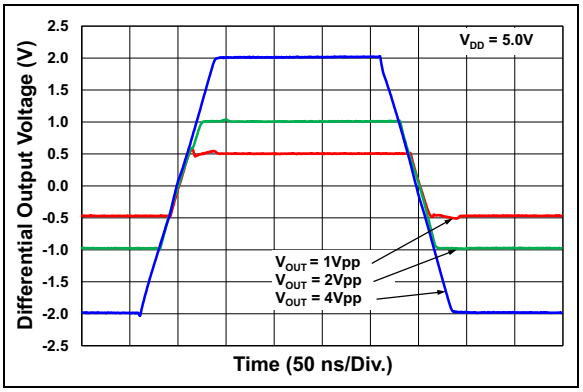

FIGURE 3-40: *Large Signal Step Response, G = 1V/V.*

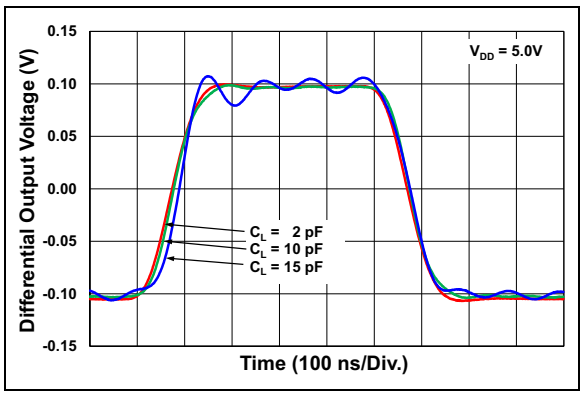

FIGURE 3-38: *Small Signal Step Response vs. C-Load, V_{OUTDM} = 200mVpp, G = 1V/V.*

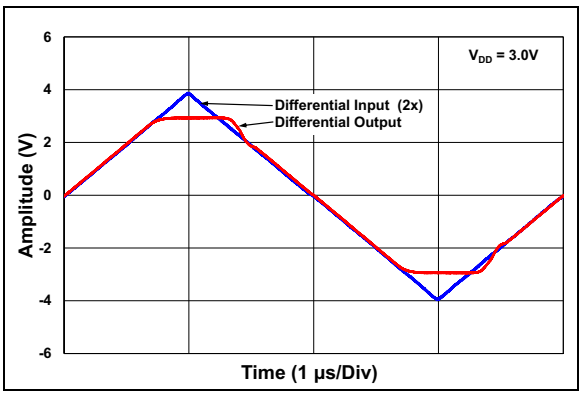

FIGURE 3-41: *Output Overdrive Recovery vs. Time, G = 2V/V.*

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Note: Unless otherwise indicated, T_A = 25°C, V_{DD} - V_{SS} = 2.5V to 5.5V, V_{OCM} = open, V_{ICM} = mid-supply, PD\ = V_{DD}, single-ended input, 50Ω input match, G = 1V/V, R_F = R_G = 1 kΩ, C_L = 0 pF and R_L = 1 kΩ between the differential outputs.

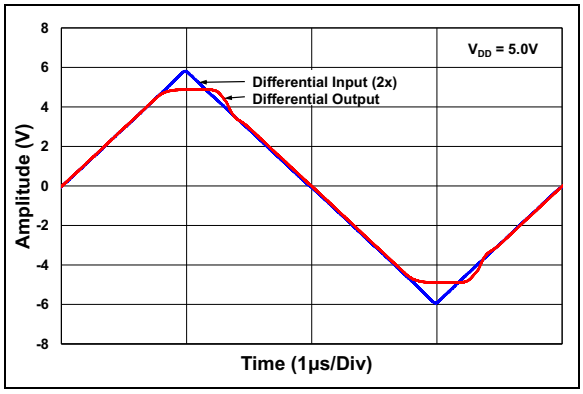

FIGURE 3-42: *Output Overdrive Recovery vs. Time, G = 2V/V.*

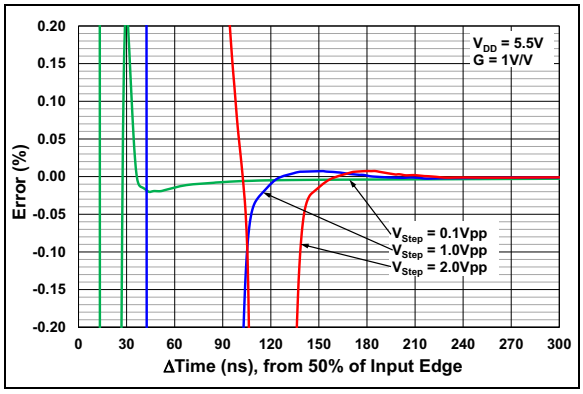

FIGURE 3-45: *Settling Time vs V_{OUTDM} (Simulation).*

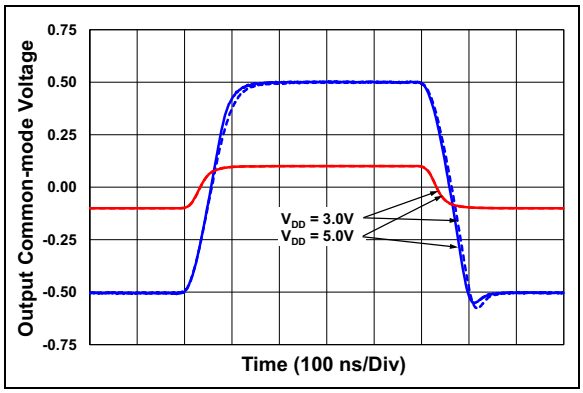

FIGURE 3-43: *V_{OCM} Small- (0.2V Step) and Large (1V step) Signal Step Response.*

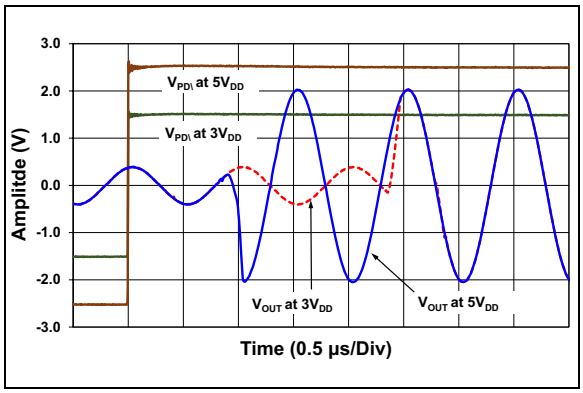

FIGURE 3-46: *PD\ Turn-On Transient Response, Input Signal: 1 MHz Sine, 2Vpp.*

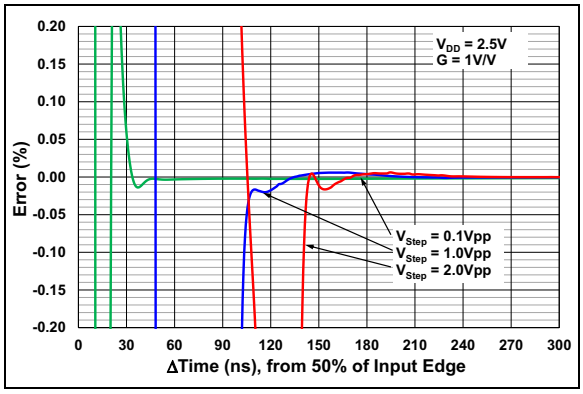

FIGURE 3-44: *Settling Time vs. V_{OUTDM} (Simulation).*

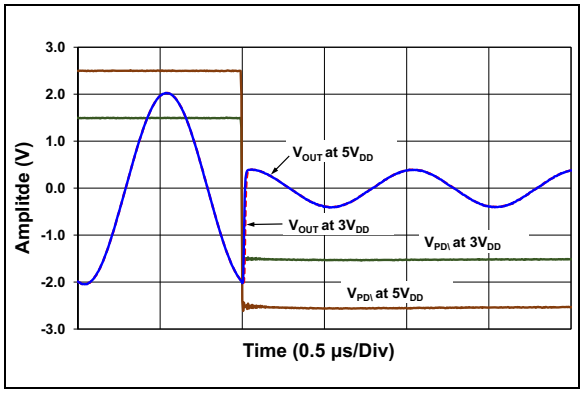

FIGURE 3-47: *PD\ Turn-Off Transient Response, Input Signal: 1 MHz Sine, 2Vpp.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} - V_{SS} = 2.5V to 5.5V, V_{OCM} = open, V_{ICM} = mid-supply, PD\ = V_{DD}, single-ended input, 50Ω input match, G = 1V/V, R_F = R_G = 1 kΩ, C_L = 0 pF and R_L = 1 kΩ between the differential outputs.

3.4 DC Precision

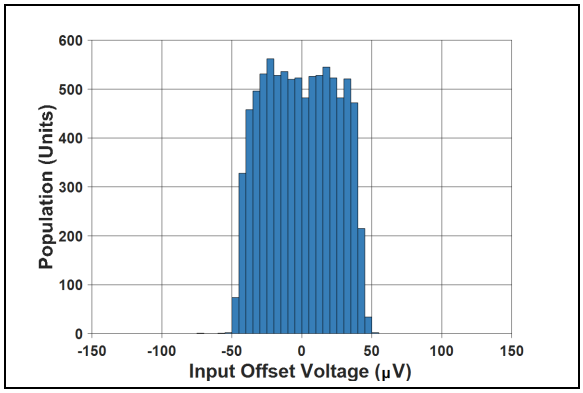

FIGURE 3-48: *Input Offset Voltage Histogram (Factory Trimmed), V_{DD} = 2.5V.*

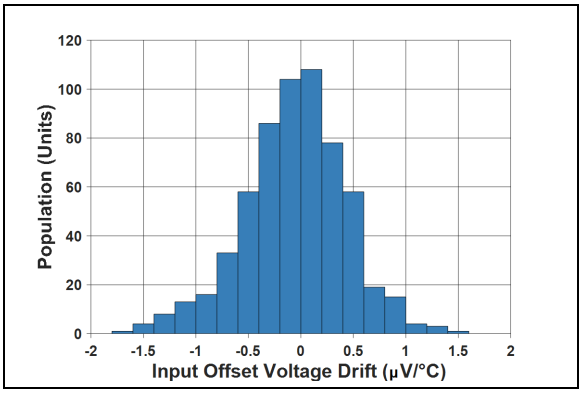

FIGURE 3-51: *Input Offset Voltage Drift Histogram, V_{DD} = 5.5V.*

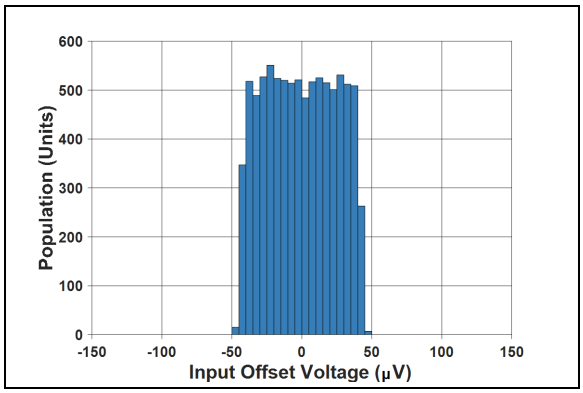

FIGURE 3-49: *Input Offset Voltage Histogram (Factory Trimmed), VDD = 5.5V.*

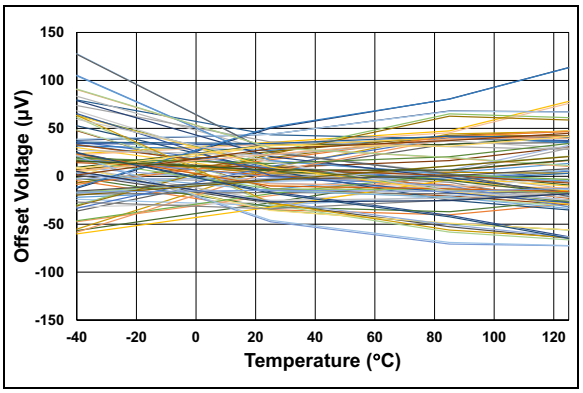

FIGURE 3-52: *Input Offset Voltage vs Temperature (45 Units), V_{DD} = 2.5V and 5.5V.*

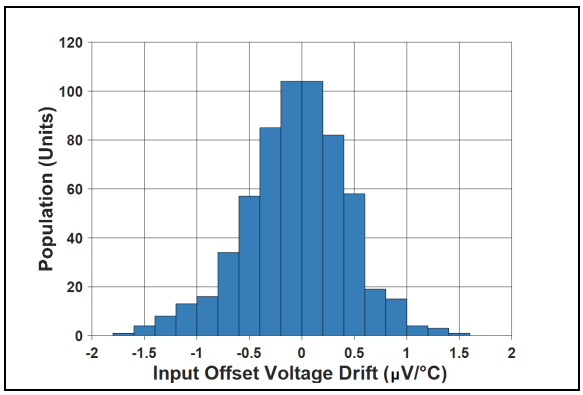

FIGURE 3-50: *Input Offset Voltage Drift histogram; V_{DD} = 2.5V.*

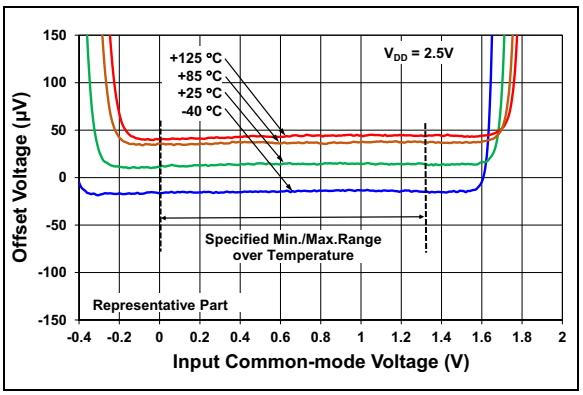

FIGURE 3-53: *Input Offset Voltage vs. Input Common-Mode Voltage.*

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Note: Unless otherwise indicated, T_A = 25°C, V_{DD} - V_{SS} = 2.5V to 5.5V, V_{OCM} = open, V_{ICM} = mid-supply, PD\ = V_{DD}, single-ended input, 50Ω input match, G = 1V/V, R_F = R_G = 1 kΩ, C_L = 0 pF and R_L = 1 kΩ between the differential outputs.

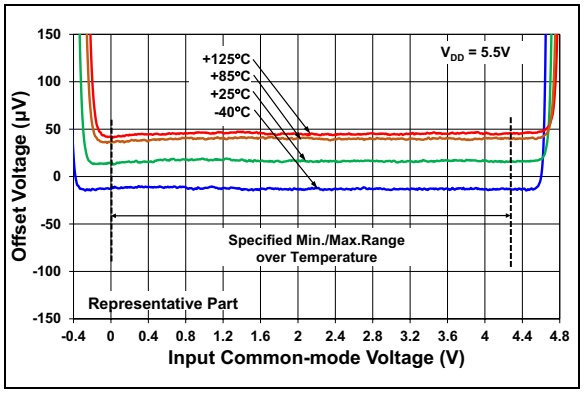

FIGURE 3-54: *Input Offset Voltage vs. Input Common-Mode Voltage.*

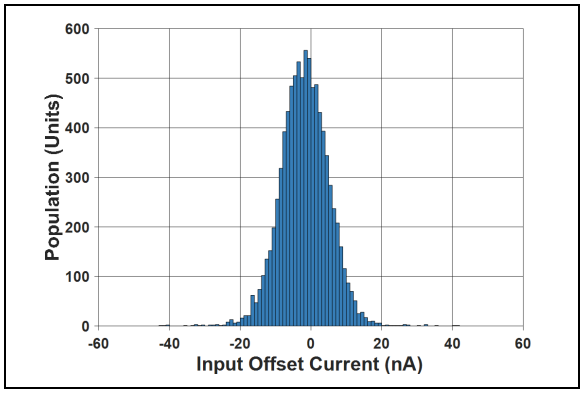

FIGURE 3-57: *Input Offset Current Histogram, V_{DD} = 2.5V.*

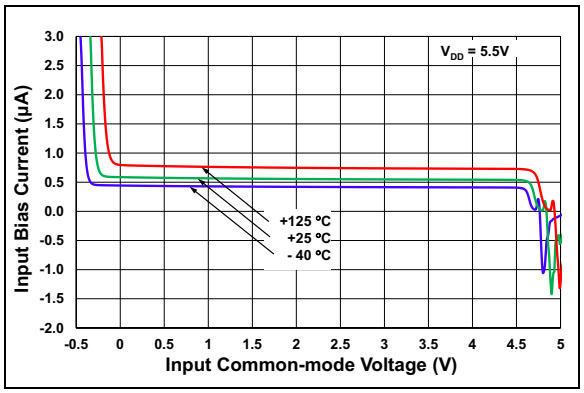

FIGURE 3-55: *Input Bias Current vs. Input Common-Mode Voltage.*

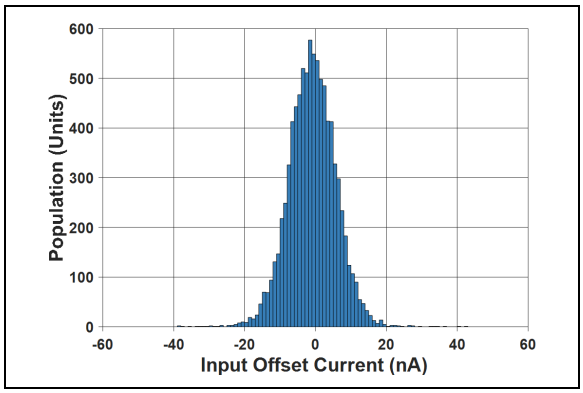

FIGURE 3-58: *Input Offset Current Histogram, V_{DD} = 5.5V.*

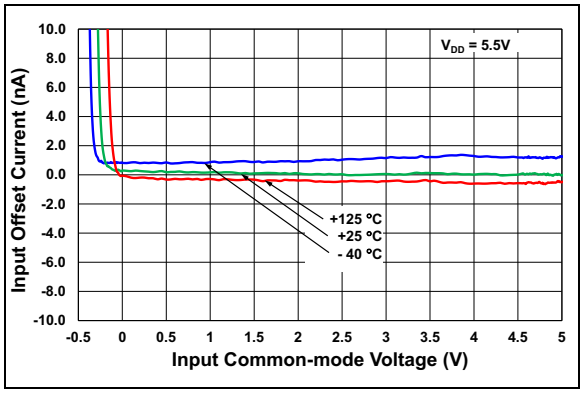

FIGURE 3-56: *Input Offset Current vs. Input Common-mode Voltage.*

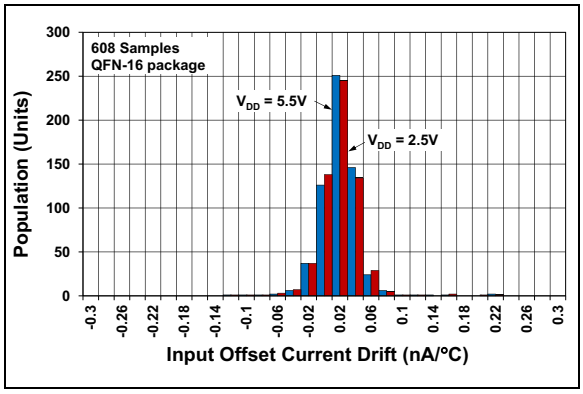

FIGURE 3-59: *Input Offset Current Drift Histogram.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} - V_{SS} = 2.5V to 5.5V, V_{OCM} = open, V_{ICM} = mid-supply, PD\ = V_{DD}, single-ended input, 50Ω input match, G = 1V/V, R_F = R_G = 1 kΩ, C_L = 0 pF and R_L = 1 kΩ between the differential outputs.

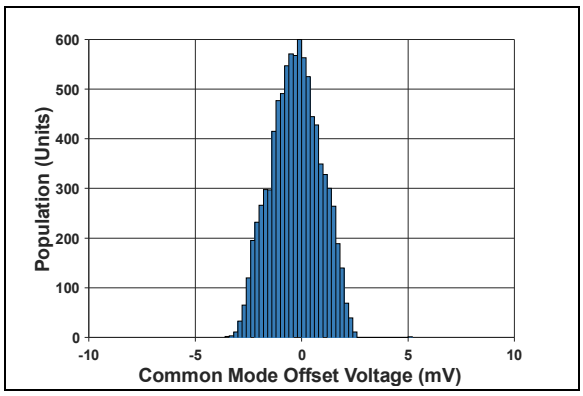

FIGURE 3-60: *V_{OCM} Offset Voltage Histogram, V_{OCM} Pin Floating, V_{DD} = 2.5V.*

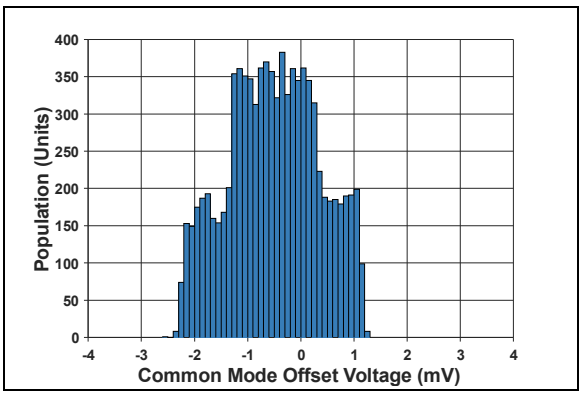

FIGURE 3-62: *V_{OCM} Offset Voltage Histogram, V_{OCM} Pin Driven to Mid-Supply, V_{DD} = 2.5V.*

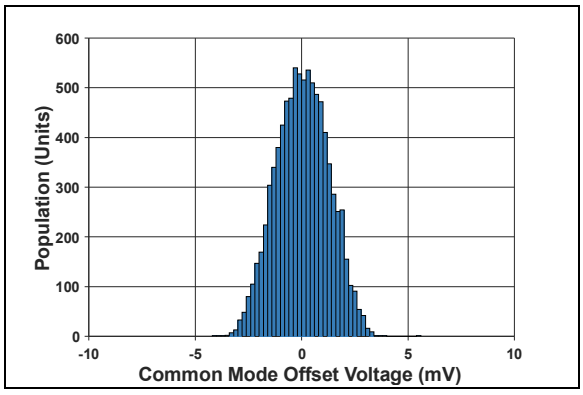

FIGURE 3-61: *V_{OCM} Offset Voltage Histogram, V_{OCM} Pin Floating, V_{DD} = 5.5V.*

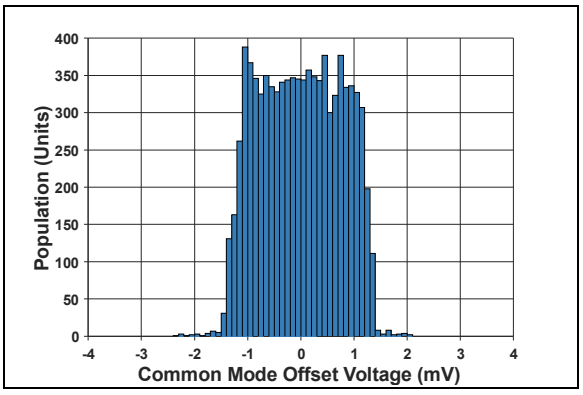

FIGURE 3-63: *V_{OCM} Offset Voltage Histogram, V_{OCM} Pin Driven to Mid-Supply, V_{DD} = 5.5V.*

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Note: Unless otherwise indicated, T_A = 25°C, V_{DD} - V_{SS} = 2.5V to 5.5V, V_{OCM} = open, V_{ICM} = mid-supply, PD\ = V_{DD}, single-ended input, 50Ω input match, G = 1V/V, R_F = R_G = 1 kΩ, C_L = 0 pF and R_L = 1 kΩ between the differential outputs.

3.5 Other DC Voltages and Currents

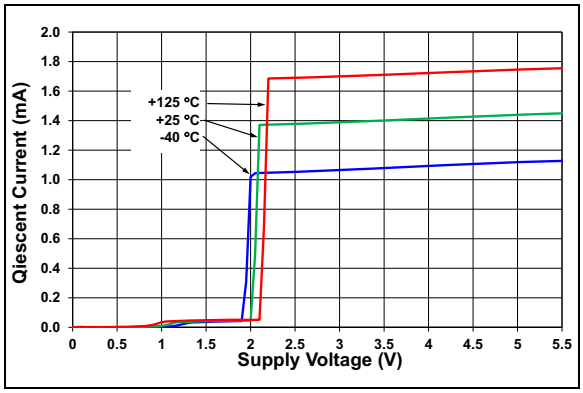

FIGURE 3-64: *Supply Current vs. Power Supply Voltage.*

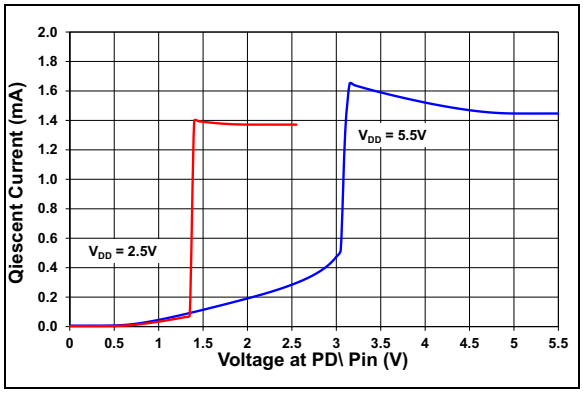

FIGURE 3-66: *Supply Current vs. PD\ Voltage.*

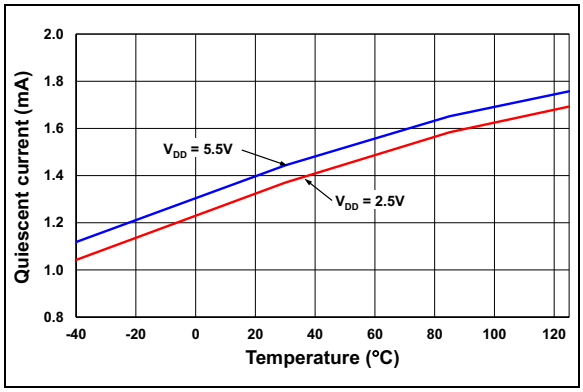

FIGURE 3-65: *Supply Current vs. Temperature.*

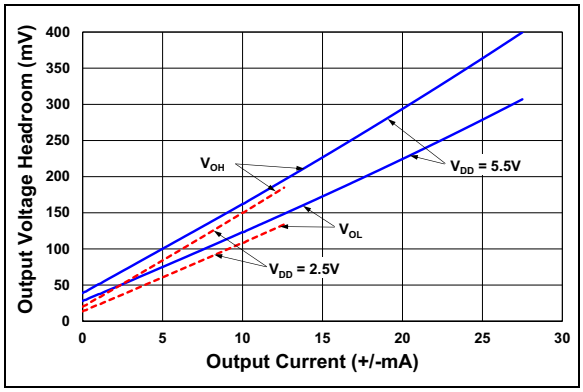

FIGURE 3-67: *Output Voltage Headroom vs. Output Current.*

NOTES:

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4.0 FUNCTIONAL DESCRIPTION

4.1 Overview

Differential Input/Output amplifiers, also called Fully Differential Amplifiers (FDA), have become common driver amplifier for Precision ADCs (SAR, Delta-Sigma) as well as High-Speed ADCs. Compared to more discrete driver circuits built from standard op amps, integrated Differential I/O amplifiers have a number of advantages:

- They allow the signal path to be DC coupled. Other, passive solutions may rely on RF-transformers that are noiseless, but effectively have a band-pass frequency response. Simple AC-coupling creates a high-pass response.
- They provide superior common-mode rejection performance.
- The input and output common-mode operating points are largely independent of the signal gain setting.
- They suppress even-order harmonic distortion.
- They allow the output common-mode voltage to be set independently of the input common-mode voltage, which provides for design flexibility when interfacing to ADCs requiring a certain Vcm for best dynamic performance.
- They increase the dynamic range by a factor of 2 (6 dB) due to their differential, complementary output signals.
- They allow the gain to be set in a wide range, including attenuation (G < 1V/V).

An integrated, differential I/O amplifier is very similar in architecture to a standard, voltage-feedback operational amplifier, with a few differences. Both types of amplifiers have differential inputs. Differential I/O amplifiers have balanced differential outputs, while a standard operational amplifier's output is single-ended. In a differential I/O amplifier the output common-mode voltage can be controlled independently of the differential output voltage through an additional input, the V_{OCM} pin. The purpose of the V_{OCM} input is to set the output common-mode voltage for the two differential output pins. In a standard operational amplifier with single-ended output, the output common-mode voltage and the signal are the same.

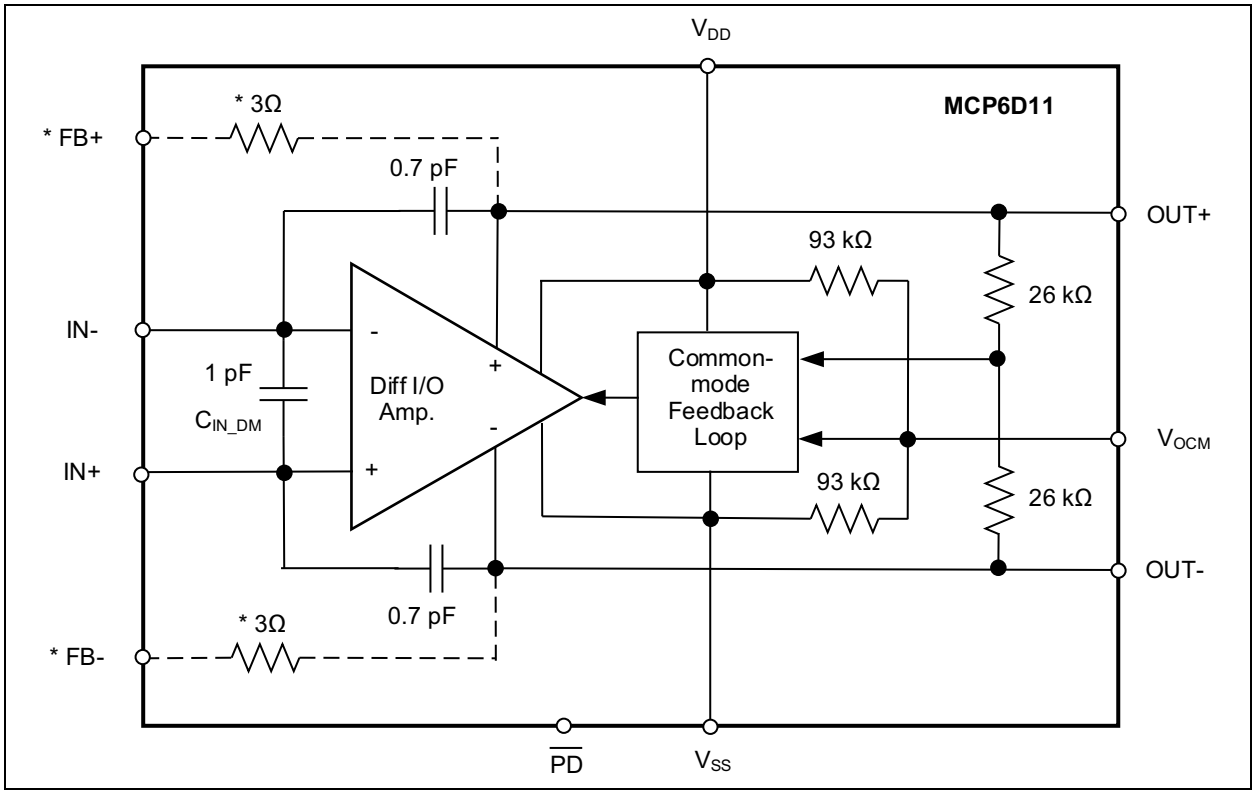

FIGURE 4-1: *MCP6D11 Block Diagram; (*) Internal Metal-Trace Impedances (3Ω) and Pins FB+/- Apply to QFN-16 Package Only.*

The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to arbitrarily set the output common-mode level in level shifting applications. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the V_{OCM} input pin, without affecting the differential output voltage. The result is nearly perfectly balanced differential outputs of identical amplitude and exactly 180° apart in phase over a wide frequency range. The circuit can be used with either a differential or a single-ended input, and the voltage gain is equal to the ratio of R_F to R_G.

As a general rule, differential I/O amplifier circuits will benefit from matched feedback networks (R_F/R_G) to eliminate any common-mode input signal to differential output conversion. However, even if the external feedback networks are mismatched, the internal common-mode feedback loop will still force the outputs to remain balanced. The amplitudes of the signals at each output will remain equal and 180° out of phase. The input-to-output differential-mode gain will vary proportionately to the feedback mismatch, but the output balance will be unaffected. Ratio matching errors in the external resistors will result in a degradation of the circuit's ability to reject input common-mode signals, similar to a four-resistor difference amplifier made from a conventional op amp.

The output common-mode voltage is generated at the mid point of the internal resistor string that is between V_{OUT+} and V_{OUT-}. This voltage is fed into the common-mode feedback loop amplifier and compared to the reference voltage, V_{OCM}.

The V_{OCM} input pin connects to an internal resistor divider (2 x 93 kΩ). If the V_{OCM} pin is left open, a voltage approximately halfway between V_{DD} and V_{SS} will develop due to this internal resistor network. An externally applied voltage at the V_{OCM} pin can be used to overdrive the internal bias voltage if better accuracy or flexibility is desired.

For a standard operational amplifier, there is typically one feedback path from the output to the negative input. The fully differential amplifier operates with two feedback paths as established with the feedback resistors RF, each from one of the outputs to its respective input.

The input stage of the MCP6D11 uses bipolar devices for superior noise performance compared to CMOS devices with the trade-off that the input bias current is higher, typically less than 1 µA. The MCP6D11 has a differential input capacitance of about 1 pF (C_{IN_DM}), which interacts with the feedback resistor, typically 1 kΩ. To optimize the frequency response two internal 0.7 pF feedback capacitors were added to the design as a default compensation.

The MCP6D11 uses a proportional to absolute temperature (PTAT) biasing circuit, which is designed such that the device's quiescent current (I_Q) increases with an increase in temperature (see Figure 3-65).

4.2 Terminology and Definitions

The basic representation of a differential I/O amplifier with its two feedback networks, output load and with its associated voltage nodes is shown in Figure 4-2. The differential signal source is represented showing the signal as V_{IN-} and V_{IN+}, which combine to form the differential input signal V_{IN_DM}. An associated common-mode signal is given as V_{ICM}. Being an ideal source, the source impedance is zero and therefore not shown.

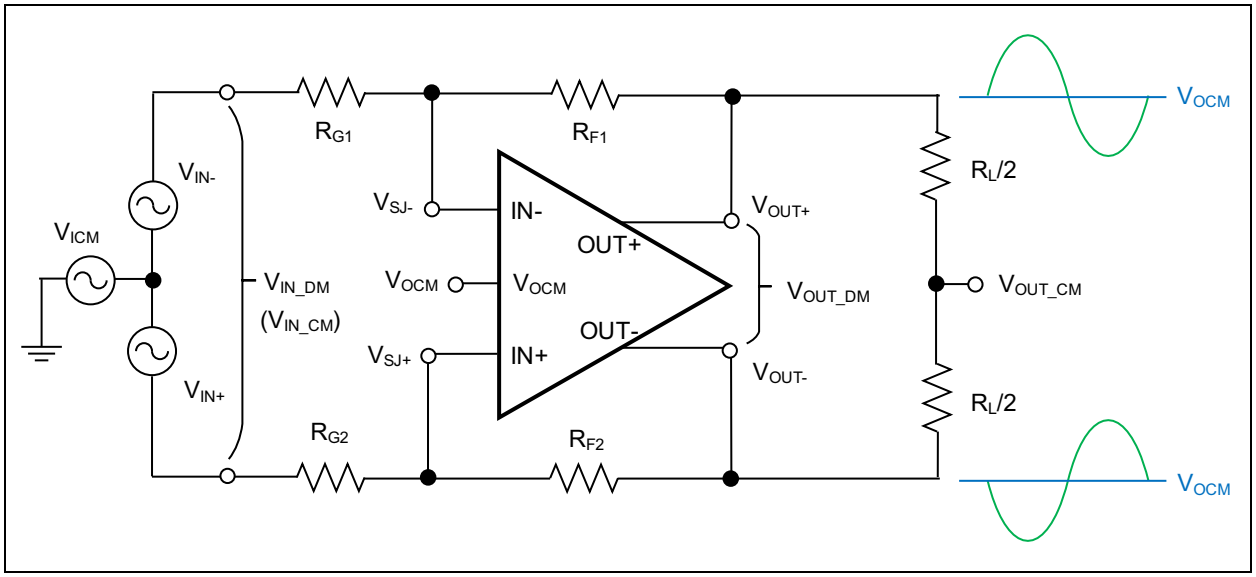

FIGURE 4-2: *Differential I/O Amplifier (Basic Representation).*

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As described earlier, the voltage on the V_{OCM} pin sets up the DC output common-mode voltage, and the AC signal will swing around this V_{OCM} voltage, as illustrated in Figure 4-2. The internal common-mode feedback loop forces the V_{OUT+} and V_{OUT-} outputs to be balanced, i.e. the signals at the two outputs are equal in amplitude but 180° out of phase.

4.2.1 DIFFERENTIAL I/O VOLTAGES

The differential input voltage is the voltage applied between the V_{IN+} and V_{IN-} inputs and the differential output voltage is the voltage seen across the OUT+ and OUT- pins. Equations for input and output differential voltages are listed below:

EQUATION 4-1:

$$V_{IN\_DM} = (V_{IN+} - V_{IN-})$$

EQUATION 4-2:

$$V_{OUT\_DM} = (V_{OUT+} - V_{OUT-}) \approx V_{IN\_DM} \times \frac{R_F}{R_G}$$

Aside from describing the source-related input voltages, it is important to also consider the amplifier's summing junction input voltages, V_{SJ-} and V_{SJ+}. Note that these depend on both the input voltage and the output voltage, as shown in Equations 4-3 and 4-4:

EQUATION 4-3:

$$V_{SJ+} = V_{IN+} \times \frac{R_{F2}}{R_{F2} + R_{G2}} + V_{OUT-} \times \frac{R_{G2}}{R_{F2} + R_{G2}}$$

EQUATION 4-4:

$$V_{SJ-} = V_{IN-} \times \frac{R_{F1}}{R_{F1} + R_{G1}} + V_{OUT+} \times \frac{R_{G1}}{R_{F1} + R_{G1}}$$

4.2.2 SIGNAL GAIN, NOISE GAIN

While more complex, any circuit analysis of differential I/O amplifiers follows essentially the same rules as standard op-amp analysis. One of the important elements of an analysis is to identify the feedback factor (beta, β); in the case of the differential I/O amplifier there are two: β_1 and β_2. Equations 4-5 and 4-6 show the expressions for each of the feedback factors based on the circuit configuration of Figure 4-2.

EQUATION 4-5:

$$\beta_1 = \frac{R_{G1}}{R_{G1} + R_{F1}}$$

EQUATION 4-6:

$$\beta_2 = \frac{R_{G2}}{R_{G2} + R_{F2}}$$

Note that any source impedance present in an actual circuit will add a resistor term in series to the R_G values. Here, R_G represents the total DC impedance seen by the respective amplifier input (IN+, IN-) back to the source or a DC reference (e.g. ground).

These feedback divider ratios will become useful for any output referred noise or error calculation and will be helpful in simplifying the algebra. Most circuit designs for differential I/O amplifiers, for example A/D converter drivers, will require matched feedback factors, $\beta_1 = \beta_2$, to maintain optimum AC and DC performance (see **Section 5.1.3 "Mismatches and DC Errors"**).

Other beta related terms that can be useful for error calculations are β_{AVG} and $\Delta\beta$, with β_{AVG} being defined as the average feedback factor and $\Delta\beta$ defined as the difference in the feedback factors; see Equations 4-7 and 4-8:

EQUATION 4-7:

$$\beta_{AVG} = \frac{\beta_1 + \beta_2}{2}$$

EQUATION 4-8:

$$\Delta\beta = \beta_1 - \beta_2$$

The differential-mode signal gain of the differential I/O amplifier is given in Equation 4-9, which includes the finite frequency dependent open-loop gain of the amplifier $A_{(S)}$ and the average feedback factor.

EQUATION 4-9:

$$Gain(G) = \frac{V_{OUT\_DM}}{V_{IN\_DM}} = \frac{R_F}{R_G} \times \left(\frac{1}{1 + \frac{1}{A_{(S)}\beta_{AVG}}} \right)$$

Recall that $A_{(S)} \times \beta$ is the loop gain of a single-ended amplifier; for the differential I/O amplifier the loop gain is based on β_{AVG}. Setting the open loop gain to infinite ($A_{(S)} \rightarrow \infty$) simplifies the equation, resulting in the expression for the ideal closed loop gain of the differential I/O amplifier. Equation 4-10 is used to select the feedback network resistors R_F and R_G and set the closed loop gain of the amplifier circuit for the differential input and output signal configuration. In the case of the single-ended input to differential output configuration, the equation becomes more complex as additional terms need to be considered; **Section 5.1.2 "Interfacing to a Single-Ended Source"**.

EQUATION 4-10:

$$G = \frac{V_{OUT\_DM}}{V_{IN\_DM}} = \frac{R_F}{R_G}$$

While the signal gain of a differential I/O amplifier is determined by $G = R_F/R_G$, the noise gain (G_N) is given to:

EQUATION 4-11:

$$G_N = \frac{2}{\beta_1 + \beta_2}$$

Where:

$$\beta_1 = \beta_2 \rightarrow G_N = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$$

This is important to remember as the noise gain needs to be considered when calculating total errors, like offsets or noise, that need to be referred to the output. Source impedance plays a factor and needs to be considered for maintaining matching between the two sides ($\beta_1 = \beta_2$).

4.2.3 INPUT AND OUTPUT COMMON-MODE VOLTAGES

The input common-mode voltage (V_{IN_CM}) for the differential I/O amplifier is defined as the average voltage of the two input pins IN+ and IN-.

EQUATION 4-12:

$$V_{IN\_CM} = \frac{V_{IN+} + V_{IN-}}{2}$$

The input common-mode voltage of the MCP6D11 typically ranges from $V_{CM\_L} = V_{SS} - 0.25V$ to $V_{CM\_H} = V_{DD} - 0.9V$. Because of the external resistive divider formed by the feedback and gain resistors, the effective V_{IN_CM} range is wider than the specified range. The input common-mode range of the amplifier depends on the Gain (G), the V_{OCM} voltage, any externally applied common-mode voltage (V_{ICM}) and the circuit configuration.

For fully differential input configurations, where $V_{IN+} = -V_{IN-}$, the common-mode input voltage can be estimated using Equation 4-13:

EQUATION 4-13:

$$V_{IN\_CM} \approx V_{OCM} \times \frac{R_G}{R_F + R_G} + V_{ICM} \times \frac{R_F}{R_F + R_G}$$

For single-ended input configurations there will be an additional input signal component (either on V_{IN+} or V_{IN-}, depending on how the source is connected) to the input common-mode voltage, as there is no out-of-phase signal applied to the other input. Applying the signal to V_{IN+} (connecting V_{IN-} to ground), the common-mode input voltage can be approximated using Equation 4-14:

EQUATION 4-14:

$$V_{IN\_CM} \approx V_{OCM} \times \frac{R_G}{R_F + R_G} + \left(V_{ICM} + \frac{V_{IN+}}{2} \right) \times \frac{R_F}{R_F + R_G}$$

Note: Here the input voltage V_{IN+} is equal to the peak input signal, $V_{IN\_P} = V_{IN\_PP}/2$. The result yields the upper value for the input common-mode voltage. To estimate the lower value use the negative term: $-V_{IN+}$ in Equation 4-14.

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The output common-mode voltage (V_{OUT_CM}) for the differential I/O amplifier is defined as the average of the two output voltages V_{OUT+} and V_{OUT-}; see Figure 4-2. The output common-mode voltage V_{OUT_CM} is primarily determined by the voltage at the V_{OCM} pin, but they are not identical due to an offset component, the common-mode offset voltage.

EQUATION 4-15:

$$V_{OUT\_CM} = \frac{(V_{OUT+} + V_{OUT-})}{2} \approx V_{OCM}$$

4.2.4 COMMON-MODE OFFSET VOLTAGE

The common-mode offset voltage (V_{OS_CM}) is defined as the difference between the output common-mode voltage and the V_{OCM} voltage.

EQUATION 4-16:

$$V_{OS\_CM} = (V_{OUT\_CM} - V_{OCM})$$

4.2.5 OUTPUT HEADROOM

Once the V_{OCM} voltage has been defined for a given amplifier configuration, verify that the desired maximum differential output swing (V_{OUT_PP}) falls within the linear output voltage range of the differential I/O amplifier. As listed in the DC Electrical Characteristics table, the MCP6D11 requires a minimum output headroom (V_{OH}, V_{OL}) of 150 mV.

EQUATION 4-17:

$$V_{OUTmax} = V_{OCM} + \frac{V_{OUTpp}}{4}$$

EQUATION 4-18:

$$V_{OUTmin} = V_{OCM} - \frac{V_{OUTpp}}{4}$$

4.2.6 OUTPUT BALANCE

An ideal differential output signal implies the two outputs of the differential amplifier should be exactly equal in amplitude and shifted 180° in phase. Hence, any imbalance in amplitude or phase between the two output signals results in an undesirable common-mode signal on the output. The Output Balance error is the measure of how well the outputs are balanced and is defined as the ratio of the output common-mode voltage (V_{OUT_CM}) to the output differential signal (V_{OUT_DM}). It is generally expressed as dB in logarithmic scale:

EQUATION 4-19:

$$Output\ Balance\ error = 20log\left|\frac{V_{OUT\_CM}}{V_{OUT\_DM}}\right|$$

The function of the internal common-mode feedback loop circuit drives the output common-mode voltage (V_{OUT_CM}) to equal the voltage level present at the V_{OCM} pin. This ensures a very good output balance over a wide bandwidth (see Figure 3-17). Note that this figure is derived from simulation results to show the best-case output balance of the MCP6D11 itself. For this, the resistor tolerance was set to zero. However, at lower frequencies, the dominant contribution to the output balance error comes from the resistor tolerance of the external feedback network ($\beta_1 \neq \beta_2$) as the imbalance creates a common-mode to differential conversion (see **Section 5.1.3 "Mismatches and DC Errors"**). At higher frequencies capacitive and parasitic effects come into play.

4.2.7 STABILITY CONSIDERATIONS

One of the primary applications for differential I/O amplifiers like the MCP6D11 is as a high-bandwidth driver amplifier for Analog-to-Digital converters, as described in **Section 5.3.1 "Driving High Precision ADCs"**. Here, the amplifier's stability is of particular concern as the output of the amplifier not only has to drive a fairly large capacitive load, isolated by only small value resistors, but also has to respond quickly to transient currents resulting from the ADC's sampling effects. In order to analyze the amplifier's stability in a closed-loop configuration, the open-loop gain (A_{OL}) and phase frequency response need to be examined. Figure 4-3 shows the simulated differential input to output open-loop gain and phase of the MCP6D11 under two loading conditions: 1kΩ load and no-load. The no-load condition removes any effect of the open-loop output impedance interacting with any external load element.

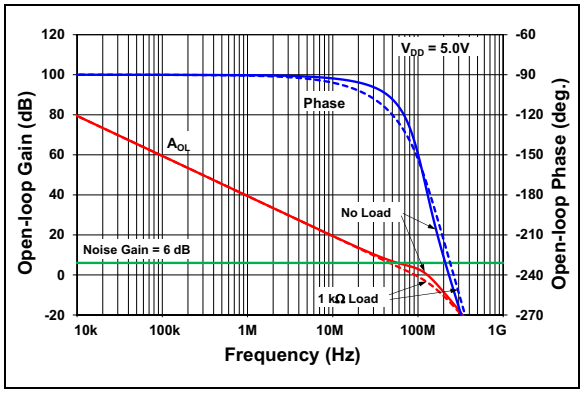

FIGURE 4-3: *Simulated Open-Loop Gain and Phase Response with No-Load and 1 kΩ Load Condition.*

For the simulation to show only the amplifier's forward path signal response, the two internal 0.7 pF feedback capacitors were removed. When operating the actual device, those 0.7 pF integrated capacitors (see Figure 4-3) are part of the feedback network that sets the noise gain and phase in the specific application. This also includes any external feedback capacitors and parasitic elements which can quickly lead to stability problems, effectively a result of insufficient phase margin. In general, the phase margin can be found at the frequency where the noise gain (G_N) and the open-loop gain magnitude intersect; the loop-gain equals unity (0 dB) at this point. The difference between the phase at that point and -180 degrees is defined as the phase margin. Using Figure 4-3 the extracted phase margin is about 63 degrees for the 1 kΩ load condition. Since the MCP6D11 operates as an inverting amplifier the noise gain remains at greater or equal to 1V/V ($G_N = 1 + R_F/R_G$). This allows the user to set the signal gain to a fractional gain ($G = R_F/R_G < 1V/V$), with the amplifier's phase margin at approximately ≥ 30 degrees. The effect of this reduced phase margin for a G = 0.1V/V configuration can be seen from in increased gain peaking shown in Figure 3-1 and Figure 3-2.

Operating the MCP6D11 with a high loop gain will result in the lowest distortion performance. Therefore, most ADC driver applications operate the amplifier at a low signal gain of 1V/V. The loop gain will decrease as A_{OL} decreases with higher frequencies. Equation 4-20 describes the loop gain for the differential I/O amplifier having two feedback factors (as discussed in **Section 4.2.2 "Signal Gain, Noise Gain"**).

EQUATION 4-20:

$$Loop\ Gain = \frac{A_{OL}}{G_N} = A_{OL} \times \beta_{AVG} \quad ,$$

with $$\beta_{AVG} = \frac{\beta_1 + \beta_2}{2}$$

Figure 4-4 shows the simulated differential open-loop output impedance of the MCP6D11. Starting at the lower frequencies, the output impedance of the rail-to-rail output stage is high, then declines with a rate of -20 dB/decade until flattening out in a mid-range frequency section. The high impedance section will be significantly reduced when the amplifier is operated in a closed-loop configuration, as shown in Figure 3-18 and Figure 3-19. At higher frequencies, the open-loop output impedance starts to increase again at a rate of +20 dB/decade, resembling a first-order inductive behavior, indicating that purely capacitive loads can lead to stability issues (see **Section 5.2.4 "Capacitive Loads"**).

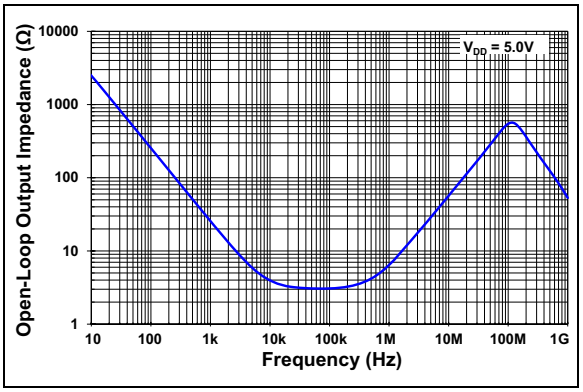

FIGURE 4-4: *Simulated Open-Loop Differential Output Impedance.*

Figure 4-3 shows the effect of the output impedance interacting with the load by comparing the frequency response of the no-load condition to the 1 kΩ load condition. The load causes the A_{OL} curve to have its 0 dB cross-over point at lower frequencies as well as increasing the phase shift.

4.3 Operation

Differential I/O Amplifiers (or Fully Differential Amplifiers) resemble standard operational amplifiers configured in an inverting gain configuration. It should be noted that the polarity signs on the inputs (V_{IN-}, V_{IN+}) and outputs (V_{OUT-}, V_{OUT+}) typically shown on differential I/O amplifiers only indicate their phase relationship, and therefore may be misleading for correctly identifying input impedances. For this, is it useful to consider that both signal inputs on the differential I/O amplifier are in fact summing junctions, indicated by the labels V_{SJ-} and V_{SJ+} shown in Figure 4-5. Because of the closed-loop feedback around the amplifier, these summing junctions represent a virtual ground and the resistors R_{G1} and R_{G2} set the input impedance seen by the source. If the input configuration is for a differential signal, the input impedance analysis is as simple as it is for an inverting op amp circuit, but more difficult in the case the input configuration is for a single-ended signal. Both situations will be discussed later in **Section 5.1**

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"Amplifier Configuration Options". Figure 4-5 shows the typical representation of a differential I/O amplifier with its feedback resistor network, and also showing an equivalent circuit implementation based on standard op amps that illustrates more clearly the inverting amplifier configuration for the differential signal path.

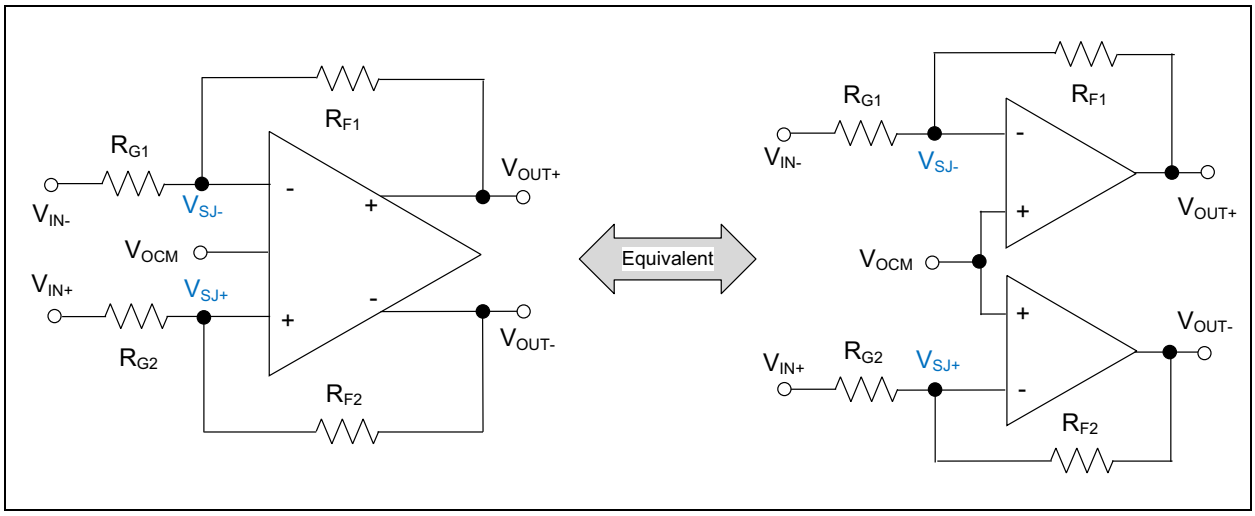

FIGURE 4-5: *Equivalent Basic Circuit Functions.*

Comparing the two equivalent differential circuits of Figure 4-5, the key difference is that in the case of the two inverting operational amplifiers, the common-mode voltage is controlled by the voltage applied to the non-inverting inputs. For the differential I/O amplifier the output common-mode voltage is controlled using an independent feedback loop circuit (see Figure 4-1).

4.3.1 V_{OCM} INPUT

As mentioned earlier (see **Section 4.1 "Overview"**), the internal feedback control-loop drives the output common-mode voltage (V_{OUT_CM}) to be equal to the voltage present at the V_{OCM} pin. When the pin is left open, V_{OCM} defaults approximately to a mid-supply voltage level set by the internal resistor divider (see Figure 4-1).

EQUATION 4-21:

$$V_{OUT\_CM} = \frac{(V_{OUT+} + V_{OUT-})}{2} \approx V_{OCM}$$

The V_{OCM} input can be connected to an external reference voltage and varied within the specified range to accommodate specific output common-mode levels and achieve tighter control and higher accuracy. Refer to Figure 3-30 and Figure 3-31 for the impact on the achievable distortion when setting the V_{OCM} voltage away from mid-supply. In any case, an external decoupling capacitor is recommended to be added on the V_{OCM} pin to reduce the otherwise high output noise for this high impedance node.

4.3.2 INPUT AND ESD PROTECTION

The design of the MCP6D11 includes comprehensive circuitry to protect the device against ESD, overvoltage and reverse-voltage events, as shown in Figure 4-6. The inputs have a primary and secondary ESD protection using diodes connected from each input terminal to the supply rails.

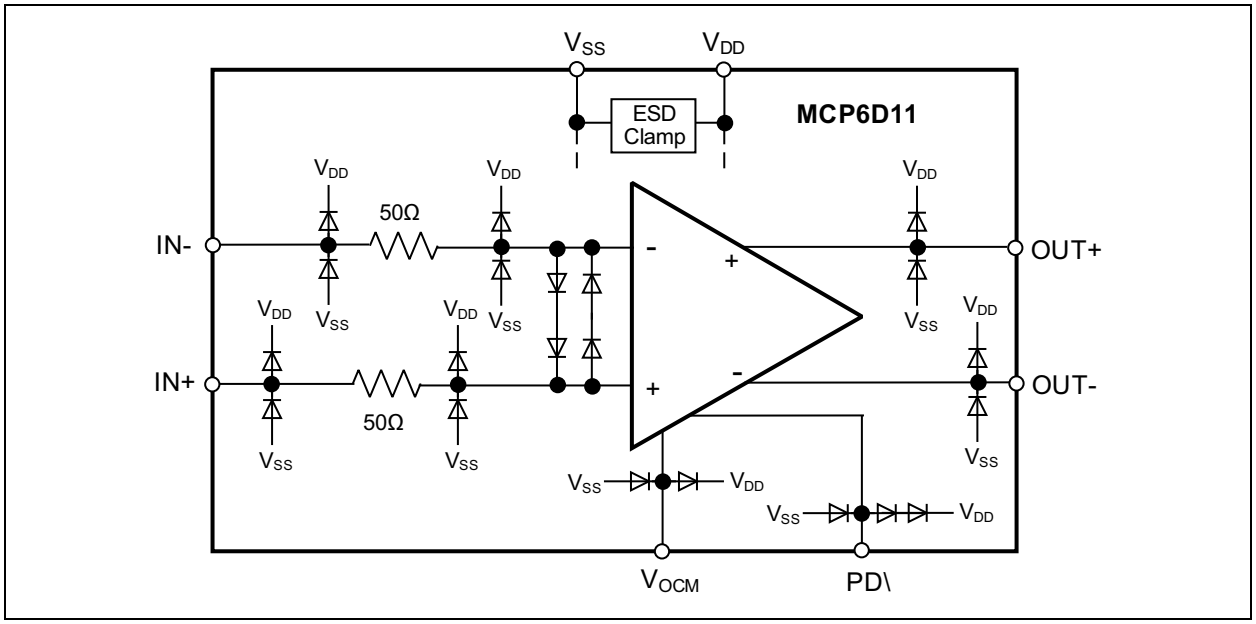

FIGURE 4-6: *ESD and Input Protection Scheme for the MCP6D11.*

The input stage of the MCP6D11 is protected against differential input voltages which exceed approximately 1.4V by two pairs of series diodes connected back-to-back between the differential amplifier inputs. If the differential input voltage exceeds 1.4V, the input current should be limited to 10 mA or less to prevent damage. Moreover, all pins have clamping diodes to both power supplies. If any pin is driven to voltages which exceed either supply, the current should be limited to under 10 mA. Internal protection diodes remain present across the input pins in both the operating and Power-Down mode. Large input signals during power-down can turn on the input differential protection diodes, thus producing a load current in the supply even with the device in Power-Down mode.

The MCP6D11 is protected with an edge-triggered ESD clamp between the supply pins, V_{DD} and V_{SS}. Care should be taken to ensure a power supply turn-on/off edge rate (dV/dt) that does not exceed the rates stated in **Section "Absolute Maximum Ratings †"** to avoid activating this clamp circuit.

4.3.3 POWER-DOWN FUNCTION (PD\)

The design of the MCP6D11 includes a power-down function which will reduce the quiescent current (I_Q) down to about 5 µA (typical). The PD\ pin is referenced to the negative supply (V_{SS}). Therefore, when operating the MCP6D11 with a negative supply voltage ensure that the voltage applied to the PD\ pin can be pulled down to within 0.4V of the negative rail. Similarly, pulling the PD\ high to within 0.4V of the positive rail will ensure normal operation. Applying voltages at intermediate levels to the PD\ pin may result in an increase in quiescent current. When this pin is pulled low ($\approx V_{SS}$) the amplifier is disabled and placed in Power-Down mode. Tying this pin to a high potential ($\approx V_{DD}$) will enable normal operation. There is no internal pull-up or pull-down resistor and the PD\ pin should not be left floating. Note that when disabling the amplifier the signal path is still present for the source signal through the external resistors, which results in relatively poor signal isolation from the input to output in Power-Down mode. The Power-Down circuit of the MCP6D11 offers very fast turn-on and turn-off times, with typically 1 µs for the turn-on time and only 40 ns for the turn-off time (see Figure 3-48 and Figure 3-49).

4.4 Test Circuits

Since most test equipment is specified for a 50Ω impedance, it requires the characterization circuit for the device-under-test (DUT) to include proper input and output termination or impedance matching. In addition, most equipment also has single-ended signal inputs or outputs. The basic characterization circuit therefore has the MCP6D11 configured for a singled-ended input with matched, 50Ω input termination, as shown in Figure 4-7. The amplifier's differential outputs drive the load resistor, which is split in order to facilitate a differential to single-ended signal conversion using a miniature RF-transformer (or Balun) while also providing a

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50Ω output impedance. The 50Ω input impedance from the network analyzer reflects through the transformer to be in parallel with the 52.3Ω resistor.

The total load impedance seen by the differential I/O amplifier is $R_L = 2 \times R_O + (R_{OT} \parallel 50\Omega)$. Due to the voltage divider on the output formed by the load component values, the amplifier's output is attenuated, see column “Attenuation” in Table 4-1. When using a transformer as shown in Figure 4-7, the signal will see a slightly higher attenuation due to the transformer insertion loss. The standard output load used for most tests is 1 kΩ which results in approximately 31.8 dB of loss. This signal loss is normalized out for the typical frequency response curves to show the gain response to the amplifier output pins. Note that the 1:1 RF-transformer acts as a bandpass filter with a usable range from about 100 kHz to 500 MHz for this application.

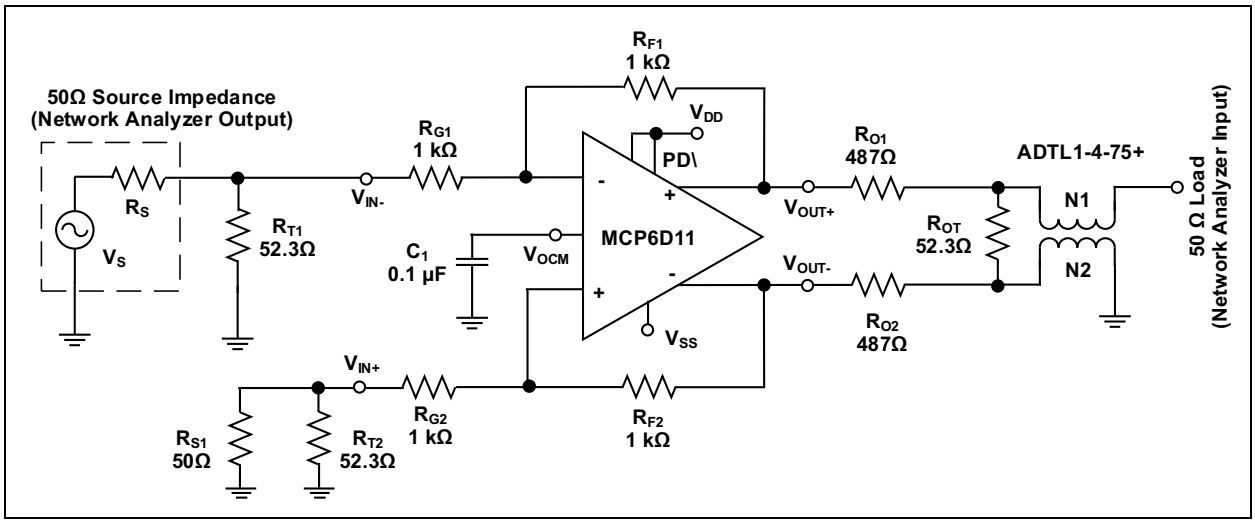

FIGURE 4-7: *Basic Characterization Circuit Configuration for Frequency Domain Tests.*

Furthermore, the components on the non-signal input side match very closely the components on the signal input side. This has the advantage of closely matching the two divider networks on each side of the amplifier. Alternatively, the three resistors on the non-signal input side, R_{G2}, R_{T2}, R_{S2}, can be replaced by a single resistor to ground using a standard E96 value of 1.02 kΩ with some loss in gain balancing between the two sides. For any active channel tests the power-down pin PD\ is tied to the positive supply (V_{DD}).

Most characterization plots are based on a 1 kΩ value for R_F ($R_{F1} = R_{F2}$). While this resistor value can be adapted for a specific application purpose, the 1 kΩ value offers a good compromise with issues related to this resistor value, specifically:

- Output loading: both feedback resistors contribute to the total load seen across the outputs; for example the total differential loads shown in Figure 4-7 is 1 kΩ || 2 kΩ = 667Ω. The 1 kΩ value also reduces the power dissipated in the feedback networks.
- Noise contribution: appears as the ($4kTR_F$) term and the current noise multiplied by the resistor value (see paragraph Noise Analysis).
- Feedback pole at the summing junction inputs: this pole is created by the feedback resistor (R_F) value and the 1.0 pF differential input capacitance, C_{IN_DM}, (plus any PC-board parasitic) and adds a zero in the noise gain, resulting in a reduced phase margin in most cases. The two internal 0.7 pF feedback capacitors (see Figure 4-1) combine with the external feedback resistors to introduce a zero in the noise gain, reducing the effect of the feedback pole.

TABLE 4-1: COMPONENT VALUES FOR DIFFERENTIAL TO SINGLE-ENDED OUTPUT USING A 1:1 TRANSFORMER

R_L	R_{O1}, R_{O2}	R_{OT}	Attenuation
100Ω	25Ω	open	6 dB
200Ω	86.6Ω	69.8Ω	16.8 dB
499Ω	237Ω	56.2Ω	25.5 dB
1 kΩ	487Ω	52.3Ω	31.8 dB
2 kΩ	976Ω	51.1Ω	37.9 dB

4.4.1 DUAL-SUPPLY VERSUS SINGLE SUPPLY CHARACTERIZATION

Although most end-equipment applications use a single-supply implementation, the factory device characterization is typically done using a dual-balanced supply. For example, a 5V test uses a ±2.5V supply and a 3V test uses a ±1.5V supply with the V_{OCM} input pin at ground. Using a dual supply keeps the input and output common-mode voltages near mid-supply with optimal headroom for the output swing and no DC bias currents for level shifting. It also avoids the need for additional DC blocking capacitors that could restrict the signal bandwidth. This setup is used for characterizations such as the frequency response, harmonic distortion, and noise plots. Some of the time domain plots are done with a single supply to obtain the correct movement of the input common-mode voltage.

4.4.2 SIMULATED CHARACTERIZATION CURVES

Some of the characterization data can only be generated through simulation in order to reflect the actual performance of the device without being constrained by hardware and measurement errors. One example of such a case is the output balance plot of Figure 3-17, which shows the best-case output balance by using exact matching on the external resistors for the single-ended input to differential output configuration. As discussed earlier, in practice the output balance is being constrained by the resistor value mismatch primarily at low frequencies but will converge with the high frequency portion of Figure 3-17 due to parasitic effects.

Other Performance Figures that are based on simulations are:

- A_{OL} gain and phase, see Figure 3-16.
- Settling times, see Figure 3-44 and Figure 3-45.
- Closed loop output impedance versus frequency, see Figure 3-18 and Figure 3-19.
- CMRR vs frequency, see Figure 3-14.
- PSRR vs frequency, Figure 3-15.

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5.0 APPLICATION INFORMATION

5.1 Amplifier Configuration Options

When applying Differential I/O amplifiers there are two common configurations: interfacing to a differential source and driving the output differentially, or interfacing to a single-ended source and converting the signal into a differential output. Depending on the nature and impedance of the source, an input impedance match needs to be implemented. Accomplishing the optimum matching will be different for each configuration. As mentioned earlier, operating the differential I/O amplifier in a lab environment often requires configuration for matched 50Ω single-ended inputs and outputs (see **Section 4.4 "Test Circuits"**). However, for many signal chain applications the issue of impedance matching may be neglected as the source has sufficiently low impedance in the bandwidth of interest. But it is generally important to understand the interaction between a source impedance and the gain-setting network of a differential I/O amplifier.

5.1.1 INTERFACING TO A DIFFERENTIAL SOURCE

A differential signal source V_{SDiff}, with its associated output impedances R_{S1} and R_{S2}, is directly connected (dc-coupled) to the differential I/O amplifier, as shown in Figure 5-1. Alternatively, two capacitors can be inserted in series with each R_G resistor to achieve an ac-coupled configuration. Because the voltage between the two amplifier summing junction inputs is driven to a null by negative feedback, they are virtually connected, and the differential input resistance, Z_{IN_AMP}, is simply $R_{G1} + R_{G2}$. Keep in mind that there is a frequency dependency to Z_{IN_AMP} which may require for some applications to place a termination resistor, R_T, between the signal inputs, as shown in Figure 5-2. When calculating the amplifier gain the source impedance, R_S (shown here split in half for symmetry) needs to be added to the R_G value; assuming a balanced design the gain is given to:

EQUATION 5-1:

$$G = \frac{R_F}{R_G + R_S}$$

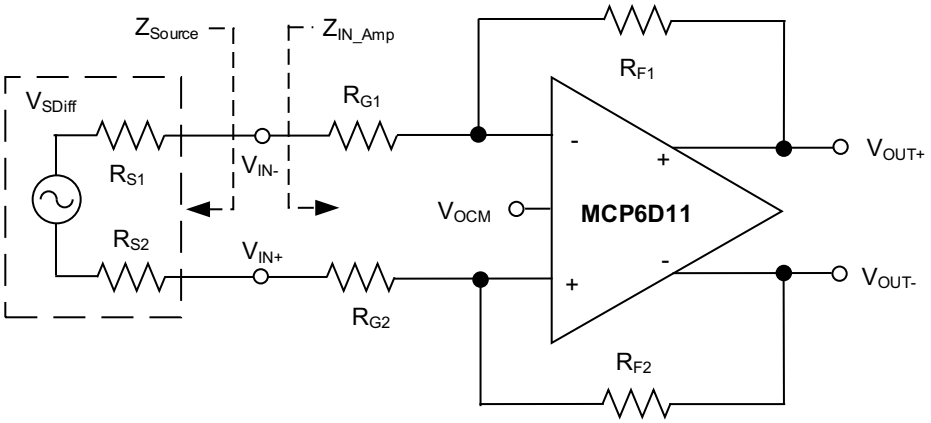

FIGURE 5-1: *Differential I/O Amplifier Driven by a Differential Source with DC-Coupling.*

When driving a signal over a longer distance, for example twisted-pair cables, termination with a resistor across the differential inputs may be required, as illustrated in Figure 5-2. The termination resistor, R_T, will appear in parallel to the sum of the two R_G resistors. The calculation of R_T is shown in Equation 5-2:

EQUATION 5-2:

$$R_T = \frac{1}{\frac{1}{R_S} - \frac{1}{(R_{G1} + R_{G2})}}$$

For example, with $R_{G1} = R_{G2} = 500\Omega$, and if the source impedance to match up to is $R_S = 100\Omega$ ($R_{S1} = R_{S2} = 50\Omega$), then the required value for R_T is 111Ω. Hence, the amplifiers input impedance Z_{IN_AMP}, as seen by the source will be $(R_T \parallel (R_{G1} + R_{G2})) = 100\Omega$.

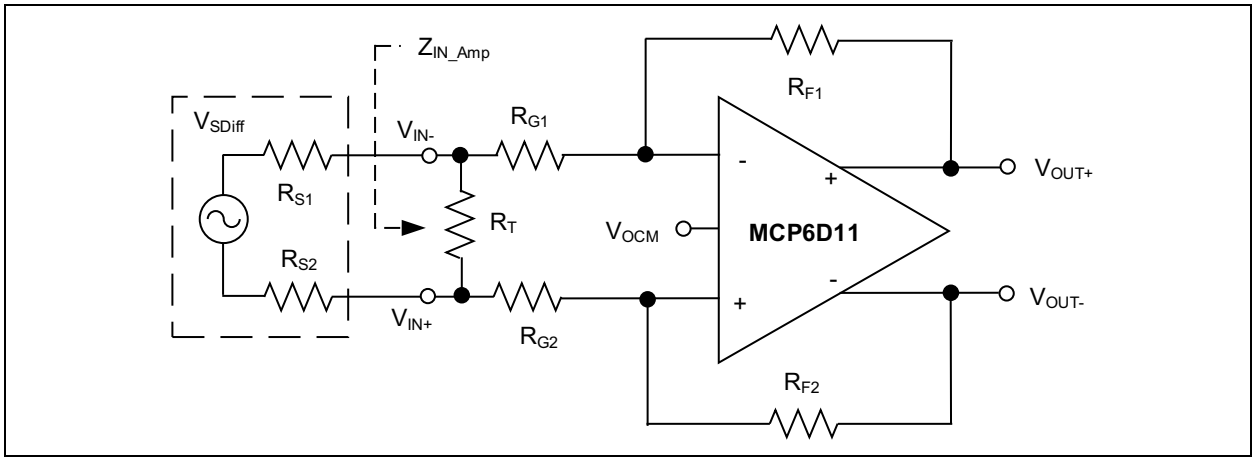

FIGURE 5-2: *Differential I/O Amplifier in Differential Configuration with Input Termination.*

The DC biasing levels are determined as described in **Section 4.2 "Terminology and Definitions"**. For a true differential input, the common-mode voltages on the summing junction inputs of the amplifier remain fixed and do not move with the input signal (unlike the single-ended input configurations where the input common-mode voltages do vary with the input signal). For the AC coupled configuration the V_{OCM} voltage also is the input biasing voltage since there is no DC current path through the feedback and gain resistors. In either case, setting the V_{OCM} voltage to a mid-supply value, which is the default value if this pin is not externally driven, assures symmetry and therefore maximizes the achievable output swing.

5.1.2 INTERFACING TO A SINGLE-ENDED SOURCE

If the source is single-ended and referenced to ground, the differential I/O amplifier can be used to convert a single-ended input signal into a differential output signal while also providing a DC level shift; Figure 5-3 shows the basic circuit for this configuration. Again, V_S is the input source with the associated source impedance $Z_{Source} = R_S$.

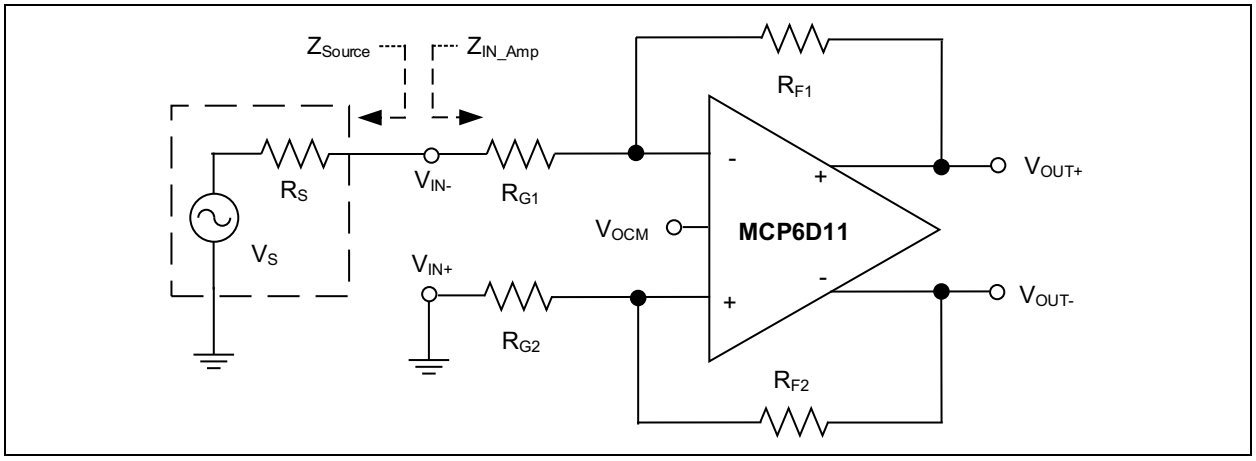

FIGURE 5-3: *Differential I/O Amplifier Driven by a Single-Ended Source with DC-Coupling.*

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As discussed earlier, any source resistance (Z_{Source}) will change the gain of the amplifier. For a single-ended input this occurs in an unbalanced way such that it affects only one side, for example R_{G1} as shown in Figure 5-3. To maintain balance between the amplifier's two feedback paths the user must set $R_{F1} = R_{F2}$ and $(R_{G1} + R_S) = R_{G2}$. The effect of resistor mismatching is discussed in **Section 5.1.3 "Mismatches and DC Errors"**. For the circuit shown in Figure 5-3 the differential output voltage is given by Equation 5-3:

EQUATION 5-3:

$$V_{OUT\_DM} = \frac{2V_S(1-\beta_1) + 2V_{OCM}(\beta_1 - \beta_2)}{(\beta_1 + \beta_2)}$$

Where: $\beta_1 = \frac{R_{G1} + R_S}{R_{G1} + R_S + R_{F1}}$,

and $\beta_2 = \frac{R_{G2}}{R_{G2} + R_{F2}}$.

In order to calculate the amplifier's input impedance, Z_{IN_AMP}, for this single-ended configuration it is important to recognize that the impedance looking in at the V_{IN-} point is actually higher than just the physical R_{G1} value, as it could be assumed based on a standard inverting op amp circuit. Compared to the differential input configuration, here the input common-mode voltage has an additional signal dependent term (see Equation 4-14) resulting in a portion of the input signal moving the summing junctions of the differential I/O amplifier in the same direction as the applied signal. This creates a signal related current flow in the non-signal side R_{G2} resistor and produces the inverted output signal. The current flow in the signal-side gain resistor R_{G1} is reduced by the moving common-mode voltage component, therefore resulting in an increased input impedance. The amplifier's common-mode feedback loop is a critical component in developing a differential output from a single-ended input signal, as it needs to dynamically adjust the input common-mode voltage in order to maintain balanced outputs. Meanwhile, the differential loop of the amplifier is forcing the voltages at the summing junctions to remain equal.

Use Equation 5-4 to determine the effective input impedance for the single-ended input configuration:

EQUATION 5-4:

$$Z_{IN\_AMP} = \frac{R_{G1}}{1 - \frac{R_F}{2 \times (R_{G1} + R_F)}}$$

Figure 5-4 shows the single-ended input circuit of Figure 5-3 extended for matching input termination, which adds resistor R_{T1}. The input impedance as seen by the source (Z_{IN}) therefore becomes:

$$Z_{IN} = R_{T1} \parallel Z_{IN\_AMP}$$

To retain balance between the feedback resistor networks it is necessary to adjust the gain resistor R_{G2} accordingly, here shown by adding R_{T2} which can be calculated as $R_{T2} = R_S \parallel R_{T1}$. If the resistor ratios are matched, the ratio of single-ended input to differential output gain is given by Equation 5-5:

EQUATION 5-5:

$$Gain\ (G) = \frac{V_{OUT\_DM}}{V_S} = \frac{R_{F1}}{R_{G1} + (R_S \parallel R_{T1})} \times \frac{2R_{T1}}{R_{T1} + R_S}$$

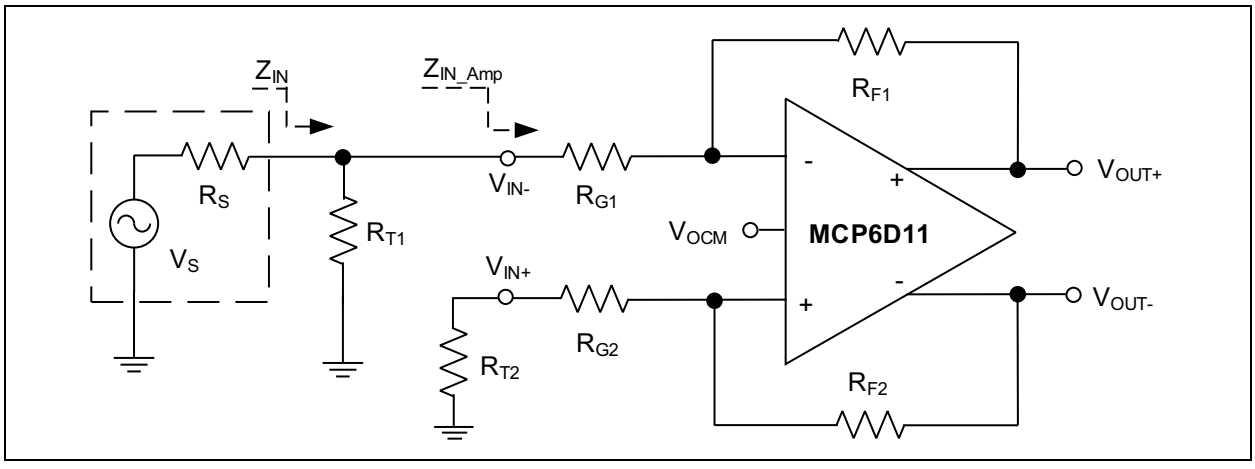

FIGURE 5-4: *Single-Ended Configuration with Input Termination and Resistor Ratio Matching.*

For the single-ended configuration with input impedance matching to a 50Ω source, Table 5-1 provides the required resistors using 1% standard values.

TABLE 5-1: R_F, R_G, R_T VALUES (1%) FOR SINGLE-ENDED INPUT PER Figure 5-4

Ideal Gain (V/V)	Act. Gain (V/V)	R_{F1}, R_{F2} (Ω)	R_{G1} (Ω)	R_{G1}^* (Ω) (Note 1)	R_{T1} (Ω)	R_{G2} (Ω)	R_{T2} (Ω) (Note 2)	Z_{IN_AMP} (Ω)	Z_{IN} (Ω)
1	0.997	1000	1000	1025.5	52.3	1020	25.5	1333	50.3
1	1.010	1000	976	1001.2	51.1	1020	25.2	1307	49.2
2	1.988	1020	499	524.5	52.3	523	25.5	754	48.9
5	5.057	1000	187	214.1	59.0	215	27.1	336	50.2
10	10.009	1020	88.7	117.4	68.1	118	28.7	183	50.6

Note 1: Effective gain resistor value: $R_{G1}^* = R_{G1} + (R_S \parallel R_{T1})$; $R_S = 50\Omega$.

2: $R_{T2} = R_{T1} \parallel R_S$.

5.1.3 MISMATCHES AND DC ERRORS

Compared to a standard op amp, the differential I/O amplifier has an additional output error term that arises from the effects of mismatching of the resistor values and feedback ratios, see **Section 4.2.2 "Signal Gain, Noise Gain"**. The user must select from standard resistor values (e.g. E96) and define the tolerance (e.g. 1% or 0.1%) suitable for the application, which will in almost all cases lead to some degree of imbalance, or difference in the feedback factors ($\Delta\beta$). For example, when selecting 1% tolerance resistors the worst case gain mismatch will be +/-2%; one side of the feedback path is at +2%, the other at -2%. Any such mismatch will cause a common-mode to differential conversion creating additional differential error terms. Opting for resistor values with a 0.1% tolerance is a good compromise between DC precision and cost.

The parameters that are affected and need to be considered for a DC error analysis are the V_{OCM} voltage, any input common-mode voltage from the source (V_{ICM}), and the input bias current.

To estimate the error contribution from V_{ICM} and V_{OCM} to the differential output voltage (V_{OUT_DM}) and assuming the differential input voltage is zero, use Equation 5-6 where the term ($\Delta\beta/\beta_{AVG}$) is the conversion gain factor to the output for the gain ratio mismatch.

EQUATION 5-6:

$$V_{OUT\_DM} \approx (V_{OCM} - V_{ICM}) \times \frac{\Delta\beta}{\beta_{AVG}}$$

The input bias current (I_B) contributes two error terms, one based on the resistor tolerance (±T; for 1% T = 0.01) and the other based on the gain mismatch. Estimate the first error term by multiplying the input bias current by (±2 x T x R_{F_Nom}), with R_{F_Nom} being the nominal feedback resistor value, for example 1 kΩ. To estimate the I_B error due to the gain mismatch multiply I_B by the average R_F value times the ($\Delta\beta/\beta_{AVG}$) is the conversion gain factor.

Additional terms for a comprehensive DC error analysis should include the input offset voltage (V_{OS}) and the input offset current (I_{OS}). Before adding to the total differential output error the input offset voltage needs to be multiplied by the noise gain (G_N), which in the case of the differential I/O amplifier is the average of the two noise gains resulting from the two mismatched R_G/R_F ratios. The error resulting from the input offset current is simply referred to the output by multiplying with the average feedback resistor value (R_{F_AVG}).

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5.2 Noise and Distortion

5.2.1 NOISE ANALYSIS

The MCP6D11 features very low noise with the voltage noise density at 5.0 nV/√Hz and the current noise density at 0.6 pA/√Hz. When analyzing the total output referred differential noise (e_{no}) of an amplifier stage the surrounding resistor network contributions need to be considered. Shown in Figure 5-5 is the general noise model of a differential I/O amplifier and its resistor feedback components.

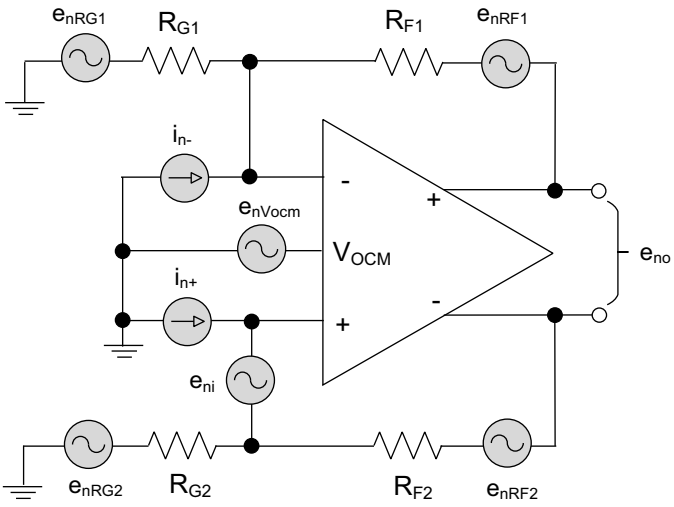

FIGURE 5-5: *Differential I/O Amplifier Noise Analysis Model.*

The analysis starts by identifying each voltage- and current-noise term and its corresponding multiplication factor (noise gain) in order to derive its contribution to the total output noise (e_{no}). The individual output-referred noise terms are then squared to combine noise as powers and are subsequently combined as a root-sum-of-squares (RSS). For the Differential I/O amplifier the voltage- and current-noise terms from each feedback path result in a 2 x contribution to the total noise as shown in Equation 5-7 below. One additional term is the common-mode voltage noise (e_{nvocm}), which normally reflects to the output as a common-mode term, unless the two feedback ratios are mismatched. Then a conversion from common-mode to differential will occur. For e_{nvocm} the gain multiplier when referred to the output is: G_N x (β_1 - β_2), which will be zero when $\beta_1 = \beta_2$.

EQUATION 5-7:

$$e_{no} = \sqrt{\frac{(2e_{ni})^2 + (2i_n \times R_{eq1})^2 + (2i_n \times R_{eq2})^2 + (2e_{nvocm} \times (\beta_1 - \beta_2))^2 + (2e_{nRG1}(1-\beta_1))^2 + (2e_{nRG2}(1-\beta_2))^2}{(\beta_1 + \beta_2)^2} + (e_{nRF1})^2 + (e_{nRF2})^2}$$

Where:

$$R_{eq1} = R_{G1} \parallel R_{F2}$$

$$R_{eq2} = R_{G2} \parallel R_{F2}$$

If the feedback ratios, β_1 and β_2 ($R_G = R_{G1} = R_{G2}$, $R_F = R_{F1} = R_{F2}$) are equal, the equation simplifies considerably to an expression very similar to a common voltage-feedback op amp's noise equation, as shown in Equation 5-8. Also, the current noise terms are assumed to be equal ($i_{n+} = i_{n-}$) and uncorrelated.

EQUATION 5-8:

$$e_{no} = \sqrt{\left[e_{ni}\left(1 + \frac{R_F}{R_G}\right)\right]^2 + 2(i_n R_F)^2 + 2\left(4kTR_G\frac{R_F}{R_G}\right)^2 + 2(4kTR_F)^2}$$

Where: 4kT = 1.64^{-20}J at 298K (25°C)

The noise contribution from resistors R_{G1}, R_{F1}, R_{G2} and R_{F2} can be calculated based on the Johnson noise equation: $e_{nR} = \sqrt{4kTR}$, where k is Boltzmann's constant (1.38065 x 10^{-23}J/K), T is the resistor's absolute temperature in Kelvin, and R is the resistor value in ohms (Ω).

By using the noise gain ($G_N = 1 + R_F/R_G$) the two resistor noise terms can be combined into a single term of ($4kTR_FG_N$) resulting in a much simplified equation for the amplifier's differential output noise:

EQUATION 5-9:

$$e_{no} = \sqrt{(e_{ni}G_N)^2 + 2(i_n R_F)^2 + 2(4kTR_F G_N)}$$

The first term of Equation 5-9 is the differential input noise times the noise gain. The second term is the input current noise times the feedback resistor - twice, since there are two uncorrelated current noise terms.

The last term is the output noise resulting from both the R_F and R_G resistors, at again twice the value for the output noise power of each side added together.

The input referred noise of the MCP6D11 can be equated to that of a 1.6 kΩ resistor. The recommended value for the feedback resistor R_F is 1kΩ, which results in the total output referred noise to be dominated by the amplifier's voltage noise. While there is flexibility in selecting different values for R_F (and similarly for R_G), lowering the feedback resistor value in order to lower its noise contribution will increase the amplifier's total output load and eventually result in an increase in distortion. Scaling the resistor value up will have the opposite effect of potentially improving distortion at the expense of higher noise contribution. However, because the feedback resistor interacts with the amplifier's input capacitance large values can lead to a noticeable reduction in phase margin and cause stability issues. A typical approach is to start with the recommended feedback resistor value and set the desired gain by scaling the gain resistor (R_G) accordingly; Table 5-2 shows some example resistor values and corresponding noise results.

TABLE 5-2: EXAMPLE OUTPUT NOISE RESULTS FOR THE SINGLE-ENDED INPUT CONFIGURATION WITH 50Ω INPUT MATCHING PER Figure 5-4

Ideal Gain (V/V)	Act. Gain (V/V)	R_{F1}, R_{F2} (Ω)	R_{G1} (Ω)	R_{T1} (Ω)	R_{G2} (Ω)	Z_{IN} (Ω)	Diff-Out Noise e_{no} (nV/√Hz)	Noise RTI (nV/√Hz)
1	0.997	1000	1000	52.3	1020	50.3	12.90	12.90
2	1.988	1020	499	52.3	523	48.9	18.02	9.06
5	5.057	1000	187	59.0	215	50.2	31.99	6.33
10	10.009	1020	88.7	68.1	118	50.6	52.60	5.26

5.2.2 FACTORS AFFECTING HARMONIC DISTORTION

In general, an amplifier's output harmonic distortion mainly relates to the open loop linearity in the output stage corrected by the loop gain at the fundamental frequency. Reducing the total load impedance, including the effect of the feedback resistor as discussed previously, the output stage open loop linearity degrades, causing an increase in harmonic distortion. Secondly, harmonic distortion will degrade as a function of the amplifier's output swing due to fine scale open loop output stage nonlinearities. A nominal swing of $2V_{pp}$ is typically used for harmonic distortion testing where Figure 3-29 illustrates the effect of going up to an $8V_{pp}$ differential swing that is more common with SAR-type ADC converters. An increase in the amplifiers' gain correspondingly reduces the available loop gain to correct errors resulting in an increase in harmonic distortion terms.

The MCP6D11 has a nearly constant distortion level when the V_{OCM} operating point is moved within the allowed range; see Figure 3-30 and Figure 3-31. Driving the V_{OCM} voltage beyond this range or the output voltages close to the supply rails will rapidly degrade the distortion performance.

The device characterization used primarily resistors with a 1% tolerance. The resulting imbalance of the feedback factors does not directly degrade the distortion performance of the amplifier, but rather DC related errors (see section **Section 5.1.3 "Mismatches and DC Errors"**).

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5.2.3 SIGNAL BANDWIDTH LIMITATIONS

Although the MCP6D11 has a unity gain bandwidth of 90 MHz, it is primarily intended as driver for lower sample rate, high-precision ADCs with baseband input signal bandwidths in the DC to 100 kHz range. The high open loop gain and bandwidth of the MCP6D11 provides ultra-low distortion and fast settling times. Maximum power bandwidth is limited by the slew rate capability, which is typically 25V/µs. Operation with input signals above 100 kHz with near full output swings will see an increase in distortion levels (see Figure 3-22).

5.2.4 CAPACITIVE LOADS

Directly connecting a capacitive load to the output pins of a closed loop amplifier such as the MCP6D11 can lead to an unstable response; see the step response plots into a capacitive load Figure 3-37 and Figure 3-38. As illustrated in Figure 4-4, the rail-to-rail output stage of the MCP6D11 exhibits an inductive characteristic in the open loop output impedance at higher frequencies. This inductive open loop output impedance will interact with any capacitance present at the amplifier's outputs causing an additional phase shift, i.e. phase margin reduction. Account for the total capacitive load by considering all contributions from sources including feedback capacitors, next-stage input capacitance and PC-board parasitics. Larger values of feedback capacitors (C_F greater than 10 pF) can risk a low phase margin. Including a 10Ω to 15Ω series resistor with a feedback capacitor can be used to reduce this effect.

In most cases, inserting small value resistors (R_{ISO}) in series with each of the amplifier's outputs will isolate the capacitive load and can help avoiding or eliminating stability problems. Refer to Figure 5-6 for suggested R_{ISO} values. In general, as the noise gain (G_N) of the device increases the value of the R_{ISO} resistor can be reduced while still obtaining a dampened response.

Even when the application may not require the use of series R_{ISO} resistors, good practice is to leave a footprint for the R_{ISO} components on the PC-board layout (a 0Ω value initially) for later adjustment in case the response appears unacceptable.

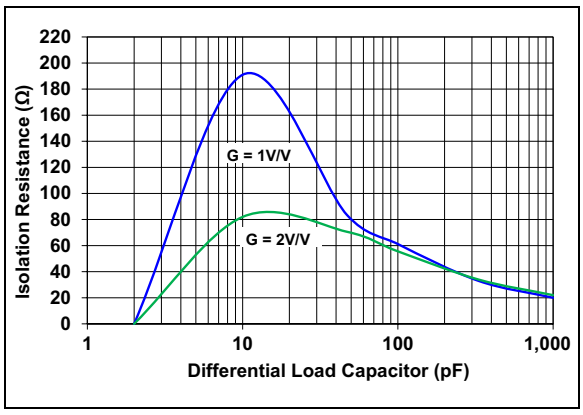

FIGURE 5-6: *R_{ISO} vs. Differential Load Capacitor.*

5.3 Application Example

5.3.1 DRIVING HIGH PRECISION ADCS

The MCP6D11 differential I/O amplifier was designed primarily as an integrated front-end driver amplifier solution for high resolution ADCs, such as the SAR ADC MCP33131D. The 16-bit MCP33131D is part of a family of low-power 16-/14-/12-Bit, 1Msps SAR ADCs that feature differential inputs which are preferably driven by an amplifier with differential outputs to preserve their full performance.

The circuit in Figure 5-7 shows the MCP6D11 amplifier in a dc-coupled differential-input to differential-output configuration driving the MCP33131D while operating on a single-supply. The circuit can easily be adapted for a single-ended input to differential output configuration.

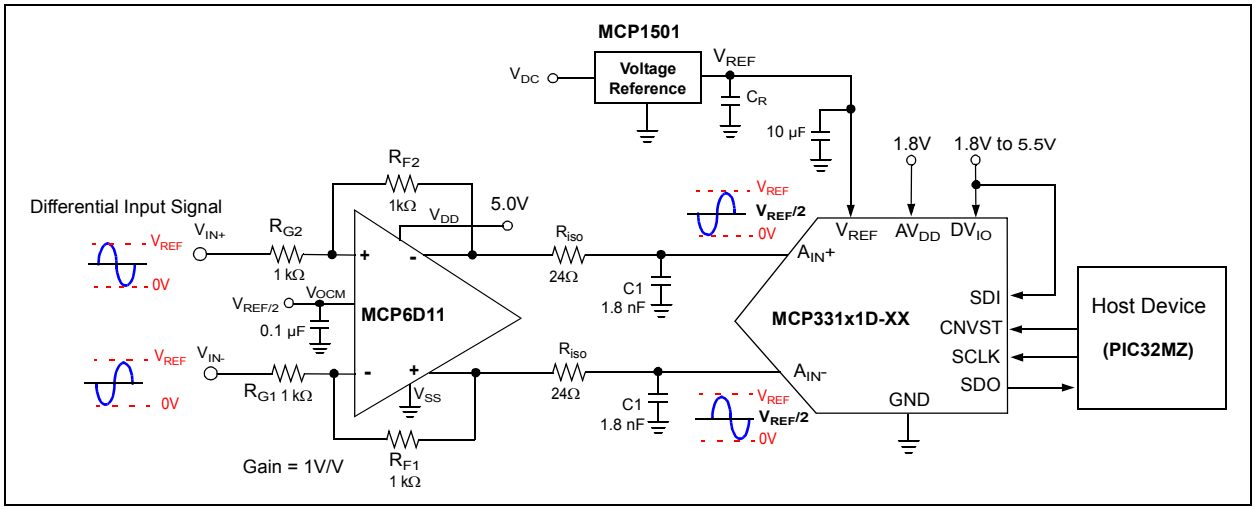

FIGURE 5-7: *Circuit Example for the MCP6D11 Driving the 16-bit 1Msps SAR ADC MCP33131D.*

In almost all cases, a single-pole RC low-pass filter should be placed between the driver amplifier and the ADC, as shown in Figure 5-7. The input stage of the ADC is a sample-and-hold and the internal capacitor appears as a capacitive load to the driver amplifier. The typical sampling capacitor of the MCP33131D is 62 pF (differential). As part of the sampling process, significant charge injection occurs, resulting in fast current pulses that the amplifier output needs to react to while settling from this transient load condition to the new signal value within the allowed acquisition time. Here, the RC components serve a number of purposes. The capacitor (C1) helps to dampen the charge injection effects by providing a charge reservoir for an instantaneous current transfer with the ADC's sampling capacitor. Therefore, the value of this charge capacitor (C1) needs to be several times larger than the ADC sampling capacitor, however too high values will load the amplifier and result in increased distortion. The capacitor should be a NP0- or C0G -type due to their superior electrical and temperature stability.

The two series resistors (R_{ISO}) primarily serve to isolate the capacitive loading due to capacitor C1 plus the sampling capacitor from the amplifier outputs and improved stability. Their value, along with the value of C1, should be chosen to achieve the desired settling behavior. For example, settling to 15-bit accuracy will require approximately 10 RC time constants. The number of time constants may vary between ADC models, depending on how the internal Sample-and-Hold circuit operates. It is generally best to keep the resistor value as low as possible while maintaining stability. High resistor values can be detrimental and lead to increased distortion. The RC network also performs a low-pass function and sets a bandwidth limit for the noise. However, as a single-pole filter, it is of limited use as an anti-aliasing filter. To implement a higher-order anti-aliasing filter, the MCP6D11 differential I/O amplifier can be configured to perform this function, such as an MFB-type filter.

The -3 dB frequency of the RC filter is calculated using Equation 5-10:

EQUATION 5-10:

$$f_{-3dB} = \frac{1}{2\pi R_{ISO}(C1 + C_{Sampling})}$$

Note: The ADC input capacitance should be factored into the frequency response of the input filter.

Shown in Figure 5-8 is the FFT of the MCP6D11 driving the MCP33131 differentially using a 4V ADC reference voltage resulting in an 8Vpp full-scale range (FSR). The 9.674 kHz input signal is set to -1 dBFS and the second and third harmonic is down at -113.3 dBc and -111.3 dBc respectively, with THD at -104.9 dBc.

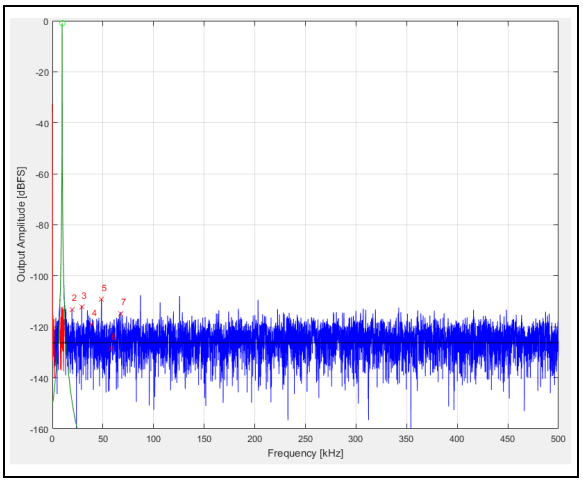

FIGURE 5-8: *FFT Result of the MCP6D11 driving the MCP33131D, FSR = 8Vpp, fin = 9.7 kHz at -1dBFS.*

Figure 5-9 shows the FFT for the same configuration as in Figure 5-8, now with the input signal at 100 kHz. The highest harmonic is HD3 at -92.8 dBc while the second harmonic is at -101.6 dBc. THD is measured at -91.3 dBc.

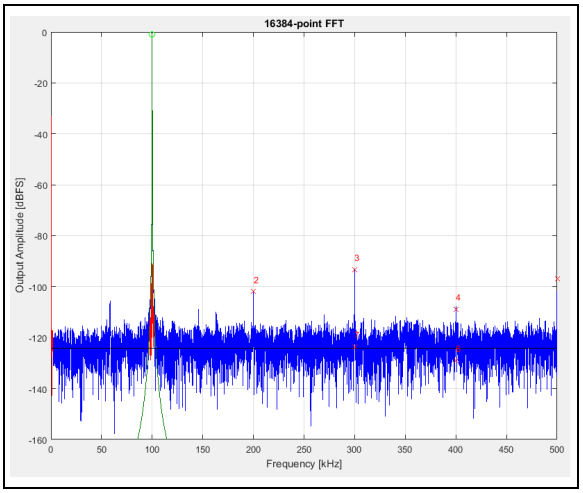

FIGURE 5-9: *FFT Result of the MCP6D11 Driving the MCP33131D, FSR = 8Vpp, fin = 100 kHz at -1 dBFS.*

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5.4 Application Tips

5.4.1 SUPPLY BYPASSING CAPACITORS

When operating the MCP6D11 in a single-supply configuration (V_{SS} = Ground), only the V_{DD} pin will require supply bypass capacitors. Using split supplies ensure that both amplifier supply pins have similar bypass capacitors tied to a low-noise analog ground. The QFN-16 package has four pins for the V_{DD} and V_{SS} supply connections, which are usually tied together on the PCB and the bypass capacitor can be shared for each set of four supply pins. The primary high-frequency bypass capacitors should be placed as close to the amplifier's supply pins as possible with direct connection to a low impedance analog ground. Use a 1 nF and a 0.1 µF leadless surface mount (e.g. size 0603), ceramic capacitor in parallel for each supply. For best high-frequency decoupling, consider X2Y-type capacitors that offer a much higher self-resonance frequency over standard capacitors. Most applications benefit from adding a bulk capacitor (e.g. 2.2 µF to 10 µF, tantalum or ceramic) within approximately 20 mm (0.8 inch) of the supply pins, which can be shared among multiple MCP6D11 devices.

5.4.2 V_{OCM} BYPASSING

In addition to the supply decoupling, the VOCM pin should be bypassed with a 0.1 µF leadless surface mount, ceramic capacitor for either case, externally driven or left open. This will reduce the noise feedthrough to the amplifier's output from this high impedance input.

5.4.3 PCB LAYOUT

While the MCP6D11 amplifier may be used to for relatively low signal frequencies (f < 500 kHz), it is critical to apply high-frequency PC-board techniques in order to preserve the low distortion and fast step response capabilities of the device. The input summing junctions and the differential outputs in particular of the MCP6D11 are very sensitive to parasitic capacitances even as low as 0.5 pF.

Following are some specific recommendations:

- Continuous ground planes usually work well to establish a low impedance analog ground potential. Also, multi-layer PCB designs often use power planes. When used, the user must make sure that both power and ground planes include keep-out areas under and around the device and around sensitive nodes on the feedback and gain setting components (e.g. R_G, R_F, C_F).
- The feedback resistors (R_F) should be placed with minimum trace length between the amplifier's output and summing function input pins.
- The gain resistors (R_G) should connect to the summing junction pins with minimum trace length.
- When using the QFN-16 package, note that the FB+ and FB- pins are duplicates of the output pins (OUT+, OUT-) but are placed conveniently close to the corresponding inputs such that the external feedback resistor (R_F) can be placed with minimum trace length. This minimizes potential parasitic capacitances affecting sensitive device pins. Note that the internal trace adds about 3Ω to the external feedback resistor value.
- When routing differential/complementary signals, ensure a highly symmetric layout placement with identical trace length. Even small amounts of asymmetry can lead to distortion and balance errors. Routing such signal traces over a longer distance will in most cases require microstrip layout and impedance matching techniques.
- Use surface mount small geometry 0603 or 0402 size resistors and capacitors to minimize parasitic capacitance effects.
- The exposed thermal pad on the QFN-16 package should be soldered to a low-noise ground or power plane. While the pad is electrically isolated from the die it must be connected preferably to a ground plane (alternatively a power plane) and not be left floating.

NOTES:

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6.0 DESIGN AIDS

Microchip provides the basic design aids needed for the MCP6D11 family of op amps.

6.1 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/maps, MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, a customer can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for data sheets, purchase and sampling of Microchip parts.

6.2 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

ADN003: *"Select the Right Operational Amplifier for your Filtering Circuits"*, DS21821

AN722: *"Operational Amplifier Topologies and DC Specifications"*, DS00722

AN723: *"Operational Amplifier AC Specifications and Applications"*, DS00723

AN884: *"Driving Capacitive Loads With Op Amps"*, DS00884

AN990: *"Analog Sensor Conditioning Circuits – An Overview"*, DS00990

AN1177: *"Op Amp Precision Design: DC Errors"*, DS01177

AN1228: *"Op Amp Precision Design: Random Noise*", DS01228

AN1258: *"Op Amp Precision Design: PCB Layout Techniques"*, DS01258

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NOTES:

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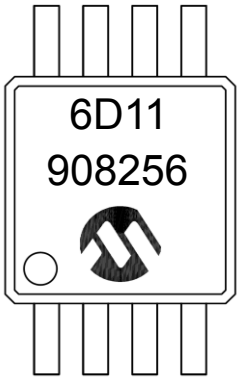
7.0 PACKAGING INFORMATION

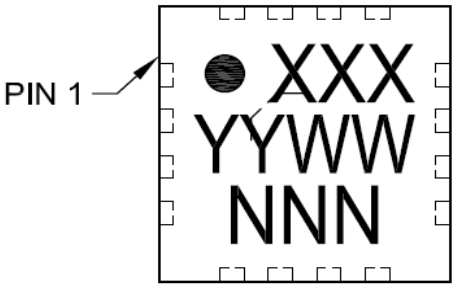
7.1 Package Marking Information

8-Lead MSOP

Example

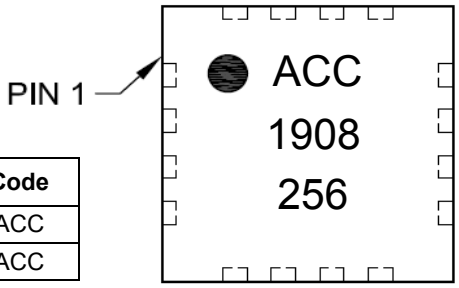


16-Lead, 3x3 mm QFN



Part Number	Code
MCP6D11-E/MG	ACC
MCP6D11T-E/MG	ACC

Example

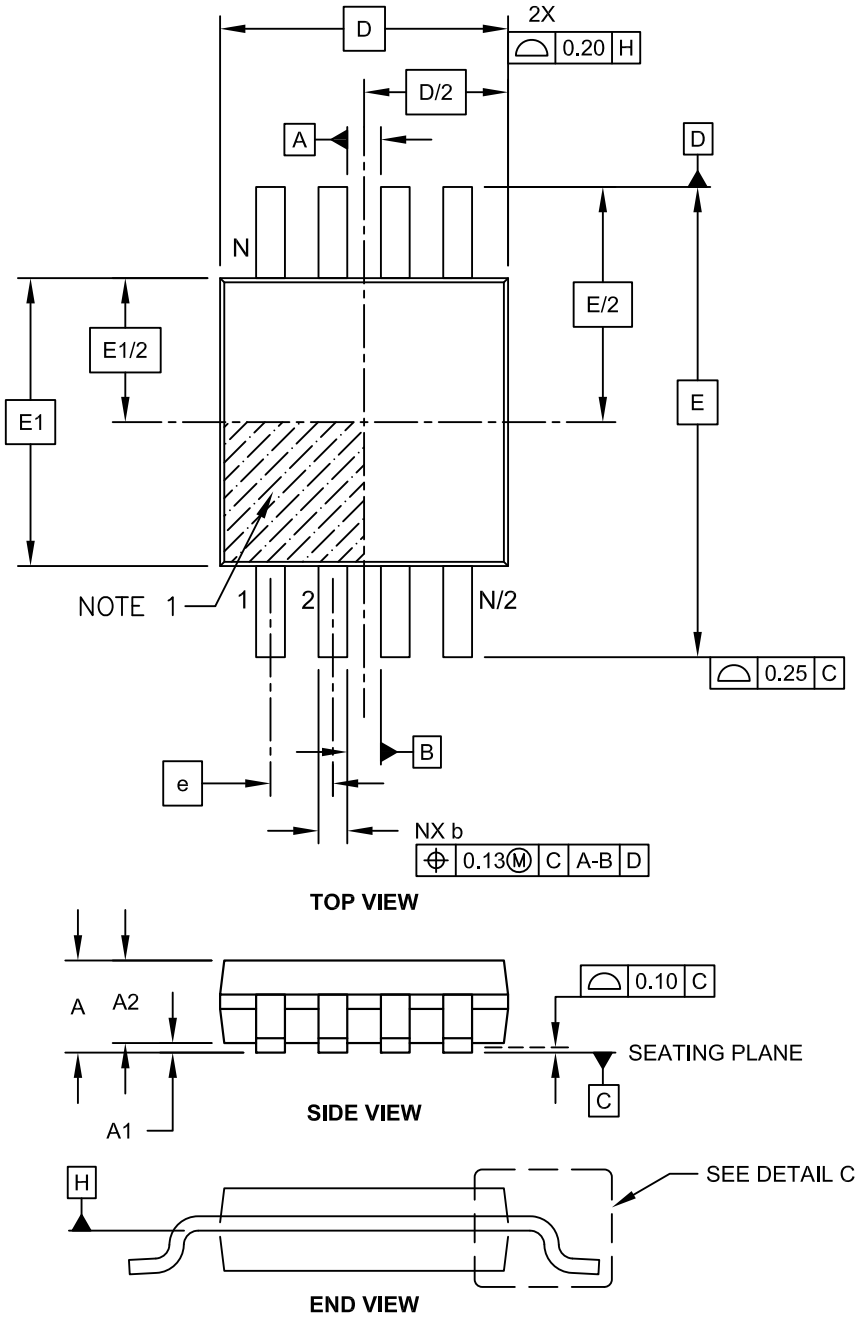


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

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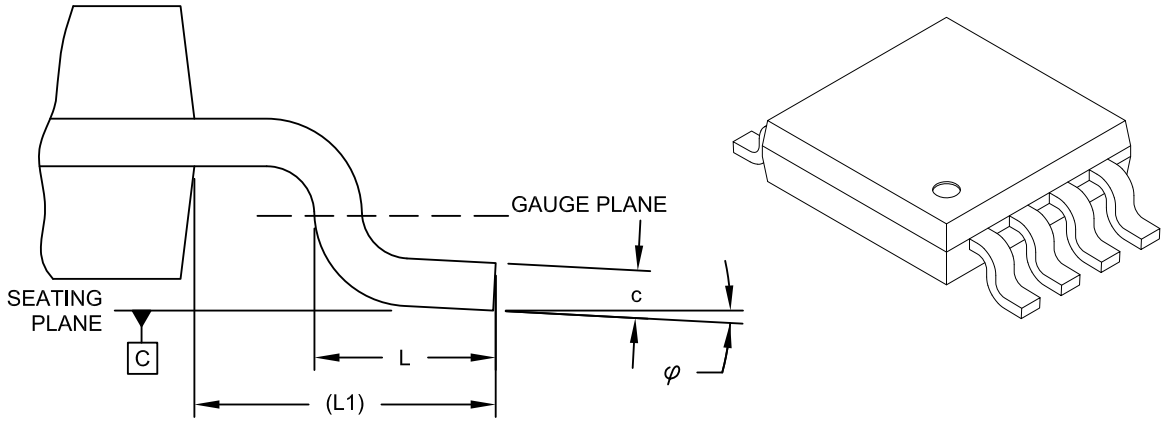


DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

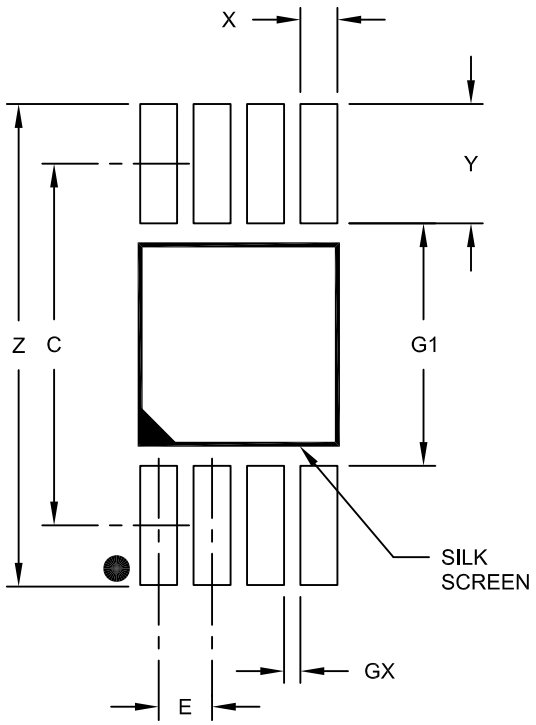
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

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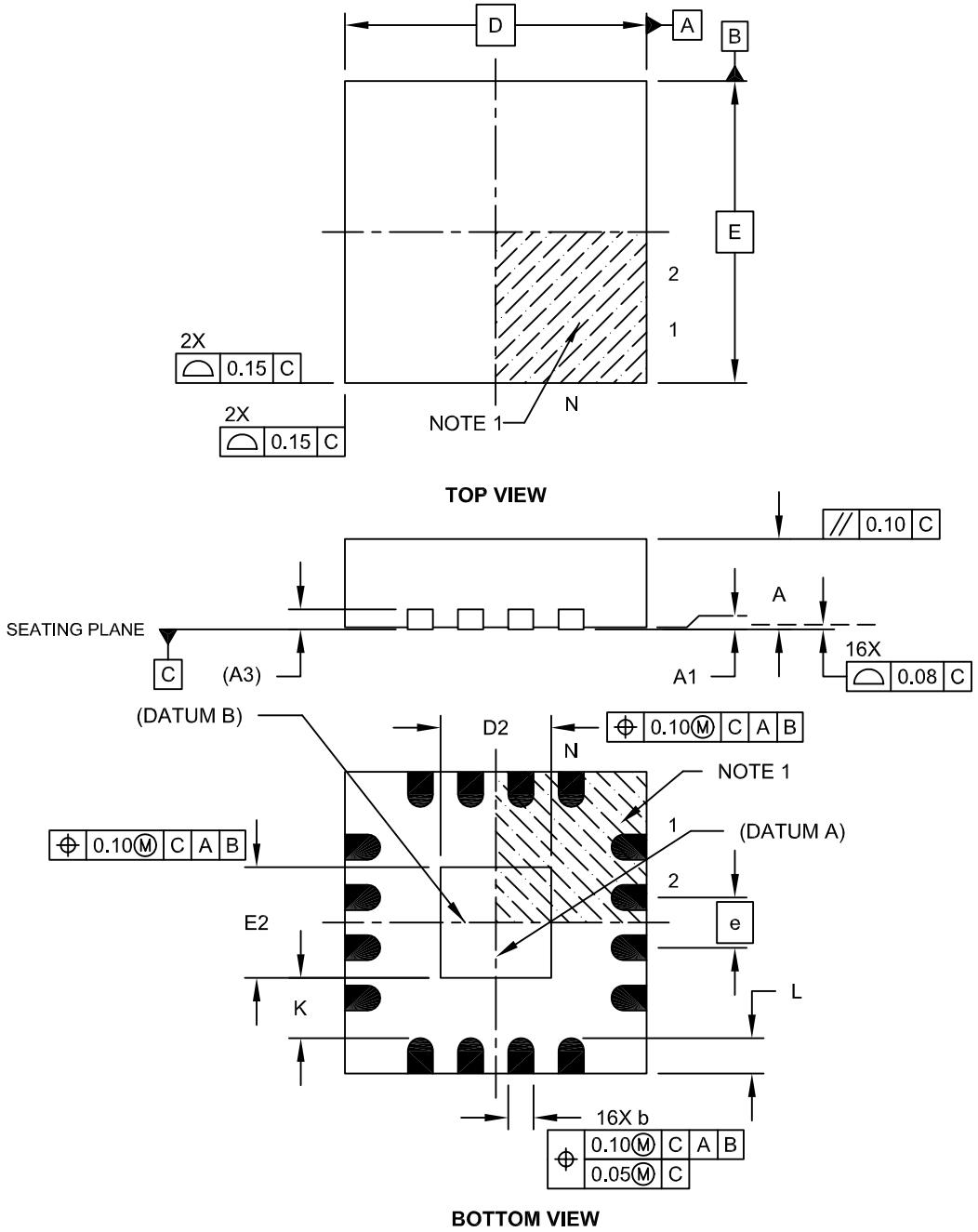
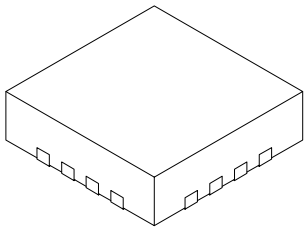


Microchip Technology Drawing C04-142A Sheet 1 of 2

16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.00	1.10	1.50
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.00	1.10	1.50
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.25	0.35	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-142A Sheet 2 of 2

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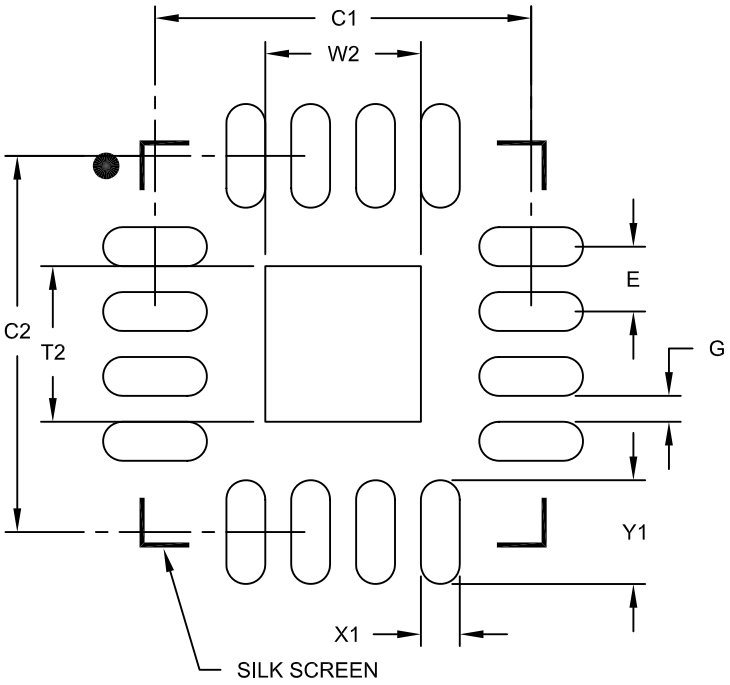
16-Lead Plastic Quad Flat, No Lead Package (MG) – 3x3x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.20
Optional Center Pad Length	T2			1.20
Contact Pad Spacing	C1		2.90	
Contact Pad Spacing	C2		2.90	
Contact Pad Width (X16)	X1			0.30
Contact Pad Length (X16)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (February 2019)

- Initial release of this Data Sheet.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	MCP6D11 - Low Noise, Precision, 90 MHz Differential I/O Amplifier	
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	MS MG	= 8-Lead Plastic Micro Small Outline Package (MSOP) = 16-Lead Quad Flat No Lead Package (QFN)

Examples:

a)	MCP6D11-E/MS	Extended temperature, MSOP package
b)	MCP6D11-E/MG	Extended temperature, QFN package
c)	MCP6D11T-E/MS	Extended temperature, MSOP package, Tape and Reel
d)	MCP6D11T-E/MG	Extended temperature, QFN package, Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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