# Quad 2-Input NAND Schmitt Trigger

The MC74VHC132 is an advanced high speed CMOS Schmitt NAND trigger fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

Pin configuration and function are the same as the MC74VHC00, but the inputs have hysteresis and, with its Schmitt trigger function, the VHC132 can be used as a line receiver which will receive slow input signals.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0~V, allowing the interface of 5.0~V systems to 3.0~V systems.

### **Features**

- High Speed:  $t_{PD} = 4.9 \text{ ns (Typ)}$  at  $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 2 \mu A \text{ (Max)}$  at  $T_A = 25 \text{°C}$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 0.8 \text{ V (Max)}$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance:

Human Body Model > 2000 V; Machine Model > 200 V

- Chip Complexity: 72 FETs or 18 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

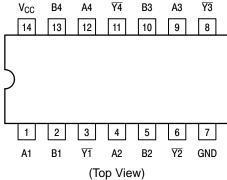


Figure 1. Pinout: 14-Lead Packages



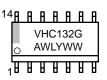
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## MARKING DIAGRAMS



SOIC-14 D SUFFIX CASE 751A





TSSOP-14 DT SUFFIX CASE 948G



A = Assembly Location

WL, L = Wafer Lot Y = Year WW, W = Work Week G or = Pb-Free Package

(Note: Microdot may be in either location)

## **FUNCTION TABLE**

Inp	Output	
Α	В	Y
L	L	Н
L	Н	Н
Н	L	Н
H	Н	L

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

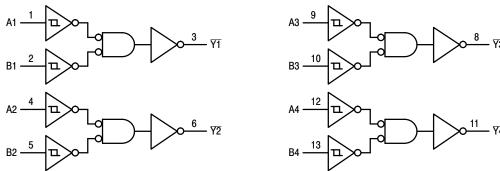


Figure 2. Logic Diagram

## **MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit	
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V	
V <sub>in</sub>	DC Input Voltage		-0.5 to +7.0	V
V <sub>out</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> +0.5	V	
I <sub>IK</sub>	Input Diode Current	-20	mA	
I <sub>OK</sub>	Output Diode Current		±20	mA
I <sub>out</sub>	DC Output Current, per Pin		±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GI	Supply Current, V <sub>CC</sub> and GND Pins		mA
P <sub>D</sub>	Power Dissipation in Still Air,	SOIC Packages† TSSOP Package†	500 450	mW
T <sub>stg</sub>	Storage Temperature		-65 to +150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating – SOIC Packages: – 7 mW/°C from 65° to 125°C TSSOP Package: – 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	5.5	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	<b>-</b> 55	+ 125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

			V <sub>CC</sub>	٦	Γ <sub>A</sub> = 25°0	С	$T_A = -55$	to +125°C	
Symbol	Parameter	Test Conditions	V	Min	Тур	Max	Min	Max	Unit
V <sub>T+</sub>	Positive Threshold Voltage (Figure 5)		3.0 4.5 5.5			2.20 3.15 3.85		2.20 3.15 3.85	V
V <sub>T-</sub>	Negative Threshold Voltage (Figure 5)		3.0 4.5 5.5	0.9 1.35 1.65			0.90 1.35 1.65		V
V <sub>H</sub>	Hysteresis Voltage (Figure 5)		3.0 4.5 5.5	0.30 0.40 0.50		1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50  \mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	3.0 4.5	2.58 3.94			2.48 3.80		
V <sub>OL</sub>	Maximum Low–Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50  \mu\text{A}$	2.0 3.0 4.5		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	3.0 4.5			0.36 0.36		0.44 0.44	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μΑ
I <sub>CC</sub>	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			2.0		20.0	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS (Input $t_f = t_f = 3.0 \text{ns}$ )

				1	A = 25°	С	T <sub>A</sub> = -55 t	to +125°C	
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay,  A or B to $\overline{Y}$	$V_{CC} = 3.3 \pm 0.3 \text{ V}$	$C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		7.6 10.1	11.9 15.4	1.0 1.0	14.0 17.5	ns
	AUIBIOT	$V_{CC} = 5.0 \pm 0.5 \text{ V}$	C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		4.9 6.4	7.7 9.7	1.0 1.0	9.0 11.0	
C <sub>in</sub>	Maximum Input Capacitance				4	10		10	pF

		Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
$C_{PD}$	Power Dissipation Capacitance (Note 1)	16	pF

C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/4 (per gate). C<sub>PD</sub> is used to determine the no–load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## **NOISE CHARACTERISTICS** (Input $t_r = t_f = 3.0 \text{ns}$ , $C_L = 50 \text{pF}$ , $V_{CC} = 5.0 \text{ V}$ )

		T <sub>A</sub> = 25°C		
Symbol	Characteristic	Тур	Max	Unit
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.3	0.8	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-0.3	-0.8	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage		3.5	V
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		1.5	V

## **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC74VHC132DG	SOIC-14 55 Units / I (Pb-Free)	
MC74VHC132DR2G	SOIC-14 (Pb-Free)	2500 Tape & Reel
MC74VHC132DTR2G	TSSOP-14 (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

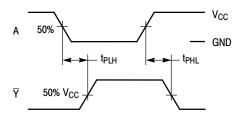
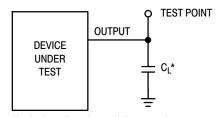
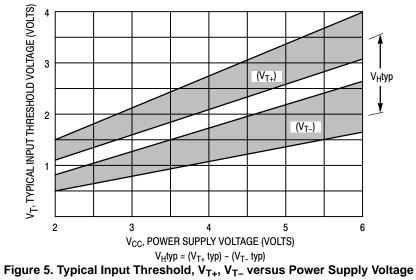


Figure 3. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 4. Test Circuit



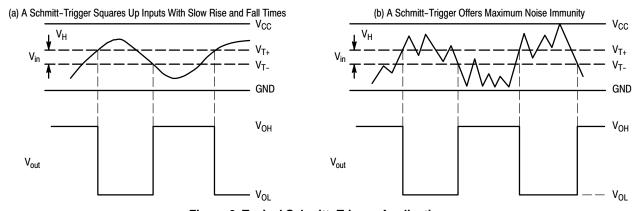


Figure 6. Typical Schmitt-Trigger Applications

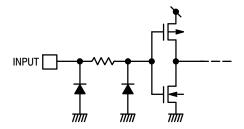
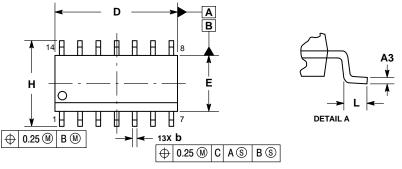
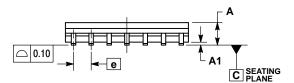


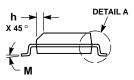
Figure 7. Input Equivalent Circuit

## **PACKAGE DIMENSIONS**

SOIC-14 CASE 751A-03 ISSUE L







- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

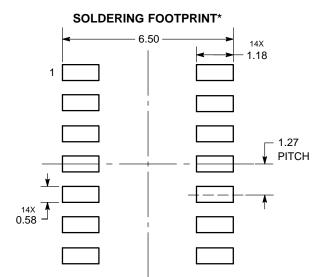
  2. CONTROLLING DIMENSION: MILLIMETERS.

  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.

  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.

  5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	8411 1 18	ETERO	INIO		
	MILLIMETERS		INCHES		
DIM	MIN MAX		MIN	MAX	
Α	1.35	1.75	0.054	0.068	
A1	0.10	0.25	0.004	0.010	
A3	0.19	0.25	0.008	0.010	
b	0.35	0.49	0.014	0.019	
D	8.55	8.75	0.337	0.344	
Е	3.80	4.00	0.150	0.157	
е	1.27	1.27 BSC		BSC	
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.019	
L	0.40	1.25	0.016	0.049	
М	0 °	7°	0 °	7°	

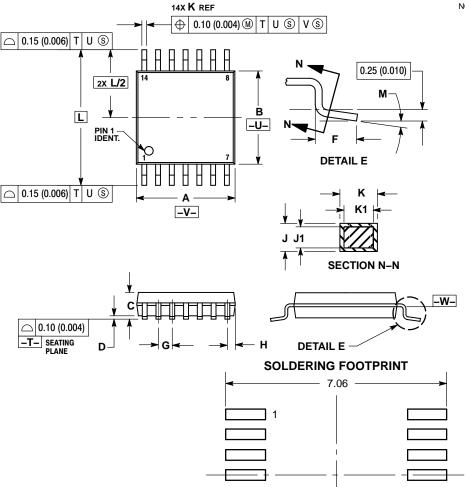


**DIMENSIONS: MILLIMETERS** 

<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### PACKAGE DIMENSIONS

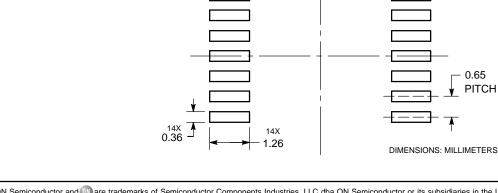
## TSSOP-14 CASE 948G **ISSUE C**



#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER. 3. DIMENSION A DOES NOT INCLUDE MOLD
- J. DIMENSION A DUES MOIT INCLUDE MOLD
  FLASH, PROTRUSIONS OR GATE BURRS.
  MOLD FLASH OR GATE BURRS SHALL NOT
  EXCEED 0.15 (0.006) PER SIDE.
  1. DIMENSION B DOES NOT INCLUDE
  INTERLEAD FLASH OR PROTRUSION.
  INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С	-	1.20		0.047	
D	0.05	0.15 0.0		0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026	BSC	
Н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40	BSC	0.252 BSC		
М	0 °	8 °	0°	8 °	



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