Quad 2-Input AND Gate

High–Performance Silicon–Gate CMOS

Features

- Outputs Source/Sink 24 mA
- 'ACT08 Has TTL Compatible Inputs
- These are Pb–Free Devices

V_{CC}



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ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.



Figure 1. Pinout: 14–Lead Packages Conductors (Top View)

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V
VI	DC Input Voltage		$-0.5 \leq V_{I} \leq V_{CC} + 0.5$	V
Vo	DC Output Voltage	(Note 1)	$-0.5 \le V_O \le V_{CC} + 0.5$	V
I _{IK}	DC Input Diode Current		±20	mA
I _{OK}	DC Output Diode Current		±50	mA
I _O	DC Output Sink/Source Current		±50	mA
I _{CC}	DC Supply Current per Output Pin		±50	mA
I _{GND}	DC Ground Current per Output Pin		±50	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
TL	Lead temperature, 1 mm from Case for 10 Seco	nds	260	°C
TJ	Junction temperature under Bias		+ 150	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC TSSOP	125 170	°C/W
P _D	Power Dissipation in Still Air at 85°C	SOIC TSSOP	125 170	mW
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating Oxy	rgen Index: 30% – 35%	UL 94 V-0 @ 0.125 in	
V _{ESD}	Ň	n Body Model (Note 3) Aachine Model (Note 4) Device Model (Note 5)	> 2000 > 200 > 1000	V
I _{Latch-Up}	Latch–Up Performance Above V _{CC} and Below	/ GND at 85°C (Note 6)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.

The package thermal impedance is calculated in accordance with JESD51–7.
 Tested to EIA/JESD22–A114–A.

4. Tested to EIA/JESD22-A115-A.

5. Tested to JESD22-C101-A.

6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Тур	Max	Unit		
M		′AC	2.0	5.0	6.0	Ň	
V _{CC}	Supply Voltage	'ACT	4.5	5.0	5.5	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)		0	-	V _{CC}	V	
	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	-	150	-	ns/V	
t. t.		V _{CC} @ 4.5 V	-	40	-		
		V _{CC} @ 5.5 V	-	25	_		
	Input Rise and Fall Time (Note 2)	V _{CC} @ 4.5 V	-	10	-		
t _r , t _f	'ACT Devices except Schmitt Inputs	V _{CC} @ 5.5 V	-	8.0	-	ns/V	
TJ	Junction Temperature (PDIP)		_	_	140	°C	
T _A	Operating Ambient Temperature Range		-40	25	85	°C	
I _{OH}	Output Current – High		-	_	-24	mA	
I _{OL}	Output Current – Low		-	_	24	mA	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times. 2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

					74AC		74AC	
						+25°C	T _A = –40°C to +85°C	
Symbol	Parameter	Con	ditions	V _{CC} (V)	Тур	Guar	anteed Limits	Unit
V _{IH}	Minimum High Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	/	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V
V _{IL}	Maximum Low Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	/	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V
V _{OH}	Minimum High Level Output Voltage	I _{OUT} = -50 μA		3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V
		V _{IN} = V _{IL} or V _I I _{OH}	_H (Note 3) –12 mA –24 mA –24 mA	3.0 4.5 5.5	_ _ _	2.56 3.86 4.86	2.46 3.76 4.76	v
V _{OL}	Maximum Low Level Output Voltage	V _{IN} = V _{IL} or V _I	_H (Note 3) 12 mA 24 mA 24 mA	3.0 4.5 5.5	_ _ _	0.36 0.36 0.36	0.44 0.44 0.44	V
I _{IN}	Maximum Input Leakage Current	V _I = V _{CC} , GNI)	5.5	-	±0.1	±1.0	μΑ
I _{OLD}	Minimum Dynamic (Note 4)	V _{OLD} = 1.65 V	' Max	5.5	-	-	75	mA
I _{OHD}	Output Current	V _{OHD} = 3.85 \	/ Min	5.5	-	-	-75	mA
I _{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or (GND	5.5	-	4.0	40	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

3. All outputs loaded; thresholds on input associated with output under test.

4. Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS

				74AC		74	AC		
		V _{CC} (V)	-	₄ = +25° _L = 50 p		to +	-40°C 85°C 50 pF		Fig.
Symbol	Parameter	(Note5)	Min	Тур	Max	Min	Max	Unit	No.
t _{PLH}	Propagation Delay	3.3 5.0	1.5 1.5	7.5 5.5	9.5 7.5	1.0 1.0	10.0 8.5	ns	3–5
t _{PHL}	Propagation Delay	3.3 5.0	1.5 1.5	7.0 5.5	8.5 7.0	1.0 1.0	9.0 7.5	ns	3–5

5. Voltage Range 3.3 V is 3.3 V ±0.3 V. Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

					74ACT		74ACT	
				v _{cc}	T _A = +25°C		T _A = −40°C to +85°C	
Symbol	Parameter	Conditio	ons	(V)	Тур	Guar	anteed Limits	Unit
V _{IH}	Minimum High Level	V _{OUT} = 0.1 V		4.5	1.5	2.0	2.0	V
Input Voltage	or V _{CC} – 0.1 V		5.5	1.5	2.0	2.0	v	
V _{IL}	Maximum Low Level	V _{OUT} = 0.1 V		4.5	1.5	0.8	0.8	V
Input Voltage	Input Voltage	or V _{CC} – 0.1 V		5.5	1.5	0.8	0.8	v
V _{OH}	Minimum High Level	I _{OUT} = -50 μA		4.5	4.49	4.4	4.4	V
	Output Voltage			5.5	5.49	5.4	5.4	v
		$V_{IN} = V_{IL} \text{ or } V_{IH}$ (N	lote 6)					V
			–24 mA	4.5	-	3.86	3.76	
			–24 mA	5.5	-	4.86	4.76	
V _{OL}	Maximum Low Level	I _{OUT} = 50 μA		4.5	0.001	0.1	0.1	V
	Output Voltage			5.5	0.001	0.1	0.1	V
		$V_{IN} = V_{IL} \text{ or } V_{IH}$ (N	lote 6)					V
			24 mA	4.5	-	0.36	0.44	
			24 mA	5.5	-	0.36	0.44	
I _{IN}	Maximum Input Leakage Current	$V_{I} = V_{CC}, \text{ GND}$		5.5	-	±0.1	±1.0	μΑ
ΔI_{CCT}	Additional Max. I _{CC} /Input	$V_{I} = V_{CC} - 2.1 V$		5.5	0.6	-	1.5	mA
I _{OLD}	Minimum Dynamic (Note 7)	V _{OLD} = 1.65 V Ma	х	5.5	-	-	75	mA
I _{OHD}	Output Current	V _{OHD} = 3.85 V Min	า	5.5	-	-	-75	mA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND		5.5	-	4.0	40	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. All outputs loaded; thresholds on input associated with output under test.
7. Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS

				74ACT		74A	СТ		
		V _{CC} (V)		₄ = +25° ∟ = 50 p		T _A = - to +8 C _L = \$	35°C		Fig.
Symbol	Parameter	(Note 8)	Min	Тур	Max	Min	Max	Unit	No.
t _{PLH}	Propagation Delay	5.0	1.0	-	9.0	1.0	10.0	ns	3–5
t _{PHL}	Propagation Delay	5.0	1.0	-	9.0	1.0	10.0	ns	3–5

8. Voltage Range 5.0 V is 5.0 V ± 0.5 V.

CAPACITANCE

Symbol	Parameter	Test Conditions	Value Typ	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.0 V	4.5	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 5.0 V	20	pF

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74AC08DG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74AC08DR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74AC08DTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
MC74ACT08DG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74ACT08DR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74ACT08DTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SOIC-14 NB CASE 751A-03 ISSUE K



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP-14 CASE 948G **ISSUE B**



NOTES:

- NOTES:
 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION. SHALL NOT EXCEED 0.25
- OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- (0.010) FER SIDE. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION, ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION. TERMINIA UNIMERS ARE SHOWN FOR 5.
- TERMINAL NUMBERS ARE SHOWN FOR 6.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE W–.

	MILLIMETERS		INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
Н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
κ	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40		0.252 BSC		
Μ	0 °	8 °	0 °	8 °	



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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