



# MC34129 MC33129

## High Performance Current Mode Controllers

The MC34129/MC33129 are high performance current mode switching regulators specifically designed for use in low power digital telephone applications. These integrated circuits feature a unique internal fault timer that provides automatic restart for overload recovery. For enhanced system efficiency, a start/run comparator is included to implement bootstrapped operation of  $V_{CC}$ . Other functions contained are a temperature compensated reference, reference amplifier, fully accessible error amplifier, sawtooth oscillator with sync input, pulse width modulator comparator, and a high current totem pole driver ideally suited for driving a power MOSFET.

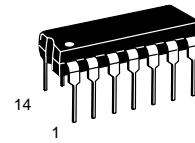
Also included are protective features consisting of soft-start, undervoltage lockout, cycle-by-cycle current limiting, adjustable deadtime, and a latch for single pulse metering.

Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in many other applications.

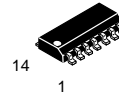
- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-by-Cycle Current Limiting
- Continuous Retry after Fault Timeout
- Soft-Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- High Current Totem Pole Driver
- Input Undervoltage Lockout
- Low Startup and Operating Current
- Direct Interface with Motorola SENSEFET Products

### HIGH PERFORMANCE CURRENT MODE CONTROLLERS

#### SEMICONDUCTOR TECHNICAL DATA

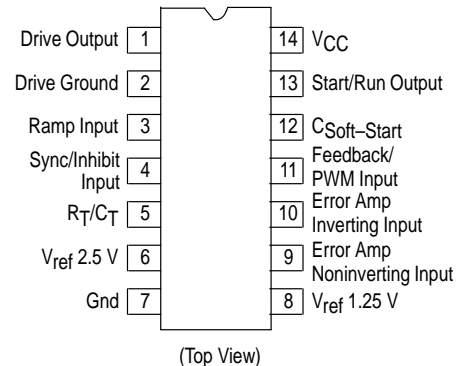


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 646

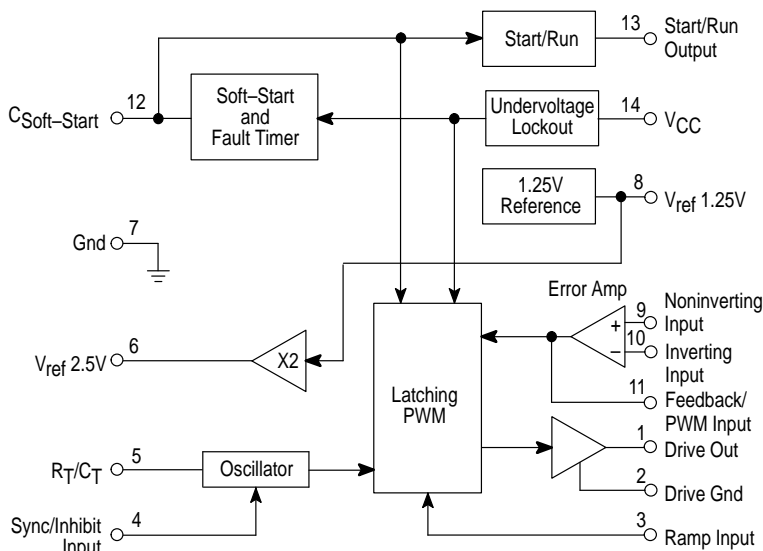


**D SUFFIX**  
PLASTIC PACKAGE  
CASE 751A  
(SO-14)

#### PIN CONNECTIONS



#### Simplified Block Diagram



#### ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34129D	$T_A = 0^\circ \text{ to } +70^\circ \text{C}$	SO-14
MC34129P		Plastic DIP
MC33129D	$T_A = -40^\circ \text{ to } +85^\circ \text{C}$	SO-14
MC33129P		Plastic DIP

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V <sub>CC</sub> Zener Current	I <sub>Z(VCC)</sub>	50	mA
Start/Run Output Zener Current	I <sub>Z(Start/Run)</sub>	50	mA
Analog Inputs (Pins 3, 5, 9, 10, 11, 12)	–	–0.3 to 5.5	V
Sync Input Voltage	V <sub>sync</sub>	–0.3 to V <sub>CC</sub>	V
Drive Output Current, Source or Sink	I <sub>DRV</sub>	1.0	A
Current, Reference Outputs (Pins 6, 8)	I <sub>ref</sub>	20	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Case 751A Maximum Power Dissipation @ T <sub>A</sub> = 70°C Thermal Resistance, Junction-to-Air	P <sub>D</sub> R <sub>θJA</sub>	552 145	mW °C/W
P Suffix, Plastic Package Case 646 Maximum Power Dissipation @ T <sub>A</sub> = 70°C Thermal Resistance, Junction-to-Air	P <sub>D</sub> R <sub>θJA</sub>	800 100	mW °C/W
Operating Junction Temperature	T <sub>J</sub>	+150	°C
Operating Ambient Temperature MC34129 MC33129	T <sub>A</sub>	0 to +70 –40 to +85	°C
Storage Temperature Range	T <sub>stg</sub>	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 10 V, T<sub>A</sub> = 25°C [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
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## REFERENCE SECTIONS

Reference Output Voltage, T <sub>A</sub> = 25°C 1.25 V Ref., I <sub>L</sub> = 0 mA 2.50 V Ref., I <sub>L</sub> = 1.0 mA	V <sub>ref</sub>	1.225 2.375	1.250 2.500	1.275 2.625	V
Reference Output Voltage, T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub> 1.25 V Ref., I <sub>L</sub> = 0 mA 2.50 V Ref., I <sub>L</sub> = 1.0 mA	V <sub>ref</sub>	1.200 2.250	– –	1.300 2.750	V
Line Regulation (V <sub>CC</sub> = 4.0 V to 12 V) 1.25 V Ref., I <sub>L</sub> = 0 mA 2.50 V Ref., I <sub>L</sub> = 1.0 mA	Reg <sub>line</sub>	– –	2.0 10	12 50	mV
Load Regulation 1.25 V Ref., I <sub>L</sub> = –10 μA to +500 μA 2.50 V Ref., I <sub>L</sub> = –0.1 mA to +1.0 mA	Reg <sub>load</sub>	– –	1.0 3.0	12 25	mV

## ERROR AMPLIFIER

Input Offset Voltage (V <sub>in</sub> = 1.25 V) T <sub>A</sub> = 25°C T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub>	V <sub>IO</sub>	– –	1.5 –	– 10	mV
Input Offset Current (V <sub>in</sub> = 1.25 V)	I <sub>IO</sub>	–	10	–	nA
Input Bias Current (V <sub>in</sub> = 1.25 V) T <sub>A</sub> = 25°C T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub>	I <sub>IB</sub>	– –	25 –	– 200	nA
Input Common Mode Voltage Range	V <sub>ICR</sub>	–	0.5 to 5.5	–	V
Open Loop Voltage Gain (V <sub>O</sub> = 1.25 V)	A <sub>VOL</sub>	65	87	–	dB
Gain Bandwidth Product (V <sub>O</sub> = 1.25 V, f = 100 kHz)	GBW	500	750	–	kHz
Power Supply Rejection Ratio (V <sub>CC</sub> = 5.0 V to 10 V)	PSRR	65	85	–	dB
Output Source Current (V <sub>O</sub> = 1.5 V)	I <sub>Source</sub>	40	80	–	μA
Output Voltage Swing High State (I <sub>Source</sub> = 0 μA) Low State (I <sub>Sink</sub> = 500 μA)	V <sub>OH</sub> V <sub>OL</sub>	1.75 –	1.96 0.1	2.25 0.15	V

NOTE: 1. T<sub>low</sub> = 0°C for MC34129  
–40°C for MC33129

T<sub>high</sub> = +70°C for MC34129  
+85°C for MC33129

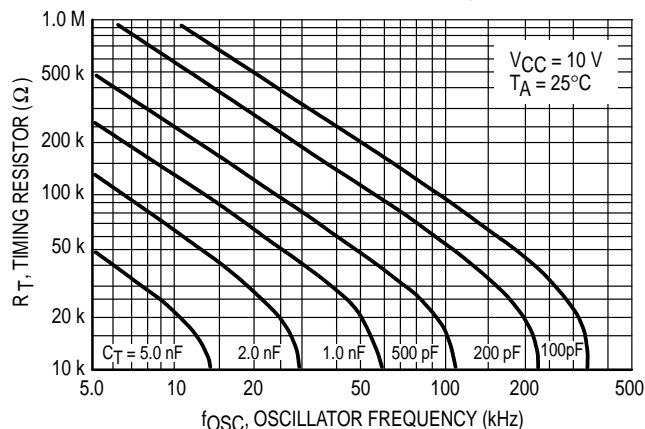
## ELECTRICAL CHARACTERISTICS ( $V_{CC} = 10\text{ V}$ , $T_A = 25^\circ\text{C}$ [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
<b>PWM COMPARATOR</b>					
Input Offset Voltage ( $V_{in} = 1.25\text{ V}$ )	$V_{IO}$	150	275	400	mV
Input Bias Current	$I_{IB}$	–	–120	–250	$\mu\text{A}$
Propagation Delay, Ramp Input to Drive Output	$t_{PLH(IN/DRV)}$	–	250	–	ns
<b>SOFT-START</b>					
Capacitor Charge Current (Pin 12 = 0 V)	$I_{chg}$	0.75	1.2	1.50	$\mu\text{A}$
Buffer Input Offset Voltage ( $V_{in} = 1.25\text{ V}$ )	$V_{IO}$	–	15	40	mV
Buffer Output Voltage ( $I_{Sink} = 100\text{ }\mu\text{A}$ )	$V_{OL}$	–	0.15	0.225	V
<b>FAULT TIMER</b>					
Restart Delay Time	$t_{DLY}$	200	400	600	$\mu\text{s}$
<b>START/RUN COMPARATOR</b>					
Threshold Voltage (Pin 12)	$V_{th}$	–	2.0	–	V
Threshold Hysteresis Voltage (Pin 12)	$V_H$	–	350	–	mV
Output Voltage ( $I_{Sink} = 500\text{ }\mu\text{A}$ )	$V_{OL}$	9.0	10	10.3	V
Output Off-State Leakage Current ( $V_{OH} = 15\text{ V}$ )	$I_{S/R(leak)}$	–	0.4	2.0	$\mu\text{A}$
Output Zener Voltage ( $I_Z = 10\text{ mA}$ )	$V_Z$	–	( $V_{CC} + 7.6$ )	–	V
<b>OSCILLATOR</b>					
Frequency ( $R_T = 25.5\text{ k}\Omega$ , $C_T = 390\text{ pF}$ )	$f_{OSC}$	80	100	120	kHz
Capacitor $C_T$ Discharge Current (Pin 5 = 1.2 V)	$I_{dischg}$	240	350	460	$\mu\text{A}$
Sync Input Current High State ( $V_{in} = 2.0\text{ V}$ ) Low State ( $V_{in} = 0.8\text{ V}$ )	$I_{IH}$ $I_{IL}$	– –	40 15	125 35	$\mu\text{A}$
Sync Input Resistance	$R_{in}$	12.5	32	50	$\text{k}\Omega$
<b>DRIVE OUTPUT</b>					
Output Voltage High State ( $I_{Source} = 200\text{ mA}$ ) Low State ( $I_{Source} = 200\text{ mA}$ )	$V_{OH}$ $V_{OL}$	8.3 –	8.9 1.4	– 1.8	V
Low State Holding Current	$I_H$	–	225	–	$\mu\text{A}$
Output Voltage Rise Time ( $C_L = 500\text{ pF}$ )	$t_r$	–	390	–	ns
Output Voltage Fall Time ( $C_L = 500\text{ pF}$ )	$t_f$	–	30	–	ns
Output Pull-Down Resistance	$R_{PD}$	100	225	350	$\text{k}\Omega$
<b>UNDERVOLTAGE LOCKOUT</b>					
Startup Threshold	$V_{th}$	3.0	3.6	4.2	V
Hysteresis	$V_H$	5.0	10	15	%
<b>TOTAL DEVICE</b>					
Power Supply Current $R_T = 25.5\text{ k}\Omega$ , $C_T = 390\text{ pF}$ , $C_L = 500\text{ pF}$	$I_{CC}$	1.0	2.5	4.0	mA
Power Supply Zener Voltage ( $I_Z = 10\text{ mA}$ )	$V_Z$	12	14.3	–	V

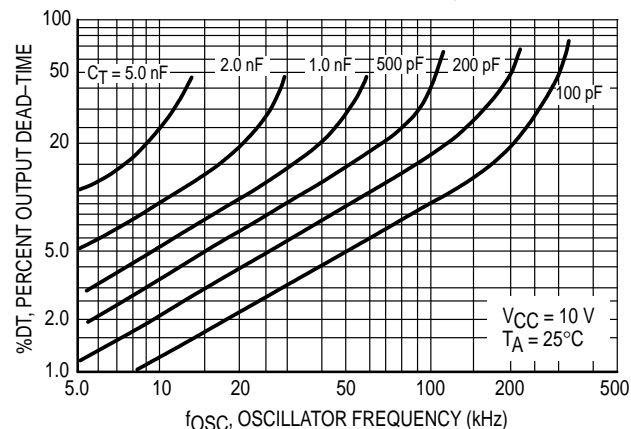
**NOTE:** 1.  $T_{low} = 0^\circ\text{C}$  for MC34129  
–40°C for MC33129

$T_{high} = +70^\circ\text{C}$  for MC34129  
+85°C for MC33129

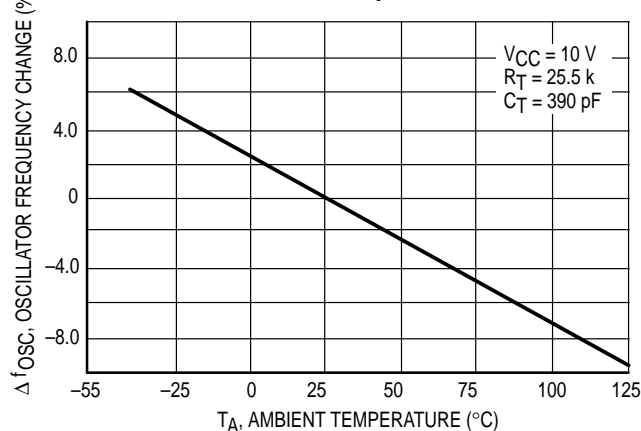
**Figure 1. Timing Resistor versus Oscillator Frequency**



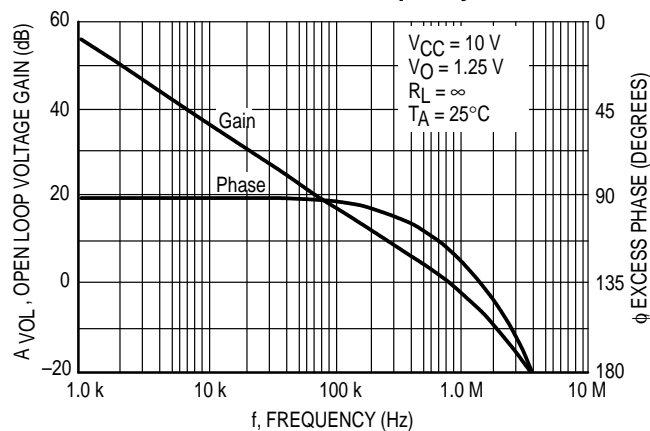
**Figure 2. Output Deadtime versus Oscillator Frequency**



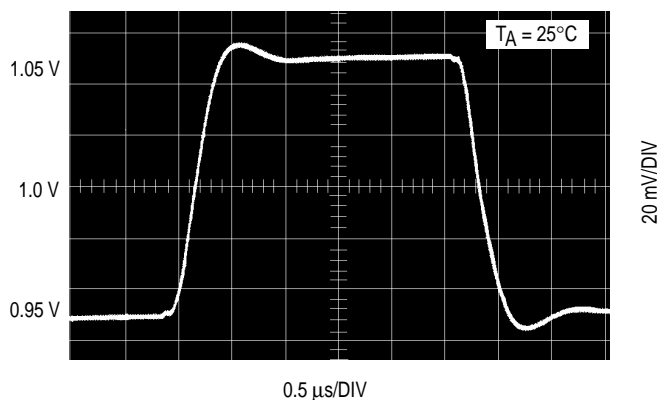
**Figure 3. Oscillator Frequency Change versus Temperature**



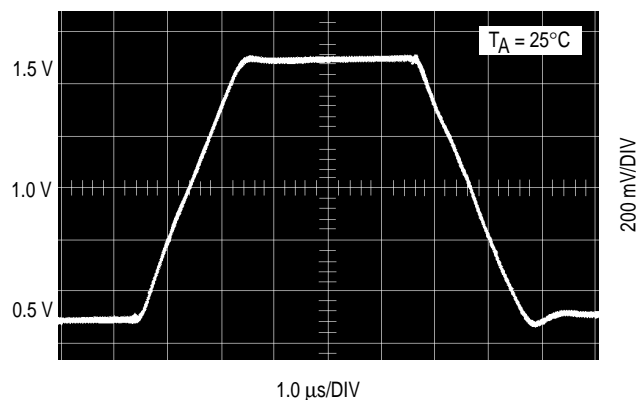
**Figure 4. Error Amp Open Loop Gain and Phase versus Frequency**



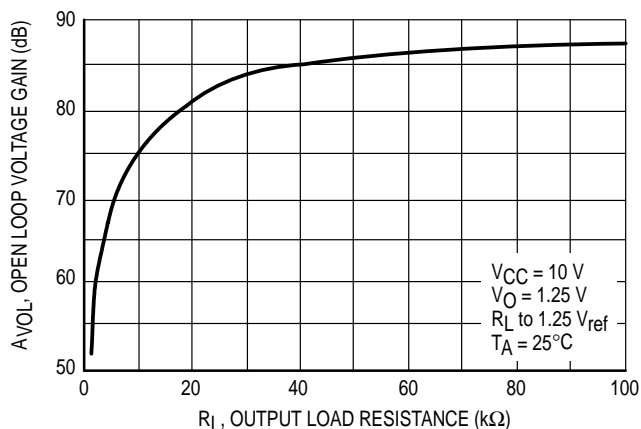
**Figure 5. Error Amp Small-Signal Transient Response**



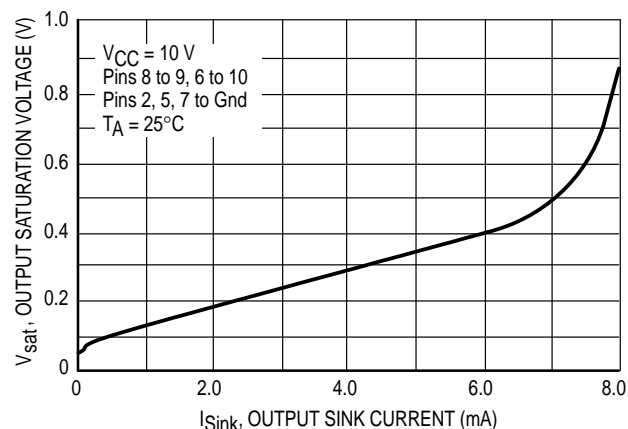
**Figure 6. Error Amp Large-Signal Transient Response**



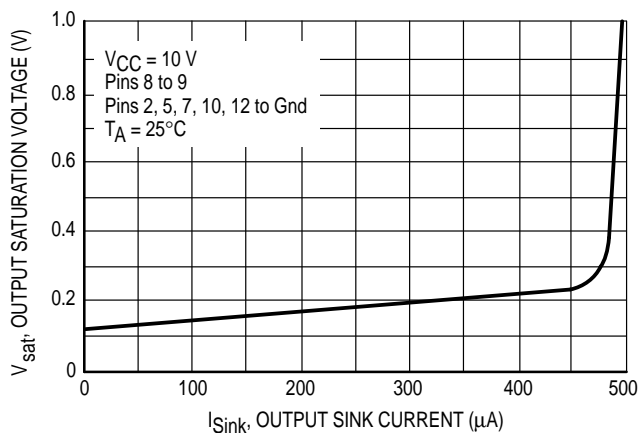
**Figure 7. Error Amp Open Loop DC Gain versus Load Resistance**



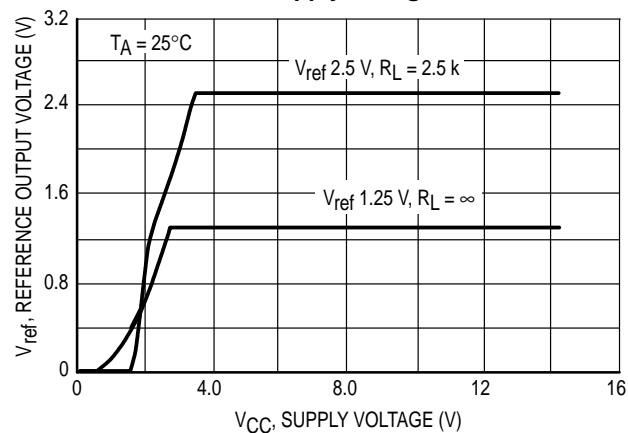
**Figure 8. Error Amp Output Saturation versus Sink Current**



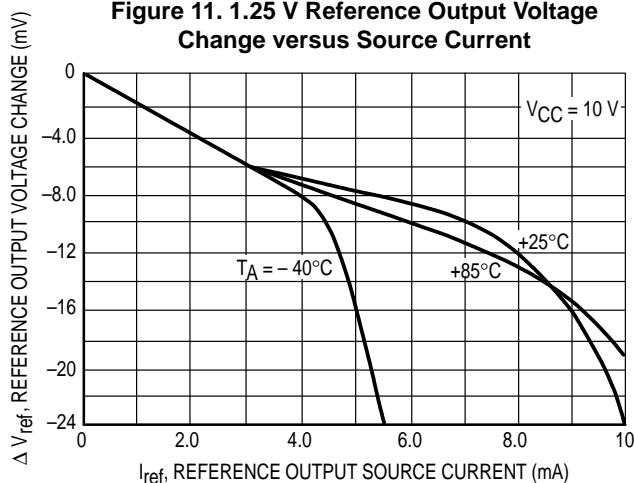
**Figure 9. Soft-Start Buffer Output Saturation versus Sink Current**



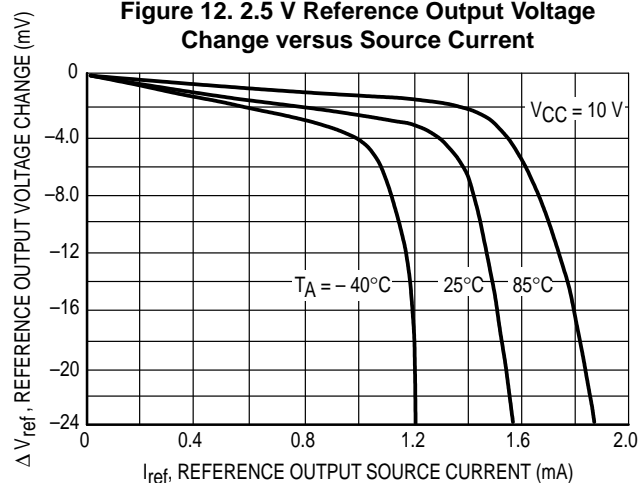
**Figure 10. Reference Output Voltage versus Supply Voltage**



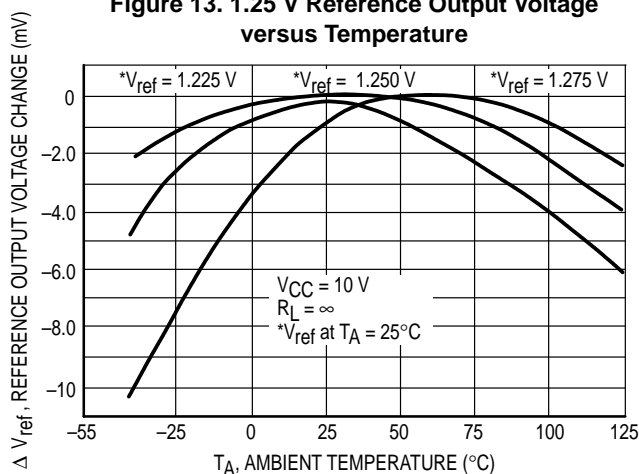
**Figure 11. 1.25 V Reference Output Voltage Change versus Source Current**



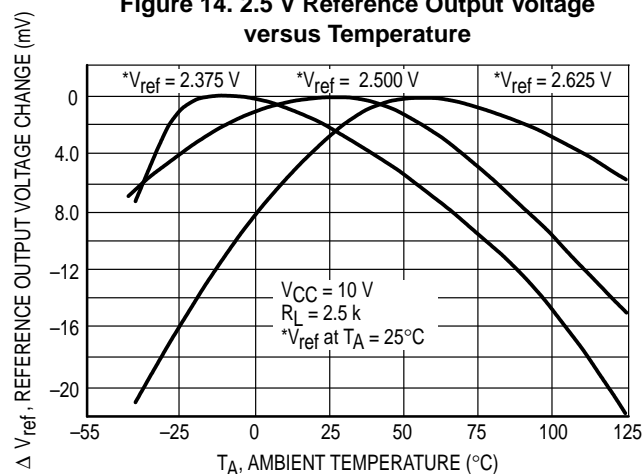
**Figure 12. 2.5 V Reference Output Voltage Change versus Source Current**



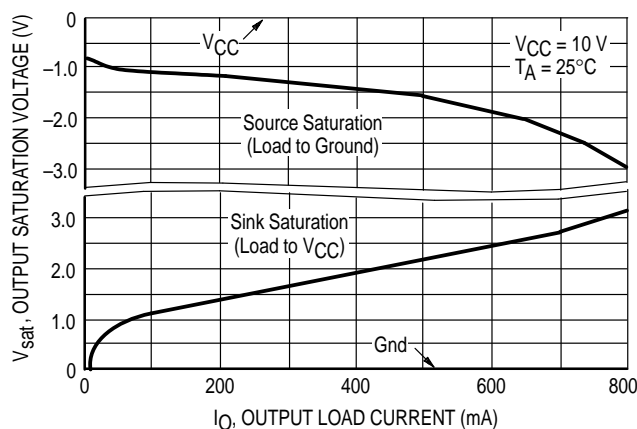
**Figure 13. 1.25 V Reference Output Voltage versus Temperature**



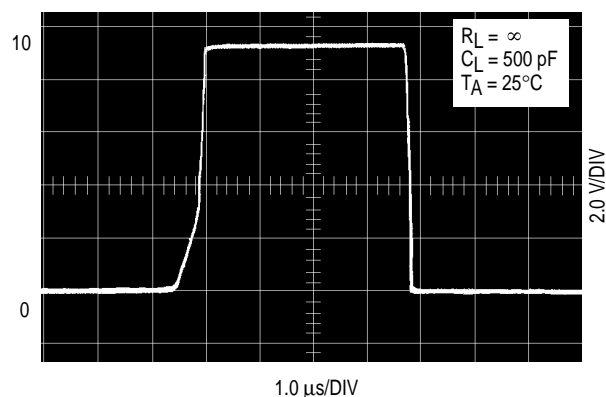
**Figure 14. 2.5 V Reference Output Voltage versus Temperature**



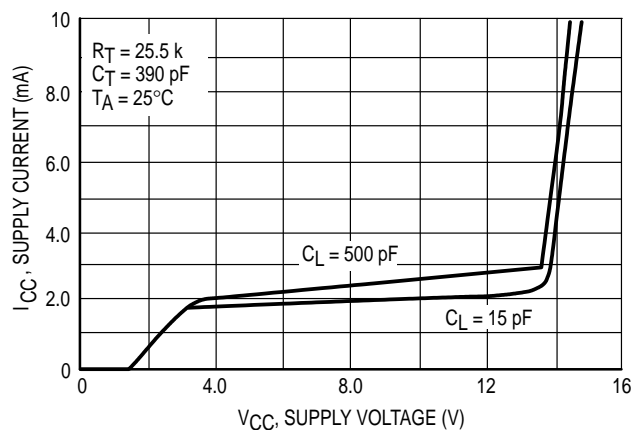
**Figure 15. Drive Output Saturation versus Load Current**



**Figure 16. Drive Output Waveform**



**Figure 17. Supply Current versus Supply Voltage**



## PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Drive Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
2	Drive Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
3	Ramp Input	A voltage proportional to the inductor current is connected to this input. The PWM uses this information to terminate output switch conduction.
4	Sync/Inhibit Input	A rectangular waveform applied to this input will synchronize the Oscillator and limit the maximum Drive Output duty cycle. A dc voltage within the range of 2.0 V to $V_{CC}$ will inhibit the controller.
5	$R_T/C_T$	The free-running Oscillator frequency and maximum Drive Output duty cycle are programmed by connecting resistor $R_T$ to $V_{ref}$ 2.5 V and capacitor $C_T$ to Ground. Operation to 300 kHz is possible.
6	$V_{ref}$ 2.50 V	This output is derived from $V_{ref}$ 1.25 V. It provides charging current for capacitor $C_T$ through resistor $R_T$ .
7	Ground	This pin is the control circuitry ground return and is connected back to the source ground.
8	$V_{ref}$ 1.25 V	This output furnishes a voltage reference for the Error Amplifier noninverting input.
9	Error Amp Noninverting Input	This is the noninverting input of the Error Amplifier. It is normally connected to the 1.25 V reference.
10	Error Amp Inverting Input	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
11	Feedback/PWM Input	This pin is available for loop compensation. It is connected to the Error Amplifier and Soft-Start Buffer outputs, and the Pulse Width Modulator input.
12	$C_{Soft-Start}$	A capacitor $C_{Soft-Start}$ is connected from this pin to Ground for a controlled ramp-up of peak inductor current during startup.
13	Start/Run Output	This output controls the state of an external bootstrap transistor. During the start mode, operating bias is supplied by the transistor from $V_{in}$ . In the run mode, the transistor is switched off and bias is supplied by an auxiliary power transformer winding.
14	$V_{CC}$	This pin is the positive supply of the control IC. The controller is functional over a minimum $V_{CC}$ range of 4.2 V to 12 V.

**Freescale Semiconductor, Inc.**

## Oscillator

## PWM Comparator and Latch

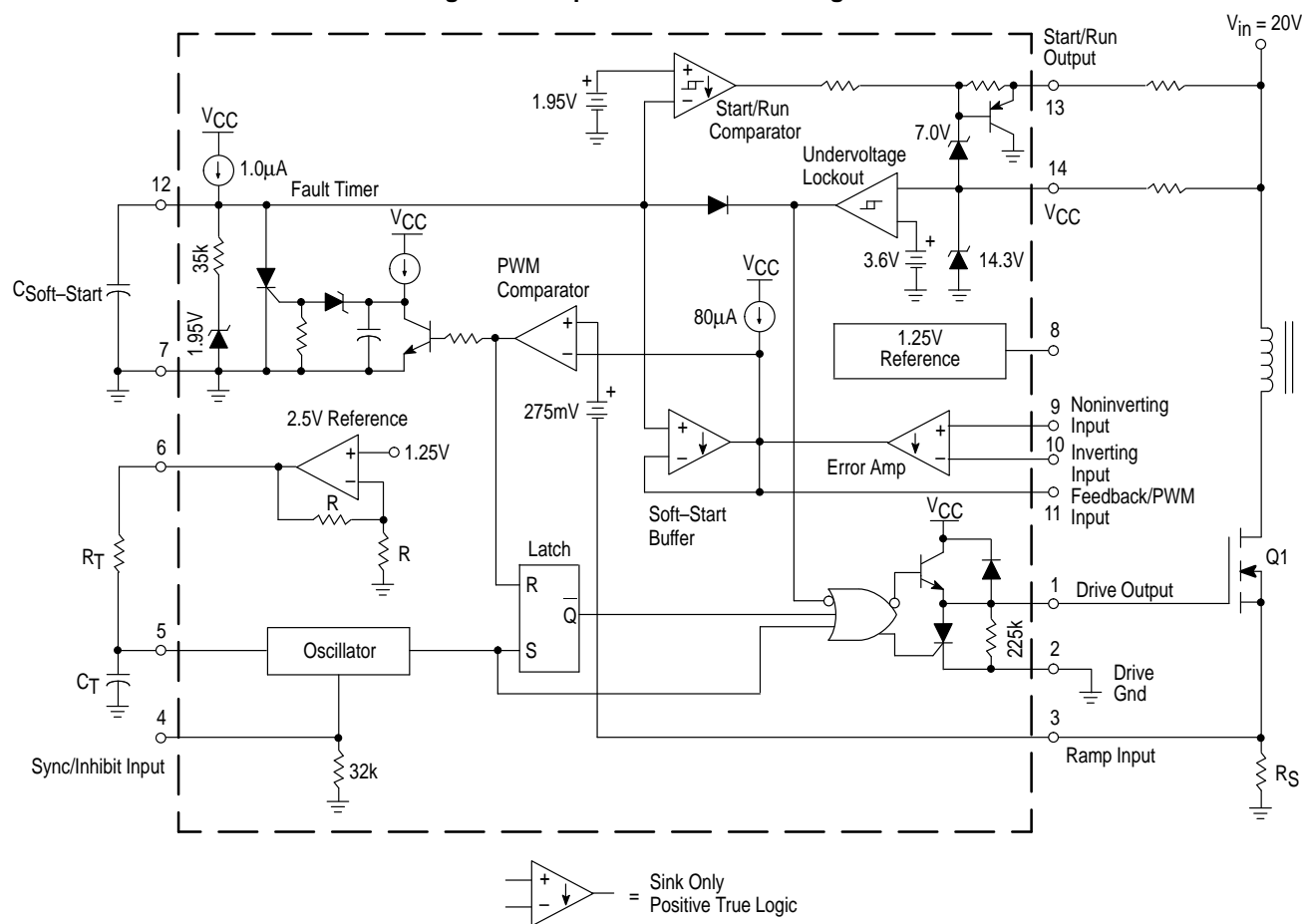
$$I_{pk} = \frac{V_{(Pin\ 11)} - 0.275\ V}{R_S}$$
$$I_{pk(max)} = \frac{1.95 \text{ V} - 0.275}{R_S} = \frac{1.675 \text{ V}}{R_S}$$

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Ramp Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 25.

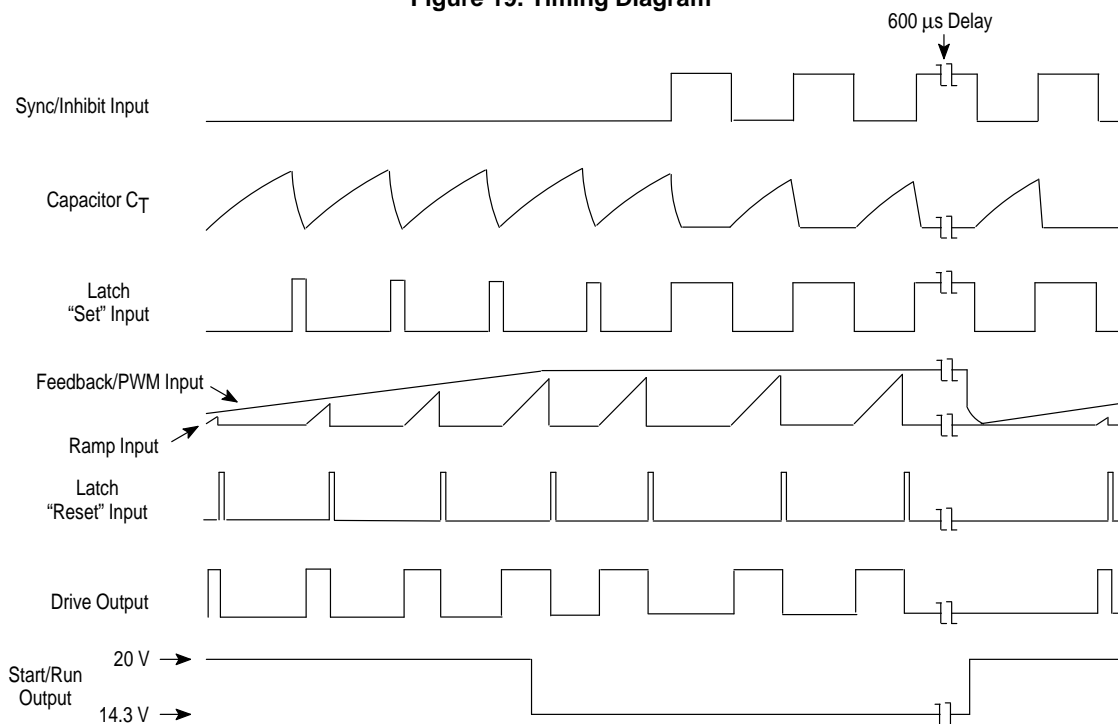
A fully-compensated Error Amplifier with access to both inputs and output is provided for maximum design flexibility. The Error Amplifier output is common with that of the Soft-Start Buffer. These outputs are open-collector (sink only) and are ORed together at the inverting input of the PWM Comparator. With this configuration, the amplifier that demands lower peak inductor current dominates control of the loop. Soft-Start is mandatory for stable startup when power is provided through a high source impedance such as the long twisted pair used in telecommunications. It effectively removes the load from the output of the switching power supply upon initial startup. The Soft-Start Buffer is configured as a unity gain follower with the noninverting input connected to Pin 12. An internal 1.0  $\mu\text{A}$  current source charges the soft-start capacitor ( $C_{\text{Soft-Start}}$ ) to an internally clamped level of 1.95 V. The rate of change of peak inductor current, during startup, is programmed by the capacitor value selected. Either the Fault Timer or the Undervoltage Lockout can discharge the soft-start capacitor.



**Figure 18. Representative Block Diagram**



**Figure 19. Timing Diagram**



## Fault Timer

This unique circuit prevents sustained operating in a lockout condition. This can occur with conventional switching control ICs when operating from a power source with a high series impedance. If the power required by the load is greater than that available from the source, the input voltage will collapse, causing the lockout condition. The Fault Timer provides automatic recovery when this condition is detected. Under normal operating conditions, the output of the PWM Comparator will reset the Latch and discharge the internal Fault Timer capacitor on a cycle-by-cycle basis. Under operating conditions where the required power into the load is greater than that available from the source ( $V_{in}$ ), the Ramp Input voltage (plus offset) will not reach the comparator threshold level (Pin 11), and the output of the PWM Comparator will remain low. If this condition persists for more than 600  $\mu$ s, the Fault Timer will activate, discharging  $C_{Soft-Start}$  and initiating a soft-start cycle. The power supply will operate in a skip cycle or hiccup mode until either the load power or source impedance is reduced. The minimum fault timeout is 200  $\mu$ s, which limits the useful switching frequency to a minimum of 5.0 kHz.

## Start/Run Comparator

A bootstrap startup circuit is included to improve system efficiency when operating from a high input voltage. The output of the Start/Run Comparator controls the state of an external transistor. A typical application is shown in Figure 21. While  $C_{Soft-Start}$  is charging, startup bias is supplied to  $V_{CC}$  (Pin 14) from  $V_{in}$  through transistor Q2. When  $C_{Soft-Start}$  reaches the 1.95 V clamp level, the Start-Run output switches low ( $V_{CC} = 50$  mV), turning off Q2. Operating bias is now derived from the auxiliary bootstrap winding of the transformer, and all drive power is efficiently converted down from  $V_{in}$ . The start time must be long enough for the power supply output to reach regulation. This will ensure that there is sufficient bias voltage at the auxiliary bootstrap winding for sustained operation.

$$t_{Start} = \frac{1.95VC_{Soft-Start}}{1.0 \mu A} = 1.95 C_{Soft-Start} \text{ in } \mu F$$

The Start/Run Comparator has 350 mV of hysteresis. The output off-state is clamped to  $V_{CC} + 7.6$  V by the internal zener and PNP transistor base-emitter junction.

## Drive Output and Drive Ground

The MC34129 contains a single totem-pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to  $\pm 1.0$  A peak drive current and has a typical fall time of 30 ns with a 500 pF load. The totem-pole stage consists of an NPN transistor for turn-on drive and a high speed SCR for turn-off. The SCR design requires less average supply current ( $I_{CC}$ ) when compared to conventional switching control ICs that use an all NPN totem-pole. The SCR accomplishes this during turn-off of the MOSFET, by utilizing the gate charge as regenerative on-bias, whereas the conventional all transistor design requires continuous base current. Conversion efficiency in low power applications is greatly enhanced with this reduction of  $I_{CC}$ . The SCR's low-state holding current ( $I_H$ ) is typically 225  $\mu$ A. An internal 225 k $\Omega$  pull-down resistor is included to shunt the Drive Output off-state leakage to ground when the Undervoltage Lockout is active. A separate Drive Ground is provided to reduce the effects of switching transient noise imposed on the Ramp Input. This feature becomes particularly useful when the  $I_{pk(max)}$  clamp level is reduced. Figure 24 shows the proper implementation of the MC34129 with a current sensing power MOSFET.

## Undervoltage Lockout

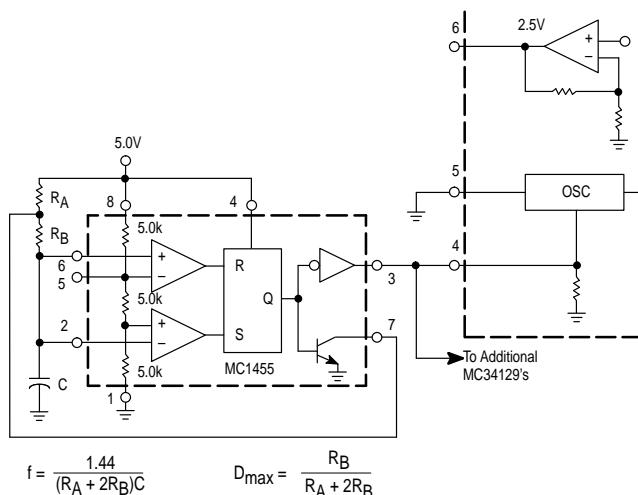
The Undervoltage Lockout comparator holds the Drive Output and  $C_{Soft-Start}$  pins in the low state when  $V_{CC}$  is less than 3.6 V. This ensures that the MC34129 is fully functional before the output stage is enabled and a soft-start cycle begins. A built-in hysteresis of 350 mV prevents erratic output behavior as  $V_{CC}$  crosses the comparator threshold voltage. A 14.3 V zener is connected as a shunt regulator from  $V_{CC}$  to ground. Its purpose is to protect the MOSFET gate from excessive drive voltage during system startup. An external 9.1 V zener is required when driving low threshold MOSFETs. Refer to Figure 21. The minimum operating voltage range of the IC is 4.2 V to 12 V.

## References

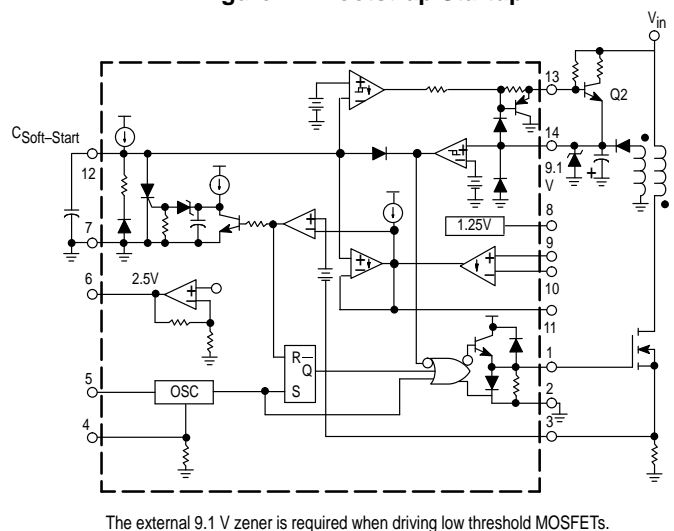
The 1.25 V bandgap reference is trimmed to  $\pm 2.0\%$  tolerance at  $T_A = 25^\circ\text{C}$ . It is intended to be used in conjunction with the Error Amp. The 2.50 V reference is derived from the 1.25 V reference by an internal op amp with a fixed gain of 2.0. It has an output tolerance of  $\pm 5.0\%$  at  $T_A = 25^\circ\text{C}$  and its primary purpose is to supply charging current to the oscillator timing capacitor.

**For further information, please refer to AN976.**

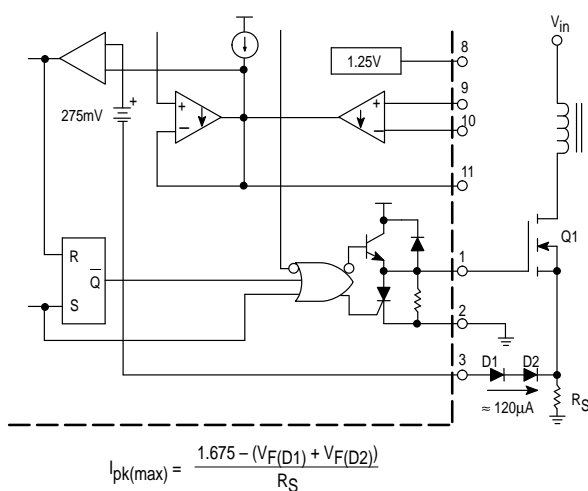
**Figure 20. External Duty Cycle Clamp and Multi-Unit Synchronization**



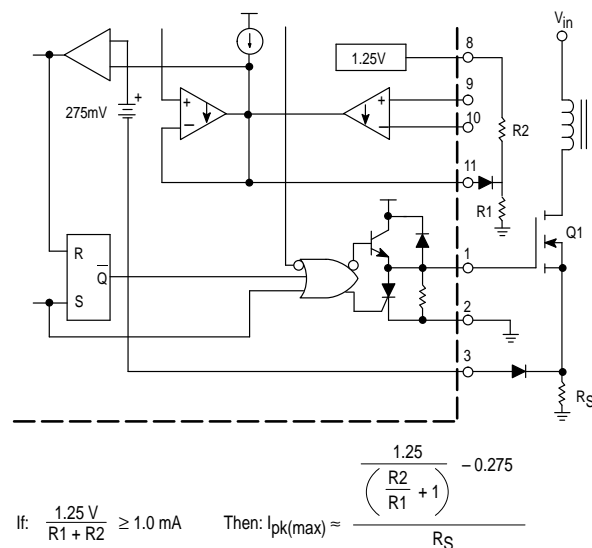
**Figure 21. Bootstrap Startup**



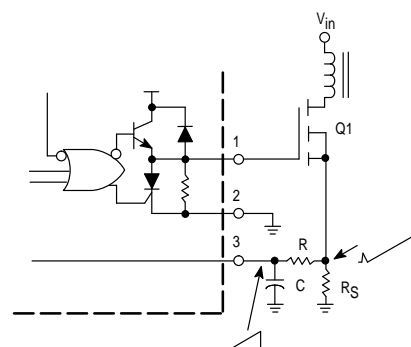
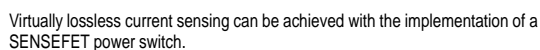
**Figure 22. Discrete Step Reduction of Clamp Level**



**Figure 23. Adjustable Reduction of Clamp Level**

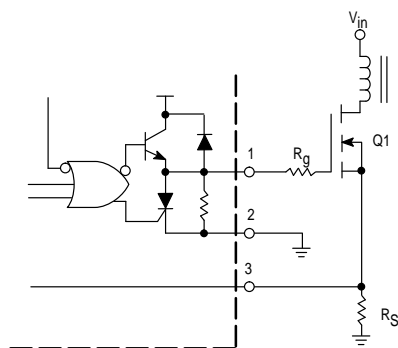


### Figure 25. Current Waveform Spike Suppression

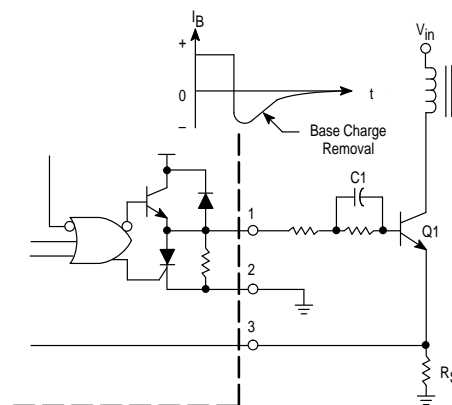


The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

### Figure 27. Bipolar Transistor Drive

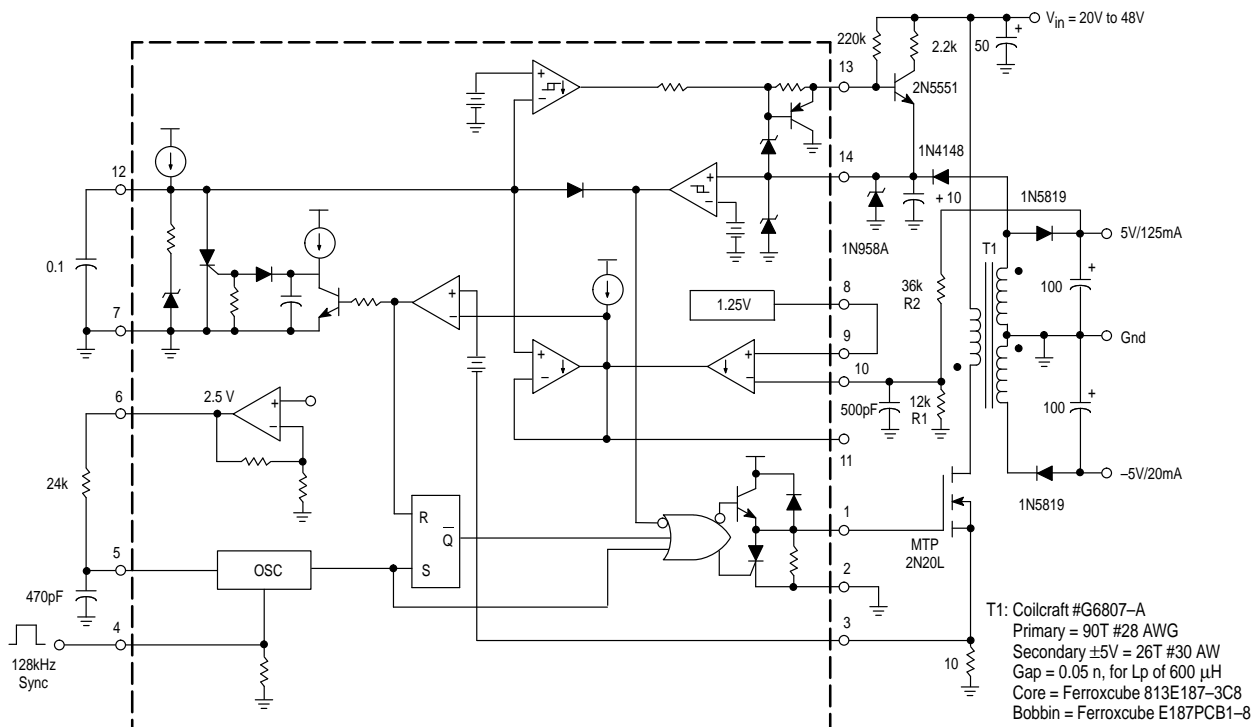


Series gate resistor  $R_g$  will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C1.

**Figure 28. Non-Isolated 725 mW Flyback Regulator**



Test	Conditions	Results
Line Regulation 5.0 V	$V_{in} = 20 \text{ V to } 40 \text{ V}$ , $I_{out} 5.0 \text{ V} = 125 \text{ mA}$ , $I_{out} -5.0 \text{ V} = 20 \text{ mA}$	$\Delta = 1.0 \text{ mV}$
Load Regulation 5.0 V	$V_{in} = 30 \text{ V}$ , $I_{out} 5.0 \text{ V} = 0 \text{ mA to } 150 \text{ mA}$ , $I_{out} -5.0 \text{ V} = 20 \text{ mA}$	$\Delta = 2.0 \text{ mV}$
Output Ripple 5.0 V	$V_{in} = 30 \text{ V}$ , $I_{out} 5.0 \text{ V} = 125 \text{ mA}$ , $I_{out} -5.0 \text{ V} = 20 \text{ mA}$	150 mVpp
Efficiency	$V_{in} = 30 \text{ V}$ , $I_{out} 5.0 \text{ V} = 125 \text{ mA}$ , $I_{out} -5.0 \text{ V} = 20 \text{ mA}$	77%

$$V_{out} = 1.25 \left( \frac{R2}{R1} + 1 \right)$$

128kHz Sync

0.1 2.7k

6 4 5

10k

MOS5007

24k

470pF

100pF

2.5V

2.2k

1.25V

2N5551

1N5819

180pF

140k

20k

330

T1

1N5819

5V/380mA

Gnd

-5V/20mA

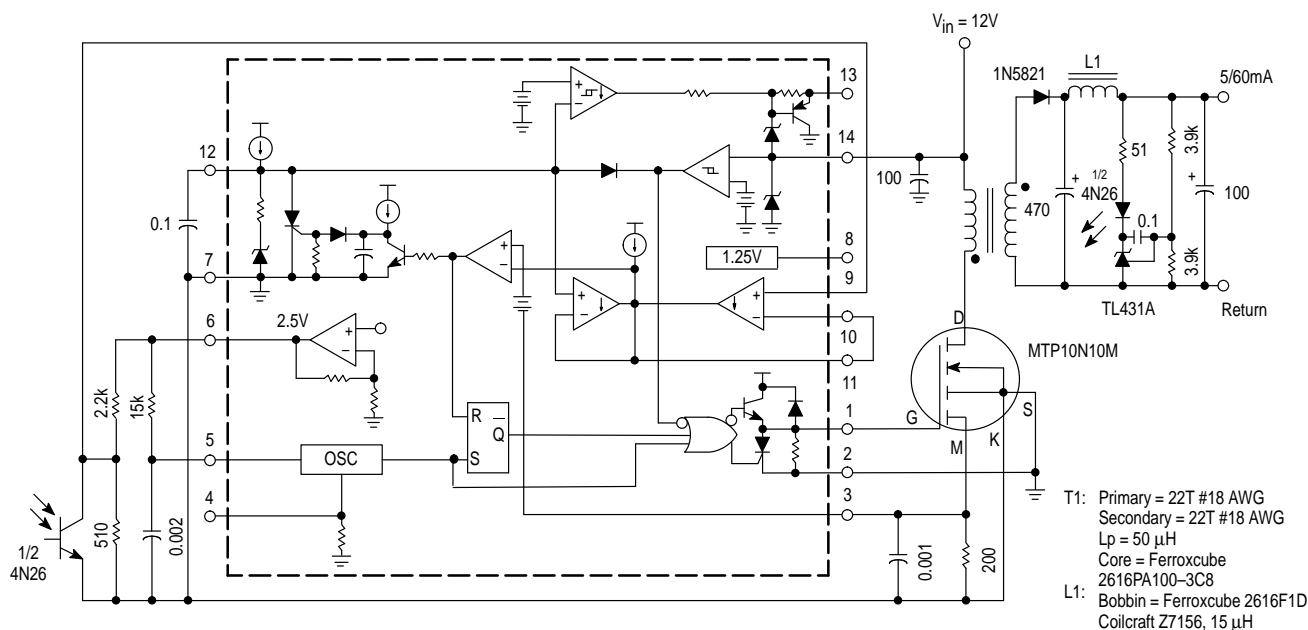
MTP 2N20

$V_{in} = 20V \text{ to } 48V$

T1: Primary = 35T #32 AWG  
 Feedback = 12T #32 AWG  
 Secondary  $\pm 5V = 7T \#32 \text{ AWG}$   
 Gap = 0.004", for  $L_p$  of 180  $\mu H$   
 Core = Ferroxcube 813E187-3C8  
 Bobbin = Ferroxcube E187PCB1-8

Test	Conditions	Results
Line Regulation 5.0 V	$V_{in} = 20\text{ V to } 40\text{ V}$ , $I_{out} 5.0\text{ V} = 380\text{ mA}$ , $I_{out} -5.0\text{ V} = 20\text{ mA}$	$\Delta = 1.0\text{ mV}$
Load Regulation 5.0 V	$V_{in} = 30\text{ V}$ , $I_{out} 5.0\text{ V} = 100\text{ mA to } 380\text{ mA}$ , $I_{out} -5.0\text{ V} = 20\text{ mA}$	$\Delta = 15\text{ mV}$
Output Ripple 5.0 V	$V_{in} = 30\text{ V}$ , $I_{out} 5.0\text{ V} = 380\text{ mA}$ , $I_{out} -5.0\text{ V} = 20\text{ mA}$	150 mVpp
Efficiency	$V_{in} = 30\text{ V}$ , $I_{out} 5.0\text{ V} = 380\text{ mA}$ , $I_{out} -5.0\text{ V} = 20\text{ mA}$	73%

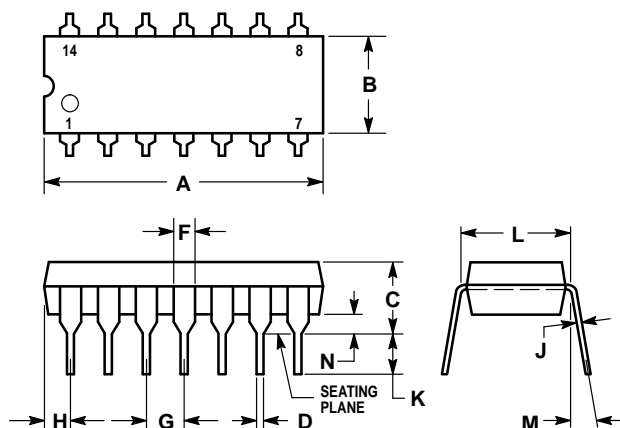
**Figure 30. Isolated 3.0 W Flyback Regulator with Secondary Side Sensing**



Test	Conditions	Results
Line Regulation	$V_{in} = 8.0 \text{ V to } 12 \text{ V}$ , $I_{out} = 600 \text{ mA}$	$\Delta = 1.0 \text{ mV}$
Load Regulation	$V_{in} = 12 \text{ V}$ , $I_{out} = 100 \text{ mA to } 600 \text{ mA}$	$\Delta = 8.0 \text{ mV}$
Output Ripple	$V_{in} = 12 \text{ V}$ , $I_{out} = 600 \text{ mA}$	20 mVpp
Efficiency	$V_{in} = 12 \text{ V}$ , $I_{out} = 600 \text{ mA}$	81%

An economical method of achieving secondary sensing is to combine the TL431A with a 4N26 optocoupler.

**P SUFFIX**  
PLASTIC PACKAGE  
CASE 646-06  
ISSUE L

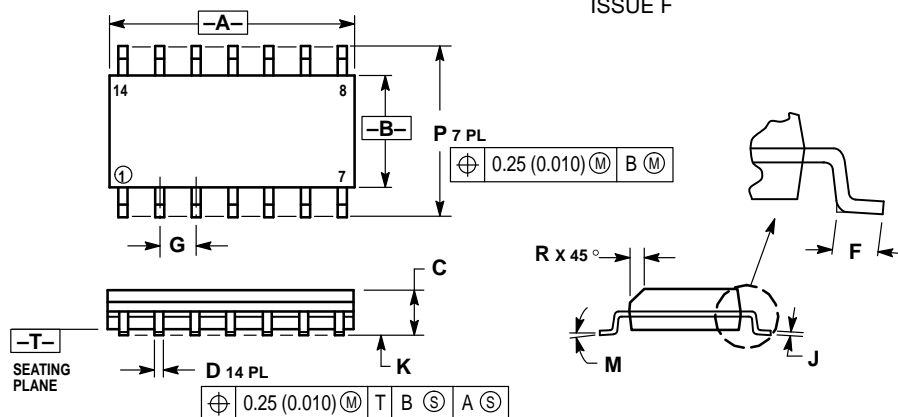


NOTES:

1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01


**D SUFFIX**  
PLASTIC PACKAGE  
CASE 751A-03  
(SO-14)  
ISSUE F



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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