RELIABILITY REPORT

FOR

**MAX803SEXR**

PLASTIC ENCAPSULATED DEVICES

August 3, 2006

# MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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**Conclusion**

The MAX803 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

**Table of Contents**



## I. Device Description

A. General

The MAX803 is a microprocessor (µP) supervisory circuit used to monitor the power supplies in µP and digital systems. It provides excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5V, +3.3V, +3.0V, or +2.5V powered circuits.

This circuit performs a single function: it asserts a reset signal whenever the $V_{CC}$ supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after $V_{CC}$ has risen above the reset threshold. Reset thresholds suitable for operation with a variety of supply voltages are available.

The MAX803 has an open-drain output stage. The MAX803's open-drain RESET-bar output requires a pull-up resistor that can be connected to a voltage higher than $V_{CC}$. The MAX803 has an active-low RESET-bar output. The reset comparator is designed to ignore fast transients on $V_{CC}$, and the outputs are guaranteed to be in the correct logic state for $V_{CC}$ down to 1V.

Low supply current makes the MAX803 ideal for use in portable equipment. The MAX803 is available in a 3-pin SC70 package.

B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| Terminal Voltage (with respect to GND) | |
| VCC | -0.3V to +6.0V |
| RESET, RESET (push-pull) | -0.3V to (VCC + 0.3V) |
| RESET (open drain) | -0.3V to +6.0V |
| Input Current, VCC | 20mA |
| Output Current, RESET, RESET | 20mA |
| Rate of Rise, VCC | 100V/µs |
| Continuous Power Dissipation (TA = +70°C) | |
| 3-Pin SC70 (derate 2.17mW/°C above +70°C) | 174mW |
| 3-Pin SOT23 (derate 4mW/°C above +70°C) | 320mW |
| Operating Temperature Range | |
| 3-Pin SC70 | -40°C to +125°C |
| 3-Pin SOT23 | -40°C to +105°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | 3-Pin Microprocessor Reset Circuits |
| B. Process: | B8 (Standard 0.8 micron silicon gate CMOS) |
| C. Number of Device Transistors: | 380 |
| D. Fabrication Location: | California, USA |
| E. Assembly Location: | Malaysia |
| F. Date of Initial Production: | January, 2000 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | **3-Pin SC70-3** |
| B. Lead Frame: | Alloy 42 |
| C. Lead Finish: | Solder Plate or 100% Matte Tin |
| D. Die Attach: | Nonconductive Epoxy |
| E. Bondwire: | Gold (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | # 05-1601-0082 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: | Level 1 |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 30 x 30 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Si (Si = 1%) |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 0.8 microns (as drawn) |
| F. Minimum Metal Spacing: | 0.8 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 160 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 6.87 \times 10^{-9}$

$\lambda$ = 6.87 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. #06-5033) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT rate of 0.17 @ 25°C and 2.92 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The MS42 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

**Table 1**
Reliability Evaluation Test Results

**MAX803SEXR**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 160 | 0 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | SC70 | 77 | 0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters<br>& functionality | | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

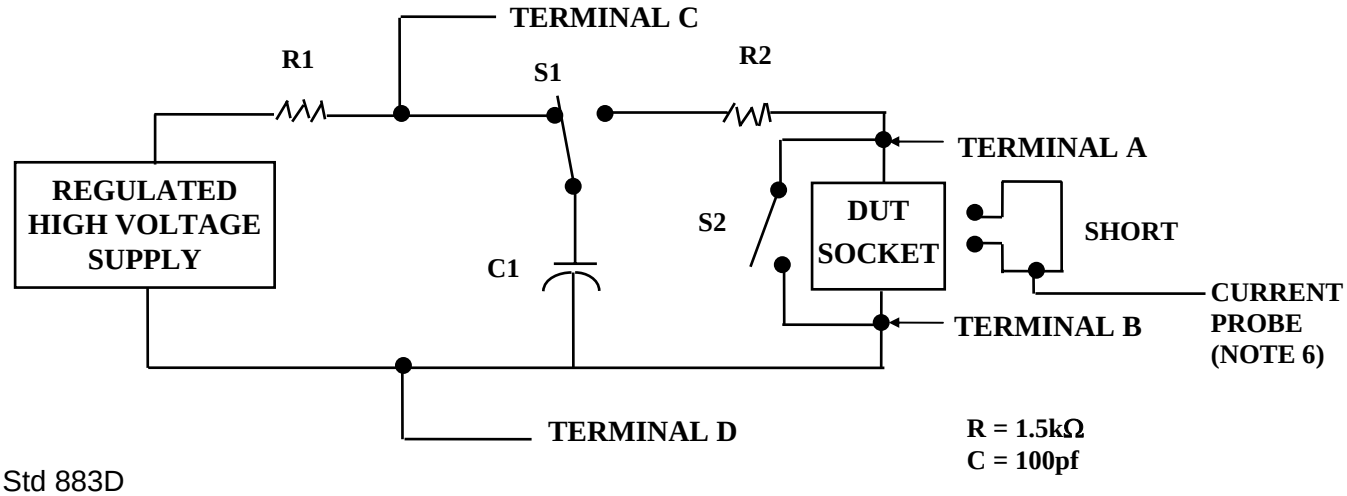
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

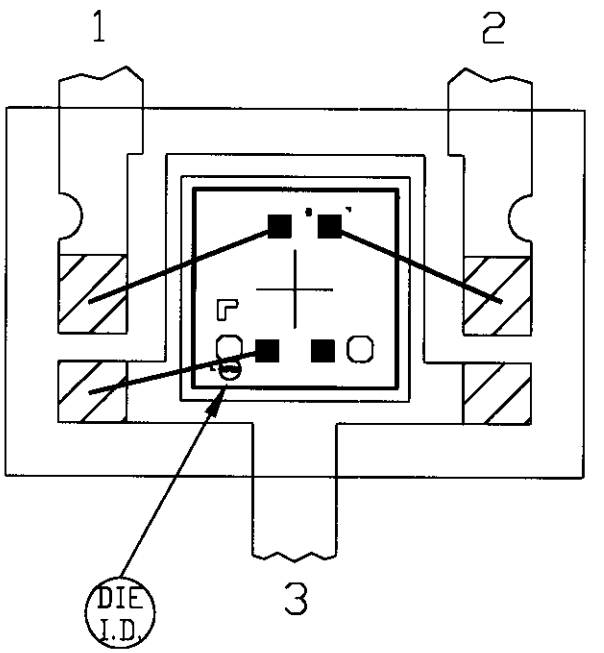
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.






SCALE: 40x

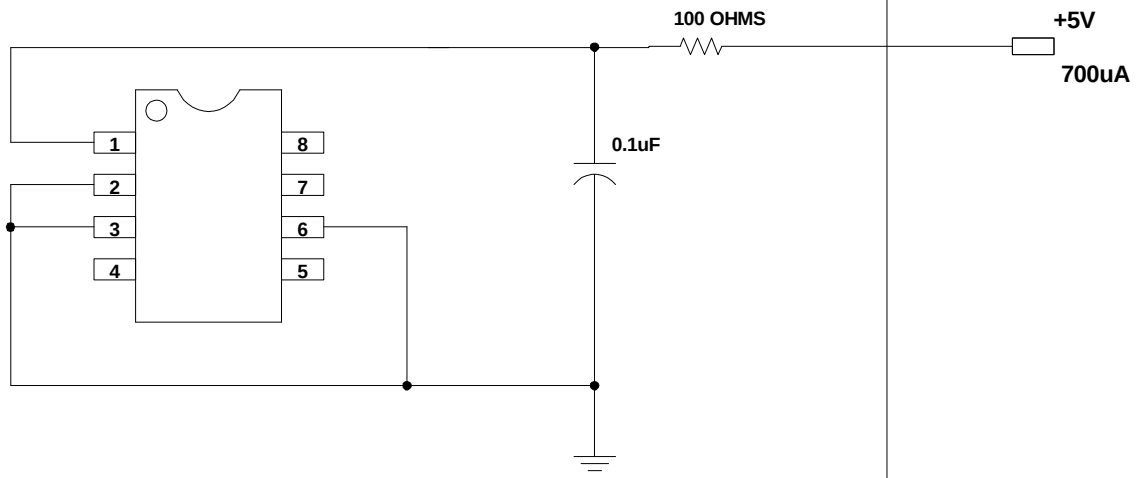
CAVITY DOWN

BONDABLE AREA

| | | | | |
|---|---|---|---|---|
| PKG.CODE: X3-2 | | APPROVALS | DATE | MAXIM |
| CAV./PAD SIZE: 34x35 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-1601-0082 / REV.: A |

ONCE PER SOCKET

ONCE PER BOARD




**8-DIP**

| | |
|---|---|
| **DEVICES: MAX 941/809/810/823/824/825/803<br>MAX 6381/6835<br>MAX. EXPECTED CURRENT = 700uA AND 15uA** | NOTES: 15 uA FOR MAX 6381 |