19-3685; Rev 1; 6/09

Low-Cost, Crystal-Based, Programmable, ASK/FSK Transceiver with Fractional-N PLL

MAX7032

General Description

The MAX7032 crystal-based, fractional-N transceiver is designed to transmit and receive ASK/OOK or FSK data in the 300MHz to 450MHz frequency range with data rates up to 33kbps (Manchester encoded) or 66kbps (NRZ encoded). This device generates a typical output power of +10dBm into a 50Ω load, and exhibits typical sensitivities of -114dBm for ASK data and -110dBm for FSK data. The MAX7032 features separate transmit and receive pins (PAOUT and LNAIN) and provides an internal RF switch that can be used to connect the transmit and receive pins to a common antenna.

The MAX7032 transmit frequency is generated by a 16-bit, fractional-N, phase-locked loop (PLL), while the receiver's local oscillator (LO) is generated by an integer-N PLL. This hybrid architecture eliminates the need for separate transmit and receive crystal reference oscillators because the fractional-N PLL allows the transmit frequency to be set within 2kHz of the receive frequency. The 12-bit resolution of the fractional-N PLL allows frequency multiplication of the crystal frequency in steps of f_{XTAL} / 4096. Retaining the fixed-N PLL for the receiver avoids the higher current drain requirements of a fractional-N PLL and keeps the receiver current drain as low as possible.

The fractional-N architecture of the MAX7032 transmit PLL allows the transmit FSK signal to be programmed for exact frequency deviations, and completely eliminates the problems associated with oscillator-pulling FSK signal generation. All frequency-generation components are integrated on-chip, and only a crystal, a 10.7MHz IF filter, and a few discrete components are required to implement a complete antenna/digital data solution.

The MAX7032 is available in a small 5mm x 5mm, 32-pin, thin QFN package, and is specified to operate in the automotive -40°C to +125°C temperature range.

Applications

2-Way Remote Keyless Entry

Security Systems

Home Automation

Remote Controls

Remote Sensing

Smoke Alarms

Garage Door Openers

Local Telemetry Systems

Features

- **+2.1V to +3.6V or +4.5V to +5.5V Single-Supply Operation**
- **Single Crystal Transceiver**
- **User-Adjustable 300MHz to 450MHz Carrier Frequency**
- **ASK/OOK and FSK Modulation**
- **User-Adjustable FSK Frequency Deviation Through Fractional-N PLL Register**
- **Agile Transmitter Frequency Synthesizer with f_{XTAL} / 4096 Carrier-Frequency Spacing**
- **+10dBm Output Power into 50Ω Load**
- **Integrated TX/RX Switch**
- **Integrated Transmit and Receive PLL, VCO, and Loop Filter**
- **> 45dB Image Rejection**
- **Typical RF Sensitivity***
  - **ASK: -114dBm**
  - **FSK: -110dBm**
- **Selectable IF Bandwidth with External Filter**
- **RSSI Output with High Dynamic Range**
- **Autopolling Low-Power Management**
- **< 12.5mA Transmit-Mode Current**
- **< 6.7mA Receive-Mode Current**
- **< 23.5µA Polling-Mode Current**
- **< 800nA Shutdown Current**
- **Fast-On Startup Feature, < 250µs**
- **Small 32-Pin, Thin QFN Package**

**0.2% BER, 4kbps Manchester-encoded data, 280kHz IF BW, average RF power*

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7032ATJ	-40°C to +125°C	32 Thin QFN-EP**

***EP = Exposed pad.*

Pin Configuration, Typical Application Circuit, and Functional Diagram appear at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

HV_{IN} to GND..-0.3V to +6.0V
PAV_{DD}, AV_{DD}, DV_{DD} to GND................................-0.3V to +4.0V
ENABLE, T/$\overline{R}$, DATA, $\overline{CS}$, DIO, SCLK, CLKOUT to
GND ....-0.3V to (HV_{IN} + 0.3V)
All Other Pins to GND..............................-0.3V to (_V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
32-Pin Thin QFN (derate 21.3mW/°C above +70°C)....1702mW
Operating Temperature Range ....-40°C to +125°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, 50Ω system impedance, AV_{DD} = DV_{DD} = P_{AVDD} = HV_{IN} = +2.1V to +3.6V, f_{RF} = 300MHz to 450MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at AV_{DD} = DV_{DD} = PAV_{DD} = HV_{IN} = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (3V Mode)	V_{DD}	HV_{IN}, PAV_{DD}, AV_{DD}, and DV_{DD} connected to power supply		2.1	2.7	3.6	V
Supply Voltage (5V Mode)	HV_{IN}	PAV_{DD}, AV_{DD}, and DV_{DD} unconnected from HV_{IN}, but connected together		4.5	5.0	5.5	V
Supply Current	I_{DD}	Transmit mode, PA off, V_{DATA} at 0% duty cycle (ASK) (Note 2)	f_{RF} = 315MHz		3.5	5.4	mA
			f_{RF} = 434MHz		4.3	6.7	mA
		Transmit mode, V_{DATA} at 50% duty cycle (ASK) (Notes 3, 4)	f_{RF} = 315MHz		7.6	12.3	mA
			f_{RF} = 434MHz		8.4	13.6	mA
		Transmit mode, V_{DATA} at 100% duty cycle (FSK)	f_{RF} = 315MHz (Note 4)		11.6	19.1	mA
			f_{RF} = 434MHz (Note 2)		12.4	20.4	mA
		T_A < +85°C, typ at +25°C (Note 4)	Receiver (ASK 315MHz)		6.1	7.9	mA
			Receiver (ASK 434MHz)		6.4	8.3	mA
			Receiver (FSK 315MHz)		6.4	8.4	mA
			Receiver (FSK 434MHz)		6.7	8.7	mA
			DRX (3V mode)		23.4	77.3	µA
			DRX (5V mode)		67.2	94.4	µA
			Deep-sleep (3V mode)		0.8	8.8	µA
			Deep-sleep (5V mode)		2.4	10.9	µA
		T_A < +125°C typ at +125°C (Note 2)	Receiver (ASK 315MHz)		6.4	8.2	mA
			Receiver (ASK 434MHz)		6.7	8.4	mA
			Receiver (FSK 315MHz)		6.8	8.7	mA
			Receiver (FSK 434MHz)		7.0	8.8	mA
			DRX (3V mode)		33.5	103.0	µA
			DRX (5V mode)		82.3	116.1	µA
			Deep-sleep (3V mode)		8.0	34.2	µA
			Deep-sleep (5V mode)		14.9	39.3	µA
Voltage Regulator	V_{REG}	HV_{IN} = 5V, I_{LOAD} = 15mA			3.0		V

DC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, 50Ω system impedance, AV_{DD} = DV_{DD} = P_{AVDD} = HV_{IN} = +2.1V to +3.6V, f_{RF} = 300MHz to 450MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at AV_{DD} = DV_{DD} = PAV_{DD} = HV_{IN} = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL I/O						
Input High Threshold	V_{IH}	(Note 2)	0.9 x HV_{IN}			V
Input Low Threshold	V_{IL}	(Note 2)			0.1 x HV_{IN}	V
Pulldown Sink Current		SCLK, ENABLE, T/$\overline{R}$, DATA (HV_{IN} = 5.5V)		20		µA
Pullup Source Current		DIO, $\overline{CS}$ (HV_{IN} = 5.5V)		20		µA
Output-Low Voltage	V_{OL}	I_{SINK} = 500µA		0.15		V
Output-High Voltage	V_{OH}	I_{SOURCE} = 500µA		HV_{IN} - 0.26		V

AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, 50Ω system impedance, AV_{DD} = DV_{DD} = PAV_{DD} = HV_{IN} = +2.1V to +3.6V, f_{RF} = 300MHz to 450MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at PAV_{DD} = AV_{DD} = DV_{DD} = HV_{IN} = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Frequency Range				300		450	MHz
Maximum Input Level	P_{RFIN}				0		dBm
Transmit Efficiency 100% Duty Cycle		f_{RF} = 315MHz (Note 6)			32		%
		f_{RF} = 434MHz (Note 6)			30		
Transmit Efficiency 50% Duty Cycle		f_{RF} = 315MHz (Note 6)			24		%
		f_{RF} = 434MHz (Note 6)			22		
Power-On Time	t_{ON}	ENABLE or T/$\overline{R}$ transition low to high, transmitter frequency settled to within 50kHz of the desired carrier			200		µs
		ENABLE or T/$\overline{R}$ transition low to high, transmitter frequency settled to within 5kHz of the desired carrier			350		
		ENABLE transition low to high, or T/$\overline{R}$ transition high to low receiver startup time (Note 5)			250		
RECEIVER							
Sensitivity		0.2% BER, 4kbps Manchester data rate, 280kHz IF BW, ±50kHz FSK deviation, average power	ASK (315MHz)		-114		dBm
			ASK (434MHz)		-113		
			FSK (315MHz)		-110		
			FSK (434MHz)		-107		
Image Rejection		(Note 8)			46		dB

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AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, 50Ω system impedance, $AV_{DD} = DV_{DD} = PAV_{DD} = HV_{IN}$ = +2.1V to +3.6V, f_{RF} = 300MHz to 450MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at $PAV_{DD} = AV_{DD} = DV_{DD} = HV_{IN}$ = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER AMPLIFIER							
Output Power	P_{OUT}	T_A = +25°C (Note 4)		4.6	10.0	15.5	dBm
		T_A = +125°C, $AV_{DD} = DV_{DD} = HV_{IN} = PAV_{DD}$ = +2.1V (Note 2)		3.9	6.7		
		T_A = -40°C, $AV_{DD} = DV_{DD} = HV_{IN} = PAV_{DD}$ = +3.6V (Note 4)			13.1	15.8	
Modulation Depth					82		dB
Maximum Carrier Harmonics		With output-matching network			-40		dBc
Reference Spur					-50		dBc
PHASE-LOCKED LOOP							
Transmit VCO Gain	K_{VCO}				340		MHz/V
Transmit PLL Phase Noise		10kHz offset, 200kHz loop BW			-68		dBc/Hz
		1MHz offset, 200kHz loop BW			-98		
Receive VCO Gain					340		MHz/V
Receive PLL Phase Noise		10kHz offset, 500kHz loop BW			-80		dBc/Hz
		1MHz offset, 500kHz loop BW			-90		
Loop Bandwidth		Transmit PLL			200		kHz
		Receive PLL			500		
Minimum Transmit Frequency Step					f_{XTAL} / 4096		kHz
Reference Frequency Input Level					0.5		V_{P-P}
Programmable Divider Range		In transmit mode (Note 4)		20		27	
LOW-NOISE AMPLIFIER/MIXER (Note 9)							
LNA Input Impedance	Z_{INLNA}	Normalized to 50Ω	f_{RF} = 315MHz		1 - j4.7		
			f_{RF} = 434MHz		1 - j3.3		
Voltage-Conversion Gain		High-gain state	f_{RF} = 315MHz		50		dB
			f_{RF} = 434MHz		45		
		Low-gain state	f_{RF} = 315MHz		13		
			f_{RF} = 434MHz		9		
Input-Referred 3rd-Order Intercept Point	IIP3	High-gain state			-42		dBm
		Low-gain state			-6		
Mixer Output Impedance					330		Ω
LO Signal Feedthrough to Antenna					-100		dBm
RSSI							
Input Impedance					330		Ω
Operating Frequency	f_{IF}				10.7		MHz
3dB Bandwidth					10		MHz

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, 50Ω system impedance, $AV_{DD} = DV_{DD} = PAV_{DD} = HV_{IN}$ = +2.1V to +3.6V, f_{RF} = 300MHz to 450MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at $PAV_{DD} = AV_{DD} = DV_{DD} = HV_{IN}$ = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain				15		mV/dB
FSK DEMODULATOR						
Conversion Gain				2.0		mV/kHz
ANALOG BASEBAND						
Maximum Data Filter Bandwidth				50		kHz
Maximum Data Slicer Bandwidth				100		kHz
Maximum Peak Detector Bandwidth				50		kHz
Maximum Data Rate		Manchester coded		33		kbps
		NRZ		66		
CRYSTAL OSCILLATOR						
Crystal Frequency	f_{XTAL}			$(f_{RF}$ - 10.7) / 24		MHz
Maximum Crystal Inductance				50		mH
Frequency Pulling by V_{DD}				2		ppm/V
Crystal Load Capacitance		(Note 7)		4.5		pF
SERIAL INTERFACE TIMING CHARACTERISTICS (see Figure 7)						
Minimum SCLK Setup to Falling Edge of $\overline{CS}$	t_{SC}			30		ns
Minimum $\overline{CS}$ Falling Edge to SCLK Rising-Edge Setup Time	t_{CSS}			30		ns
Minimum $\overline{CS}$ Idle Time	t_{CSI}			125		ns
Minimum $\overline{CS}$ Period	t_{CS}			2.125		µs
Maximum SCLK Falling Edge to Data Valid Delay	t_{DO}			80		ns
Minimum Data Valid to SCLK Rising-Edge Setup Time	t_{DS}			30		ns
Minimum Data Valid to SCLK Rising-Edge Hold Time	t_{DH}			30		ns
Minimum SCLK High Pulse Width	t_{CH}			100		ns
Minimum SCLK Low Pulse Width	t_{CL}			100		ns
Minimum $\overline{CS}$ Rising Edge to SCLK Rising-Edge Hold Time	t_{CSH}			30		ns
Maximum $\overline{CS}$ Falling Edge to Output Enable Time	t_{DV}			25		ns
Maximum $\overline{CS}$ Rising Edge to Output Disable Time	t_{TR}			25		ns

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AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, 50Ω system impedance, $AV_{DD} = DV_{DD} = PAV_{DD} = HV_{IN}$ = +2.1V to +3.6V, f_{RF} = 300MHz to 450MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at $PAV_{DD} = AV_{DD} = DV_{DD} = HV_{IN}$ = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

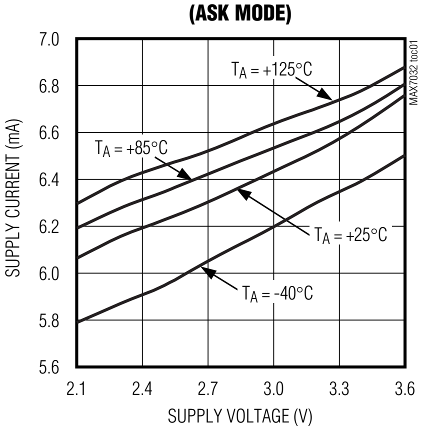
Note 1: Supply current, output power, and efficiency are greatly dependent on board layout and PAOUT match.
Note 2: 100% tested at T_A = +125°C. Guaranteed by design and characterization overtemperature.
Note 3: 50% duty cycle at 10kHz ASK data (Manchester coded).
Note 4: Guaranteed by design and characterization. Not production tested.
Note 5: Time for final signal detection; does not include baseband filter settling.
Note 6: Efficiency = P_{OUT} / (V_{DD} x I_{DD}).
Note 7: Dependent on PC board trace capacitance.
Note 8: The oscillator register (0x05) is set to the nearest integer result of f_{XTAL} / 100kHz (see the *Oscillator Frequency Register* section).
Note 9: Input impedance is measured at the LNAIN pin. Note that the impedance at 315MHz includes the 12nH inductive degeneration from the LNA source to ground. The impedance at 434MHz includes a 10nH inductive degeneration connected from the LNA source to ground. The equivalent input circuit is approximately 50Ω in series with ~ 2.2pF. The voltage conversion is measured with the LNA input matching inductor, the degeneration inductor, and the LNA/mixer tank in place, and does not include the IF filter insertion loss.

Typical Operating Characteristics

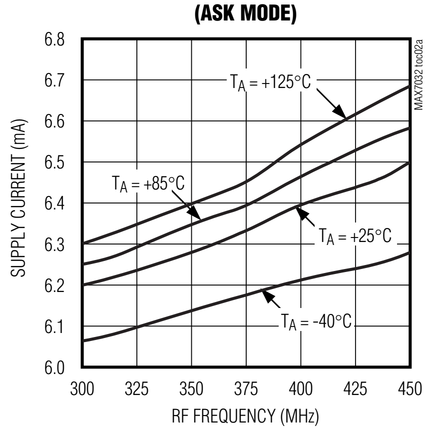
(*Typical Operating Circuit*, $PAV_{DD} = AV_{DD} = DV_{DD} = HV_{IN}$ = +3.0V, f_{RF} = 433.92MHz, T_A = +25°C, IF BW = 280kHz, data rate = 4kbps Manchester encoded, frequency deviation = ±50kHz, BER = 0.2% average RF power, unless otherwise noted.)

RECEIVER

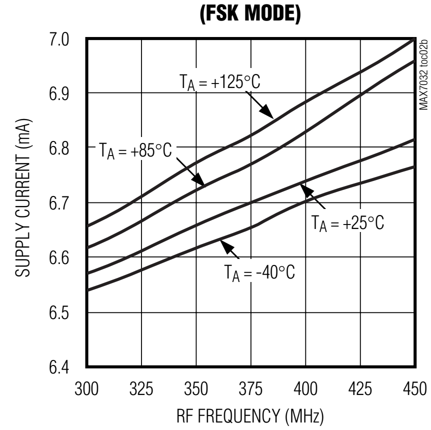
SUPPLY CURRENT vs. SUPPLY VOLTAGE (ASK MODE)



SUPPLY CURRENT vs. RF FREQUENCY (ASK MODE)



SUPPLY CURRENT vs. RF FREQUENCY (FSK MODE)

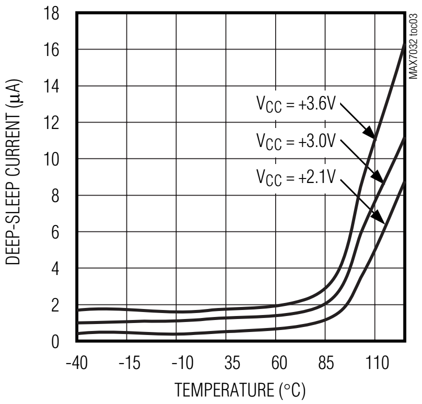


Typical Operating Characteristics (continued)

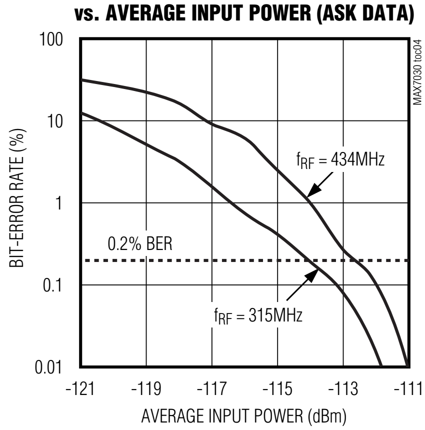
(*Typical Operating Circuit*, $PAV_{DD} = AV_{DD} = DV_{DD} = HV_{IN}$ = +3.0V, f_{RF} = 433.92MHz, T_A = +25°C, IF BW = 280kHz, data rate = 4kbps Manchester encoded, frequency deviation = ±50kHz, BER = 0.2% average RF power, unless otherwise noted.)

RECEIVER

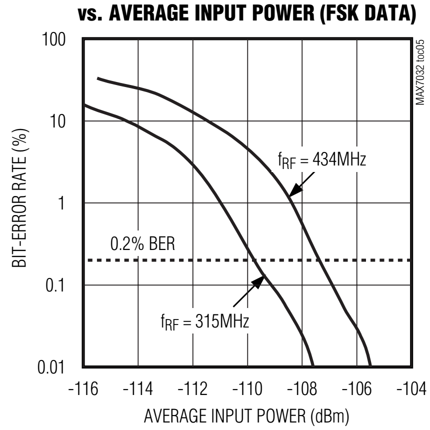
DEEP-SLEEP CURRENT vs. TEMPERATURE



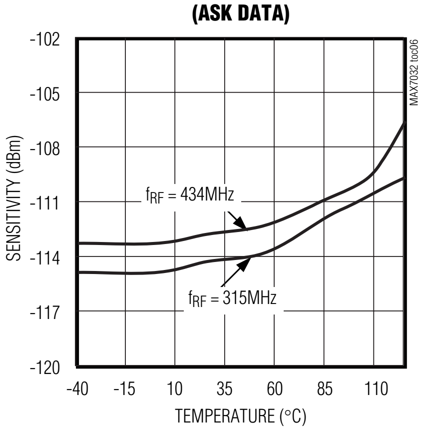
BIT-ERROR RATE vs. AVERAGE INPUT POWER (ASK DATA)



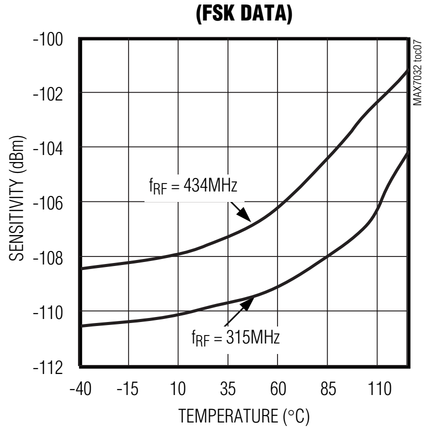
BIT-ERROR RATE vs. AVERAGE INPUT POWER (FSK DATA)



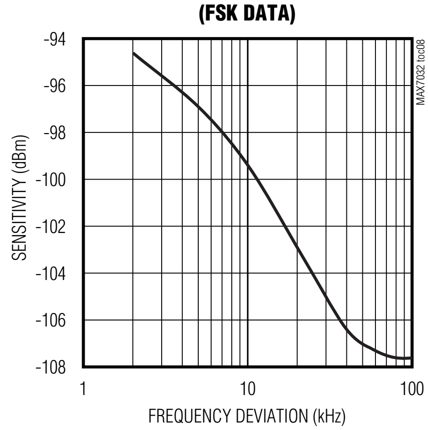
SENSITIVITY vs. TEMPERATURE (ASK DATA)



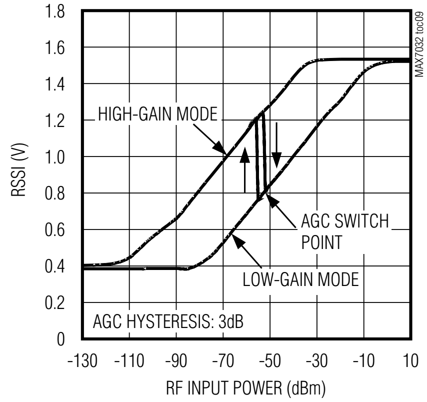
SENSITIVITY vs. TEMPERATURE (FSK DATA)



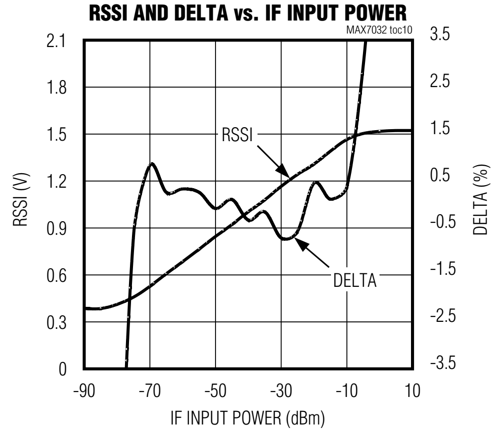
SENSITIVITY vs. FREQUENCY DEVIATION (FSK DATA)



RSSI vs. RF INPUT POWER



RSSI AND DELTA vs. IF INPUT POWER



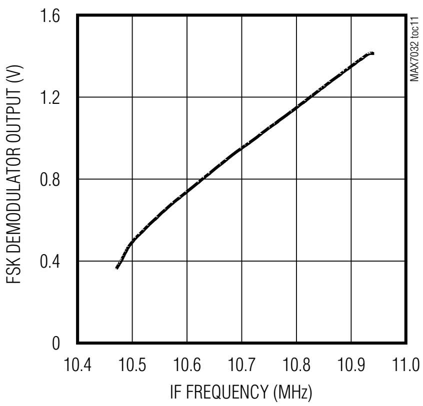
Low-Cost, Crystal-Based, Programmable, ASK/FSK Transceiver with Fractional-N PLL

Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, $PAV_{DD} = AV_{DD} = DV_{DD} = HV_{IN}$ = +3.0V, f_{RF} = 433.92MHz, T_A = +25°C, IF BW = 280kHz, data rate = 4kbps Manchester encoded, frequency deviation = ±50kHz, BER = 0.2% average RF power, unless otherwise noted.)

RECEIVER

FSK DEMODULATOR OUTPUT vs. IF FREQUENCY



SYSTEM GAIN vs. IF FREQUENCY

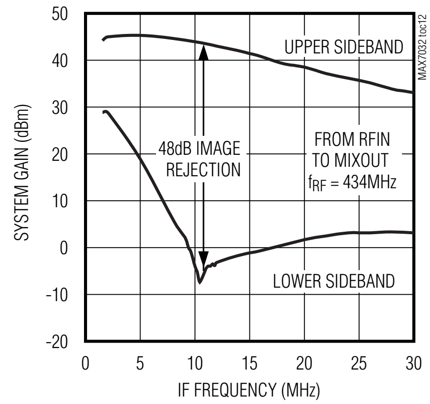
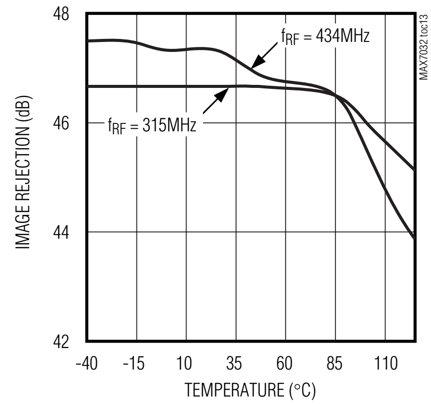
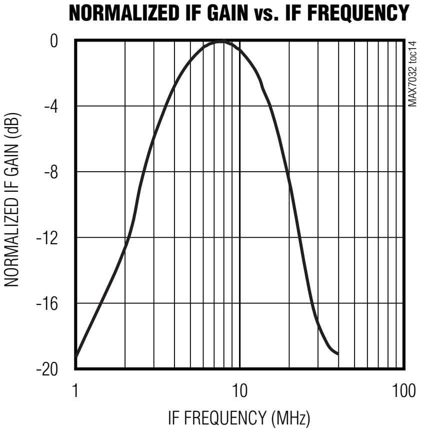


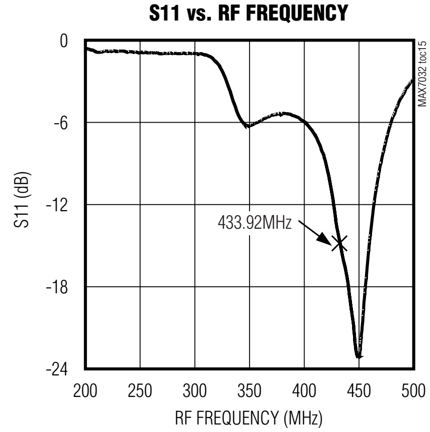
IMAGE REJECTION vs. TEMPERATURE



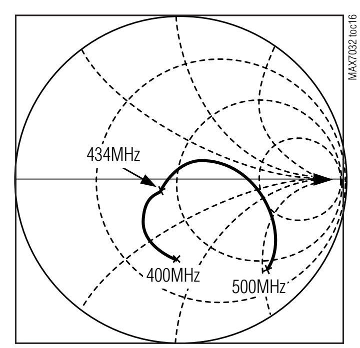
NORMALIZED IF GAIN vs. IF FREQUENCY



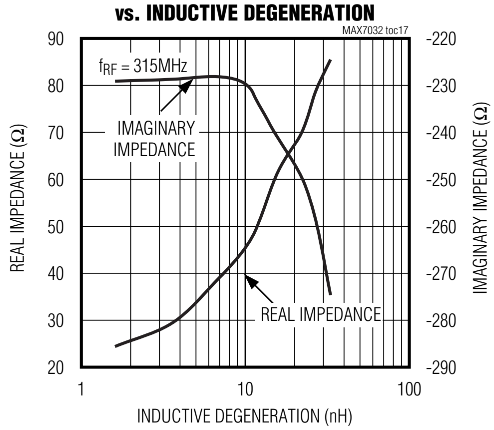
S11 vs. RF FREQUENCY



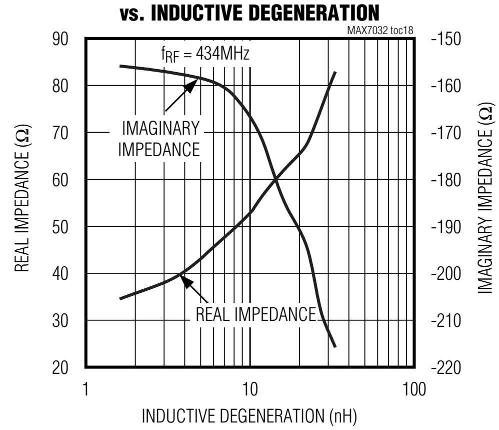
S11 SMITH PLOT OF RFIN



INPUT IMPEDANCE vs. INDUCTIVE DEGENERATION



INPUT IMPEDANCE vs. INDUCTIVE DEGENERATION



Typical Operating Characteristics (continued)

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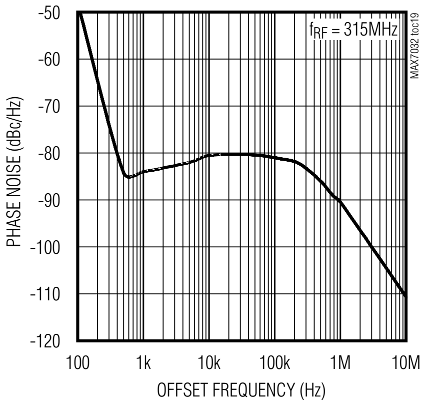
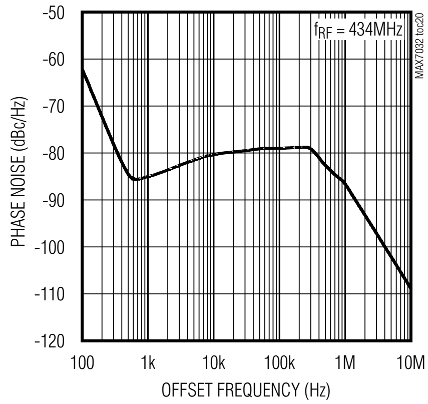
RECEIVER

PHASE NOISE vs. OFFSET FREQUENCY

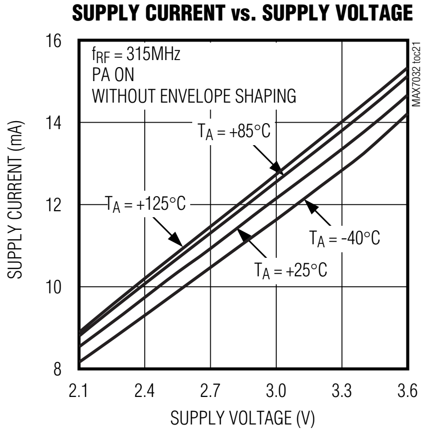


PHASE NOISE vs. OFFSET FREQUENCY

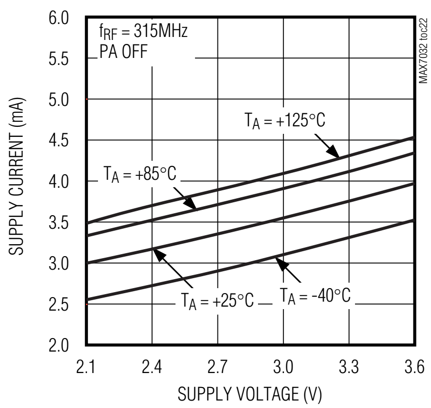


TRANSMITTER

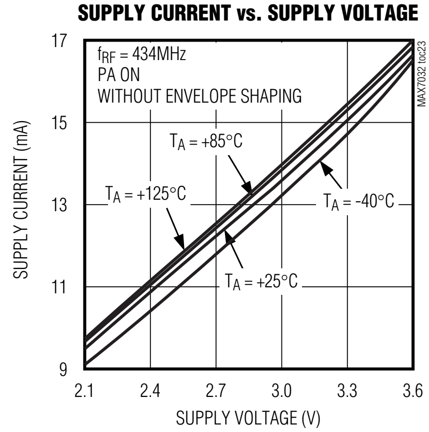
SUPPLY CURRENT vs. SUPPLY VOLTAGE



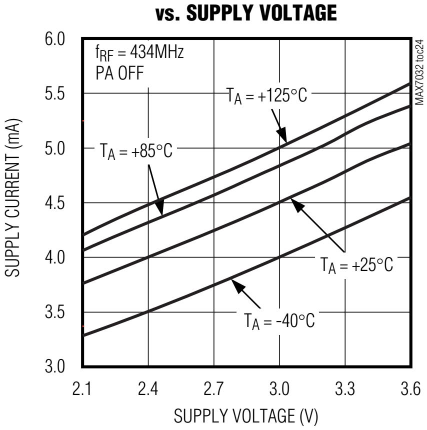
SUPPLY CURRENT vs. SUPPLY VOLTAGE



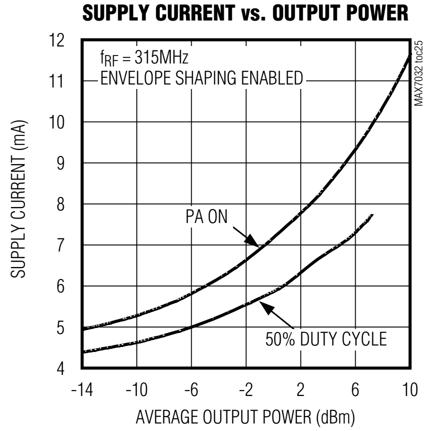
SUPPLY CURRENT vs. SUPPLY VOLTAGE



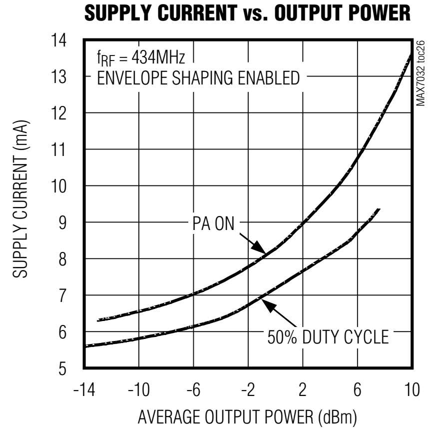
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. OUTPUT POWER



SUPPLY CURRENT vs. OUTPUT POWER



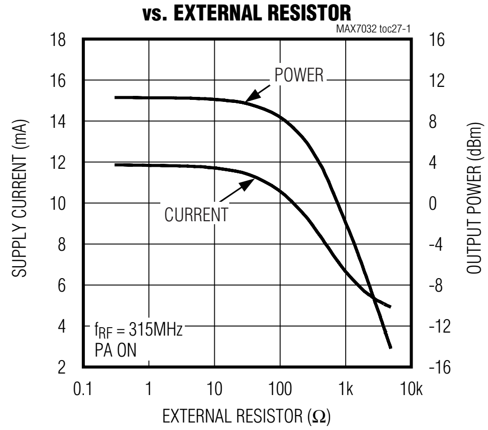
Low-Cost, Crystal-Based, Programmable, ASK/FSK Transceiver with Fractional-N PLL

Typical Operating Characteristics (continued)

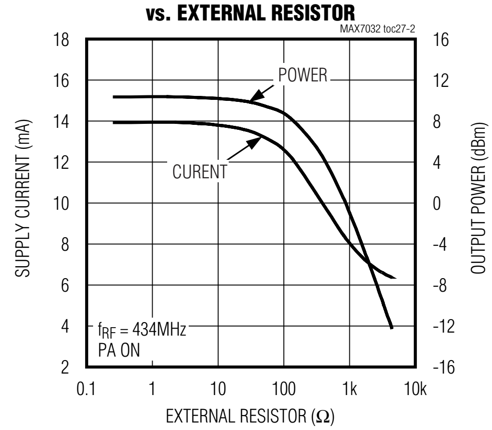
(*Typical Operating Circuit*, $PAV_{DD} = AV_{DD} = DV_{DD} = HV_{IN}$ = +3.0V, f_{RF} = 433.92MHz, T_A = +25°C, IF BW = 280kHz, data rate = 4kbps Manchester encoded, frequency deviation = ±50kHz, BER = 0.2% average RF power, unless otherwise noted.)

TRANSMITTER

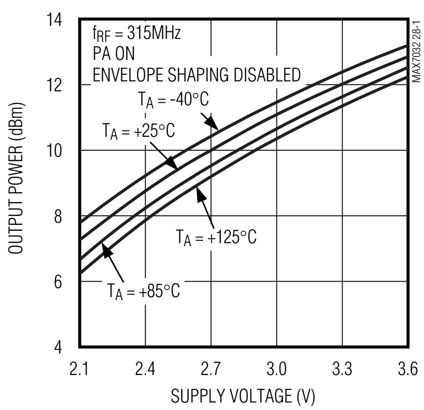
SUPPLY CURRENT AND OUTPUT POWER vs. EXTERNAL RESISTOR



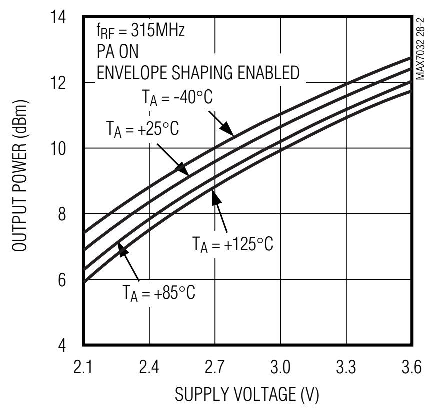
SUPPLY CURRENT AND OUTPUT POWER vs. EXTERNAL RESISTOR



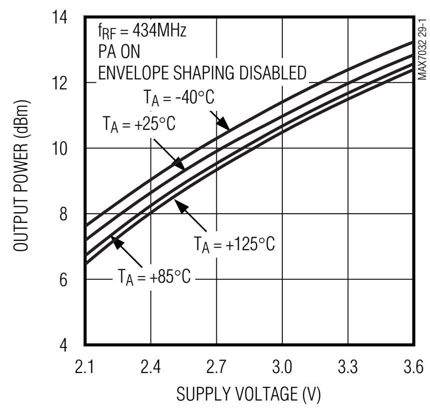
OUTPUT POWER vs. SUPPLY VOLTAGE



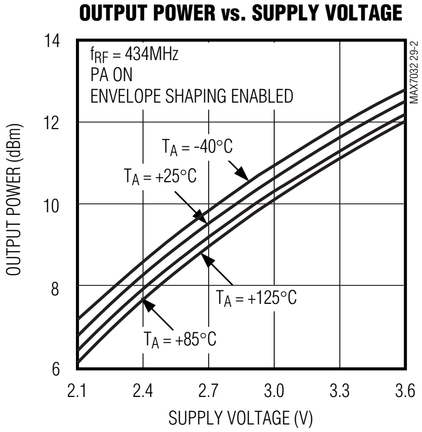
OUTPUT POWER vs. SUPPLY VOLTAGE



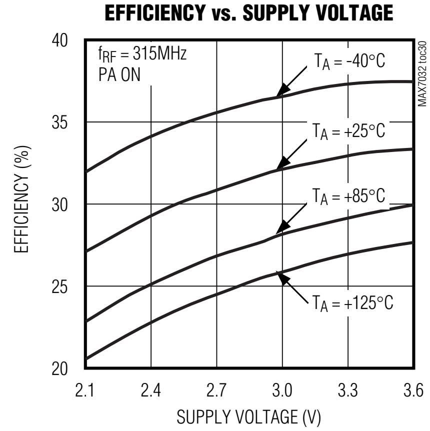
OUTPUT POWER vs. SUPPLY VOLTAGE



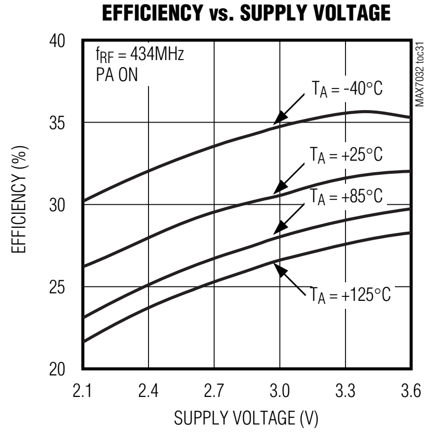
OUTPUT POWER vs. SUPPLY VOLTAGE



EFFICIENCY vs. SUPPLY VOLTAGE



EFFICIENCY vs. SUPPLY VOLTAGE

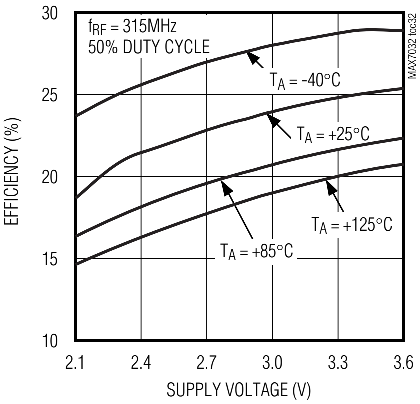


Typical Operating Characteristics (continued)

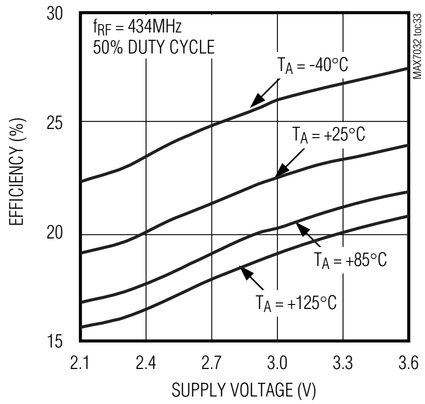
(*Typical Operating Circuit*, $PAV_{DD} = AV_{DD} = DV_{DD} = HV_{IN} = +3.0V$, f_{RF} = 433.92MHz, T_A = +25°C, IF BW = 280kHz, data rate = 4kbps Manchester encoded, frequency deviation = ±50kHz, BER = 0.2% average RF power, unless otherwise noted.)

TRANSMITTER

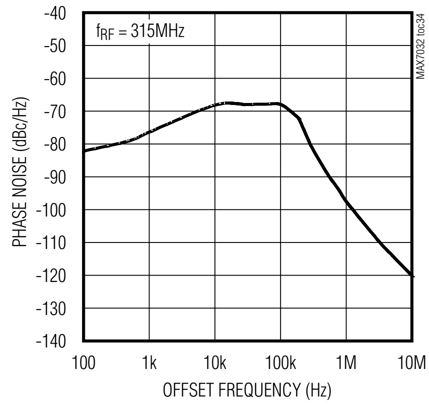
EFFICIENCY vs. SUPPLY VOLTAGE



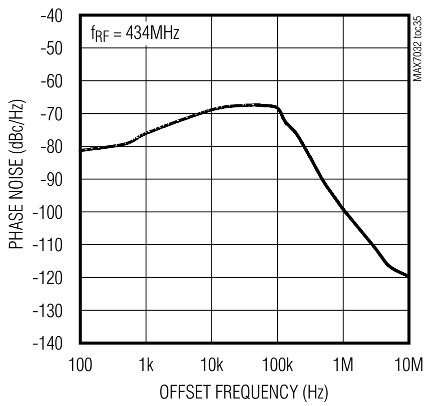
EFFICIENCY vs. SUPPLY VOLTAGE



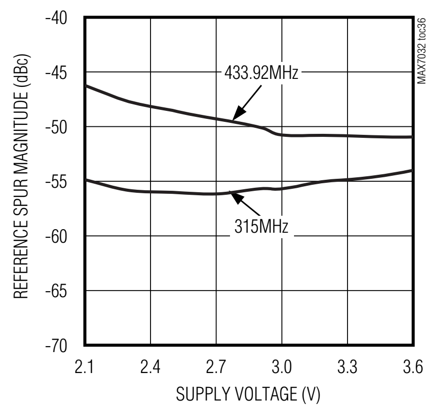
PHASE NOISE vs. OFFSET FREQUENCY



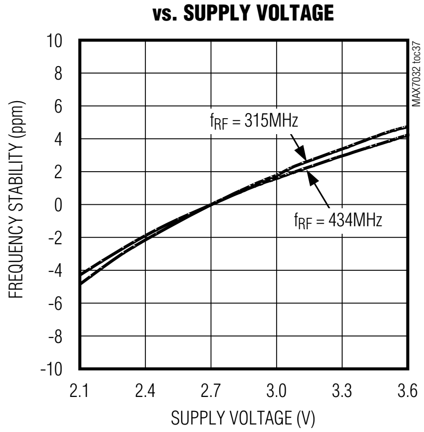
PHASE NOISE vs. OFFSET FREQUENCY



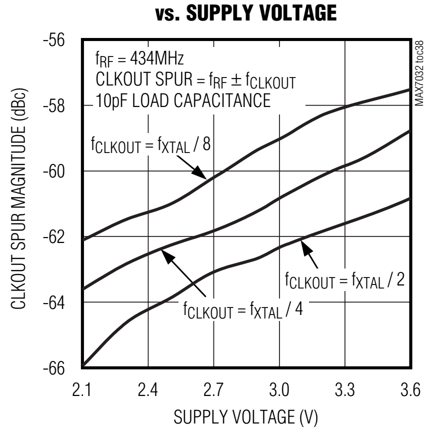
REFERENCE SPUR MAGNITUDE vs. SUPPLY VOLTAGE



FREQUENCY STABILITY vs. SUPPLY VOLTAGE



CLKOUT SPUR MAGNITUDE vs. SUPPLY VOLTAGE



Low-Cost, Crystal-Based, Programmable, ASK/FSK Transceiver with Fractional-N PLL

Pin Description

PIN	NAME	FUNCTION
1	PAV_{DD}	Power-Amplifier Supply Voltage. Bypass to GND with 0.01µF and 220pF capacitors placed as close to the pin as possible.
2	ROUT	Envelope-Shaping Output. ROUT controls the power-amplifier envelope's rise and fall times. Connect ROUT to the PA pullup inductor or optional power-adjust resistor. Bypass the inductor to GND as close to the inductor as possible with 680pF and 220pF capacitors as shown in the *Typical Application Circuit*.
3	TX/RX1	Transmit/Receive Switch Throw. Drive $T/\overline{R}$ high to short TX/RX1 to TX/RX2. Drive $T/\overline{R}$ low to disconnect TX/RX1 from TX/RX2. Functionally identical to TX/RX2.
4	TX/RX2	Transmit/Receive Switch Pole. Typically connected to ground. See the *Typical Application Circuit*.
5	PAOUT	Power-Amplifier Output. Requires a pullup inductor to the supply voltage (or ROUT if envelope shaping is desired), which may be part of the output-matching network to an antenna.
6	AV_{DD}	Analog Power-Supply Voltage. AV_{DD} is connected to an on-chip +3.0V regulator in 5V operation. Bypass AV_{DD} to GND with 0.1µF and 220pF capacitors placed as close to the pin as possible.
7	LNAIN	Low-Noise Amplifier Input. Must be AC-coupled.
8	LNASRC	Low-Noise Amplifier Source for External Inductive Degeneration. Connect an inductor to GND to set the LNA input impedance.
9	LNAOUT	Low-Noise Amplifier Output. Must be tied to AV_{DD} through a parallel LC tank filter. AC-couple to MIXIN+.
10	MIXIN+	Noninverting Mixer Input. Must be AC-coupled to the LNA output.
11	MIXIN-	Inverting Mixer Input. Bypass to AV_{DD} with a capacitor as close to LNA LC tank filter as possible.
12	MIXOUT	330Ω Mixer Output. Connect to the input of the 10.7MHz filter.
13	IFIN-	Inverting 330Ω IF Limiter Amplifier Input. Bypass to GND with a capacitor.
14	IFIN+	Noninverting 330Ω IF Limiter Amplifier Input. Connect to the output of the 10.7MHz IF filter.
15	PDMIN	Minimum-Level Peak Detector for Demodulator Output
16	PDMAX	Maximum-Level Peak Detector for Demodulator Output
17	DS-	Inverting Data Slicer Input
18	DS+	Noninverting Data Slicer Input
19	OP+	Noninverting Op Amp Input for the Sallen-Key Data Filter
20	DF	Data Filter Feedback Node. Input for the feedback of the Sallen-Key data filter.
21	RSSI	Buffered Received-Signal-Strength Indicator Output
22	$T/\overline{R}$	Transmit/ $\overline{\text{Receive}}$. Drive high to put the device in transmit mode. Drive low or leave unconnected to put the device in receive mode. It is internally pulled down. This function is also controlled by a configuration register.
23	ENABLE	Enable. Drive high for normal operation. Drive low or leave unconnected to put the device into shutdown mode.
24	DATA	Receiver Data Output/Transmitter Data Input
25	CLKOUT	Divided Crystal Clock Buffered Output
26	DV_{DD}	Digital Power-Supply Voltage. Bypass to GND with 0.01µF and 220pF capacitors placed as close to the pin as possible.

Pin Description (continued)

PIN	NAME	FUNCTION
27	HV_{IN}	High-Voltage Supply Input. For 3V operation, connect HV_{IN} to PAV_{DD}, AV_{DD}, and DV_{DD}. For 5V operation, tie only HV_{IN} to 5V. Bypass HV_{IN} to GND with 0.01µF and 220pF capacitors placed as close to the pin as possible.
28	$\overline{CS}$	Serial Interface Active-Low Chip Select
29	DIO	Serial Interface Serial Data Input/Output
30	SCLK	Serial Interface Clock Input
31	XTAL1	Crystal Input 1. Bypass to GND if XTAL2 is driven by an AC-coupled external reference.
32	XTAL2	Crystal Input 2. XTAL2 can be driven from an AC-coupled external reference.
—	EP	Exposed Pad. Solder evenly to the board's ground plane for proper operation.

Detailed Description

The MAX7032 300MHz to 450MHz CMOS transceiver and a few external components provide a complete transmit and receive chain from the antenna to the digital data interface. This device is designed for transmitting and receiving ASK and FSK data. All transmit frequencies are generated by a fractional-N-based synthesizer, allowing for very fine frequency steps in increments of f_{XTAL} / 4096. The receive LO is generated by a traditional integer-N-based synthesizer. Depending on component selection, data rates as high as 33kbps (Manchester encoded) or 66kbps (NRZ encoded) can be achieved.

Receiver

Low-Noise Amplifier (LNA)

The LNA is a cascode amplifier with off-chip inductive degeneration that achieves approximately 30dB of voltage gain that is dependent on both the antenna matching network at the LNA input, and the LC tank network between the LNA output and the mixer inputs.

The off-chip inductive degeneration is achieved by connecting an inductor from LNASRC to AGND. This inductor sets the real part of the input impedance at LNAIN, allowing for a more flexible match for low-input impedance such as a PC board trace antenna. A nominal value for this inductor with a 50Ω input impedance is 12nH at 315MHz and 10nH at 434MHz, but the inductance is affected by PC board trace length. LNASRC can be shorted to ground to increase sensitivity by approximately 1dB, but the input match must then be reoptimized.

The LC tank filter connected to LNAOUT consists of L5 and C9 (see the *Typical Application Circuit*). Select L5 and C9 to resonate at the desired RF input frequency. The resonant frequency is given by:

$$f = \frac{1}{2\pi\sqrt{L_{TOTAL} \times C_{TOTAL}}}$$

where L_{TOTAL} = L5 + $L_{PARASITICS}$ and C_{TOTAL} = C9 + $C_{PARASITICS}$.

$L_{PARASITICS}$ and $C_{PARASITICS}$ include inductance and capacitance of the PC board traces, package pins, mixer input impedance, LNA output impedance, etc. These parasitics at high frequencies cannot be ignored, and can have a dramatic effect on the tank filter center frequency. Lab experimentation must be done to optimize the center frequency of the tank. The total parasitic capacitance is generally between 5pF and 7pF.

Automatic Gain Control (AGC)

When the AGC is enabled, it monitors the RSSI output. When the RSSI output reaches 1.28V, which corresponds to an RF input level of approximately -55dBm, the AGC switches on the LNA gain-reduction attenuator. The attenuator reduces the LNA gain by 36dB, thereby reducing the RSSI output by about 540mV to 740mV. The LNA resumes high-gain mode when the RSSI output level drops back below 680mV (approximately -59dBm at the RF input) for a programmable interval called the AGC dwell time. The AGC has a hysteresis of approximately 4dB. With the AGC function, the RSSI dynamic range is increased, allowing the MAX7032 to reliably produce an ASK output for RF input levels up to 0dBm with a modulation depth of 18dB. AGC is not required and can be disabled in either ASK or FSK mode. AGC is not necessary for FSK mode because large received signal levels do not affect FSK performance.

Low-Cost, Crystal-Based, Programmable, ASK/FSK Transceiver with Fractional-N PLL

Mixer

A unique feature of the MAX7032 is the integrated image rejection of the mixer. This eliminates the need for a costly front-end SAW filter for many applications. The advantage of not using a SAW filter is increased sensitivity, simplified antenna matching, less board space, and lower cost.

The mixer cell is a pair of double-balanced mixers that perform an IQ downconversion of the RF input to the 10.7MHz intermediate frequency (IF) with low-side injection (i.e., $f_{LO} = f_{RF} - f_{IF}$). The image-rejection circuit then combines these signals to achieve a typical 46dB of image rejection over the full temperature range. Low-side injection is required as high-side injection is not possible due to the on-chip image rejection. The IF output is driven by a source follower, biased to create a driving impedance of 330Ω to interface with an off-chip 330Ω ceramic IF filter. The voltage-conversion gain driving a 330Ω load is approximately 20dB. Note that the MIXIN+ and MIXIN- inputs are functionally identical.

Integer-N Phase-Locked Loop (PLL)

The MAX7032 utilizes a fixed integer-N PLL to generate the receive LO. All PLL components, including the loop filter, VCO, charge pump, asynchronous 24x divider, and phase-frequency detector are integrated on-chip. The loop bandwidth is approximately 500kHz. The relationship between RF, IF, and reference frequencies is given by:

$$f_{REF} = (f_{RF} - f_{IF}) / 24$$

Intermediate Frequency (IF)

The IF section presents a differential 330Ω load to provide matching for the off-chip ceramic filter. The internal six AC-coupled limiting amplifiers produce an overall gain of approximately 65dB, with a bandpass filter type response centered near the 10.7MHz IF frequency with a 3dB bandwidth of approximately 10MHz. For ASK data, the RSSI circuit demodulates the IF to baseband by producing a DC output proportional to the log of the IF signal level with a slope of approximately 15mV/dB. For FSK, the limiter output is fed into a PLL to demodulate the IF. The FSK demodulation slope is approximately 2.0mV/kHz.

FSK Demodulator

The FSK demodulator uses an integrated 10.7MHz PLL that tracks the input RF modulation and converts the frequency deviation into a voltage difference. The PLL is illustrated in Figure 1. The input to the PLL comes from the output of the IF limiting amplifiers. The PLL control voltage responds to changes in the frequency of the input signal with a nominal gain of 2.0mV/kHz. For example, an FSK peak-to-peak deviation of 50kHz generates a $100mV_{P-P}$ signal on the control line. This control voltage is then filtered and sliced by the baseband circuitry.

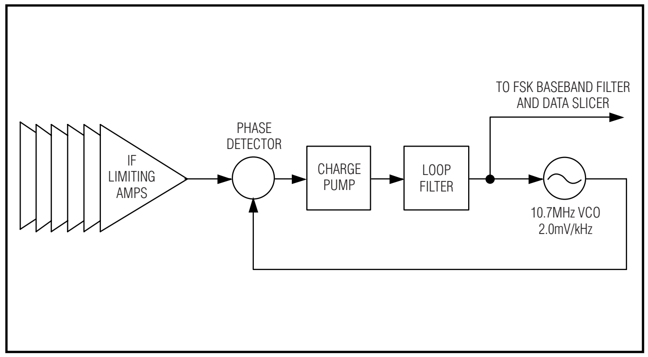


Figure 1. FSK Demodulator PLL Block Diagram

The FSK demodulator PLL requires calibration to overcome variations in process, voltage, and temperature. For more information on calibrating the FSK demodulator, see the *Calibration* section. The maximum calibration time is 150µs. In discontinuous receive (DRX) mode, the FSK demodulator calibration occurs automatically just after the IC exits sleep mode.

Data Filter

The data filter for the demodulated data is implemented as a 2nd-order lowpass Sallen-Key filter. The pole locations are set by the combination of two on-chip resistors and two external capacitors. Adjusting the value of the external capacitors changes the corner frequency to optimize for different data rates. The corner frequency in kHz should be set to approximately 3 times the fastest expected Manchester data rate in kbps from the transmitter (1.5 times the fastest expected NRZ data rate) for ASK. For FSK, the corner frequency should be set to approximately 2 times the fastest expected Manchester data rate in kbps from the transmitter (1 times the fastest expected NRZ data rate). Keeping the corner frequency near the data rate rejects any noise at higher frequencies, resulting in an increase in receiver sensitivity. Table 1 lists coefficients to calculate CF1 and CF2.

Table 1. Coefficients to Calculate CF1 and CF2

FILTER TYPE	a	b
Butterworth (Q = 0.707)	1.414	1.000
Bessel (Q = 0.577)	1.3617	0.618

The configuration shown in Figure 2 can create a Butterworth or Bessel response. The Butterworth filter offers a very flat amplitude response in the passband and a rolloff rate of 40dB/decade for the two-pole filter. The Bessel filter has a linear phase response, which works well for filtering digital data. To calculate the value of the capacitors, use the following equations, along with the coefficients in Table 1:

$$C_{F1} = \frac{b}{a(100k\Omega)(\pi)(f_C)}$$

$$C_{F2} = \frac{a}{4(100k\Omega)(\pi)(f_C)}$$

where f_C is the desired 3dB corner frequency.

For example, choose a Butterworth filter response with a corner frequency of 5kHz:

$$C_{F1} = \frac{1.000}{(1.414)(100k\Omega)(3.14)(5kHz)} \approx 450pF$$

$$C_{F2} = \frac{1.414}{(4)(100k\Omega)(3.14)(5kHz)} \approx 225pF$$

Choosing standard capacitor values changes C_{F1} to 470pF and C_{F2} to 220pF. In the *Typical Application Circuit*, C_{F1} and C_{F2} are named C16 and C17, respectively.

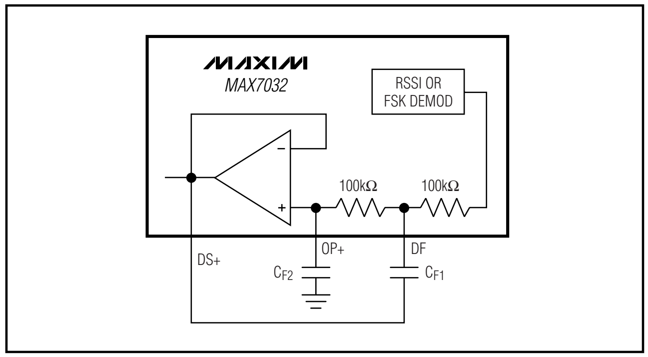


Figure 2. Sallen-Key Lowpass Data Filter

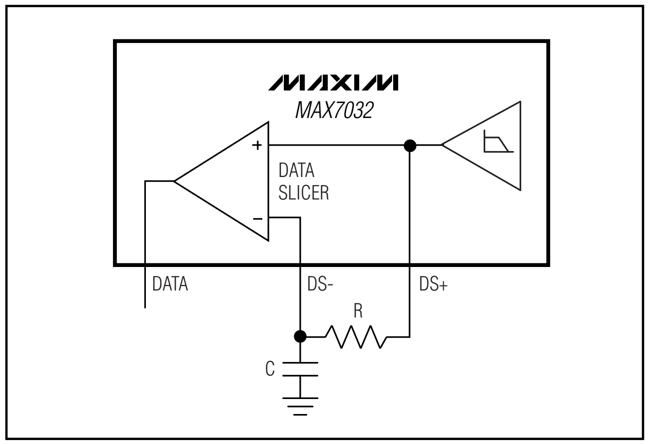


Figure 3. Generating Data Slicer Threshold Using a Lowpass Filter

Data Slicer

The data slicer takes the analog output of the data filter and converts it to a digital signal. This is achieved by using a comparator and comparing the analog input to a threshold voltage. The threshold voltage is set by the voltage on the DS- pin, which is connected to the negative input of the data-slicer comparator.

Numerous configurations can be used to generate the data-slicer threshold. For example, the circuit in Figure 3 shows a simple method using only one resistor and one capacitor. This configuration averages the analog output of the filter and sets the threshold to approximately 50% of that amplitude. With this configuration, the threshold automatically adjusts as the analog signal varies, minimizing the possibility for errors in the digital data. The values of R and C affect how fast the threshold tracks the analog amplitude. Be sure to keep the corner frequency of the RC circuit much lower (about 10 times) than the lowest expected data rate.

With this configuration, a long string of NRZ zeros or ones can cause the threshold to drift. This configuration works best if a coding scheme, such as Manchester coding, which has an equal number of zeros and ones, is used.

Figure 4 shows a configuration that uses the positive and negative peak detectors to generate the threshold. This configuration sets the threshold to the midpoint between a high output and a low output of the data filter.

Peak Detectors

The maximum peak detector (PDMAX) and minimum peak detector (PDMIN), with resistors and capacitors shown in Figure 4, create DC output voltages equal to the high and low peak values of the filtered ASK or FSK demodulated signals. The resistors provide a path for the capacitors to discharge, allowing the peak detectors to dynamically follow peak changes of the data filter output voltages.

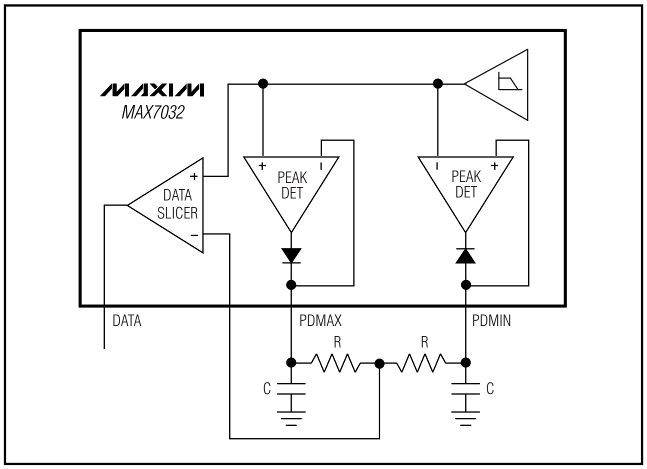


Figure 4. Generating Data Slicer Threshold Using the Peak Detectors

The maximum and minimum peak detectors can be used together to form a data slicer threshold voltage at a value midway between the maximum and minimum voltage levels of the data stream (see the *Data Slicer* section and Figure 4). The RC time constant of the peak-detector combining network should be set to at least 5 times the data period.

If there is an event that causes a significant change in the magnitude of the baseband signal, such as an AGC gain switch or a power-up transient, the peak detectors may "catch" a false level. If a false peak is detected, the slicing level is incorrect. The MAX7032 has a feature called peak-detector track enable (TRK_EN), where the peak-detector outputs can be reset (see Figure 5). If TRK_EN is set (logic 1), both the maximum and minimum peak detectors follow the input signal. When TRK_EN is cleared (logic 0), the peak detectors revert to their normal operating mode. The TRK_EN function is automatically enabled for a short time whenever the IC is first powered up, or transitions from transmit to receive mode, or recovers from the sleep portion of DRX mode, or when an AGC gain switch occurs regardless of the bit setting. Since the peak detectors exhibit a fast-attack/slow-decay response, this feature allows for an extremely fast startup or AGC recovery. See Figure 6 for an illustration of a fast-recovery sequence. In addition to the automatic control of this function, the TRK_EN bits can be controlled through the serial interface (see the *Serial Control Interface* section).

Transmitter

Power Amplifier (PA)

The PA of the MAX7032 is a high-efficiency, open-drain, switch-mode amplifier. The PA with proper

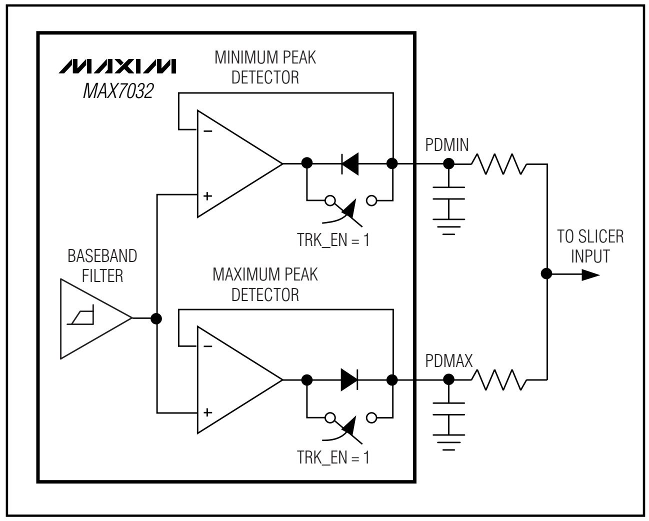


Figure 5. Peak-Detector Track Enable

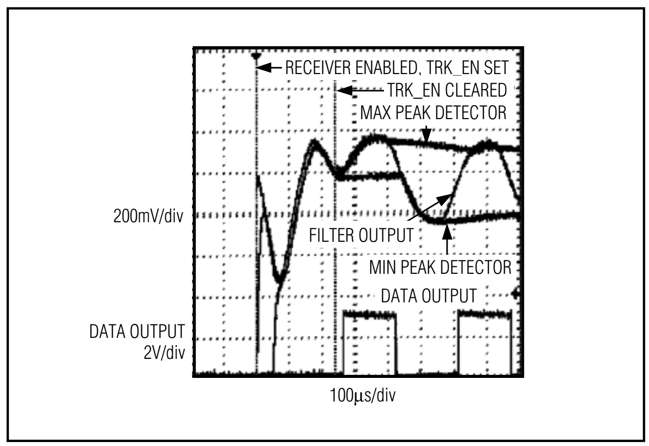


Figure 6. Fast Receiver Recovery in FSK Mode Utilizing Peak Detectors

output-matching network can drive a wide range of antenna impedances, which includes a small-loop PC board trace and a 50Ω antenna. The output-matching network for a 50Ω antenna is shown in the *Typical Application Circuit*. The output-matching network suppresses the carrier harmonics and transforms the antenna impedance to an optimal impedance at PAOUT (pin 5). The optimal impedance at PAOUT is 250Ω.

When the output-matching network is properly tuned, the PA transmits power with a high overall efficiency of up to 32%. The efficiency of the PA itself is more than 46%. The output power is set by an external resistor at

PAOUT, and is also dependent on the external antenna and antenna-matching network at the PA output.

Envelope Shaping

The MAX7032 features an internal envelope-shaping resistor, which connects between the open-drain output of the PA and the power supply (see *Typical Application Circuit*). The envelope-shaping resistor slows the turn-on/turn-off of the PA in ASK mode, and results in a smaller spectral width of the modulated PA output signal.

Fractional-N PLL

The MAX7032 utilizes a fully integrated fractional-N PLL for its transmit frequency synthesizer. All PLL components, including the loop filter, are included on chip. The loop bandwidth is approximately 200kHz. The 16-bit fractional-N topology allows the transmit frequency to be adjusted in increments of f_{XTAL} / 4096. The fine-frequency-adjustment capability enables the use of a single crystal, as the transmit frequency can be set within 2kHz of the receive frequency.

The fractional-N topology also allows exact FSK frequency deviations to be programmed, completely eliminating the problems associated with generating frequency deviations by crystal oscillator pulling.

The integer and fractional portions of the PLL divider ratio set the transmit frequency. The example below shows how to calculate f_{XTAL} and how to determine the correct values to be loaded to register TxLOW (register 0x0D and 0x0E) and TxHIGH (registers 0x0F and 0x10):

Assume the receiver/ASK transmit frequency = 315MHz, and IF = 10.7MHz:

$$f_{XTAL} = \frac{(f_{RF} - 10.7)}{24} = 12.67917\text{MHz}$$

and

$$\frac{f_{RF}}{f_{XTAL}} = 24.8439 = \text{transmit PLL divider ratio}$$

Due to the nature of the transmit PLL frequency divider, a fixed offset of 16 must be subtracted from the transmit PLL divider ratio for programming the MAX7032's transmit frequency registers. To determine the value to program the MAX7032's transmit frequency registers, convert the decimal value of the following equation to the nearest hexadecimal value:

$$\left(\frac{f_{RF}}{f_{XTAL}} - 16\right) \times 4096 = \text{decimal value to program transmit frequency registers}$$

In this example, the rounded decimal value is 36,225, or 8D81 hexadecimal. The upper byte (8D) is loaded into register 0x0D, and the low byte (81) is loaded into register 0x0E.

In FSK mode, the transmit frequencies equal the upper and lower frequencies that are programmed into the MAX7032's transmit frequency registers. Calculate the upper frequency in the same way as shown above. In ASK mode, the transmit frequency equals the lower frequency that is programmed into the MAX7032's transmit frequency registers.

Power-Supply Connections

The MAX7032 can be powered from a 2.1V to 3.6V supply or a 4.5V to 5.5V supply. If a 4.5V to 5.5V supply is used, then the on-chip linear regulator reduces the 5V supply to the 3V needed to operate the chip.

To operate the MAX7032 from a 3V supply, connect PAV_{DD}, AV_{DD}, DV_{DD}, and HV_{IN} to the 3V supply. When using a 5V supply, connect the supply to HV_{IN} only and connect AV_{DD}, PAV_{DD}, and DV_{DD} together. In both cases, bypass DV_{DD}, PAV_{DD} and HV_{IN} to GND with a 0.01µF and 220pF capacitor and bypass AV_{DD} to GND with a 0.1µF and 220pF capacitor. Bypass $T/\overline{R}$, ENABLE, DATA, $\overline{CS}$, DIO, and SCLK with 10pF capacitors to GND. Place all bypass capacitors as close to the respective pins as possible.

Transmit/Receive Antenna Switch

The MAX7032 features an internal SPST RF switch, which, when combined with a few external components, allows the transmit and receive pins to share a common antenna (see the *Typical Application Circuit)*. In receive mode, the switch is open and the power amplifier is shut down, presenting a high impedance to minimize the loading of the LNA. In transmit mode, the switch closes to complete a resonant tank circuit at the PA output and forms an RF short at the input to the LNA. In this mode, the external passive components couple the output of the PA to the antenna to protect the LNA input from strong transmitted signals.

The switch state is controlled either by an external digital input or by the $T/\overline{R}$ bit, which is bit 6 in the configuration 0 register, $T/\overline{R}$. Drive the $T/\overline{R}$ pin high to put the device in transmit mode; drive the $T/\overline{R}$ pin low to put the device in receive mode.

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Crystal Oscillator (XTAL)

The XTAL oscillator in the MAX7032 is designed to present a capacitance of approximately 3pF between the XTAL1 and XTAL2 pins. In most cases, this corresponds to a 4.5pF load capacitance applied to the external crystal when typical PC board parasitics are added. **It is very important to use a crystal with a load capacitance that is equal to the capacitance of the MAX7032 crystal oscillator plus PC board parasitics.** If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its stated operating frequency, introducing an error in the reference frequency. Crystals designed to operate with higher differential load capacitance always pull the reference frequency higher.

In actuality, the oscillator pulls every crystal. The crystal's natural frequency is really below its specified frequency, but when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the load capacitance.

Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_P = \frac{C_m}{2}\left(\frac{1}{C_{CASE} + C_{LOAD}} - \frac{1}{C_{CASE} + C_{SPEC}}\right) \times 10^6$$

where:

f_P is the amount the crystal frequency is pulled in ppm.

C_m is the motional capacitance of the crystal.

C_{CASE} is the case capacitance.

C_{SPEC} is the specified load capacitance.

C_{LOAD} is the actual load capacitance.

When the crystal is loaded as specified, i.e., $C_{LOAD} = C_{SPEC}$, the frequency pulling equals zero.

Serial Control Interface

Communication Protocol

The MAX7032 programs through a 3-wire interface. The data input must follow the timing diagrams shown in Figures 7, 8, and 9.

Note that the DIO line must be held LOW while $\overline{CS}$ is high. This is to prevent the MAX7032 from entering discontinuous receive mode if the DRX bit is high. The data is latched on the rising edge of SCLK, and therefore must be stable before that edge. The data sequencing is MSB first, the command (C[1:0] see Table 2), the register address (A[5:0] see Table 3), and the data (D[7:0] see Table 4).

Table 2. Command Bits

C[1:0]	DESCRIPTION
0x0	No operation
0x1	Write data
0x2	Read data
0x3	Master reset

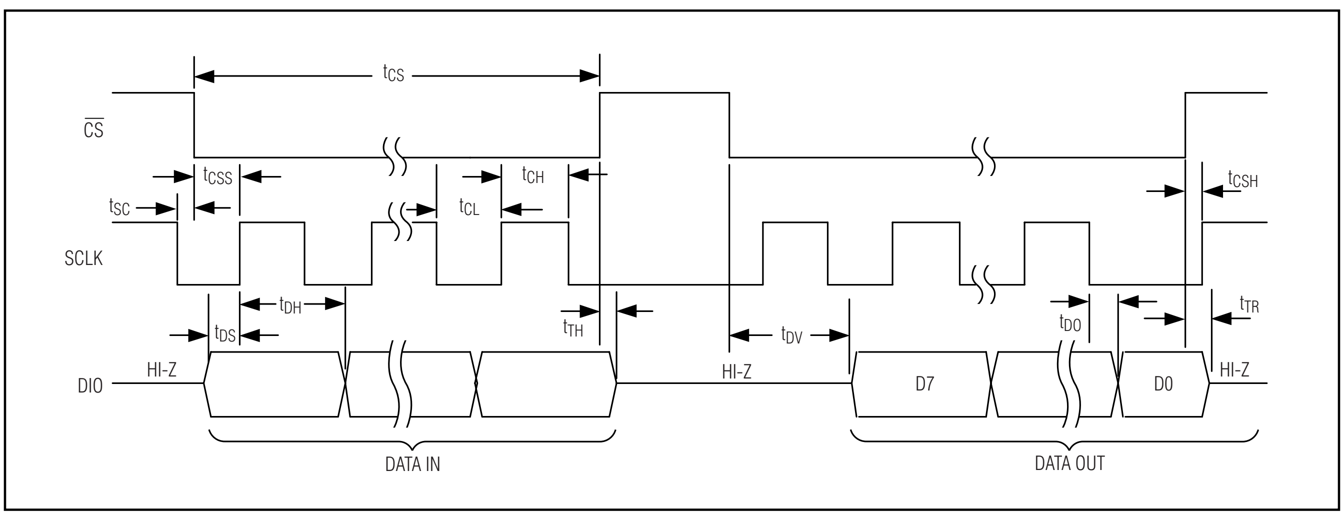

Figure 7. Serial Interface Timing Diagram

Table 3. Register Summary

REGISTER A[5:0]	REGISTER NAME	DESCRIPTION
0x00	Power configuration	Enables/disables the LNA, AGC, mixer, baseband, peak detectors, PA, and RSSI output (see Table 5).
0x01	Control	Controls AGC lock, gain state, peak-detector tracking, polling timer and FSK calibration, clock signal output, and sleep mode (see Table 6).
0x02	Configuration0	Sets options for modulation, TX/RX mode, manual-gain mode, discontinuous receive mode, off-timer and on-timer prescalers (see Table 7).
0x03	Configuration1	Sets options for automatic FSK calibration, clock output, output clock divider ratio, AGC dwell timer (see Tables 8, 10, 11, and 12).
0x05	Oscillator frequency	Sets the internal clock frequency divisor. This register must be set to the integer result of f_{XTAL} / 100kHz (see the *Oscillator Frequency Register* section).
0x06	Off timer—t_{OFF} (upper byte)	Sets the duration that the MAX7032 remains in low-power mode when DRX is active (see Table 12).
0x07	Off timer—t_{OFF} (lower byte)	
0x08	CPU recovery timer—t_{CPU}	Increases maximum time the MAX7032 stays in lower power mode while CPU wakes up when DRX is active (see Table 13).
0x09	RF settling timer—t_{RF} (upper byte)	During the time set by the RF settling timer, the MAX7032 is powered on with the peak detectors and the data outputs disabled to allow time for the RF section to settle. DIO must be driven low at any time during t_{LOW} = t_{CPU} + t_{RF} + t_{ON} or the timer sequence restarts (see Table 14).
0x0A	RF settling timer—t_{RF} (lower byte)	
0x0B	On timer—t_{ON} (upper byte)	Sets the duration that the MAX7032 remains in active mode when DRX is active (see Table 15).
0x0C	On timer—t_{ON} (lower byte)	
0x0D	Transmitter low-frequency setting—TxLOW (upper byte)	Sets the low frequency (FSK) of the transmitter or the carrier frequency of ASK for the fractional-N synthesizer.
0x0E	Transmitter low-frequency setting—TxLOW (lower byte)	
0x0F	Transmitter high-frequency setting—TxHIGH (upper byte)	Sets the high frequency (FSK) of the transmitter for the fractional-N synthesizer.
0x10	Transmitter high-frequency setting—TxHIGH (lower byte)	
0x1A	Status register (read only)	Provides status for PLL lock, AGC state, crystal operation, polling timer, and FSK calibration (see Table 9).

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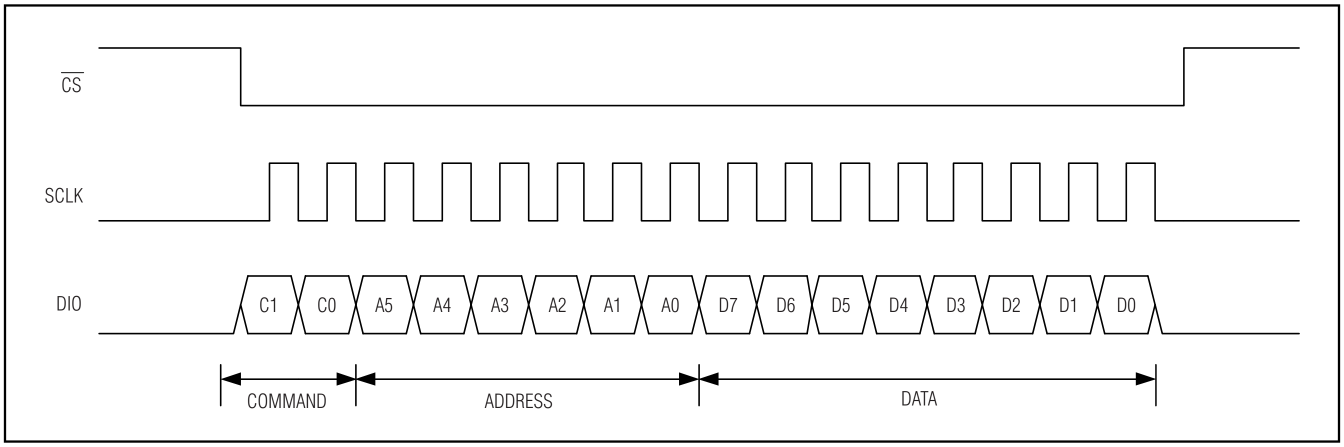

Figure 8. Data Input Diagram

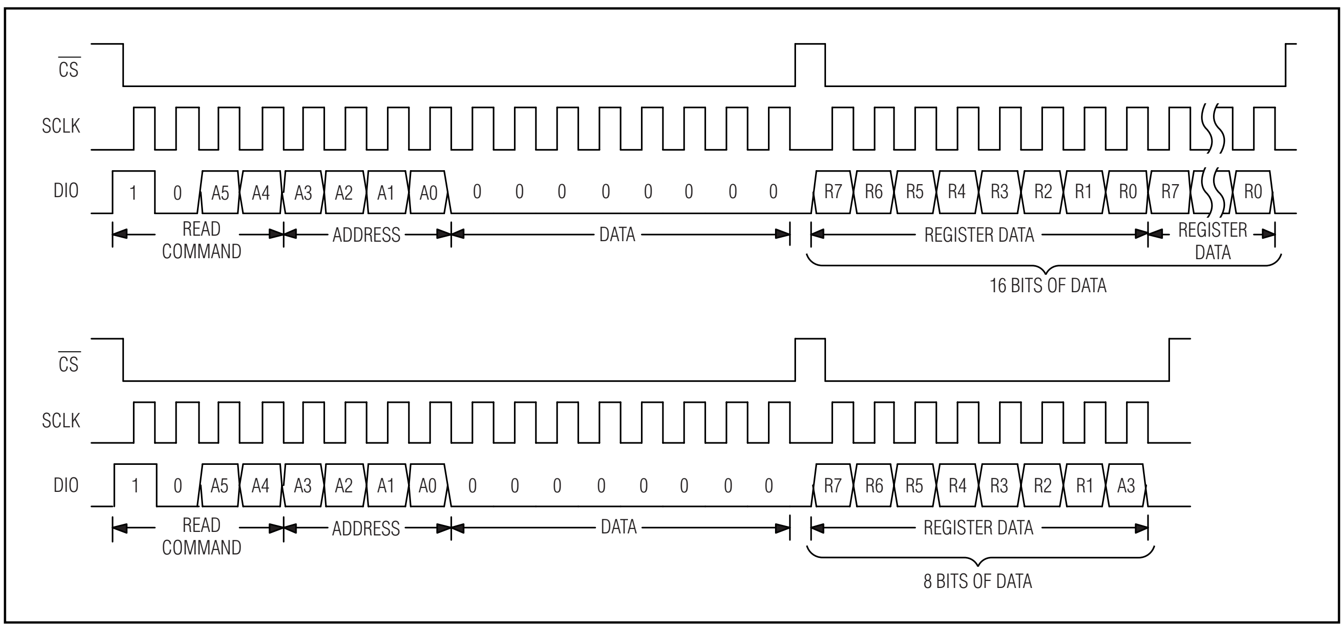

Figure 9. Read Command on a 3-Wire Serial Interface

DIO is selected as an output of the MAX7032 for the following $\overline{CS}$ cycle whenever a READ command is received. The CPU must tri-state the DIO line on the cycle of $\overline{CS}$ that follows a read command, so the MAX7032 can drive the data output line. Figure 9 shows the diagram of the 3-wire interface. Note that the user can choose to send either 16 cycles of SLCK or just eight cycles as all the registers are 8-bits wide. The user must drive DIO low at the end of the read sequence.

The MASTER RESET command (0x3) (see Table 2) sends a reset signal to all the internal registers of the MAX7032 just like a power-off and power-on sequence would do. The reset signal remains active for as long as $\overline{CS}$ is high after the command is sent.

Table 4. Register Configuration

NAME (ADDRESS)	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
POWER[7:0] (0x00)	LNA	AGC	MIXER	BaseB	PkDet	PA	RSSIO	X
CONTRL[7:0] (0x01)	AGCLK	GAIN	TRK_EN	—	PCAL	FCAL	CKOUT	SLEEP
CONF0[7:0] (0x02)	Mode	T/$\overline{R}$	MGAIN	DRX	OFPS1	OFPS0	ONPS1	ONPS0
CONF1[7:0] (0x03)	—	ACAL	CLKOF	CDIV1	CDIV0	DT2	DT1	DT0
OSC[7:0] (0x05)	OSC7	OSC6	OSC5	OSC4	OSC3	OSC2	OSC1	OSC0
t_{OFF}[15:8] (0x06)	t_{OFF} 15	t_{OFF} 14	t_{OFF} 13	t_{OFF} 12	t_{OFF} 11	t_{OFF} 10	t_{OFF} 9	t_{OFF} 8
t_{OFF} [7:0] (0x07)	t_{OFF} 7	t_{OFF} 6	t_{OFF} 5	t_{OFF} 4	t_{OFF} 3	t_{OFF} 2	t_{OFF} 1	t_{OFF} 0
t_{CPU}[7:0] (0x08)	t_{CPU} 7	t_{CPU} 6	t_{CPU} 5	t_{CPU} 4	t_{CPU} 3	t_{CPU} 2	t_{CPU} 1	t_{CPU} 0
t_{RF}[15:8] (0x09)	t_{RF} 15	t_{RF} 14	t_{RF} 13	t_{RF} 12	t_{RF} 11	t_{RF} 10	t_{RF} 9	t_{RF} 8
t_{RF} [7:0] (0x0A)	t_{RF} 7	t_{RF} 6	t_{RF} 5	t_{RF} 4	t_{RF} 3	t_{RF} 2	t_{RF} 1	t_{RF} 0
t_{ON}[15:8] (0x0B)	t_{ON} 15	t_{ON} 14	t_{ON} 13	t_{ON} 12	t_{ON} 11	t_{ON} 10	t_{ON} 9	t_{ON} 8
t_{ON} [7:0] (0x0C)	t_{ON} 7	t_{ON} 6	t_{ON} 5	t_{ON} 4	t_{ON} 3	t_{ON} 2	t_{ON} 1	t_{ON} 0
TxLOW[15:8] (0x0D)	TxL15	TxL14	TxL13	TxL12	TxL11	TxL10	TxL9	TxL8
TxLOW[7:0] (0x0E)	TxL7	TxL6	TxL5	TxL4	TxL3	TxL2	TxL1	TxL0
TxHIGH[15:8] (0x0F)	TxH15	TxH14	TxH13	TxH12	TxH11	TxH10	TxH9	TxH8
TxHIGH[7:0] (0x10)	TxH7	TxH6	TxH5	TxH4	TxH3	TxH2	TxH1	TxH0
STATUS[7:0] (0x1A)	LCKD	GAINS	CLKON	0	0	0	PCALD	FCALD

Continuous Receive Mode (DRX = 0)

In continuous receive mode, individual analog modules can be powered on directly through the power configuration register (register 0x00). The SLEEP bit (bit 0 in register 0x01) overrides the power configuration registers and puts the device into deep-sleep mode when set. It is also necessary to write the frequency divisor of the external crystal in the oscillator frequency register (register 0x05) to optimize image rejection and to enable accurate calibration sequences for the polling timer and the FSK demodulator. This number is the integer result of f_{XTAL} / 100kHz.

If the FSK receive function is selected, it is necessary to perform an FSK calibration to allow operation; otherwise, the demodulator is saturated. Polling timer calibration is not necessary. See the *Calibration section* for more information.

Discontinuous Receive Mode (DRX = 1)

In the discontinuous receive mode (DRX = 1), the receiver modules set to logic 1 by the power register (0x00) of the MAX7032 toggle between OFF and ON, according to internal timers t_{OFF}, t_{CPU}, t_{RF}, and t_{ON}. It is also necessary to write the frequency divisor of the external crystal in the oscillator frequency register (register 0x05). This number is the integer result of f_{XTAL} / 100kHz. Before entering the discontinuous receive mode for the first time, it is also necessary to calibrate the timers (see the *Calibration section*).

The MAX7032 uses a series of internal timers (t_{OFF}, t_{CPU}, t_{RF}, and t_{ON}) to control its power-up sequence. The timer sequence begins when both $\overline{CS}$ and DIO are one. The MAX7032 has an internal pullup on the DIO pin, so the user must tri-state the DIO line when $\overline{CS}$ goes high.

The external CPU can then go to a sleep mode during t_{OFF}. A high-to-low transition on DIO, or a low level on DIO serves as the wake-up signal for the CPU, which must then start its wake-up procedure, and drive DIO low before t_{LOW} expires (t_{CPU} + t_{RF} + t_{ON}). Once t_{RF} expires and t_{ON} is active, the MAX7032 enables the data output. The CPU must then keep DIO low for as long as it may need to analyze any received data. Releasing DIO after t_{ON} expires causes the MAX7032 to pull up DIO, reinitiating the t_{OFF} timer.

Table 5. Power-Configuration Register (Address: 0x00)

BIT ID	BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
LNA	LNA enable	7	1 = Enable LNA 0 = Disable LNA
AGC	AGC enable	6	1 = Enable AGC 0 = Disable AGC
MIXER	Mixer enable	5	1 = Enable mixer 0 = Disable mixer
BaseB	Baseband enable	4	1 = Enable baseband 0 = Disable baseband
PkDet	Peak-detector enable	3	1 = Enable peak detector 0 = Disable peak detector
PA	Transmitter PA enable	2	1 = Enable PA 0 = Disable PA
RSSIO	RSSI amplifier enable	1	1 = Enable buffer 0 = Disable buffer
X	None	0	Not used

Table 6. Control Register (Address: 0x01)

BIT ID	BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
AGCLK	AGC locking feature	7	1 = Enable AGC lock 0 = Disable AGC lock
GAIN	Gain state	6	1 = Force manual high-gain state if MGAIN = 1 0 = Force manual low-gain state if MGAIN = 1
TRK_EN	Manual peak-detector tracking	5	1 = Force manual peak-detector tracking 0 = Release peak-detector tracking
X	None	4	Not used
PCAL	Polling timer calibration	3	1 = Perform polling timer calibration Automatically reset to zero once calibration is completed
FCAL	FSK calibration	2	1 = Perform FSK calibration Automatically reset to zero once calibration is completed
CKOUT	Crystal clock output enable	1	1 = Enable crystal clock output 0 = Disable crystal clock output
SLEEP	Sleep mode	0	1 = Deep-sleep mode, regardless the state of ENABLE pin 0 = Normal operation

Table 7. Configuration 0 Register (Address: 0x02)

BIT ID	BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
MODE	FSK or ASK modulation	7	1 = Enable FSK for both receive and transmit 0 = Enable ASK for both receive and transmit
$T/\overline{R}$	Transmit or receive	6	1 = Enable transmit mode of the transceiver, regardless the state of pin $T/\overline{R}$ 0 = Enable receive mode of the transceiver when pin $T/\overline{R}$ = 0
MGAIN	Manual gain mode	5	1 = Enable manual-gain mode 0 = Disable manual-gain mode
DRX	Discontinuous receive mode	4	1 = Enable DRX 0 = Disable DRX
OFPS1	Off-timer prescaler	3	Sets the time base for the off timer (see the *Off Timer* section)
OFPS0	Off-timer prescaler	2	
ONPS1	On-timer prescaler	1	Sets the time base for the on timer (see the *On Timer* section)
ONPS0	On-timer prescaler	0	

Table 8. Configuration 1 Register (Address: 0x03)

BIT ID	BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
X	None	7	Not used
ACAL	Automatic FSK calibration	6	1 = Enable automatic FSK calibration approximately once every 60s 0 = Disable automatic FSK calibration
CLKOF	Continuous clock output (even during t_{OFF} or when EN pin is low)	5	1 = Enable continuous clock output when CKOUT = 1 0 = Continuous clock output; if CKOUT = 1, clock output is active during T_{ON} (DRX mode) or when EN pin is high (continuous receive mode)
CDIV1	Crystal divider	4	CLKOUT crystal-divider MSB
CDIV0	Crystal divider	3	CLKOUT crystal-divider LSB
DT2	AGC dwell timer	2	AGC dwell timer MSB
DT1	AGC dwell timer	1	AGC dwell timer
DT0	AGC dwell timer	0	AGC dwell timer LSB

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Table 9. Status Register (Read Only) (Address: 0x1A)

BIT ID	BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
LCKD	Lock detect	7	1 = Internal PLL is locked 0 = Internal PLL is not locked so the MAX7032 does not receive or transmit data
GAINS	AGC gain state	6	1 = LNA in high-gain state 0 = LNA in low-gain state
CLKON	Clock/crystal alive	5	1 = Valid clock at crystal inputs 0 = No valid clock signal seen at the crystal inputs
X	None	4	Zero
X	None	3	Zero
X	None	2	Zero
PCALD	Polling timer calibration done	1	1 = Polling timer calibration is completed 0 = Polling timer calibration is in progress or not completed
FCALD	FSK calibration done	0	1 = FSK calibration is completed 0 = FSK calibration is in progress or not completed

Table 10. Clock Output Divider Ratio Configuration

CKOUT	CDIV1	CDIV0	CLOCKOUT FREQUENCY
0	X	X	Disabled at logic 0
1	0	0	f_{XTAL}
1	0	1	f_{XTAL} / 2
1	1	0	f_{XTAL} / 4
1	1	1	f_{XTAL} / 8

Oscillator Frequency Register (Address 0x05)

The MAX7032 has an internal frequency divider that divides down the crystal frequency to 100kHz. The MAX7032 uses the 100kHz clock signal when calibrating itself and also to set image-rejection frequency. The hexadecimal value written to the oscillator frequency register is the nearest integer result of f_{XTAL} / 100kHz.

For example, if data is being received at 315MHz, the crystal frequency is 12.67917MHz. Dividing the crystal frequency by 100kHz and rounding to the nearest integer gives 127, or 0x7F hex. So for 315MHz, 0x7F would be written to the oscillator frequency register.

AGC Dwell Timer (Address 0x03)

The AGC dwell timer holds the AGC in low-gain state for a set amount of time after the power level drops below the AGC switching threshold. After that set amount of time, if the power level is still below the AGC threshold, the LNA goes into high-gain state. This is important for ASK since the modulated data may have a high level above the threshold and a low level below the threshold, which without the dwell timer would cause the AGC to switch on every bit.

The AGC dwell time is dependent on the crystal frequency and the bit settings of the AGC dwell timer. To calculate the dwell time, use the following equation:

$$\text{Dwell Time} = \frac{2^K}{f_{XTAL}}$$

where K is an odd integer in decimal from 9 to 23; see Table 11.

To calculate the value of K, use the following equation and use the next odd integer higher than the calculated result:

$$K \geq 3.3 \times \log_{10} (\text{Dwell Time} \times f_{XTAL})$$

For Manchester Code (50% duty cycle), set the dwell time to at least twice the bit period. For NRZ data, set the dwell to greater than the period of the longest string of zeros or ones. For example, using Manchester Code at 315MHz (f_{XTAL} = 12.679MHz) with a data rate of 4kbps (bit period = 125µs), the dwell time needs to be greater than 250µs:

$$K \geq 3.3 \times \log_{10} (250\mu s \times 12.679MHz) \approx 11.553$$

Choose the register value to be the next odd integer value higher than 11.553, which is K = 13. The default value of the AGC dwell timer on power-up or rest is zero (K = 9).

Table 11. AGC Dwell Timer Configuration (Address 0x03)

DT2	DT1	DT0	DESCRIPTION
0	0	0	K = 9
0	0	1	K = 11
0	1	0	K = 13
0	1	1	K = 15
1	0	0	K = 17
1	0	1	K = 19
1	1	0	K = 21
1	1	1	K = 23

Calibration

The MAX7032 must be calibrated to ensure accurate timing of the off timer in discontinuous receive mode or when receiving FSK signals. The first step in calibration is ensuring that the oscillator frequency register (register: 0x05) has been programmed with the correct divisor value (see the *Oscillator Frequency Register* section). Next, enable the mixer to turn the crystal driver on.

Calibrate the polling timer by setting PCAL = 1 in the control register (register 0x01, bit 3). Upon completion, the PCALD bit in the status register (register 0x1A, bit 1) is 1, and the PCAL bit is reset to zero. If using the MAX7032 in continuous receive mode, polling timer calibration is not needed.

To calibrate the FSK receiver, set FCAL = 1. Upon completion, the FCALD bit in the status register (register 0x08) is one, and the FCAL bit is reset to zero.

When in continuous receive mode and receiving FSK data, recalibrate the FSK receiver after a significant change in temperature or supply voltage. An autocal feature is provided that performs a calibration every minute (ACAL bit, Table 8). When in discontinuous receive mode, the polling timer and FSK receiver (if enabled) are automatically calibrated every wake-up cycle.

Off Timer (t_{OFF})

The off timer, t_{OFF} (see Figure 10), is a 16-bit timer that is configured using register 0x06 for the upper byte, register 0x07 for the lower byte, and bits OFPS1 and OFPS0 in the configuration 0 register (register 0x02, bit 3 and bit 2, respectively). Table 12 summarizes the configuration of the t_{OFF} timer. The OFPS1 and OFPS0 bits set the size of the shortest time possible (t_{OFF} time base). The data written to the t_{OFF} registers (register 0x06 and register 0x07) are multiplied by the time base to give the total t_{OFF} time. See the example below. On power-up, the off-timer registers are reset to zero and must be written before using DRX mode.

Table 12. Off-Timer (t_{OFF}) Configuration

OFPS1	OFPS0	t_{OFF} TIME BASE	MIN t_{OFF} REG 0x06 = 0x00; REG 0x07 = 0x01	MAX t_{OFF} REG 0x06 = 0xFF; REG 0x07 = 0xFF
0	0	120µs	120µs	7.86s
0	1	480µs	480µs	31.46s
1	0	1920µs	1.92ms	2 min 6s
1	1	7680µs	7.68ms	8 min 23s

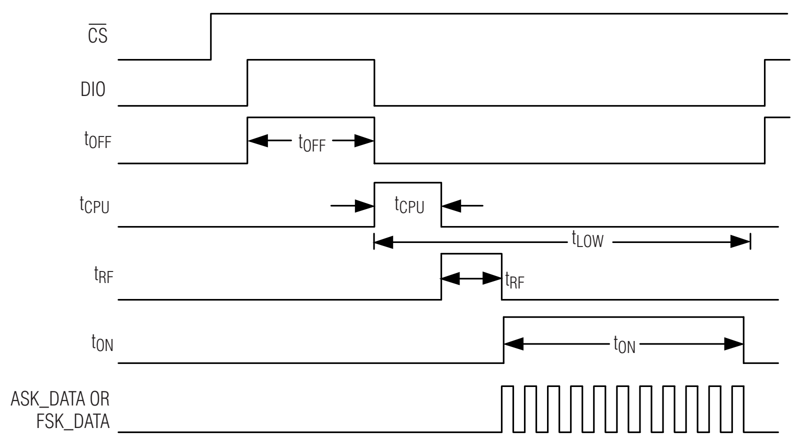


Figure 10. DRX Mode Sequence of the MAX7032

Set OFPS1 to be 1 and OFPS0 to be 1. That sets the t_{OFF} time base (1 LSB) to be 7680µs. Set REG 0x06 and REG 0x07 to be FFFF, which is 65535 in decimal. Therefore, the total t_{OFF} is:

$$t_{OFF} = 7680µs \times 65535 = 8min\ 23s$$

During t_{OFF}, the MAX7032 is operating with very low supply current (23.4µA typ), where all its modules are turned off, except for the t_{OFF} timer itself. Upon completion of the t_{OFF} time, the MAX7032 signals the user by asserting DIO low.

CPU Recovery Timer (t_{CPU})

The CPU recovery timer, t_{CPU} (see Figure 10) is used to delay power up of the MAX7032, thereby providing extra power savings and giving the CPU time to complete its own power-on sequence. The CPU is signaled to begin powering up when the DIO line is pulled low by the MAX7032 at the end of t_{OFF}. Then, t_{CPU} begins counting, while DIO is held low by the MAX7032. At the end of t_{CPU}, the t_{RF} counter begins.

t_{CPU} is an 8-bit timer, configured through register 0x08. The possible t_{CPU} settings are summarized in Table 13. The data written to the t_{CPU} register (register 0x08) is multiplied by 120µs to give the total t_{CPU} time. See the example below. On power-up, the CPU timer register is reset to zero and must be written before using DRX mode.

Set REG 0x08 to be FF in hex, which is 255 in decimal. Therefore, the total t_{CPU} is:

$$t_{CPU} = 120µs \times 255 = 30.6ms$$

RF Settling Timer (t_{RF})

The RF settling timer, t_{RF} (see Figure 10), allows the RF sections of the MAX7032 to power up and stabilize before ASK or FSK data is received. t_{RF} begins counting once t_{CPU} has expired. At the beginning of t_{RF}, the modules selected in the power control register (register 0x00) are all powered up and the peak detectors are in the track mode and have the t_{RF} period to settle.

t_{RF} is a 16-bit timer, configured through register 0x09 (upper byte) and register 0x0A (lower byte). The possible t_{RF} settings are listed in Table 14. The data written to the t_{RF} register (register 0x09 and register 0x0A) are multiplied by 120µs to give the total t_{RF} time. See the example in the *CPU Recovery Time* (*t_{CPU}*) section. On power-up, the RF timer registers are reset to zero and must be written before using DRX mode.

Table 13. CPU Recovery Timer (t_{CPU}) Configuration

TIME BASE (µs)	MIN t_{CPU} REG 0x08 = 0x01 (µs)	MAX t_{CPU} REG 0x08 = 0xFF (ms)
120	120	30.6

Table 14. RF Settling Timer (t_{RF}) Configuration

t_{RF} TIME BASE (µs)	MIN t_{RF} REG 0x09 = 0x00 REG 0x0A = 0x01 (µs)	MAX t_{RF} REG 0x09 = 0xFF REG 0x0A = 0xFF (s)
120	120	7.86

Table 15. On-Timer (t_{ON}) Configuration

ONPS1	ONPS0	t_{ON} TIME BASE	MIN t_{ON} REG 0x0B = 0x00 REG 0x0C = 0x01	MAX t_{ON} REG 0x0B = 0xFF REG 0x0C = 0xFF
0	0	120µs	120µs	7.86s
0	1	480µs	480µs	31.46s
1	0	1920µs	1.92µs	2 min 6s
1	1	7680µs	7.68µs	8 min 23s

On Timer (t_{ON})

The on timer, t_{ON} (see Figure 10), is a 16-bit timer that is configured through register 0x0B for the upper byte, register 0x0C for the lower byte (Table 15). The information stored in this timer provides an additional way to control the duration of the on time of the receiver.

The CPU must begin driving DIO low any time during $t_{LOW} = t_{CPU} + t_{RF} + t_{ON}$. If the CPU fails to drive DIO low at the end of t_{ON}, DIO is pulled high through the internal pullup resistor, and the time sequence is restarted, leaving the MAX7032 powered down. Any time the DIO line is driven high while the DRX = 1, the DRX sequence is initiated, as defined in Figure 10. In the event that the CPU is processing data, after t_{ON} expires, the CPU should keep the MAX7032 awake by holding the DIO line low.

The data written to the t_{ON} register (register 0x0B and register 0x0C) are multiplied by the t_{ON} time base (Table 15) to give the total t_{ON} time. See the example in the *Off Timer* (*t_{OFF}*) section. On power-up, the on-timer register is reset to zero and must be written before using DRX mode.

Transmitter Low-Frequency Register (TxLOW)

The TxLOW register sets the divider information of the fractional-N synthesizer for the lower transmit frequency in FSK mode. See the example given in the *Fractional-N PLL* section. In ASK mode, TxLOW determines the carrier frequency.

Transmitter High-Frequency Register (TxHIGH)

The TxHIGH register sets the divider information of the fractional-N synthesizer for the upper transmit frequency in the FSK mode. In ASK mode, the content of TxHIGH is not used. The 16-bit register contains the binary representation of the Tx PLL divider ratio, which is shown in the example in the *Fractional-N PLL* section.

Applications Information

Output Matching to 50Ω

When matched to a 50Ω system, the MAX7032's PA is capable of delivering +10dBm of output power at V_{DD} = +2.7V. The output of the PA is an open-drain transistor that requires external impedance matching and pullup inductance for proper biasing. The pullup inductance from the PA to PAV_{DD} serves three main purposes: it resonates the capacitive PA output, provides biasing for the PA, and becomes a high-frequency choke to prevent RF energy from coupling into V_{DD}. The network also forms a bandpass filter that provides attention for the higher order harmonics.

Output Matching to PC Board Loop Antenna

In most applications, the MAX7032 must be impedance matched to a small-loop antenna. The antenna is usually fabricated out of a copper trace on a PC board in a rectangular, circular, or square pattern. The antenna has an impedance that consists of a lossy component and a radiative component. To achieve high radiating efficiency, the radiative component should be as high as possible, while minimizing the lossy component. In addition, the loop antenna has an inherent loop inductance associated with it (assuming the antenna is terminated to ground). For example, in a typical application, the radiative impedance is less than 0.5Ω, the lossy impedance is less than 0.7Ω, and the inductance is approximately 50nH to 100nH.

Layout Considerations

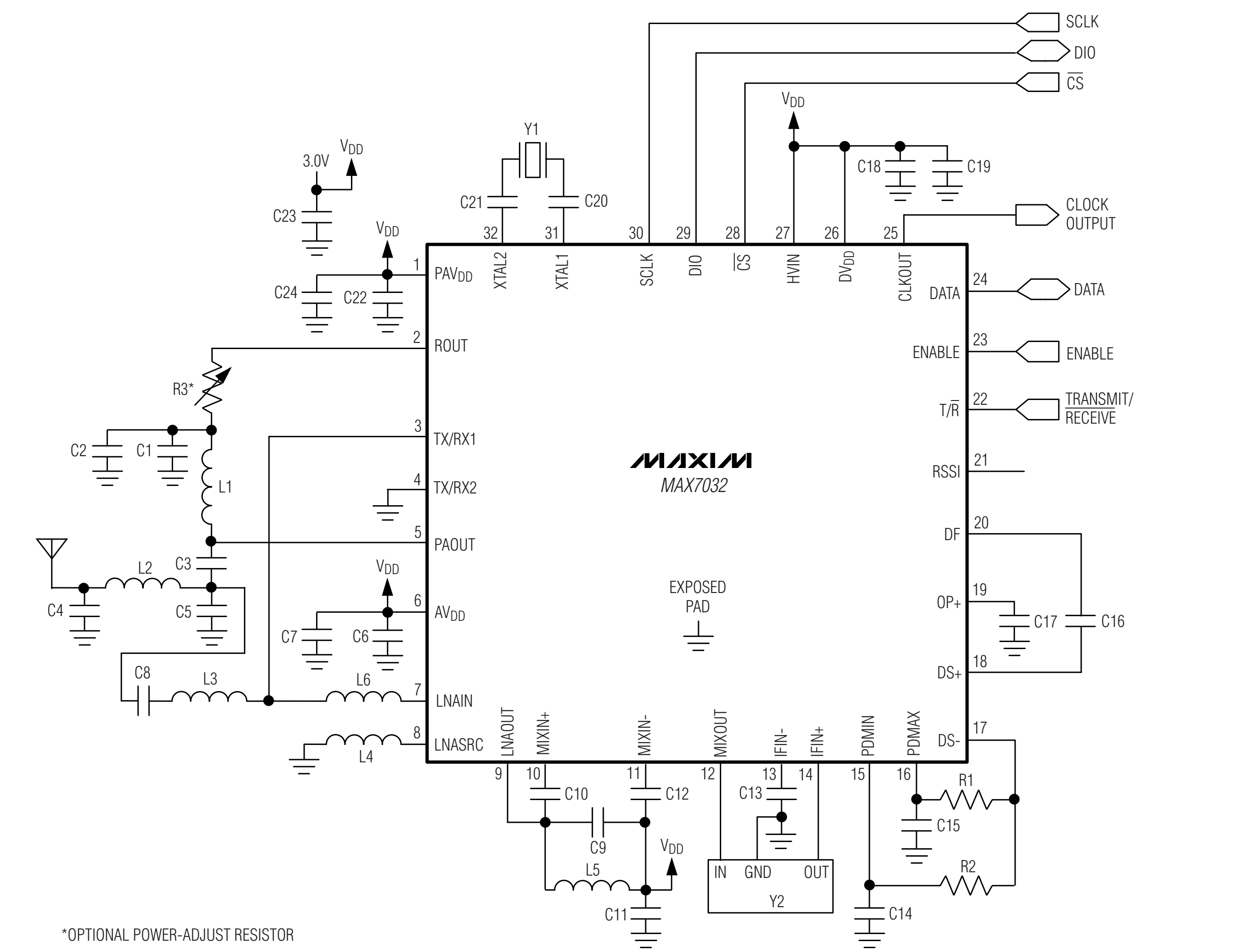
A properly designed PC board is an essential part of any RF/microwave circuit. On high-frequency inputs and outputs, use controlled-impedance lines and keep them as short as possible to minimize losses and radiation. At high frequencies, trace lengths that are on the order of λ / 10 or longer act as antennas, where λ is the wavelength.

Low-Cost, Crystal-Based, Programmable, ASK/FSK Transceiver with Fractional-N PLL

Keeping the traces short also reduces parasitic inductance. Generally, 1in of PC board trace adds about 20nH of parasitic inductance. The parasitic inductance can have a dramatic effect on the effective inductance of a passive component. For example, a 0.5in trace connecting to a 100nH inductor adds an extra 10nH of inductance, or 10%.

To reduce parasitic inductance, use wider traces and a solid ground or power plane below the signal traces. Also, use low-inductance connections to the ground plane, and place decoupling capacitors as close to all V_{DD} pins and HV_{IN} as possible.

Typical Application Circuit



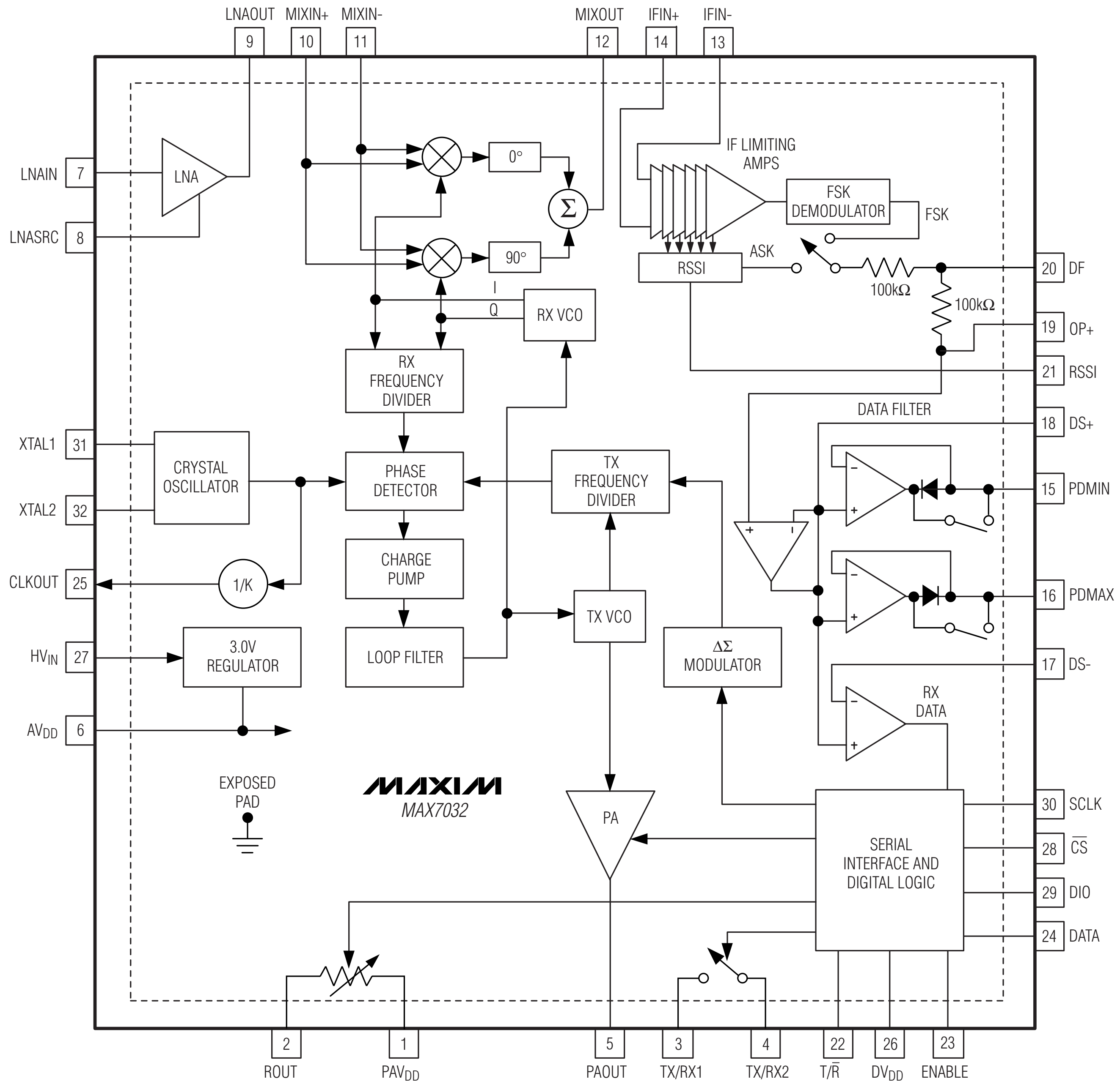
*OPTIONAL POWER-ADJUST RESISTOR

Table 16. Component Values for Typical Application Circuit

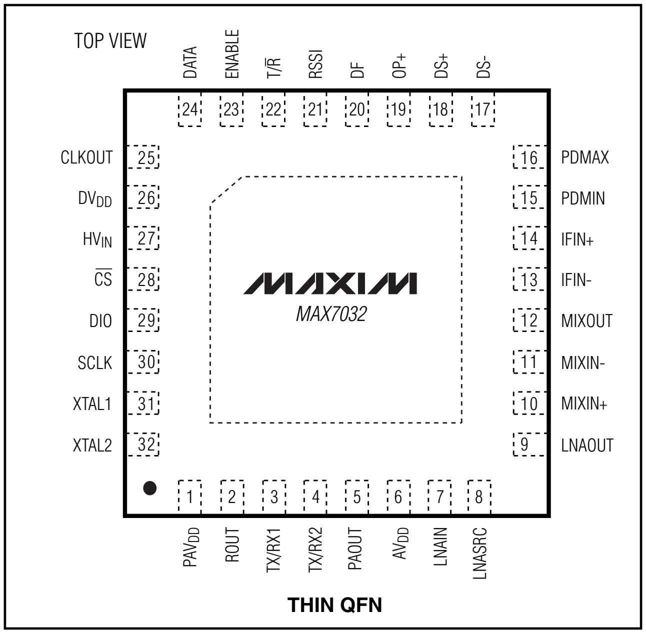
COMPONENT	VALUE FOR 433.92MHz RF	VALUE FOR 315MHz RF	DESCRIPTION
C1	220pF	220pF	10%
C2	680pF	680pF	10%
C3	6.8pF	12pF	5%
C4	6.8pF	10pF	5%
C5	10pF	22pF	5%
C6	220pF	220pF	10%
C7	0.1µF	0.1µF	10%
C8	100pF	100pF	5%
C9	1.8pF	2.7pF	±0.1pF
C10	100pF	100pF	5%
C11	220pF	220pF	10%
C12	100pF	100pF	5%
C13	1500pF	1500pF	10%
C14	0.047µF	0.047µF	10%
C15	0.047µF	0.047µF	10%
C16	470pF	470pF	10%
C17	220pF	220pF	10%
C18	220pF	220pF	10%
C19	0.01µF	0.01µF	10%
C20	100pF	100pF	5%
C21	100pF	100pF	5%
C22	220pF	220pF	10%
C23	0.01µF	0.01µF	10%
C24	0.01µF	0.01µF	10%
L1	22nH	27nH	Coilcraft 0603CS
L2	22nH	30nH	Coilcraft 0603CS
L3	22nH	30nH	Coilcraft 0603CS
L4	10nH	12nH	Coilcraft 0603CS
L5	16nH	30nH	Murata LQW18A
L6	68nH	100nH	Coilcraft 0603CS
R1	100kΩ	100kΩ	5%
R2	100kΩ	100kΩ	5%
R3	0Ω	0Ω	—
Y1	17.63416MHz	12.67917MHz	Crystal, 4.5pF load capacitance
Y2	10.7MHz ceramic filter	10.7MHz ceramic filter	Murata SFECV10.7 series

Note: *Component values vary depending on PC board layout.*

Functional Diagram



Pin Configuration



Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
32 Thin QFN-EP	T3255-3	**21-0140**

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/05	Initial release	—
1	6/09	Made correction in *Power Amplifier (PA)* section	16