MAX2104CCM
Rev. A

RELIABILITY REPORT

FOR

MAX2104CCM

PLASTIC ENCAPSULATED DEVICES

January 28, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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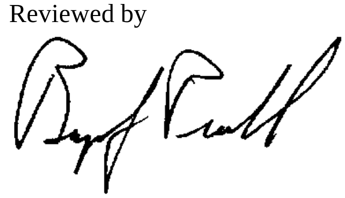


Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX2104 Successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX2104 low-cost direct-conversion tuner IC is designed for use in digital direct-broadcast satellite (DBS) television set-top box units. Its direct-conversion architecture reduces system cost compared to devices with IF-based architectures. The MAX2104 directly converts L-band signals to baseband signals using a broadband I/Q downconverter. The operating frequency range extends from 925MHz to 2175MHz.

The IC includes an LNA gain control, I and Q downconverting mixers, lowpass filters with gain control and frequency control, a local oscillator (LO) buffer with a 90° quadrature network, and a charge-pump based PLL for frequency control. The MAX2104 also has an on-chip LO, requiring only an external varactor-tuned LC tank for operation. The output of the LO drives the internal quadrature generator and dual modulus prescaler. An on-chip crystal amplifier drives a reference divider as well as a buffer amplifier to drive off-chip circuitry. The MAX2104 is offered in a 48-pin TQFP-EP package.

B. Absolute Maximum Ratings

Item	Rating
Vcc to GND	-0.5V to +7V
All other pins to GND	-0.3V to (VCC + 0.3V)
RF1+ to RF1-, RF2+ to RF2-, TANK+ to TANK-, IDC+ to IDC-, QDC+ to QDC-	+/-2V
IOUT_,QOUT_ to GND Short Circuit Duration	10s
PSOU+, PSOUT- to GND Short Circuit Duration	10s
Continuous Current (any pin)	20mA
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+150°C
Continuous Power Dissipation (TA = +70°C)	
48-Pin TQFP	1500mW
Derates above +70°C	
48-Pin TQFP	27mW/°C

II. Manufacturing Information

A. Description/Function: Direct-Conversion Tuner IC for Digital DBS Application

B. Process: GST2 – High Speed Double Poly-Silicon Bipolar Process

C. Number of Device Transistors:

D. Fabrication Location: Oregon, USA

E. Assembly Location: Malaysia

F. Date of Initial Production: January, 1999

III. Packaging Information

A. Package Type: **48-Lead TQFP**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.02mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-7001-0319

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 96 x 96

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Poly / Au

D. Backside Metallization: None

E. Minimum Metal Width: 2 microns (as drawn)

F. Minimum Metal Spacing: 2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 9823 \times 50 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 9.70 \times 10^{-9}$ λ = 9.70 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**) located on the Maxim website at http://www.maxim-ic.com .

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The WR31 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX2104CCM

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	50	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic Process/Package Data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

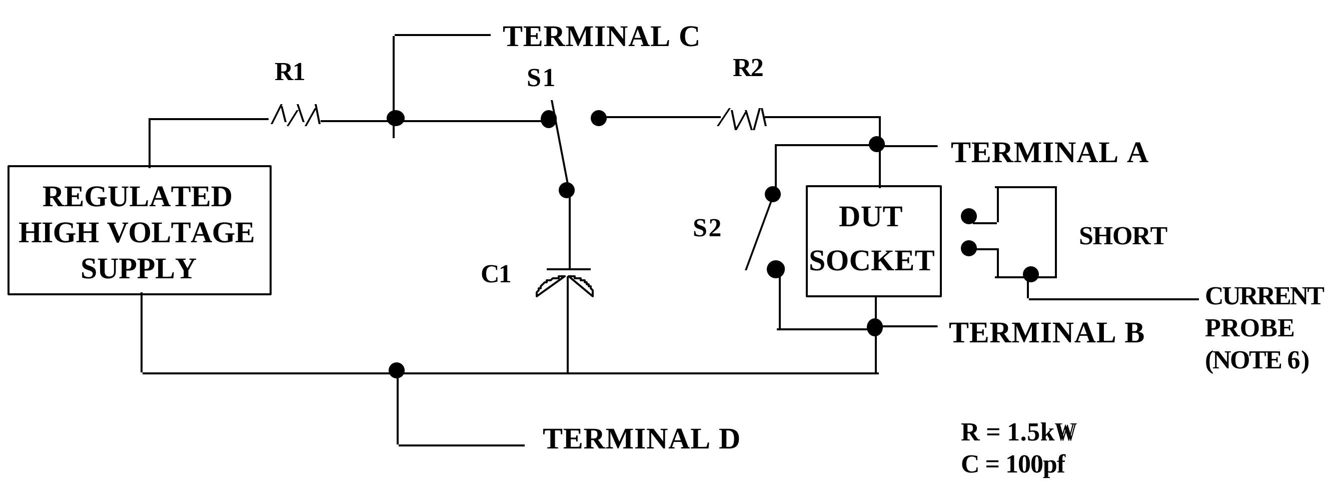
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

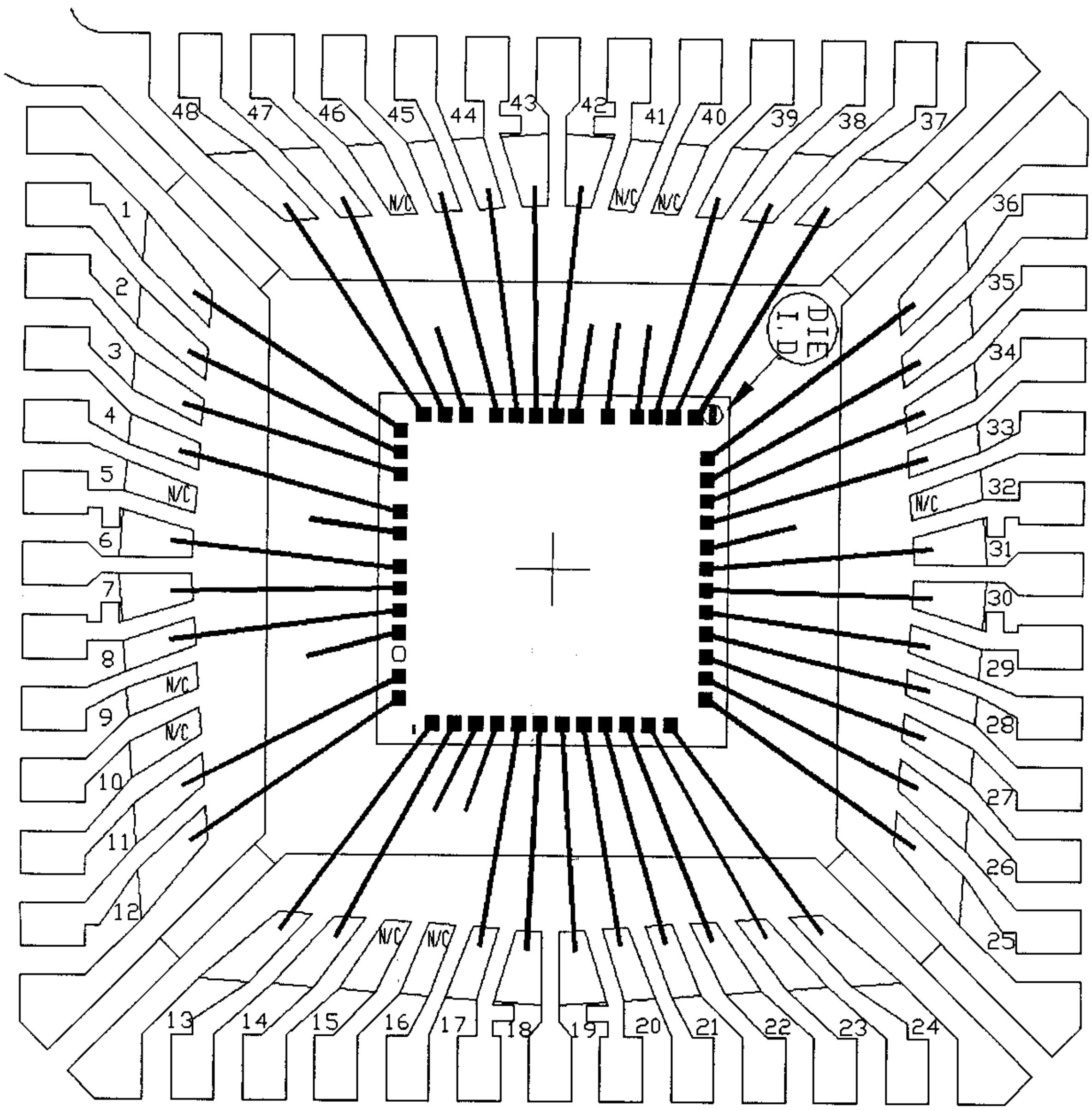
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: C48E-7		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 157x157	PKG. DESIGN			BUILDSHEET NUMBER: 05-7001-0319	REV.: C