19-1811; Rev 2; 4/09

EVALUATION KIT AVAILABLE

MAXIM

Dual-Output Step-Down DC-DC Converter for PDA/Palmtop Computers

General Description

The MAX1775 dual, step-down DC-DC converter generates both the main (+3.3V at over 2A) and core (+1.8V at up to 1.5A) supplies for a complete power solution for PDAs, subnotebooks, and other hand-held devices. The main output is adjustable from +1.25V to +5.5V. The core output is adjustable from 1V to 5V. Both switching converters operate at up to 1.25MHz for small external components and use synchronous rectifiers to achieve efficiencies up to 95%. Operation with up to 100% duty cycle provides the lowest possible dropout voltage to extend useful battery life.

The MAX1775 accepts inputs from +2.7V up to +28V, allowing use with many popular battery configurations as well as AC-DC wall adapters. Digital soft-start reduces battery current surges at power-up. Both the main and core converters have separate shutdown inputs. The MAX1775 comes in a small 16-pin QSOP package.

The MAX1775 evaluation kit is available to help reduce design time.

Features

- **Dual, High-Efficiency, Synchronous Rectified Step-Down Converter**
- **Main Power**
  - **Adjustable from +1.25V to +5.5V**
  - **Over 2A Load Current**
  - **Up to 95% Efficiency**
- **Core Power**
  - **Adjustable from 1V to 5V**
  - **Internal Switches**
  - **Up to 1.5A Load Current**
  - **Up to 92% Efficiency**
- **100% (max) Duty Cycle**
- **Up to 1.25MHz Switching Frequency**
- **Input Voltage Range from +2.7V to +28V**
- **170µA Quiescent Current**
- **5µA Shutdown Current**
- **Digital Soft-Start**
- **Independent Shutdown Inputs**

Applications

Hand-Held Computers

PDAs

Internet Access Tablets

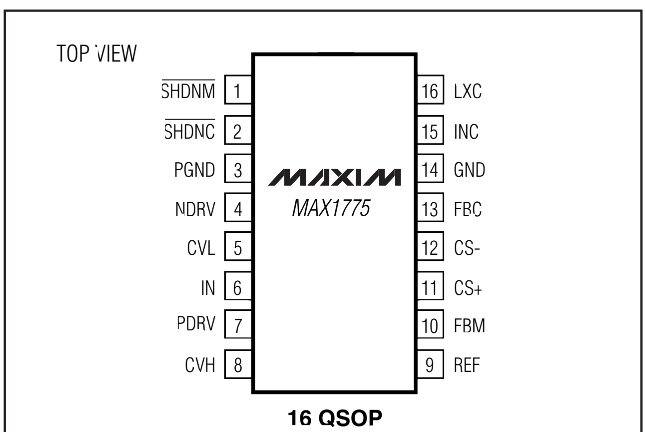
POS Terminals

Subnotebooks

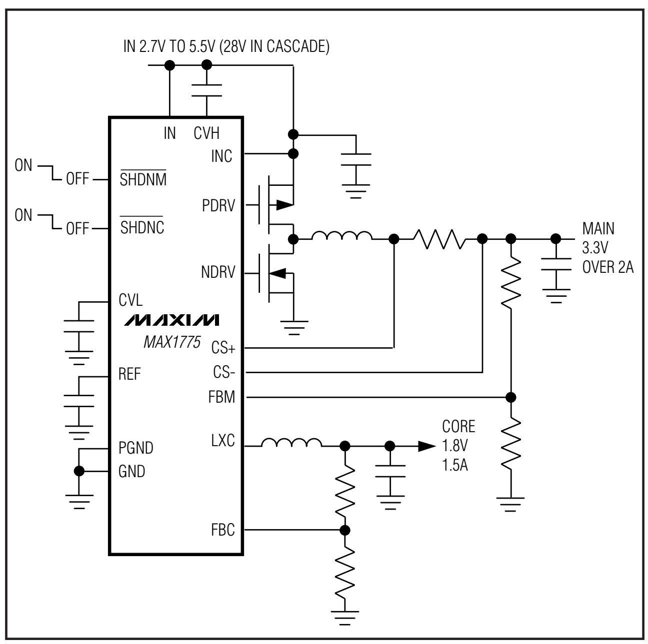
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1775EEE	-40°C to +85°C	16 QSOP

Pin Configuration



Typical Operating Circuit



Dual-Output Step-Down DC-DC Converter for PDA/Palmtop Computers

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDNM}$, CVH to GND.......................................-0.3V to +30V
IN to CVH, PDRV ....-0.3V to +6V
PDRV to GND..................................(V_{CVH} - 0.3V) to (V_{IN} + 0.3V)
PGND to GND ....-0.3V to +0.3V
All Other Pins to GND...-0.3V to +6V
Core Output Short Circuit...Continuous

Continuous Power Dissipation
16-Pin QSOP (derate 7.1mW/°C above +70°C)..........571mW
Operating Temperature ....-40°C to +85°C
Storage Temperature...-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +12V, V_{MAIN} = V_{INC} = V_{CS-} = V_{CS+} = +3.3V, V_{CORE} = +1.8V, Circuit of Figure 4, **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}		2.7		28	V
Input Quiescent Supply Current	I_{IN}	V_{FBM} = +1.5V, V_{FBC} = +1.5V, $V_{\overline{SHDNM}}$ = $V_{\overline{SHDNC}}$ = +3.3V		15	30	µA
CS- Quiescent Supply Current	I_{CS-}	V_{FBM} = +1.5V, V_{FBC} = +1.5V, $V_{\overline{SHDNM}}$ = $V_{\overline{SHDNC}}$ = +3.3V		110	220	µA
Core Regulator Quiescent Supply Current	I_{INC}	V_{FBM} = +1.5V, V_{FBC} = +1.5V, $V_{\overline{SHDNM}}$ = $V_{\overline{SHDNC}}$ = +3.3V		60	120	µA
IN Shutdown Supply Current		$\overline{SHDNM}$ = $\overline{SHDNC}$ = GND		5	30	µA
MAIN REGULATOR						
Main Output Voltage Adjust Range			1.25		5.5	V
FBM Regulation Threshold	V_{FBM}	$V_{(CS+ - CS-)}$ = 0 to +60mV, V_{IN} = +2.7V to +28V	1.21	1.25	1.29	V
FBM Input Current	I_{FBM}	V_{FBM} = +1.3V	-0.1		0.1	µA
Current-Limit Threshold	V_{CLM}	V_{CS+} - V_{CS-}	60	80	100	mV
Minimum Current-Limit Threshold	V_{MIN}	V_{CS+} - V_{CS-}	6	15	24	mV
Valley Current Threshold	V_{VALLEY}	V_{CS+} - V_{CS-}	40	50	60	mV
Zero Current Threshold	V_{ZERO}	V_{CS+} - V_{CS-}	0		15	mV
PDRV, NDRV Gate Drive Resistance		V_{CS-} = +3.3V, I_{LOAD} = 50mA		2	4.4	Ω
CS- to CVL Switch Resistance		I_{CVL} = 50mA		4.5	8	Ω
PDRV, NDRV Dead Time				50		ns
Maximum Duty Cycle			100			%
Minimum On-Time			200	400	650	ns
Minimum Off-Time			200	400	650	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +12V, V_{MAIN} = V_{INC} = V_{CS-} = V_{CS+} = +3.3V, V_{CORE} = +1.8V, Circuit of Figure 4, **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Maximum Duty Cycle			100		%
Minimum On-Time			200	650	ns
Minimum Off-Time			200	650	ns
CORE REGULATOR					
Input Voltage Range	V_{INC}		2.6	5.5	V
INC Undervoltage Lockout		V_{INC} rising	2.39	2.55	V
		V_{INC} falling	2.29	2.45	
Core Output Voltage Adjust Range			1.0	5.0	V
Maximum Core Load Current		(Note 1)	1		A
FBC Regulation Threshold	V_{FBC}	V_{INC} = +2.5V to +5.5V, I_{OUTC} = 0 to 200mA	0.97	1.03	V
FBC Input Current	I_{FBC}	V_{FBC} = +1.3V	-0.1	0.1	µA
Dropout Voltage (INC to LXC)		I_{OUTC} = 400mA		0.2	V
LXC Leakage Current	I_{LXC}	V_{INC} = +5.5V, V_{LXC} = 0 to +5.5V	-10	10	µA
LXC P-Channel, N-Channel On-Resistance				0.5	Ω
LXC P-Channel Current Limit			1200	3050	mA
LXC P-Channel Minimum Current			100	400	mA
LXC N-Channel Valley Current			880	2450	mA
LXC N-Channel Zero-Crossing Current			35	175	mA
Maximum Duty Cycle			100		%
Minimum On-Time			150	670	ns
Minimum Off-Time			150	670	ns
REFERENCE					
Reference Voltage	V_{REF}		1.22	1.27	V
Reference Load Regulation		I_{REF} = 0 to 50µA		10	mV
Reference Line Regulation		V_{CS-} = +2.5V to +5.5V, I_{REF} = 50µA		5	mV
Reference Sink Current	I_{REF}		10		µA
CVL, CVH REGULATORS					
CVL Output Voltage	V_{CVL}	I_{CVL} = 50mA, V_{IN} = +2.7V, V_{CS-} = 0V	2.6	3.1	V
CVH Output Voltage	V_{CVH}	V_{IN} = +4V, I_{CVH} = 25mA		V_{IN} - 2.8	V
		V_{IN} = +12V, I_{CVH} = 50mA		V_{IN} - 3.7	
CVL Undervoltage Lockout		V_{CVL} rising	2.40	2.55	V
		V_{CVL} falling	2.30	2.45	

Dual-Output Step-Down DC-DC Converter for PDA/Palmtop Computers

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +12V, V_{MAIN} = V_{INC} = V_{CS-} = V_{CS+} = +3.3V, V_{CORE} = +1.8V, Circuit of Figure 4, **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
$\overline{SHDNM}$, $\overline{SHDNC}$ Input Low Voltage					0.4	V
$\overline{SHDNM}$, $\overline{SHDNC}$ Input High Voltage			2.0			V
$\overline{SHDNM}$, $\overline{SHDNC}$ Input Low Current		$\overline{SHDNM}$ = $\overline{SHDNC}$ = GND	-1		1	µA
$\overline{SHDNC}$ Input High Current		$V_{\overline{SHDNC}}$ = +5.5V			5	µA
$\overline{SHDNM}$ Input High Current		$V_{\overline{SHDNM}}$ = +5V		2		µA
		$V_{\overline{SHDNM}}$ = +28V		15	30	

ELECTRICAL CHARACTERISTICS

(V_{IN} = +12V, V_{MAIN} = V_{INC} = V_{CS-} = V_{CS+} = +3.3V, V_{CORE} = +1.8V, Circuit of Figure 4, **T_A -40°C to +85°C,** unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Voltage	V_{IN}		2.7	28	V
Input Quiescent Supply Current	I_{IN}	V_{FBM} = +1.5V, V_{FBC} = +1.5V, $V_{\overline{SHDNM}}$ = $V_{\overline{SHDNC}}$ = +3.3V		30	µA
CS- Quiescent Supply Current	I_{CS-}	V_{FBM} = +1.5V, V_{FBC} = +1.5V, $V_{\overline{SHDNM}}$ = $V_{\overline{SHDNC}}$ = +3.3V		220	µA
Core Regulator Quiescent Supply Current	I_{INC}	V_{FBM} = +1.5V, V_{FBC} = +1.5V, $V_{\overline{SHDNM}}$ = $V_{\overline{SHDNC}}$ = +3.3V		120	µA
IN Shutdown Supply Current		$\overline{SHDNM}$ = $\overline{SHDNC}$ = GND		30	µA
MAIN REGULATOR					
Main Output Voltage Adjust Range			1.25	5.5	V
FBM Regulation Threshold	V_{FBM}	$V_{(CS+\ -\ CS-)}$ = 0 to +60mV, V_{IN} = +2.7V to +28V	1.21	1.29	V
FBM Input Current	I_{FBM}	V_{FBM} = +1.3V	-0.1	0.1	µA
Current-Limit Threshold	V_{CL}	V_{CS+} - V_{CS-}	60	100	mV
Minimum Current-Limit Threshold		V_{CS+} - V_{CS-}	6	24	mV
Valley Current Threshold		V_{CS+} - V_{CS-}	40	60	mV
Zero Current Threshold		V_{CS+} - V_{CS-}	0	15	mV
PDRV, NDRV Gate Drive Resistance		V_{CS-} = +3.3V		4.4	Ω
CS- to CVL Switch Resistance		I_{CVL} = 50mA		8	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +12V, V_{MAIN} = V_{INC} = V_{CS-} = V_{CS+} = +3.3V, V_{CORE} = +1.8V, Circuit of Figure 4, **T_A -40°C to +85°C,** unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Maximum Duty Cycle			100		%
Minimum On-Time			200	650	ns
Minimum Off-Time			200	650	ns
CORE REGULATOR					
Input Voltage Range	V_{INC}		2.6	5.5	V
INC Undervoltage Lockout		V_{INC} rising	2.39	2.55	V
		V_{INC} falling	2.29	2.45	
Core Output Voltage Adjust Range			1.0	5.0	V
Maximum Core Load Current		(Note 1)	1		A
FBC Regulation Threshold	V_{FBC}	V_{INC} = +2.5V to +5.5V, I_{OUTC} = 0 to 200mA	0.97	1.03	V
FBC Input Current	I_{FBC}	V_{FBC} = +1.3V	-0.1	0.1	µA
Dropout Voltage (INC to LXC)		I_{OUTC} = 400mA		0.2	V
LXC Leakage Current	I_{LXC}	V_{INC} = +5.5V, V_{LXC} = 0 to +5.5V	-10	10	µA
LXC P-Channel, N-Channel On-Resistance				0.5	Ω
LXC P-Channel Current Limit			1200	3050	mA
LXC P-Channel Minimum Current			100	400	mA
LXC N-Channel Valley Current			880	2450	mA
LXC N-Channel Zero-Crossing Current			35	175	mA
Maximum Duty Cycle			100		%
Minimum On-Time			150	670	ns
Minimum Off-Time			150	670	ns
REFERENCE					
Reference Voltage	V_{REF}		1.22	1.27	V
Reference Load Regulation		I_{REF} = 0 to 50µA		10	mV
Reference Line Regulation		V_{CS-} = +2.5V to +5.5V, I_{REF} = 50µA		5	mV
Reference Sink Current	I_{REF}		10		µA
CVL, CVH REGULATORS					
CVL Output Voltage	V_{CVL}	I_{CVL} = 50mA, V_{IN} = +2.7V, V_{CS-} = 0V	2.6	3.1	V
CVH Output Voltage	V_{CVH}	V_{IN} = +4V, I_{CVH} = 25mA		V_{IN} - 2.8	V
		V_{IN} = +12V, I_{CVH} = 50mA		V_{IN} - 3.7	
CVL Undervoltage Lockout		V_{CVL} rising	2.40	2.55	V
		V_{CVL} falling	2.30	2.45	

Dual-Output Step-Down DC-DC Converter for PDA/Palmtop Computers

ELECTRICAL CHARACTERISTICS (continued)

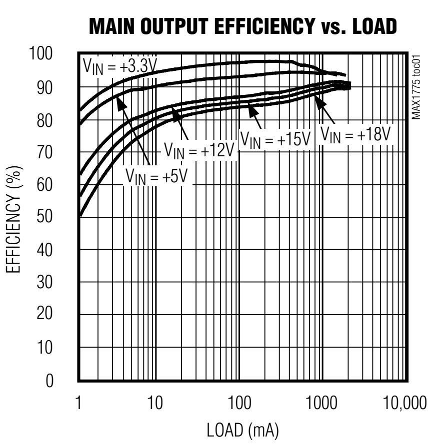
(V_{IN} = +12V, V_{MAIN} = V_{INC} = V_{CS-} = V_{CS+} = +3.3V, V_{CORE} = +1.8V, Circuit of Figure 4, **T_A -40°C to +85°C,** unless otherwise noted.) (Note 2)

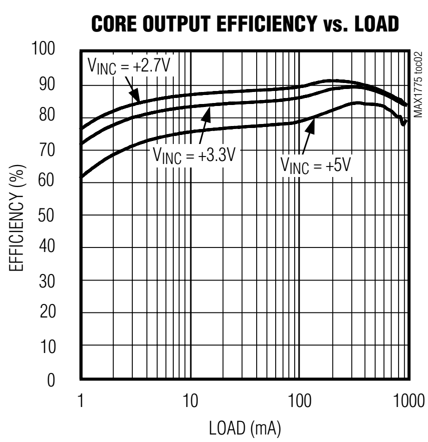
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
LOGIC INPUTS					
$\overline{SHDNM}$, $\overline{SHDNC}$ Input Low Voltage				0.4	V
$\overline{SHDNM}$, $\overline{SHDNC}$ Input High Voltage			2.0		V
$\overline{SHDNM}$, $\overline{SHDNC}$ Input Low Current		$\overline{SHDNM}$ = $\overline{SHDNC}$ = GND	-1	1	µA
$\overline{SHDNC}$ Input High Current		$V_{\overline{SHDNC}}$ = +5.5V		5	µA
$\overline{SHDNM}$ Input High Current		$V_{\overline{SHDNM}}$ = +28V		30	µA

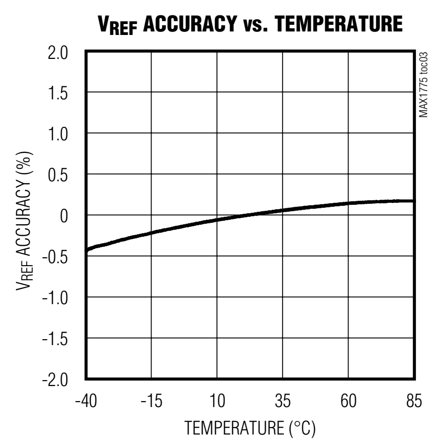
Note 1: This parameter is guaranteed based on the LXC P-channel current limit and the LXC N-channel valley current.
Note 2: Specifications to -40°C are guaranteed by design and not production tested.

Typical Operating Characteristics

(Circuit of Figure 1, V_{MAIN} = +3.3V, V_{CORE} = +1.8V, T_A = +25°C, unless otherwise noted.)





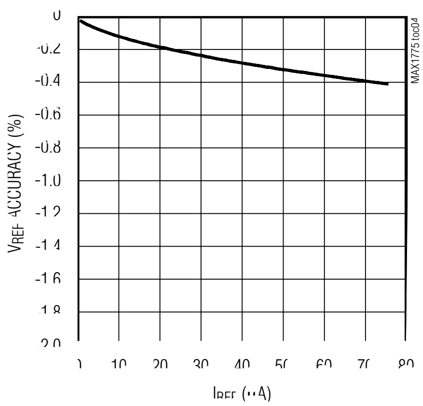


Dual-Output Step-Down DC-DC Converter for PDA/Palmtop Computers

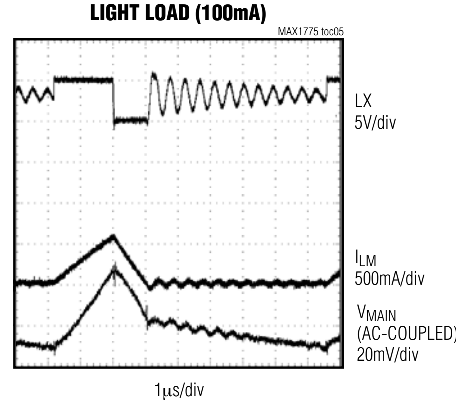
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{MAIN} = +3.3V, V_{CORE} = +1.8V, T_A = +25°C, unless otherwise noted.)

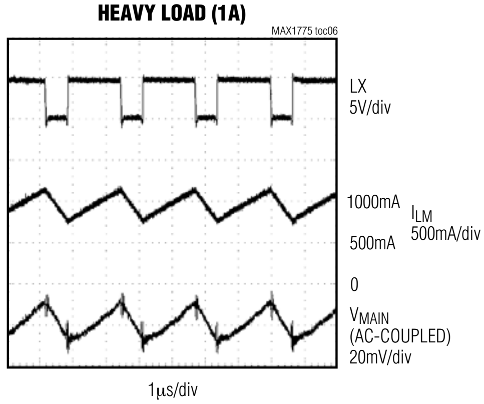
REFERENCE LOAD REGULATION



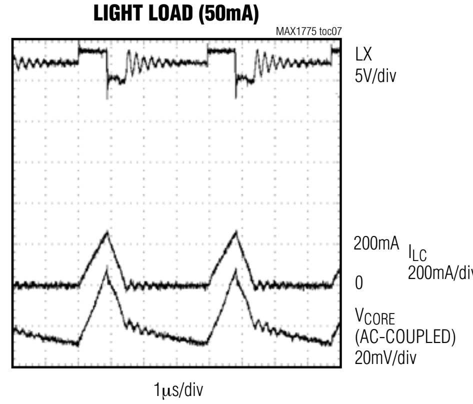
MAIN SWITCHING WAVEFORMS, LIGHT LOAD (100mA)



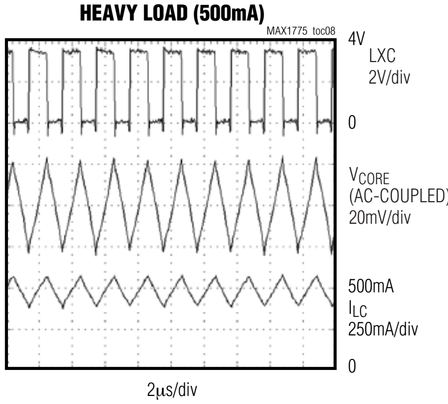
MAIN SWITCHING WAVEFORMS, HEAVY LOAD (1A)



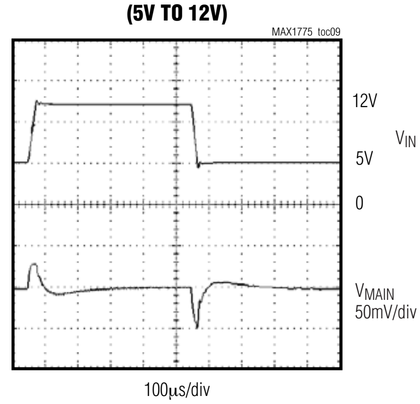
CORE SWITCHING WAVEFORMS, LIGHT LOAD (50mA)



CORE SWITCHING WAVEFORMS, HEAVY LOAD (500mA)



MAIN LINE-TRANSIENT RESPONSE (5V TO 12V)

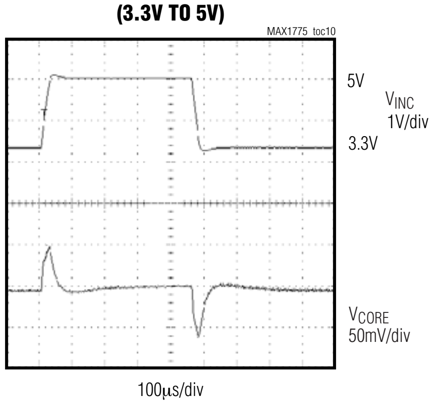


Dual-Output Step-Down DC-DC Converter for PDA/Palmtop Computers

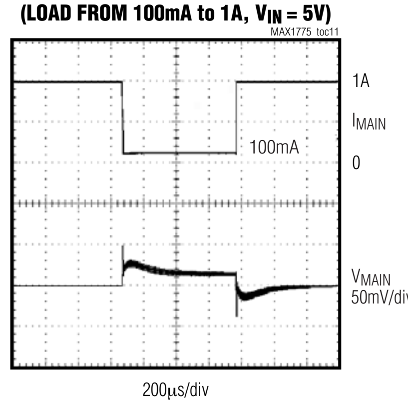
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{MAIN} = +3.3V, V_{CORE} = +1.8V, T_A = +25°C, unless otherwise noted.)

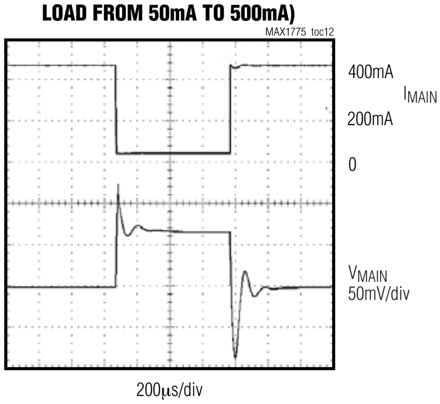
CORE LINE-TRANSIENT RESPONSE (3.3V TO 5V)



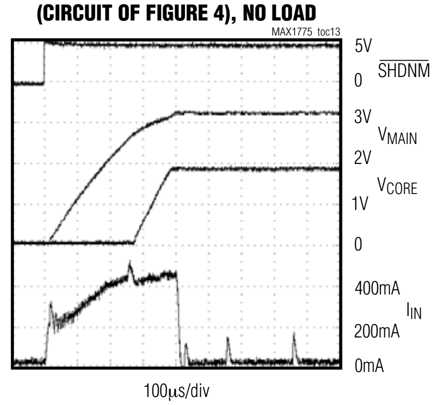
MAIN LOAD TRANSIENT (LOAD FROM 100mA to 1A, V_{IN} = 5V)



MAIN LOAD TRANSIENT (IN DROPOUT LOAD FROM 50mA TO 500mA)



TURN-ON RESPONSE (CIRCUIT OF FIGURE 4), NO LOAD



Pin Description

PIN	NAME	FUNCTION
1	$\overline{SHDNM}$	Shutdown for Main Regulator. A low voltage on $\overline{SHDNM}$ shuts off the main output. For normal operation, connect $\overline{SHDNM}$ to IN.
2	$\overline{SHDNC}$	Shutdown for Core Regulator. A low voltage on $\overline{SHDNC}$ shuts off the core output. For normal operation, connect $\overline{SHDNC}$ to CVL.
3	PGND	Power Ground. Ground for NDRV and core output synchronous rectifier. Connect all grounds together close to the IC.
4	NDRV	N-Channel Drive Output. Drives the main output synchronous rectifier MOSFET. NDRV swings between CVL and PGND.
5	CVL	Low-Side Regulator Bypass. CVL is the output of an internal LDO regulator. This is the internal power supply for the device control circuitry as well as the N-channel driver. Bypass CVL with a 1.0µF or greater capacitor to GND. When CS- is above the CVL switchover threshold (2.47V), CVL is powered from the main output.
6	IN	Power Supply Input
7	PDRV	P-Channel Drive Output. Drives the main output high-side MOSFET switch. PDRV swings between IN and CVH. The voltage at CVH is regulated at V_{IN} - 4.3V unless the input voltage is less than 5.5V.
8	CVH	High-Side Drive Bypass. CVH is the output of an internal LDO regulator with respect to V_{IN}. This is the low-side of the P-channel driver output. Bypass with a 1.0µF capacitor or greater to IN. When the input voltage is less than +5.5V, CVH is switched to PGND.
9	REF	Reference Voltage Output. Bypass REF to GND with a 0.22µF or greater capacitor.
10	FBM	Main Output Feedback. Connect FBM to a resistive voltage-divider to set main output voltage between +1.25V to +5.5V.
11	CS+	Main Regulator High-Side Current-Sense Input. Connect the sense resistor between CS+ and CS-. This voltage is used to set the current limit and to turn off the synchronous rectifier when the inductor current approaches zero.
12	CS-	Main Regulator Low-Side Current-Sense Input. Connect CS- to the main output.
13	FBC	Core Output Feedback. Connect FBC to a resistive voltage-divider to set core output between +1.0V to +5.0V.
14	GND	Analog Ground
15	INC	Core Supply Input
16	LXC	Core Converter Switching Node

Dual-Output Step-Down DC-DC Converter for PDA/Palmtop Computers

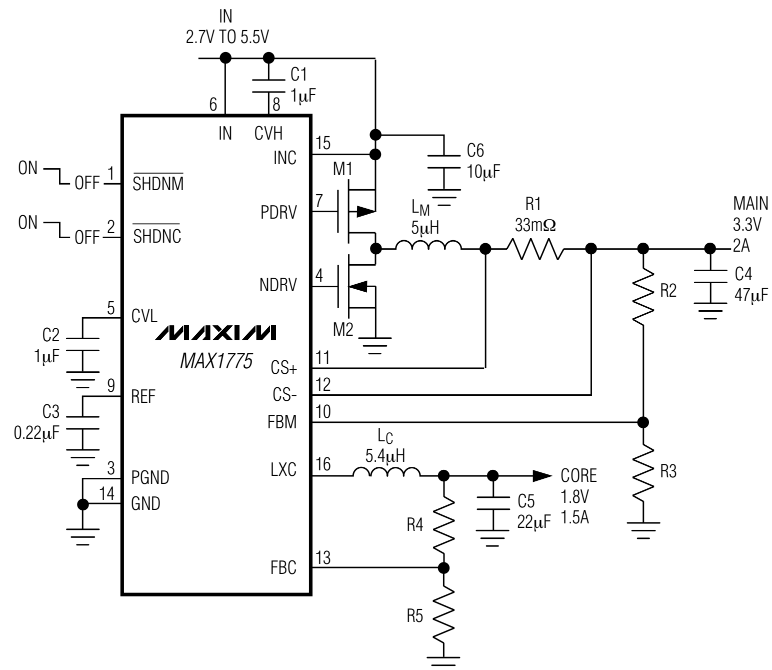


Figure 1. Typical Application Circuit (Low Input Voltage)

Detailed Description

The MAX1775 dual step-down DC-DC converter is designed to power PDA, palmtop, and subnotebook computers. Normally, these devices need two separate power supplies—one for the processor and another higher voltage supply for the peripheral circuitry. The MAX1775 provides an adjustable +1.25V to +5.5V main output designed to power the peripheral circuitry of PDAs and similar devices. The main output delivers over 2A output current. The lower voltage core converter has an adjustable +1.0V to +5.0V output, providing up to 1.5A output current. Both regulators utilize a proprietary regulation scheme, allowing PWM operation at medium to heavy loads, and automatically switch to pulse skipping at light loads for improved efficiency. Figure 1 is the typical application circuit.

Operating Modes for the Step-Down Converters

When delivering low output currents, the MAX1775 operates in discontinuous conduction mode. Current through the inductor starts at zero, rises above the minimum current limit, then ramps down to zero during each cycle (see *Typical Operating Characteristics*). The switch waveform may exhibit ringing, which occurs at the resonant frequency of the inductor and stray capacitance, due to the residual energy trapped in the core when the rectifier MOSFET turns off. This does not degrade the circuit performance.

When delivering medium-to-high output currents, the MAX1775 operates in PWM continuous-conduction mode. In this mode, current always flows through the inductor and never ramps to zero. The control circuit adjusts the switch duty cycle to maintain regulation without exceeding the peak switching current set by the current-sense resistor.

100% Duty Cycle and Dropout

The MAX1775 operates with a duty cycle up to 100%. This feature extends the input voltage range by turning the MOSFET on continuously when the supply voltage approaches the output voltage. This services the load when conventional switching regulators with less than 100% duty cycle would fail. Dropout voltage is defined as the difference between the input and output voltages when the input is low enough for the output to drop out of regulation. Dropout depends on the MOSFET drain-to-source on-resistance, current-sense resistor, and inductor series resistance, and is proportional to the load current:

$$\text{Dropout voltage} = I_{OUT} \times [R_{DS(ON)} + R_{SENSE} + R_{INDUCTOR}]$$

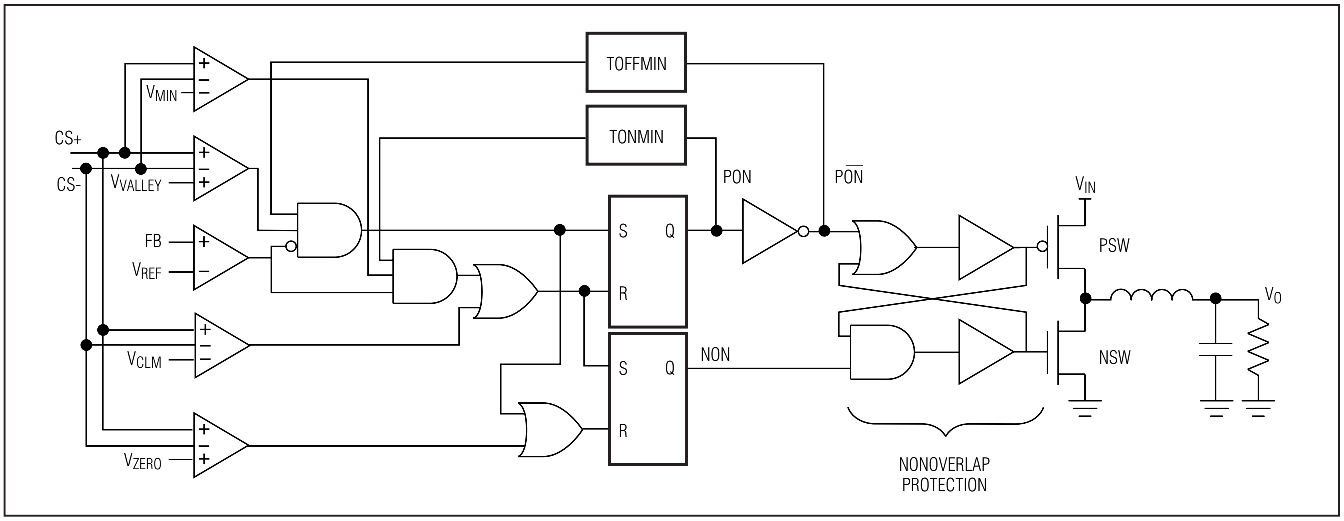


Figure 2. Simplified Control System Block Diagram

Regulation Control Scheme

The MAX1775 has a unique operating scheme that allows PWM operation at medium and high current, with automatic switching to pulse-skipping mode at lower currents to improve light-load efficiency. Figure 2 shows a simplified block diagram.

Under medium- and heavy-load operation, the inductor current is continuous and the part operates in PWM mode. In this mode, the switching frequency is set by either the minimum on-time or the minimum off-time, depending on the duty cycle. The duty cycle is approximately the output voltage divided by the input voltage. If the duty cycle is less than 50%, the minimum on-time controls the frequency; and the frequency is approximately $f \approx 2.5MHz \times D$, where D is the duty cycle. If the duty cycle is greater than 50%, the minimum off-time sets the frequency; and the frequency is approximately $f \approx 2.5MHz \times (1 - D)$.

In both cases, the voltage is regulated by the error comparator. For low duty cycles (<50%), the P-channel MOSFET turns on for the minimum on-time, causing fixed-on-time operation. During the P-channel MOSFET on-time, the output voltage rises. Once the P-channel MOSFET turns off, the voltage drops to the regulation threshold, at which time another cycle is initiated. For high duty cycles (>50%), the P-channel MOSFET remains off for the minimum off-time, causing fixed off-time operation. In this case, the P-channel MOSFET remains on until the output voltage rises to the regulation threshold. Then the P-channel MOSFET turns off for the minimum off-time, initiating another cycle.

By switching between fixed on-time and fixed off-time operation, the MAX1775 can operate at high input-output ratios, yet still operate up to 100% duty cycle for low dropout. Note that when operating in fixed on-time, the minimum output voltage is regulated; but in fixed off-time operation, the maximum output voltage is regulated. Thus, as the input voltage drops below approximately twice the output voltage, a decrease in line regulation can be expected. The drop in voltage is approximately $V_{DROP} \approx V_{RIPPLE}$. At light output loads, the inductor current is discontinuous, causing the MAX1775 to operate at lower frequencies, reducing the MOSFET gate drive and switching losses. In discontinuous mode, under most circumstances, the on-time will be a fixed minimum of 400ns.

The MAX1775 features four separate current-limit threshold detectors and a watchdog timer for each of its step-down converters. In addition to the more common peak current detector and zero crossing detector, each converter also provides a valley current detector (I_{VALLEY}) and a minimum current detector (I_{MIN}). I_{VALLEY} is used to force the inductor current to drop to a lower level after hitting peak current before allowing the P-channel MOSFET to turn on. This is a safeguard against inductor current significantly overshooting above the peak current when the inductor discharges too slowly when V_{OUT}/L is small. I_{MIN} is useful in ensuring that a minimum current is built up in the inductor before turning off the P-channel MOSFET. This helps the inductor to charge the output near dropout when dI/dt is small (because $(V_{IN} - V_{OUT}) / L$ is small) to avoid multiple

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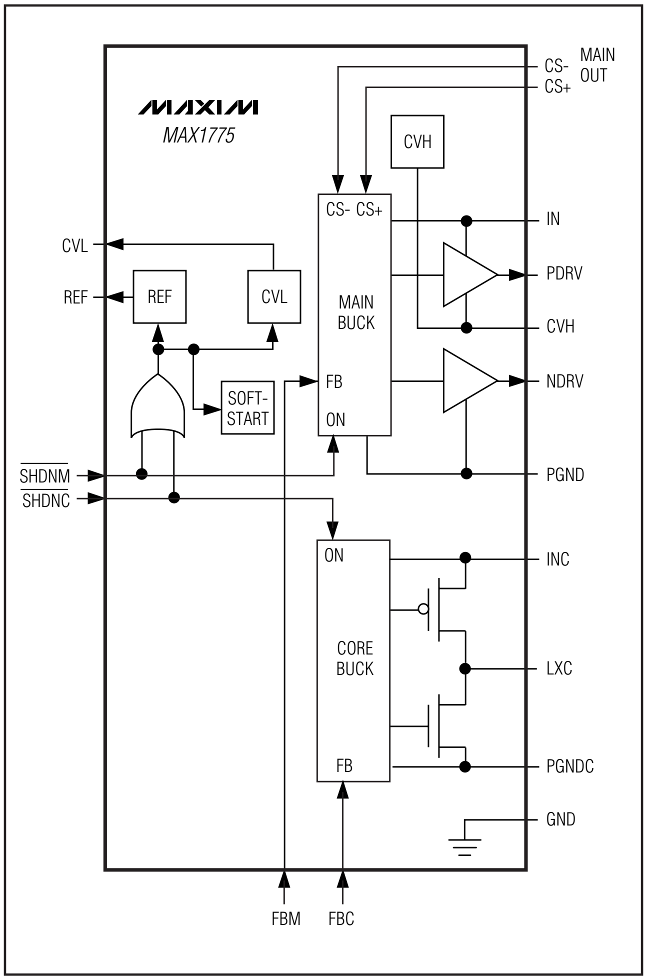

Figure 3. Simplified Block Diagram

pulses and low efficiency. This feature, however, is disabled during dropout and light-load conditions where the inductor current may take too long to reach the I_{MIN} value. A watchdog timer overrides I_{MIN} after the P-channel MOSFET has been on for longer than about 10µs.

Main Step-Down Converter

The main step-down converter features adjustable +1.25V to +5.5V output, delivering over 2A from a +2.7V to +28V input (see *Setting the Output Voltages*). The use of external MOSFETs and a current-sense resistor maximizes design flexibility. The MAX1775 offers a synchronous rectifier MOSFET driver that improves efficiency by eliminating losses through a diode. The two MOSFET drive outputs, PDRV and NDRV, control these external MOSFETs. The output swing of these outputs is limited to reduce power consumption by limiting the amount of injected gate charge (see *Internal Linear Regulators*). The main current limit is sensed through a small sense resistor at the converter output (see *Setting the Current Limit*). Driving $\overline{\text{SHDNM}}$ low puts the main converter in a low-power shutdown mode. The core regulator is still functional when the main converter is in shutdown.

Core Step-Down Converter

The core step-down converter produces a +1.0V to +5.0V output from a +2.6V to +5.5V input. The low-voltage input allows the use of internal power MOSFETs, taking advantage of their low $R_{DS(ON)}$, improving efficiency and reducing board space. Like the main converter, the core regulator makes use of an N-channel MOSFET synchronous rectifier, improving efficiency and eliminating the need for an external Schottky diode. Current sensing is internal to the device, eliminating the need for an external sense resistor. The maximum and minimum current limits are sensed through the P-channel MOSFET, while the valley current and zero crossing current are sensed through the N-channel MOSFET. The core output voltage is measured at FBC through a resistive voltage-divider. This divider can be adjusted to set the output voltage level (see *Setting the Output Voltages*). The core input can be supplied from the main regulator or an external supply that does not exceed +5.5V (see *High-Voltage Configuration* and *Low-Voltage Configuration*). The core converter can be shut down independent of the main converter by driving $\overline{\text{SHDNC}}$ low. If the main converter output is supplying power to the core and is shut down, $\overline{\text{SHDNM}}$ controls both outputs. Figure 3 is a simplified block diagram.

Internal Linear Regulators

There are two linear regulators internal to the MAX1775. A high-voltage linear regulator accepts inputs up to +28V, reducing it to +2.8V at CVL to provide power to the MAX1775. Once the voltage at CS- reaches +2.47V, CVL is switched to CS, allowing it to be driven from the main converter, improving efficiency. CVL supplies the internal bias to the IC and power for the NDRV gate driver.

The CVH regulator provides the low-side voltage for the main regulator's PDRV output. The voltage at CVH is regulated at 4.3V below V_{IN} to limit the voltage swing on PDRV, reducing gate charge and improving efficiency (Figure 3).

Reference

The MAX1775 has an accurate internally trimmed +1.25V reference at REF. REF can source no more than 50µA. Bypass REF to GND with a 0.22µF capacitor.

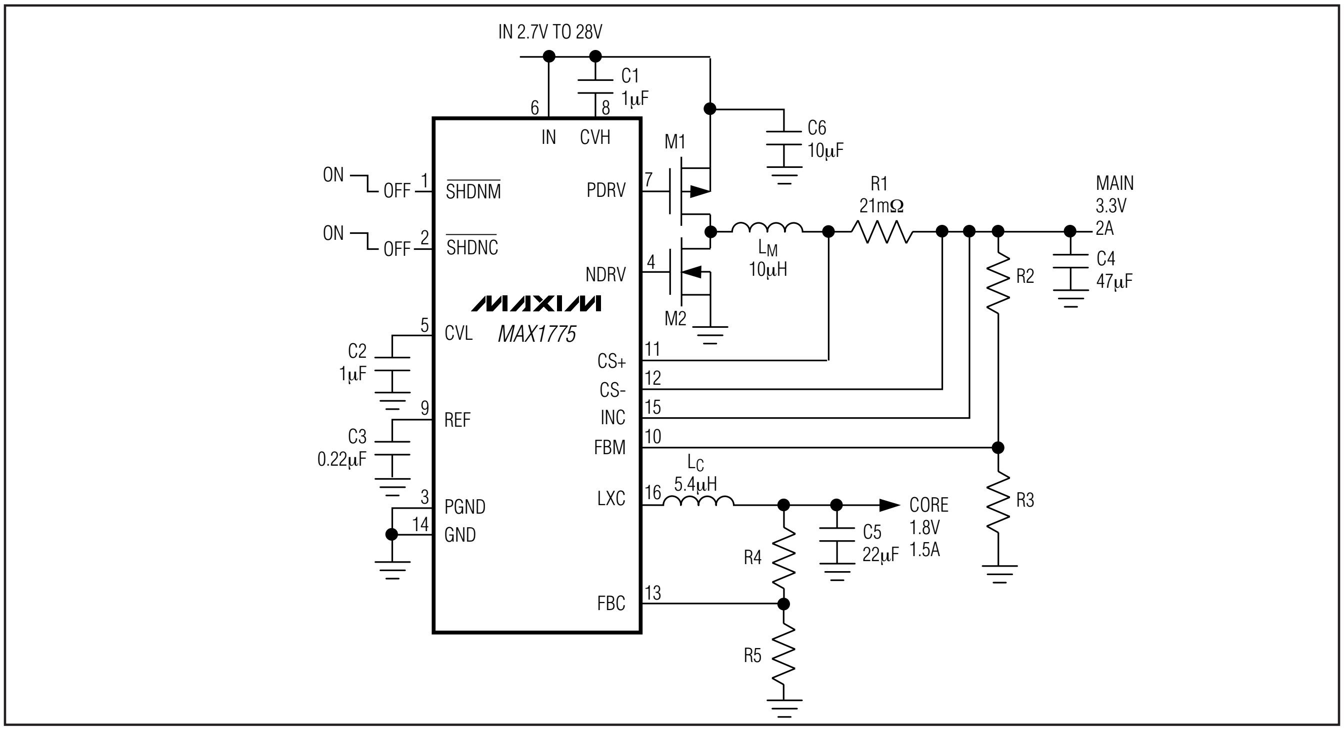

Figure 4. High Input Voltage Cascaded Configuration

Design Procedure

Low-Voltage Configuration

To improve efficiency and conserve board space, the core regulator operates from low input voltages, taking advantage of internal low-voltage, low-on-resistance MOSFETs. When the input voltage remains below 5.5V, run the core converter directly from the input by connecting INC to IN (Figure 1). This configuration takes advantage of the core's low-voltage design and improves efficiency.

High-Voltage Configuration

For input voltages greater than 5.5V, cascade the main and core converters by connecting INC to the main output voltage. In this configuration (Figure 4), the core converter is powered from the main output. Ensure that the main output can simultaneously supply its load and the core input current. In this configuration, the main output voltage must be set above the 2.6V minimum input voltage of the core converter.

Setting the Output Voltages

The main output voltage may be set from +1.25V and +5.5V with two external resistors connected as a voltage-divider to FBM (Figure 1). Resistor values can be calculated by the following equation:

$$R2 = R3 \times [(V_{OUTM} / V_{FBM}) - 1]$$

where V_{FBM} = +1.25V. Choose R3 to be 40kΩ or less.

The core regulator output is adjustable from +1.0V to +5.0V through two external resistors connected as a voltage-divider to FBC (Figure 1). Resistor values can be calculated through the following equation:

$$R4 = R5 \times [(V_{OUTC} / V_{FBC}) - 1]$$

where V_{FBC} = +1.0V. Choose R5 to be 30kΩ or less.

Setting the Current Limit

The main regulator current limit is set externally through a small current-sense resistor, R1 (Figure 1). The value of R1 can be calculated by the following equation:

$$R1 = \frac{V_{CLM}}{\left(1.3\ I_{OUT}\right)}$$

where V_{CLM} = 80mV is the current-sense threshold, and I_{OUT} is the current delivered to the output. The core converter current limit is set internally and cannot be modified.

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Careful layout of the current-sense signal traces is imperative. Place R1 as close to the MAX1775 as possible. The two traces should have matching length and width, be as far as possible from noisy switching signals, and be close together to improve noise rejection. These traces should be used for current-sense signal routing only and should not carry any load current. Refer to the MAX1775 Evaluation Kit for layout examples.

Inductor Selection

The essential parameters for inductor selection are inductance and current rating. The MAX1775 operates with a wide range of inductance values.

Calculate the inductance value for either core or main, L_{MIN}:

$$L_{MIN} = (V_{IN} - V_{OUT}) \times T_{ONMIN} / I_{RIPPLE}$$

where T_{ONMIN} is typically 400ns, and I_{RIPPLE} is the continuous conduction ripple current. In continuous conduction, I_{RIPPLE} should be chosen to be 30% of the maximum load current. With high inductor values, the MAX1775 begins continuous-conduction operation at a lower fraction of full load (see *Detailed Description*).

The inductor's saturation current must be greater than the peak switching current to prevent core saturation. Saturation occurs when the inductor's magnetic flux density reaches the maximum level the core can support, and inductance starts to fall. The inductor heating current rating must be greater than the maximum load current to prevent overheating. For optimum efficiency, the inductor series resistance should be less than the current-sense resistance.

Capacitor Selection

Choose output filter capacitors to service the output ripple current with acceptable voltage ripple. ESR in the output capacitor is a major contributor to output ripple. For the main converter, low-ESR capacitors such as polymer, ceramic, or even tantalum are recommended. For the core converter, choosing a low-ESR tantalum capacitor with enough ESR to generate about 1% ripple voltage across the output is helpful in ensuring stability.

Voltage ripple is the sum of contributions from ESR and the capacitor value:

$$V_{RIPPLE} \approx V_{RIPPLE,ESR} + V_{RIPPLE,C}$$

For tantalum capacitors, the ripple is determined mostly by the ESR. Voltage ripple due to ESR is:

$$V_{RIPPLE,ESR} \approx R_{ESR} \times I_{RIPPLE}$$

For ceramic capacitors, the ripple is mostly due to the capacitance. The ripple due to the capacitance is approximately:

$$V_{RIPPLE,C} \approx L\, I_{RIPPLE}^2 / 2C_{OUT}V_{OUT}$$

where V_{OUT} is the average output voltage. From this equation, estimate the output capacitor values for given voltage ripple as follows:

$$C_{OUT} = 1/2 \times L\, I_{RIPPLE}^2 / (V_{RIPPLE,COUT} \times V_{OUT})$$

This equation is suitable for initial capacitor selection. Final values should be set by testing a prototype or evaluation kit. When using tantalum capacitors, use good soldering practices to prevent excessive heat from damaging the devices and increasing their ESR. Also, ensure that the tantalum capacitors' surge-current ratings exceed the startup inrush and peak switching currents.

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple at IN, caused by the circuit's switching. Use a low-ESR capacitor. Two smaller-value low-ESR capacitors can be connected in parallel if necessary. Choose input capacitors with working voltage ratings higher than the maximum input voltage. Typically 4µF of input capacitance for every 1A of load current is sufficient. More capacitance may improve battery life and noise immunity.

Place a surface-mount ceramic capacitor at IN very close to the source of the high-side P-channel MOSFET. This capacitor bypasses the MAX1775, minimizing the effects of spikes and ringing on the MAX1775's operation.

Bypass REF with 0.22µF or greater. Place this capacitor within 0.2in (5mm) of the IC, next to REF, with a direct trace to GND.

MOSFET Selection

The MAX1775 drives an external enhancement-mode P-channel MOSFET and a synchronous-rectifier N-channel MOSFET. When selecting the MOSFETs, important parameters to consider are on-resistance ($R_{DS(ON)}$), maximum drain-to-source voltage ($V_{DS(MAX)}$), maximum gate-to-source voltage ($V_{GS(MAX)}$), and minimum threshold voltage ($V_{TH(MIN)}$).

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 QSOP	E16-5	21-0055

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	4/09	Corrected R1 resistor value in Figure 4 and other style errors	1, 3, 5, 13, 14