



Low-Voltage, Quad-/Hex-/Octal-Voltage μ P Supervisors

General Description

The MAX16000–MAX16007 are low-voltage, quad-/hex-/octal-voltage μ P supervisors in small thin QFN and TSSOP packages. These devices provide supervisory functions for complex multivoltage systems. The MAX16000/MAX16001/MAX16002 monitor four voltages, the MAX16003/MAX16004/MAX16005 monitor six voltages, and the MAX16006/MAX16007 monitor eight voltages.

The MAX16000/MAX16001/MAX16003/MAX16004/MAX16006 offer independent outputs for each monitored voltage. The MAX16001/MAX16002/MAX16004–MAX16007 offer a reset output that asserts whenever any of the monitored voltages fall below their respective thresholds or the manual reset input is asserted. The reset output remains asserted for the reset timeout after all voltages are above their respective thresholds and the manual reset input is deasserted. The minimum reset timeout is internally set to 140ms or can be adjusted with an external capacitor.

All open-drain outputs have internal 30 μ A pullups that eliminate the need for external pullup resistors. However, each output can be driven with an external voltage up to 5.5V. Other features offered include a manual reset input, a tolerance pin for selecting 5% or 10% input thresholds, and a margin enable function for deasserting the outputs during margin testing.

The MAX16001/MAX16002/MAX16004–MAX16007 offer a watchdog timer that asserts RESET or an independent watchdog output (MAX16005) when the watchdog timeout period (1.6s typ) is exceeded. The watchdog timer can be disabled by floating the input.

These devices are offered in 12-, 16-, 20-, and 24-lead thin QFN and 16-lead TSSOP packages. These are fully specified from -40°C to +125°C.

Applications

Storage Equipment
Servers
Networking/Telecommunication Equipment
Multivoltage ASICs

Selector Guide appears at end of data sheet.

Features

- ◆ Fixed Thresholds for 5V, 3.3V, 3V, 2.5V, 1.8V, 1.5V, 1.2V, and 0.9V Systems
- ◆ Adjustable Thresholds Monitor Voltages Down to 0.4V
- ◆ Open-Drain Outputs with Internal Pullups Reduce the Number of External Components
- ◆ Fixed 140ms (min) or Capacitor-Adjustable Reset Timeout
- ◆ Manual Reset, Margin Enable, and Tolerance Select Inputs
- ◆ Watchdog Timer
 - 1.6s (typ) Timeout Period
 - 54s Startup Delay After Reset (Except MAX16005)
- ◆ Independent Watchdog Output (MAX16005)
- ◆ RESET Output Indicates All Voltages Present
- ◆ Independent Voltage Monitors
- ◆ Guaranteed Correct Logic State Down to $V_{CC} = 1V$
- ◆ Small (4mm x 4mm) Thin QFN Package
- ◆ TSSOP (5mm x 4.4mm) Package (MAX16005)

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|--------------|-----------------|-------------|
| MAX16000_TC+ | -40°C to +125°C | 12 TQFN-EP* |

Note: The “_” is a placeholder for the input voltage threshold. See Table 1.

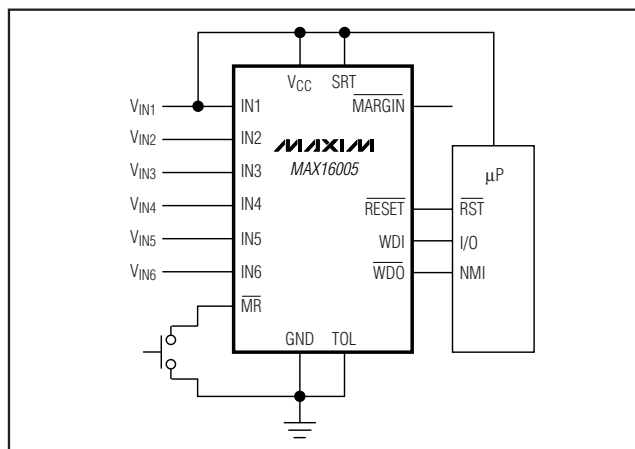
+ Denotes lead(Pb)-free/RoHS-compliant package.

For tape-and-reel, add a “T” after the “+.” Tape-and-reel are offered in 2.5k increments.

*EP = Exposed pad.

Ordering Information continued at end of data sheet.

Typical Operating Circuit



Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

ABSOLUTE MAXIMUM RATINGS

V_{CC}, OUT₋, IN₋, RESET₋, WDO₋ to GND -0.3V to +6V
 TOL, MARGIN, MR, SRT, WDI₋ to GND -0.3V to V_{CC} + 0.3
 Input/Output Current (RESET₋, MARGIN,
 SRT, MR, TOL, OUT₋, WDO₋, WDI₋) ±20mA
 Continuous Power Dissipation (T_A = +70°C)
 12-Pin TQFN (derate 16.9mW/°C above +70°C) 1349mW
 16-Pin TQFN (derate 16.9mW/°C above +70°C) 1349mW
 20-Pin TQFN (derate 16.9mW/°C above +70°C) 1355mW
 24-Pin TQFN (derate 16.9mW/°C above +70°C) 1666mW
 16-Pin TSSOP (derate 9.4mW/°C above +70°C) 754mW

Operating Temperature Range -40°C to +125°C
 Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (soldering, 10s) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------|--|-------|-------|-------|-------|
| Operating Voltage Range | V _{CC} | (Note 2) | 1.0 | | 5.5 | V |
| Supply Current | I _{CC} | V _{CC} = 3.3V, OUT ₋ , RESET ₋ not asserted (Note 3) | | 45 | 65 | μA |
| | | V _{CC} = 5V, OUT ₋ , RESET ₋ not asserted | | 50 | 70 | |
| UVLO (Undervoltage Lockout) | V _{UVLO} | V _{CC} rising | 1.62 | 1.8 | 1.98 | V |
| IN₋ (See Table 1) | | | | | | |
| Threshold Voltages (IN ₋ Falling) | V _{TH} | 5V threshold, TOL = GND | 4.50 | 4.625 | 4.75 | V |
| | | 5V threshold, TOL = V _{CC} | 4.25 | 4.375 | 4.50 | |
| | | 3.3V threshold, TOL = GND | 2.970 | 3.053 | 3.135 | |
| | | 3.3V threshold, TOL = V _{CC} | 2.805 | 2.888 | 2.970 | |
| | | 3.0V threshold, TOL = GND | 2.70 | 2.775 | 2.85 | |
| | | 3.0V threshold, TOL = V _{CC} | 2.55 | 2.625 | 2.70 | |
| | | 2.5V threshold, TOL = GND | 2.250 | 2.313 | 2.375 | |
| | | 2.5V threshold, TOL = V _{CC} | 2.125 | 2.188 | 2.250 | |
| | | 1.8V threshold, TOL = GND | 1.62 | 1.665 | 1.71 | |
| | | 1.8V threshold, TOL = V _{CC} | 1.53 | 1.575 | 1.62 | |
| | | 1.5V threshold, TOL = GND | 1.350 | 1.388 | 1.425 | |
| | | 1.5V threshold, TOL = V _{CC} | 1.275 | 1.313 | 1.350 | |
| | | 1.2V threshold, TOL = GND | 1.08 | 1.11 | 1.14 | |
| | | 1.2V threshold, TOL = V _{CC} | 1.02 | 1.05 | 1.08 | |
| | | 0.9V threshold, TOL = GND | 0.810 | 0.833 | 0.855 | |
| | | 0.9V threshold, TOL = V _{CC} | 0.765 | 0.788 | 0.810 | |

Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

MAX16000-MAX16007

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------------|---------------------|---|-----------------------|-------|-------|-------------------|
| Adjustable Threshold (IN_ Falling) | V _{TH} | TOL = GND | 0.388 | 0.394 | 0.400 | V |
| | | TOL = V _{CC} | 0.366 | 0.372 | 0.378 | |
| IN_ Hysteresis | V _{TH_HYS} | IN_ rising | 0.5 | | | % V _{TH} |
| IN_ Input Current | | Fixed thresholds | 3 | | 16 | μA |
| | | Adjustable thresholds | -100 | | +100 | nA |
| RESET | | | | | | |
| Reset Timeout | t _{RP} | SRT = V _{CC} | 140 | 200 | 280 | ms |
| | | C _{SRT} = 1500pF (Note 4) | 2.43 | 3.09 | 3.92 | |
| | | C _{SRT} = 100pF | 0.206 | | | |
| | | C _{SRT} = open | 50 | | | μs |
| SRT Ramp Current | I _{SRT} | V _{SRT} = 0V | 460 | 600 | 740 | nA |
| SRT Threshold | | | 1.173 | 1.235 | 1.293 | V |
| SRT Hysteresis | | | 100 | | | mV |
| IN_ to Reset Delay | t _{RD} | IN_ falling | 20 | | | μs |
| RESET Output-Voltage Low | V _{OL} | V _{CC} = 3.3V, I _{SINK} = 10mA, RESET asserted | 0.30 | | | V |
| | | V _{CC} = 2.5V, I _{SINK} = 6mA, RESET asserted | 0.30 | | | |
| | | V _{CC} = 1.2V, I _{SINK} = 50μA, RESET asserted | 0.30 | | | |
| RESET Output-Voltage High | V _{OH} | V _{CC} ≥ 2.0V, I _{SOURCE} = 6μA, RESET deasserted | 0.8 x V _{CC} | | | V |
| MR Input-Voltage Low | V _{IL} | | 0.3 x V _{CC} | | | V |
| MR Input-Voltage High | V _{IH} | | 0.7 x V _{CC} | | | V |
| MR Minimum Pulse Width | | | 1 | | | μs |
| MR Glitch Rejection | | | 100 | | | ns |
| MR to Reset Delay | | | 200 | | | ns |
| MR Pullup Resistance | | Pulled up to V _{CC} | 12 | 20 | 28 | kΩ |
| OUTPUTS (OUT_) | | | | | | |
| OUT_ Output-Voltage Low | V _{OL} | V _{CC} = 3.3V, I _{SINK} = 2mA | 0.30 | | | V |
| | | V _{CC} = 2.5V, I _{SINK} = 1.2mA | 0.30 | | | |
| OUT_ Output-Voltage High | V _{OH} | V _{CC} ≥ 2.0V, I _{SOURCE} = 6μA | 0.8 x V _{CC} | | | V |
| IN_ to OUT_ Propagation Delay | t _D | (V _{TH} + 100mV) to (V _{TH} - 100mV) | 20 | | | μs |

Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C). (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------|---|-----------------------|-------|-----------------------|-------|
| REFERENCE OUTPUT (MAX16005 Only) | | | | | | |
| Reference Short-Circuit Current | | Shorted to GND | | 0.8 | | mA |
| Reference Output Accuracy | V _{REF} | No load | 1.200 | 1.235 | 1.270 | V |
| Line Regulation | | | | 0.005 | | % / V |
| Reference Load Regulation | | Sourcing, 0 ≤ I _{REF} ≤ 40μA | | 10 | | Ω |
| WATCHDOG TIMER (MAX16001/MAX16002/MAX16004-MAX16007) | | | | | | |
| WDI Input-Voltage Low | V _{IL} | | | | 0.3 x V _{CC} | V |
| WDI Input-Voltage High | V _{IH} | | 0.7 x V _{CC} | | | V |
| WDI Pulse Width | | (Note 5) | 50 | | | ns |
| Watchdog Timeout Period | t _{WDI} | | 1.12 | 1.6 | 2.40 | s |
| Watchdog Startup Period | | MAX16001/2/4/6/7 | 35 | 54 | 72 | s |
| Watchdog Input Current | | V _{WDI} = 0 to V _{CC} (Note 5) | -1 | | +1 | μA |
| WD \overline{O} Output-Voltage Low (MAX16005 Only) | V _{OL} | V _{CC} = 3.3V, I _{SINK} = 2mA | | | 0.30 | V |
| | | V _{CC} = 2.5V, I _{SINK} = 1.2mA | | | 0.30 | |
| WD \overline{O} Output-Voltage High (MAX16005 Only) | V _{OH} | V _{CC} ≥ 2.0V, I _{SOURCE} = 6μA, WD \overline{O} deasserted | 0.8 x V _{CC} | | | V |
| DIGITAL LOGIC | | | | | | |
| TOL Input-Voltage Low | V _{IL} | | | | 0.3 x V _{CC} | V |
| TOL Input-Voltage High | V _{IH} | | 0.7 x V _{CC} | | | V |
| TOL Input Current | | TOL = V _{CC} | | | 100 | nA |
| MARGIN \overline{I} Input-Voltage Low | V _{IL} | | | | 0.3 x V _{CC} | V |
| MARGIN \overline{I} Input-Voltage High | V _{IH} | | 0.7 x V _{CC} | | | V |
| MARGIN \overline{I} Pullup Resistance | | Pulled up to V _{CC} | 12 | 20 | 28 | kΩ |
| MARGIN \overline{I} Delay Time | t _{MD} | Rising or falling (Note 6) | | 50 | | μs |

Note 1: Devices are tested at T_A = +25°C and guaranteed by design for T_A = T_{MIN} to T_{MAX}.

Note 2: The outputs are guaranteed to be in the correct logic state down to V_{CC} = 1V.

Note 3: Measured with WDI, MARGIN \overline{I} , and MR unconnected.

Note 4: The minimum and maximum specifications for this parameter are guaranteed by using the worst case of the SRT ramp current and SRT threshold specifications.

Note 5: Guaranteed by design and not production tested.

Note 6: Amount of time required for logic to lock/unlock outputs from margin testing.

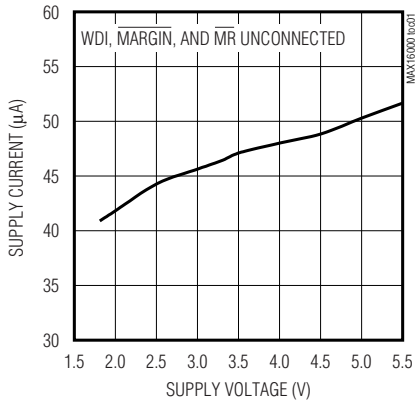
Low-Voltage, Quad-/Hex-/Octal-Voltage μ P Supervisors

Typical Operating Characteristics

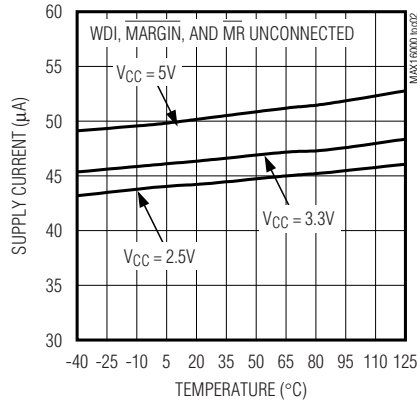
($V_{CC} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX16000-MAX16007

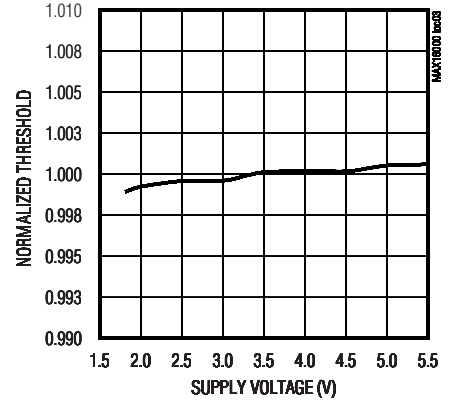
SUPPLY CURRENT vs. SUPPLY VOLTAGE



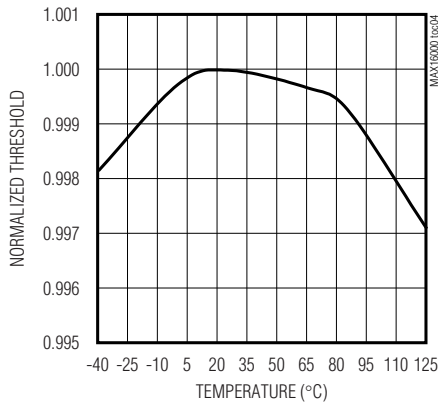
SUPPLY CURRENT vs. TEMPERATURE



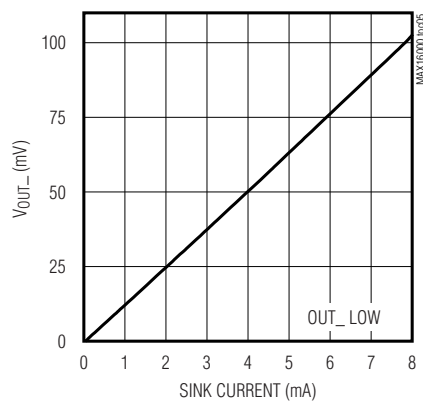
NORMALIZED THRESHOLD vs. SUPPLY VOLTAGE



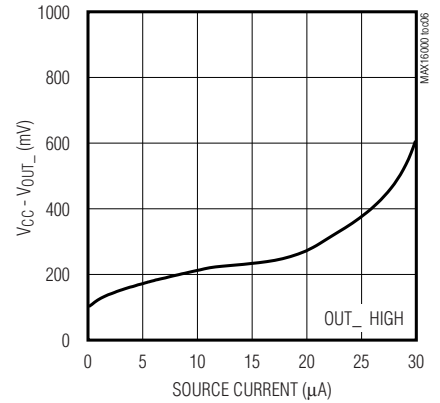
NORMALIZED THRESHOLD vs. TEMPERATURE



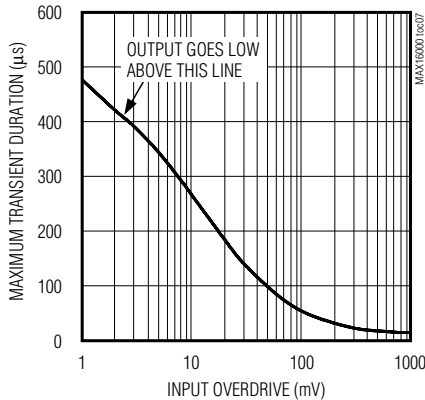
OUTPUT VOLTAGE vs. SINK CURRENT



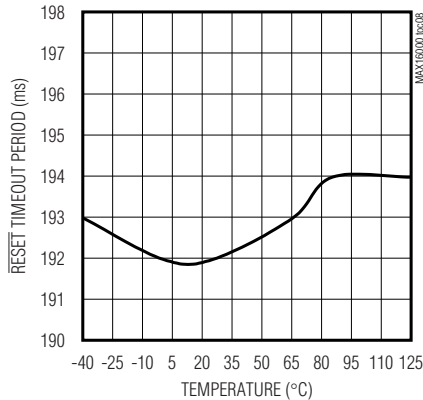
OUTPUT VOLTAGE vs. SOURCE CURRENT



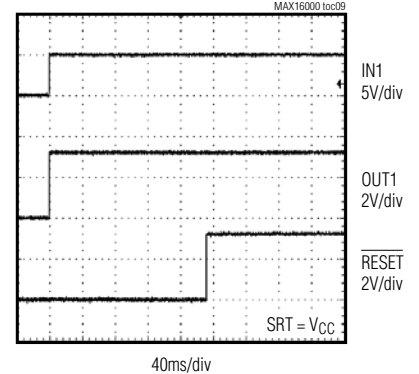
MAXIMUM TRANSIENT DURATION vs. INPUT OVERDRIVE



RESET TIMEOUT PERIOD vs. TEMPERATURE



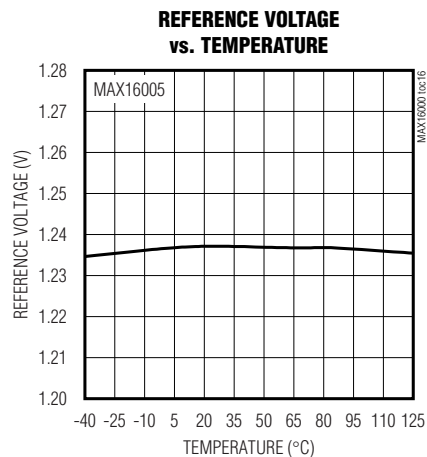
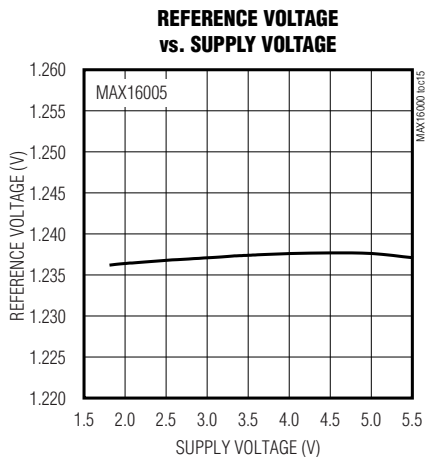
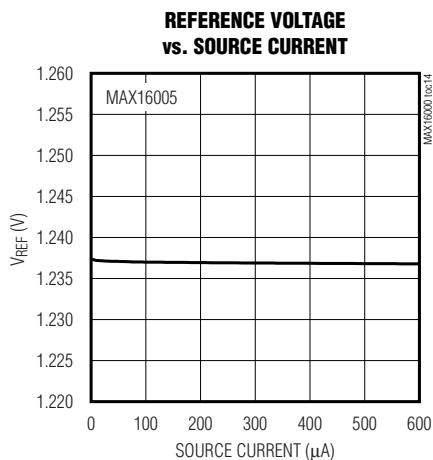
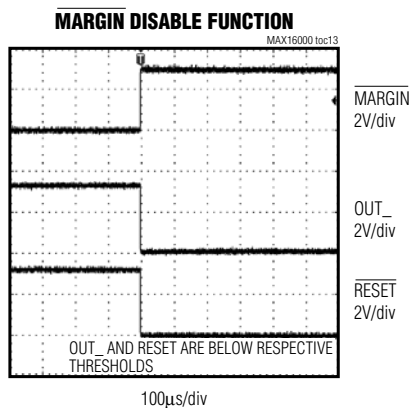
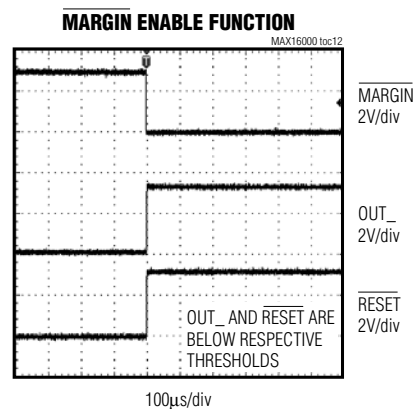
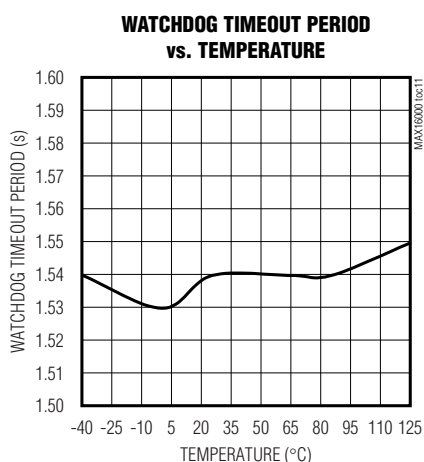
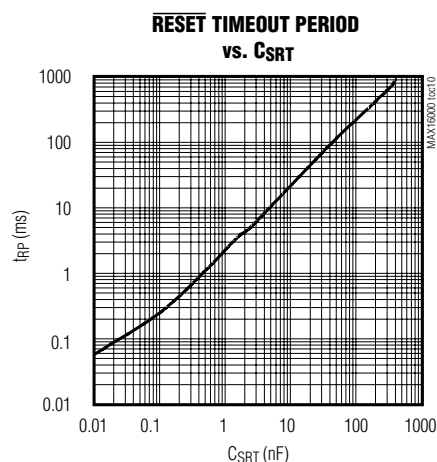
RESET TIMEOUT DELAY



Low-Voltage, Quad-/Hex-/Octal-Voltage μ P Supervisors

Typical Operating Characteristics (continued)

($V_{CC} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

Pin Description (MAX16000/MAX16001/MAX16002)

| PIN | | | NAME | FUNCTION |
|----------|----------|----------|-----------------|--|
| MAX16000 | MAX16001 | MAX16002 | | |
| 1 | 1 | 1 | IN3 | Monitored Input Voltage 3. See Table 1 for the input voltage threshold. |
| 2 | 2 | 2 | IN4 | Monitored Input Voltage 4. See Table 1 for the input voltage threshold. |
| 3 | 4 | 4 | GND | Ground |
| 4 | 5 | 5 | V _{CC} | Unmonitored Power-Supply Input |
| 5 | 6 | — | OUT3 | Output 3. When the voltage at IN3 falls below its threshold, OUT3 goes low and stays low until the voltage at IN3 exceeds its threshold. The open-drain output has a 30μA internal pullup to V _{CC} . |
| 6 | 7 | — | OUT4 | Output 4. When the voltage at IN4 falls below its threshold, OUT4 goes low and stays low until the voltage at IN4 exceeds its threshold. The open-drain output has a 30μA internal pullup to V _{CC} . |
| 7 | 10 | 8 | MARGIN | Active-Low Manual Deassert Input. Pull MARGIN low to deassert all outputs (go into high state), regardless of the voltage at any monitored input. |
| 8 | 11 | — | OUT2 | Output 2. When the voltage at IN2 falls below its threshold, OUT2 goes low and stays low until the voltage at IN2 exceeds its threshold. The open-drain output has a 30μA internal pullup to V _{CC} . |
| 9 | 12 | — | OUT1 | Output 1. When the voltage at IN1 falls below its threshold, OUT1 goes low and stays low until the voltage at IN1 exceeds its threshold. The open-drain output has a 30μA internal pullup to V _{CC} . |
| 10 | 14 | 10 | IN1 | Monitored Input Voltage 1. See Table 1 for the input voltage threshold. |
| 11 | 15 | 11 | IN2 | Monitored Input Voltage 2. See Table 1 for the input voltage threshold. |
| 12 | 16 | 12 | TOL | Threshold Tolerance Input. Connect TOL to GND to select 5% threshold tolerance. Connect TOL to V _{CC} to select 10% threshold tolerance. |
| — | 3 | 3 | WDI | Watchdog Timer Input. If WDI remains low or high for longer than the watchdog timeout period, RESET is asserted. The timer clears whenever a reset is asserted or a rising or falling edge on WDI is detected. The watchdog timer enters a startup period that allows 54s for the first transition to occur before a reset. Leave WDI unconnected to disable the watchdog timer. The WDI floating-state detector uses a small 400nA current. Therefore, do not connect WDI to anything that will source or sink more than 200nA. Note that the leakage current specification for most three-state drivers exceeds 200nA. |
| — | 8 | 6 | MR | Active-Low Manual Reset Input. Pull MR low to assert RESET low. RESET remains low for the reset timeout period after MR is deasserted. MR is pulled up to V _{CC} through a 20kΩ resistor. |
| — | 9 | 7 | SRT | Set Reset Timeout Input. Connect a capacitor from SRT to GND to set the reset timeout period. The reset timeout period can be calculated as follows: Reset Timeout (s) = 2.06 × 10 ⁶ (Ω) × C _{SRT} (F). For the internal timeout period of 140ms (min), connect SRT to V _{CC} . |
| — | 13 | 9 | RESET | Active-Low Reset Output. RESET asserts low when any of the monitored voltages falls below its respective threshold or MR is asserted. RESET remains asserted for the reset timeout period after all monitored voltages exceed their respective thresholds and MR is deasserted. This open-drain output has a 30μA internal pullup. |
| — | — | — | EP | Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal resistance path from the IC junction to the PCB. Do not use as the electrical connection to GND. |

MAX16000–MAX16007

Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

Pin Description (MAX16003/MAX16004/MAX16005)

| PIN | | | | NAME | FUNCTION |
|----------|----------|-------------------|------------------|----------------------------|---|
| MAX16003 | MAX16004 | MAX16005 TSSOP | MAX16005 TQFN | | |
| 1 | 1 | 3 | 1 | IN4 | Monitored Input Voltage 4. See Table 1 for the input voltage threshold. |
| 2 | 2 | 4 | 2 | IN5 | Monitored Input Voltage 5. See Table 1 for the input voltage threshold. |
| 3 | 3 | 5 | 3 | IN6 | Monitored Input Voltage 6. See Table 1 for the input voltage threshold. |
| 4 | 5 | 7 | 5 | GND | Ground |
| 5 | 6 | 8 | 6 | VCC | Unmonitored Power-Supply Input |
| 6 | 7 | — | — | OUT4 | Output 4. When the voltage at IN4 falls below its threshold, OUT4 goes low and stays low until the voltage at IN4 exceeds its threshold. The open-drain output has a 30μA internal pullup to VCC. |
| 7 | 8 | — | — | OUT5 | Output 5. When the voltage at IN5 falls below its threshold, OUT5 goes low and stays low until the voltage at IN5 exceeds its threshold. The open-drain output has a 30μA internal pullup to VCC. |
| 8 | 9 | — | — | OUT6 | Output 6. When the voltage at IN6 falls below its threshold, OUT6 goes low and stays low until the voltage at IN6 exceeds its threshold. The open-drain output has a 30μA internal pullup to VCC. |
| 9 | 12 | 13 | 11 | $\overline{\text{MARGIN}}$ | Manual Deassert Input. Pull $\overline{\text{MARGIN}}$ low to deassert all outputs (go into high state), regardless of the voltage at any monitored input. |
| 10 | 13 | — | — | OUT3 | Output 3. When the voltage at IN3 falls below its threshold, OUT3 goes low and stays low until the voltage at IN3 exceeds its threshold. The open-drain output has a 30μA internal pullup to VCC. |
| 11 | 14 | — | — | OUT2 | Output 2. When the voltage at IN2 falls below its threshold, OUT2 goes low and stays low until the voltage at IN2 exceeds its threshold. The open-drain output has a 30μA internal pullup to VCC. |
| 12 | 15 | — | — | OUT1 | Output 1. When the voltage at IN1 falls below its threshold, OUT1 goes low and stays low until the voltage at IN1 exceeds its threshold. The open-drain output has a 30μA internal pullup to VCC. |
| 13 | 17 | 15 | 13 | IN1 | Monitored Input Voltage 1. See Table 1 for the input voltage threshold. |
| 14 | 18 | 16 | 14 | IN2 | Monitored Input Voltage 2. See Table 1 for the input voltage threshold. |
| 15 | 19 | 1 | 15 | IN3 | Monitored Input Voltage 3. See Table 1 for the input voltage threshold. |

Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

Pin Description (MAX16003/MAX16004/MAX16005) (continued)

| PIN | | | | NAME | FUNCTION |
|----------|----------|-------------------|------------------|---------------------------|---|
| MAX16003 | MAX16004 | MAX16005 TSSOP | MAX16005 TQFN | | |
| 16 | 20 | 2 | 16 | TOL | Threshold Tolerance Input. Connect TOL to GND to select 5% threshold tolerance. Connect TOL to V _{CC} to select 10% threshold tolerance. |
| — | 4 | 6 | 4 | WDI | Watchdog Timer Input. MAX16004: If WDI remains low or high for longer than the watchdog timeout period, RESET is asserted and the timer is cleared. The timer also clears whenever a reset is asserted or a rising or falling edge on WDI is detected. The watchdog timer enters a startup period that allows 54s for the first transition to occur before a reset. Leave WDI unconnected to disable the watchdog timer. MAX16005: If WDI remains low or high for longer than the watchdog timeout period, WDO is asserted. The timer clears whenever a rising or falling edge on WDI is detected. Leave WDI unconnected to disable the watchdog timer. The MAX16005 does not have a startup period. MAX16004/MAX16005: The WDI floating-state detector uses a small 100nA current. Therefore, do not connect WDI to anything that will source or sink more than 50nA. Note that the leakage current specification for most three-state drivers exceeds 50nA. |
| — | 10 | 11 | 9 | $\overline{\text{MR}}$ | Active-Low Manual Reset Input. Pull $\overline{\text{MR}}$ low to assert RESET low. RESET remains low for the reset timeout period after $\overline{\text{MR}}$ is deasserted. $\overline{\text{MR}}$ is pulled up to V _{CC} through a 20kΩ resistor. |
| — | 11 | 12 | 10 | SRT | Set Reset Timeout Input. Connect a capacitor from SRT to GND to set the reset timeout period. The reset timeout period can be calculated as follows: Reset Timeout (s) = $2.06 \times 10^6 (\Omega) \times C_{\text{SRT}} (\text{F})$. For the internal timeout period of 140ms (min), connect SRT to V _{CC} . |
| — | 16 | 14 | 12 | $\overline{\text{RESET}}$ | Active-Low Reset Output. $\overline{\text{RESET}}$ asserts low when any of the monitored voltages falls below its respective threshold or $\overline{\text{MR}}$ is asserted. $\overline{\text{RESET}}$ remains asserted for the reset timeout period after all monitored voltages exceed their respective thresholds and $\overline{\text{MR}}$ is deasserted. This open-drain output has a 30μA internal pullup. |
| — | — | 9 | 7 | REF | Reference Output. The reference output voltage of 1.23V can source up to 40μA. |
| — | — | 10 | 8 | $\overline{\text{WDO}}$ | Active-Low Watchdog Output. $\overline{\text{WDO}}$ asserts and stays low whenever any of the IN ₊ inputs fall below their respective thresholds. $\overline{\text{WDO}}$ deasserts without a timeout delay when all the IN ₊ inputs rise above their thresholds. When all the IN ₊ inputs rise above their thresholds, $\overline{\text{WDO}}$ asserts low whenever the watchdog timer times out. $\overline{\text{WDO}}$ deasserts after a valid WDI transition or if $\overline{\text{MR}}$ is pulled low. The watchdog timer begins counting after the reset timeout period once $\overline{\text{MR}}$ goes high. Pull MARGIN low to deassert $\overline{\text{WDO}}$. |
| — | — | — | — | EP | Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal resistance path from the IC junction to the PCB. Do not use as the electrical connection to GND. |

MAX16000–MAX16007

Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

Pin Description (MAX16006/MAX16007)

| PIN | | NAME | FUNCTION |
|----------|----------|------------------------|--|
| MAX16006 | MAX16007 | | |
| 1 | 1 | IN5 | Monitored Input Voltage 5. See Table 1 for the input voltage threshold. |
| 2 | 2 | IN6 | Monitored Input Voltage 6. See Table 1 for the input voltage threshold. |
| 3 | 3 | IN7 | Monitored Input Voltage 7. See Table 1 for the input voltage threshold. |
| 4 | 4 | IN8 | Monitored Input Voltage 8. See Table 1 for the input voltage threshold. |
| 5 | 5 | WDI | Watchdog Timer Input. If WDI remains low or high for longer than the watchdog timeout period, $\overline{\text{RESET}}$ is asserted and the timer is cleared. The timer also clears whenever a reset is asserted or a rising or falling edge on WDI is detected. The watchdog timer enters a startup period that allows 54s for the first transition to occur before a reset. Leave WDI unconnected to disable the watchdog timer. The WDI floating-state detector uses a small 400nA current. Therefore, do not connect WDI to anything that will source or sink more than 200nA. Note that the leakage current specification for most three-state drivers exceeds 200nA. |
| 6 | 6 | GND | Ground |
| 7 | 7 | VCC | Unmonitored Power-Supply Input |
| 8 | — | OUT5 | Output 5. When the voltage at IN5 falls below its threshold, OUT5 goes low and stays low until the voltage at IN5 exceeds its threshold. The open-drain output has a 30μA internal pullup to VCC. |
| 9 | — | OUT6 | Output 6. When the voltage at IN6 falls below its threshold, OUT6 goes low and stays low until the voltage at IN6 exceeds its threshold. The open-drain output has a 30μA internal pullup to VCC. |
| 10 | — | OUT7 | Output 7. When the voltage at IN7 falls below its threshold, OUT7 goes low and stays low until the voltage at IN7 exceeds its threshold. The open-drain output has a 30μA internal pullup to VCC. |
| 11 | — | OUT8 | Output 8. When the voltage at IN8 falls below its threshold, OUT8 goes low and stays low until the voltage at IN8 exceeds its threshold. The open-drain output has a 30μA internal pullup to VCC. |
| 12 | 10 | $\overline{\text{MR}}$ | Active-Low Manual Reset Input. Pull $\overline{\text{MR}}$ low to assert $\overline{\text{RESET}}$ low. $\overline{\text{RESET}}$ remains low for the reset timeout period after $\overline{\text{MR}}$ is deasserted. $\overline{\text{MR}}$ is pulled up to VCC through a 20kΩ resistor. |
| 13 | 11 | SRT | Set Reset Timeout Input. Connect a capacitor from SRT to GND to set the reset timeout period. The reset timeout period can be calculated as follows: Reset Timeout (s) = $2.06 \times 10^6 (\Omega) \times C_{\text{SRT}} (\text{F})$. For the internal timeout period of 140ms (min), connect SRT to VCC. |

Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

Pin Description (MAX16006/MAX16007) (continued)

| PIN | | NAME | FUNCTION |
|----------|-----------------|----------------------------|--|
| MAX16006 | MAX16007 | | |
| 14 | 12 | $\overline{\text{MARGIN}}$ | Margin Disable Input. Pull $\overline{\text{MARGIN}}$ low to deassert all outputs (go into high state), regardless of the voltage at any monitored input. |
| 15 | — | OUT4 | Output 4. When the voltage at IN4 falls below its threshold, OUT4 goes low and stays low until the voltage at IN4 exceeds its threshold. The open-drain output has a 30μA internal pullup to V _{CC} . |
| 16 | — | OUT3 | Output 3. When the voltage at IN3 falls below its threshold, OUT3 goes low and stays low until the voltage at IN3 exceeds its threshold. The open-drain output has a 30μA internal pullup to V _{CC} . |
| 17 | — | OUT2 | Output 2. When the voltage at IN2 falls below its threshold, OUT2 goes low and stays low until the voltage at IN2 exceeds its threshold. The open-drain output has a 30μA internal pullup to V _{CC} . |
| 18 | — | OUT1 | Output 1. When the voltage at IN1 falls below its threshold, OUT1 goes low and stays low until the voltage at IN1 exceeds its threshold. The open-drain output has a 30μA internal pullup to V _{CC} . |
| 19 | 15 | $\overline{\text{RESET}}$ | Active-Low Reset Output. $\overline{\text{RESET}}$ asserts low when any of the monitored voltages falls below its respective threshold or $\overline{\text{MR}}$ is asserted. $\overline{\text{RESET}}$ remains asserted for the reset timeout period after all monitored voltages exceed their respective thresholds and $\overline{\text{MR}}$ is deasserted. This open-drain output has a 30μA internal pullup. |
| 20 | 16 | IN1 | Monitored Input Voltage 1. See Table 1 for the input voltage threshold. |
| 21 | 17 | IN2 | Monitored Input Voltage 2. See Table 1 for the input voltage threshold. |
| 22 | 18 | IN3 | Monitored Input Voltage 3. See Table 1 for the input voltage threshold. |
| 23 | 19 | IN4 | Monitored Input Voltage 4. See Table 1 for the input voltage threshold. |
| 24 | 20 | TOL | Threshold Tolerance Input. Connect TOL to GND to select 5% threshold tolerance. Connect TOL to V _{CC} to select 10% threshold tolerance. |
| — | 8, 9, 13, 14 | N.C. | Not Internally Connected |
| — | — | EP | Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal resistance path from the IC junction to the PCB. Do not use as the electrical connection to GND. |

MAX16000–MAX16007

Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

Table 1. Input-Voltage-Threshold Selector

| PART | IN1 | IN2 | IN3 | IN4 | IN5 | IN6 | IN7 | IN8 |
|------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| MAX16000A | 3.3 | 2.5 | ADJ | 1.8 | — | — | — | — |
| MAX16000B | 3.3 | ADJ | ADJ | 1.8 | — | — | — | — |
| MAX16000C | ADJ | 2.5 | ADJ | 1.8 | — | — | — | — |
| MAX16000D | 3.3 | 2.5 | ADJ | ADJ | — | — | — | — |
| MAX16000E | ADJ | ADJ | ADJ | ADJ | — | — | — | — |
| MAX16001A | 3.3 | 2.5 | ADJ | 1.8 | — | — | — | — |
| MAX16001B | 3.3 | ADJ | ADJ | 1.8 | — | — | — | — |
| MAX16001C | ADJ | 2.5 | ADJ | 1.8 | — | — | — | — |
| MAX16001D | 3.3 | 2.5 | ADJ | ADJ | — | — | — | — |
| MAX16001E | ADJ | ADJ | ADJ | ADJ | — | — | — | — |
| MAX16002A | 3.3 | 2.5 | ADJ | 1.8 | — | — | — | — |
| MAX16002B | 3.3 | ADJ | ADJ | 1.8 | — | — | — | — |
| MAX16002C | ADJ | 2.5 | ADJ | 1.8 | — | — | — | — |
| MAX16002D | 3.3 | 2.5 | ADJ | ADJ | — | — | — | — |
| MAX16002E | ADJ | ADJ | ADJ | ADJ | — | — | — | — |
| MAX16003A | 3.3 | 2.5 | ADJ | 1.8 | ADJ | ADJ | — | — |
| MAX16003B | 3.3 | ADJ | ADJ | 1.8 | ADJ | ADJ | — | — |
| MAX16003C | 3.3 | 2.5 | ADJ | ADJ | ADJ | ADJ | — | — |
| MAX16003D | ADJ | 2.5 | ADJ | 1.8 | ADJ | ADJ | — | — |
| MAX16003E | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ | — | — |
| MAX16004A | 3.3 | 2.5 | ADJ | 1.8 | ADJ | ADJ | — | — |
| MAX16004B | 3.3 | ADJ | ADJ | 1.8 | ADJ | ADJ | — | — |
| MAX16004C | 3.3 | 2.5 | ADJ | ADJ | ADJ | ADJ | — | — |
| MAX16004D | ADJ | 2.5 | ADJ | 1.8 | ADJ | ADJ | — | — |
| MAX16004E | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ | — | — |
| MAX16005A | 3.3 | 2.5 | ADJ | 1.8 | ADJ | ADJ | — | — |
| MAX16005B | 3.3 | ADJ | ADJ | 1.8 | ADJ | ADJ | — | — |
| MAX16005C | 3.3 | 2.5 | ADJ | ADJ | ADJ | ADJ | — | — |
| MAX16005D | ADJ | 2.5 | ADJ | 1.8 | ADJ | ADJ | — | — |
| MAX16005E | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ | — | — |
| MAX16006A | 3.3 | 2.5 | ADJ | 1.8 | ADJ | ADJ | ADJ | ADJ |
| MAX16006B | 3.3 | ADJ | ADJ | 1.8 | ADJ | ADJ | ADJ | ADJ |
| MAX16006C | 3.3 | 2.5 | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ |
| MAX16006D | ADJ | 2.5 | ADJ | 1.8 | ADJ | ADJ | ADJ | ADJ |
| MAX16006E | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ |
| MAX16006F | 5.0 | 3.3 | 3.0 | 2.5 | 1.8 | 1.5 | 1.2 | 0.9 |
| MAX16007A | 3.3 | 2.5 | ADJ | 1.8 | ADJ | ADJ | ADJ | ADJ |
| MAX16007B | 3.3 | ADJ | ADJ | 1.8 | ADJ | ADJ | ADJ | ADJ |
| MAX16007C | 3.3 | 2.5 | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ |
| MAX16007D | ADJ | 2.5 | ADJ | 1.8 | ADJ | ADJ | ADJ | ADJ |
| MAX16007E | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ |

Note: Other fixed thresholds may be available. Contact factory for availability.

Low-Voltage, Quad-/Hex-/Octal-Voltage μ P Supervisors

Functional Diagrams

MAX16000-MAX16007

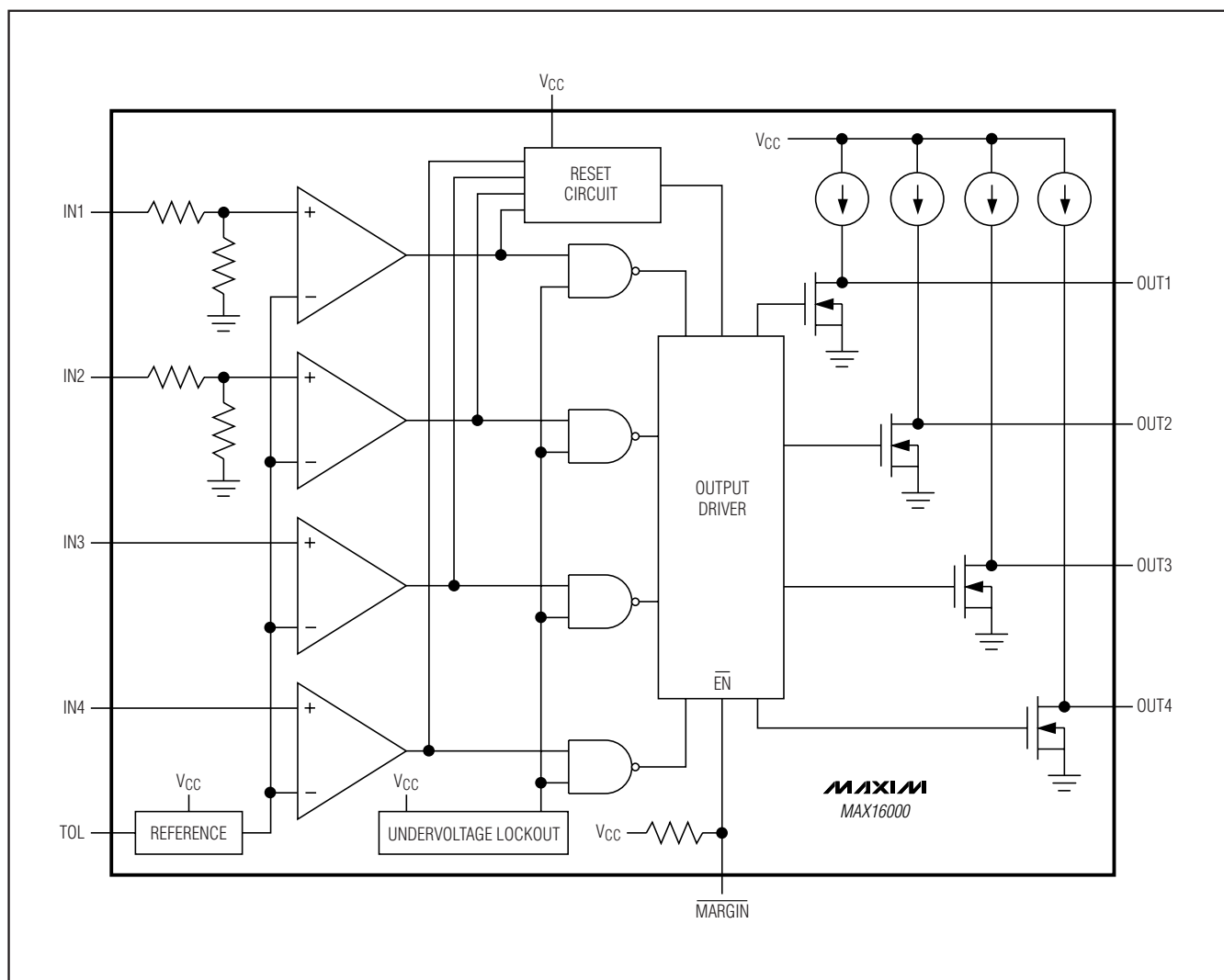


Figure 1. MAX16000D Functional Diagram

Low-Voltage, Quad-/Hex-/Octal-Voltage μ P Supervisors

Functional Diagrams (continued)

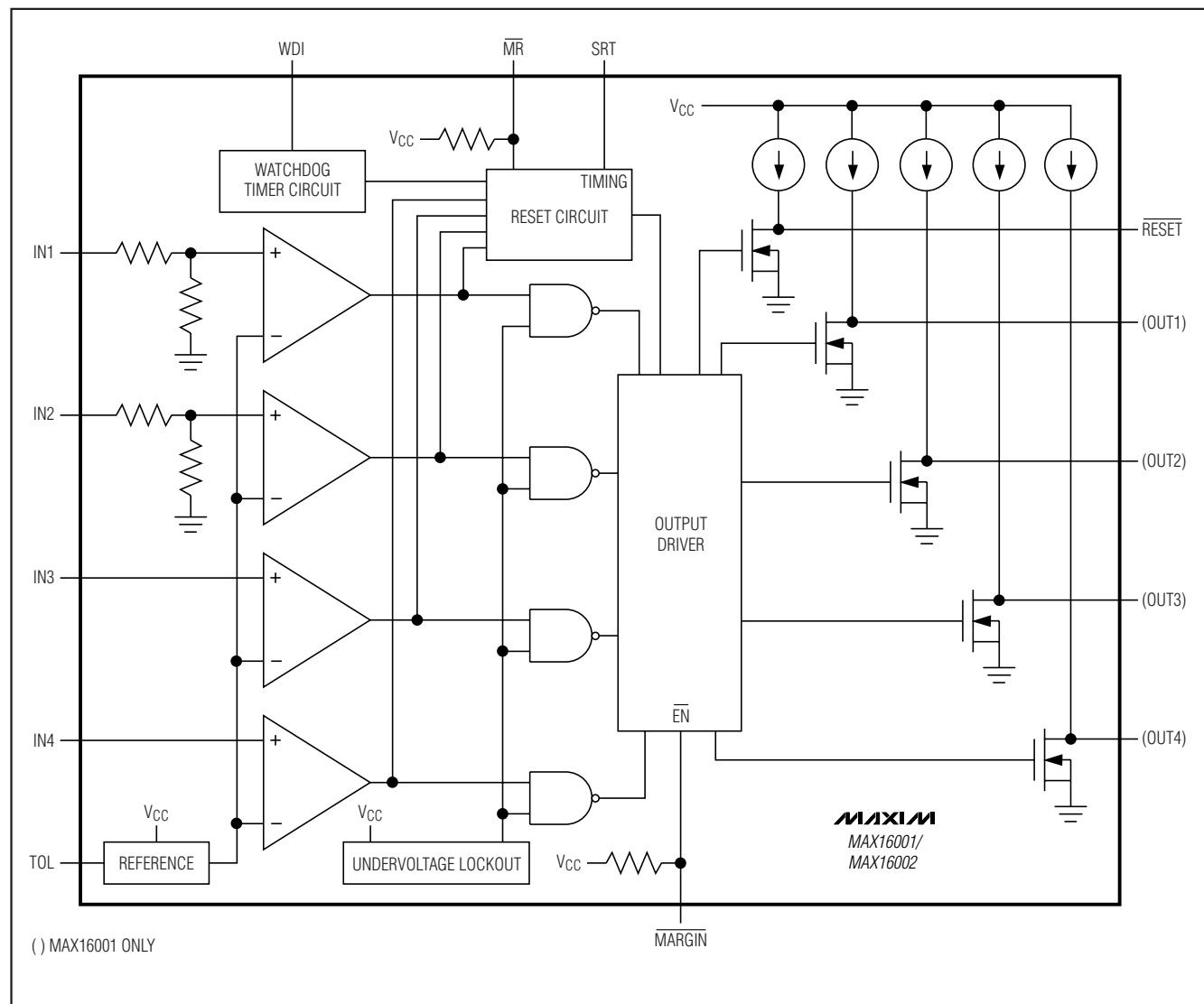


Figure 2. MAX16001D/MAX16002D Functional Diagram

Low-Voltage, Quad-/Hex-/Octal-Voltage μ P Supervisors

Functional Diagrams (continued)

MAX16000-MAX16007

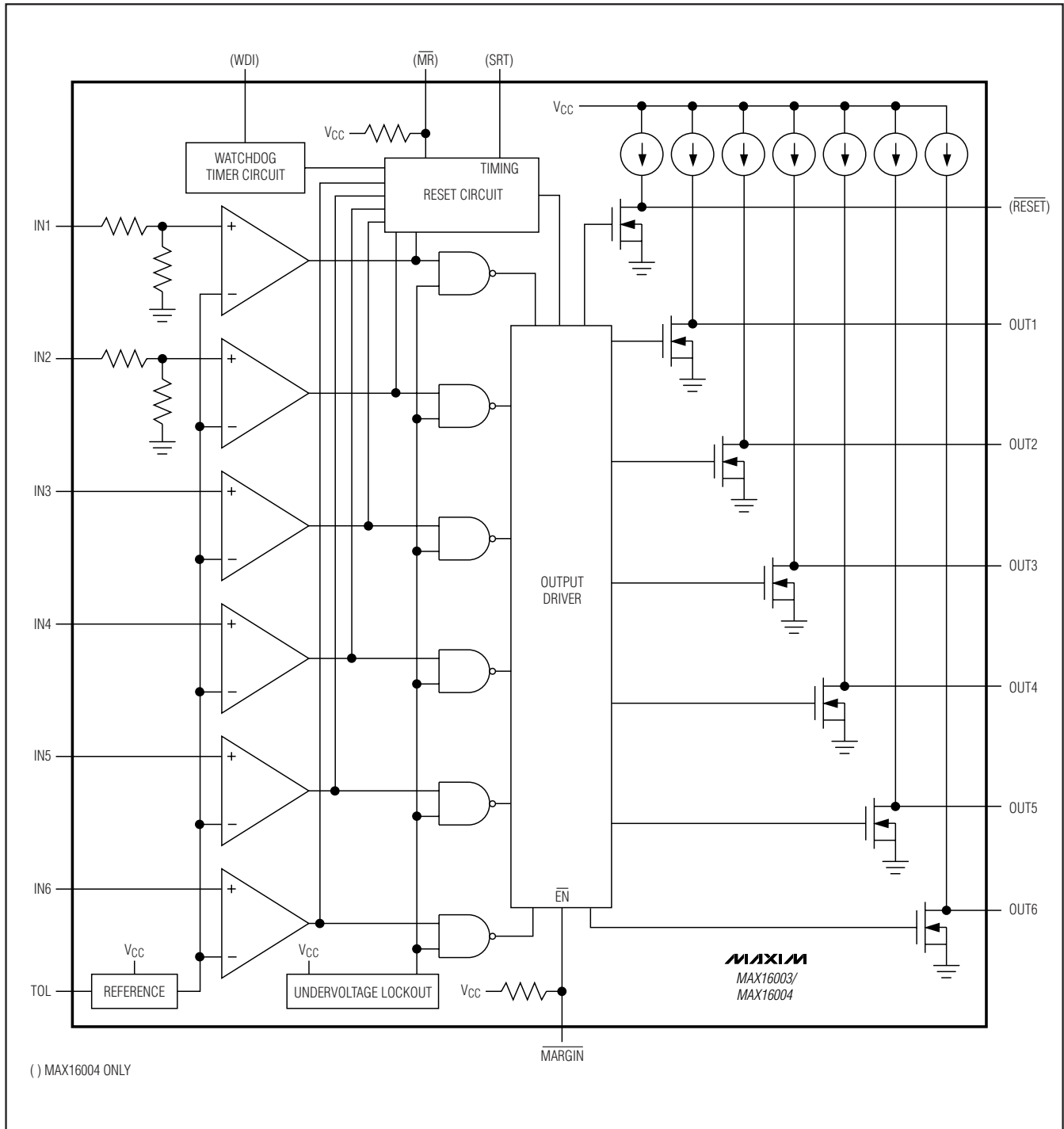


Figure 3. MAX16003C/MAX16004C Functional Diagram

Low-Voltage, Quad-/Hex-/Octal-Voltage μ P Supervisors

Functional Diagrams (continued)

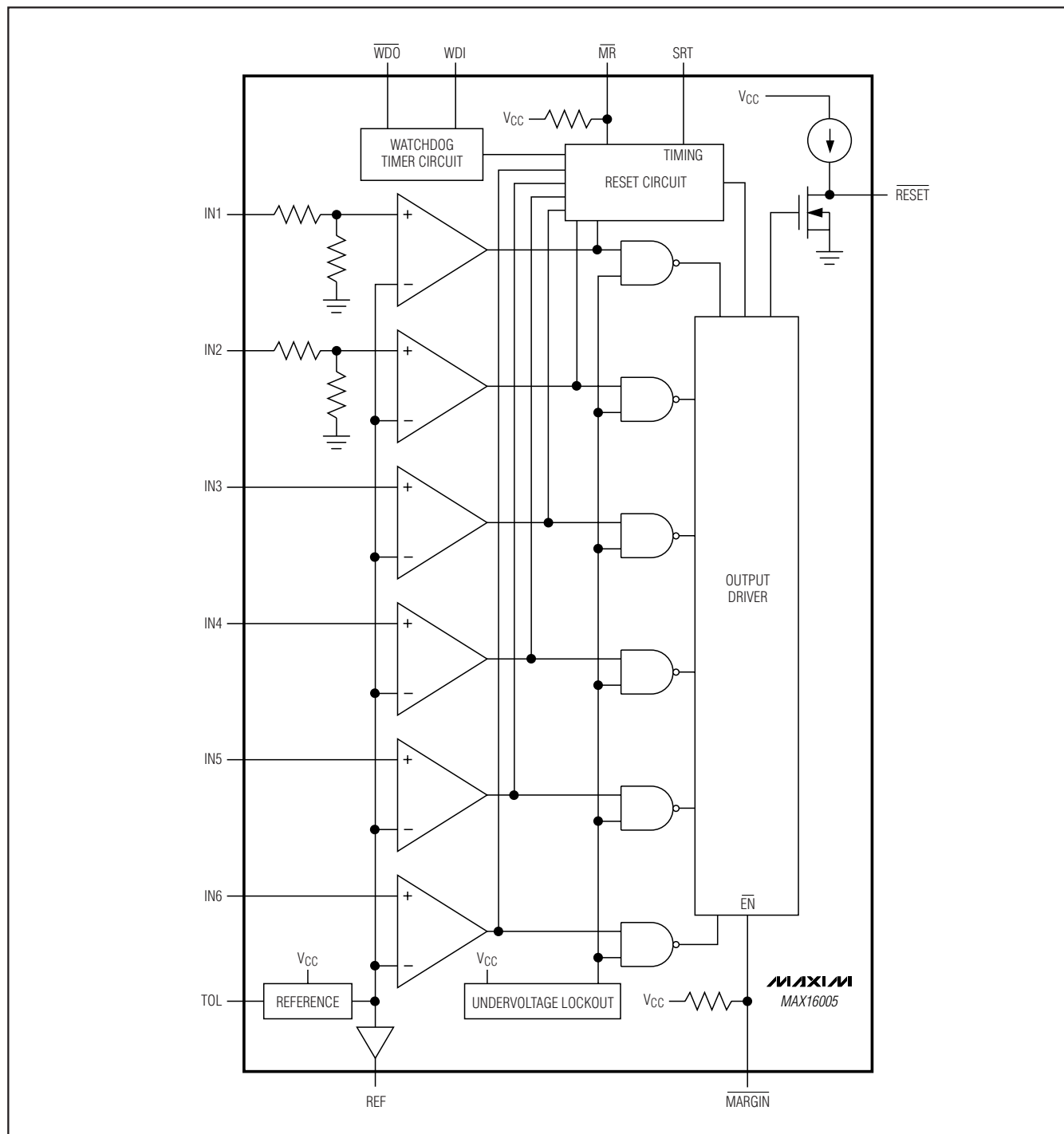


Figure 4. MAX16005C Functional Diagram

Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

Functional Diagrams (continued)

MAX16000-MAX16007

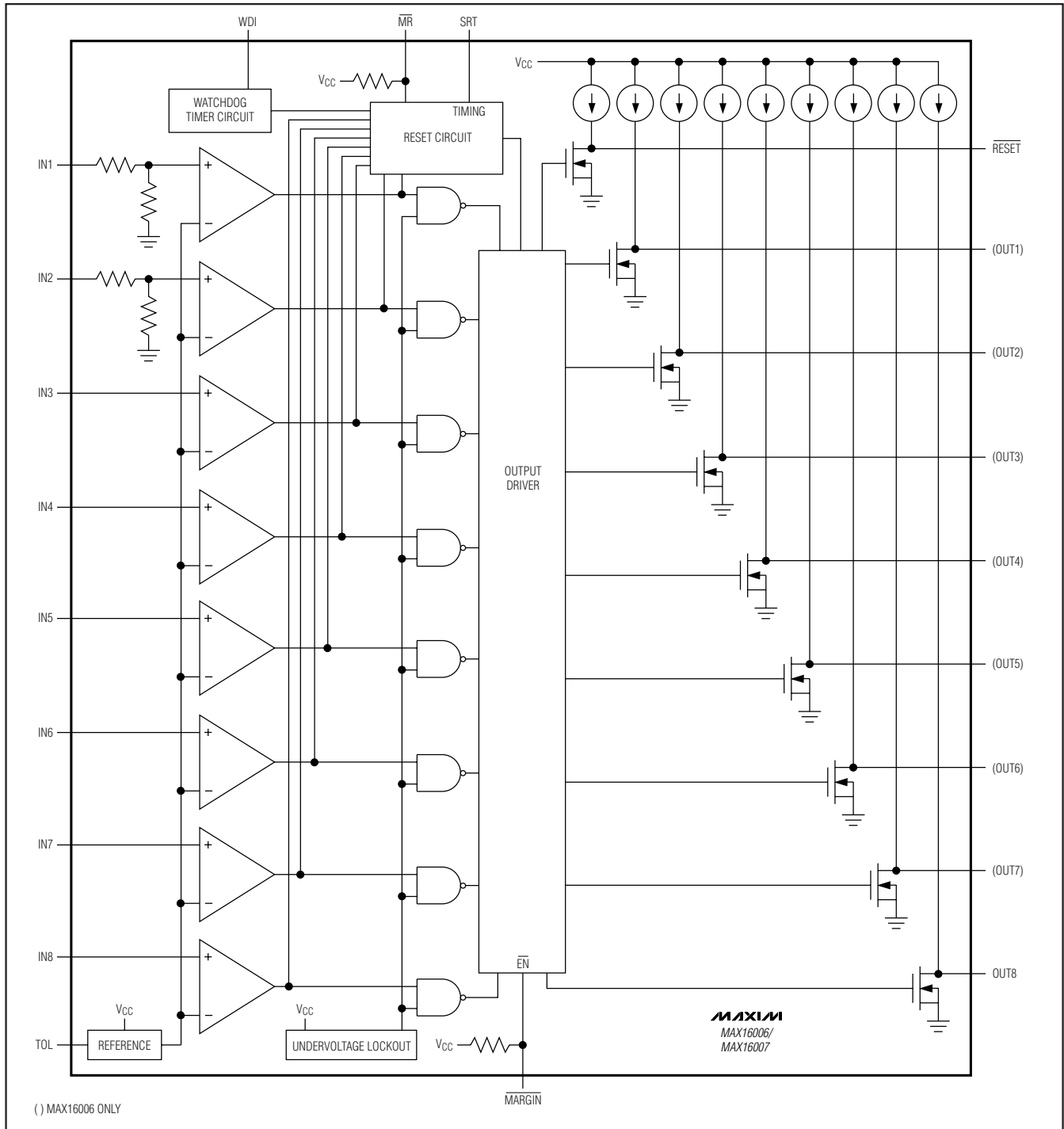


Figure 5. MAX16006C/MAX16007C Functional Diagram

Low-Voltage, Quad-/Hex-/Octal-Voltage μ P Supervisors

Detailed Description

The MAX16000–MAX16007 are low-voltage, quad-/hex-/octal-voltage μ P supervisors in small thin QFN and TSSOP packages. These devices provide supervisory functions for complex multivoltage systems. The MAX16000/MAX16001/MAX16002 monitor four voltages, the MAX16003/MAX16004/MAX16005 monitor six voltages, and the MAX16006/MAX16007 monitor eight voltages.

The MAX16000/MAX16001/MAX16003/MAX16004/MAX16006 offer independent outputs for each monitored voltage. The MAX16001/MAX16002/MAX16004–MAX16007 offer a reset output that asserts whenever any of the monitored voltages fall below their respective thresholds or the manual reset input is asserted. The reset output remains asserted for the reset timeout after all voltages are above their respective thresholds and the manual reset input is deasserted. The minimum reset timeout is internally set to 140ms or can be adjusted with an external capacitor.

All open-drain outputs have internal 30 μ A pullups that eliminate the need for external pullup resistors. However, each output can be driven with an external voltage up to 5.5V. Other features offered include a manual reset input, a tolerance pin for selecting 5% or 10% input thresholds, and a margin enable function for deasserting the outputs during margin testing.

The MAX16001/MAX16002/MAX16004–MAX16007 offer a watchdog timer that asserts RESET or an independent watchdog output (MAX16005) when the watchdog timeout period (1.6s typ) is exceeded. The watchdog timer can be disabled by floating the input.

Applications Information

Undervoltage-Detection Circuit

The open-drain outputs of the MAX16000–MAX16007 can be configured to detect an undervoltage condition. Figure 6 shows a configuration where an LED turns on when the comparator output is low, indicating an undervoltage condition. These devices can also be used in applications such as system supervisory monitoring, multivoltage level detection, and V_{CC} bar-graph monitoring (Figure 7).

Tolerance (TOL)

The MAX16000–MAX16007 feature a pin-selectable threshold tolerance. Connect TOL to GND to select 5% threshold tolerance. Connect TOL to V_{CC} to select 10% threshold tolerance.

Window Detection

A window detector circuit uses two auxiliary inputs in the configuration shown in Figure 8. External resistors set the two threshold voltages of the window detector circuit. External logic gates create the OUT signal. The window detection width is the difference between the threshold voltages (Figure 9).

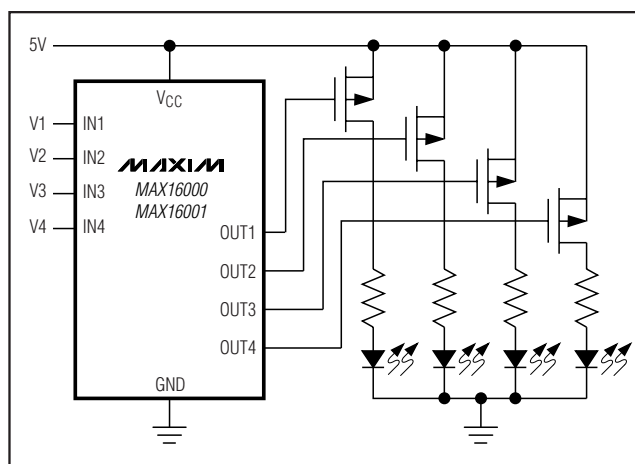


Figure 6. Quad Undervoltage Detector with LED Indicators

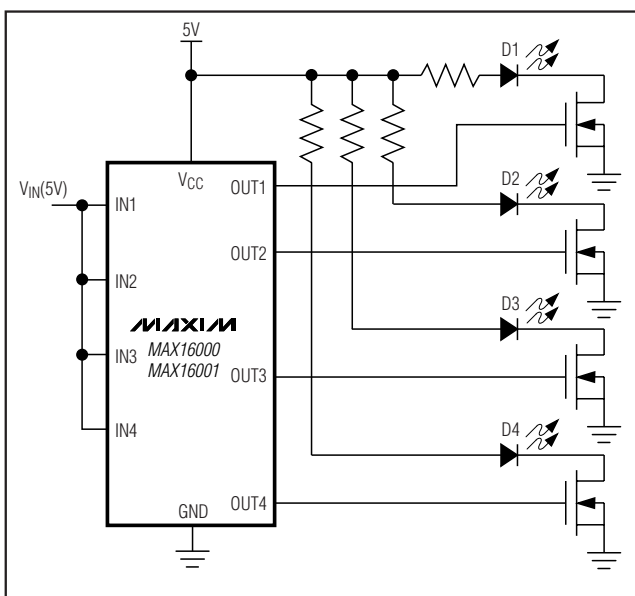


Figure 7. V_{CC} Bar-Graph Monitoring

Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

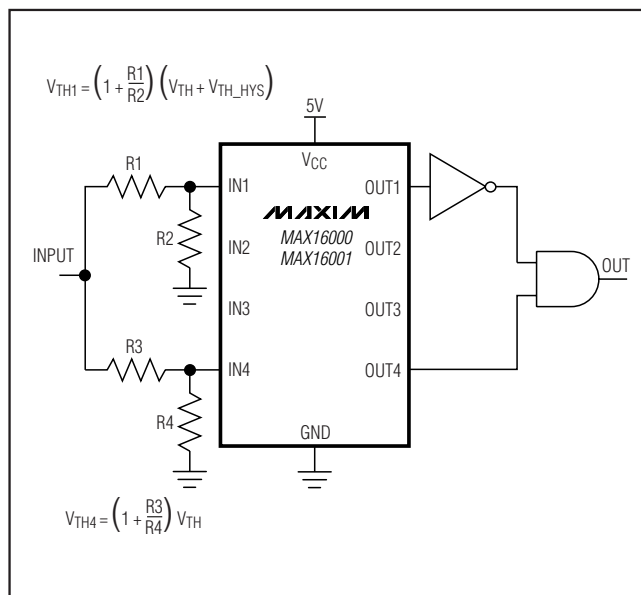


Figure 8. Window Detection

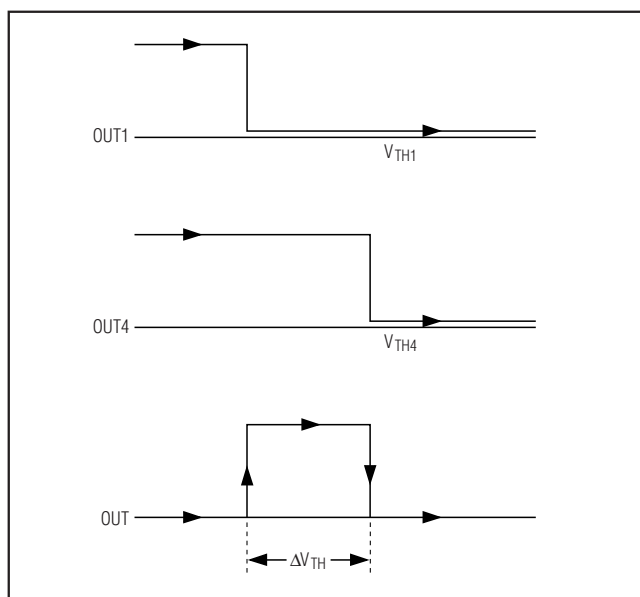


Figure 9. Output Response of Window Detector Circuit

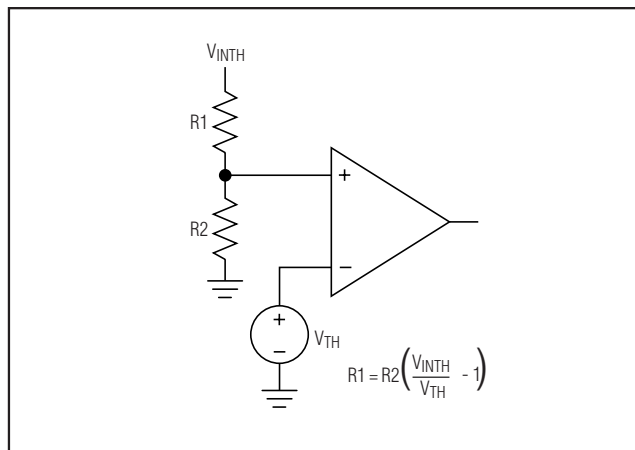


Figure 10. Setting the Adjustable Input

Adjustable Input

These devices offer several monitor options with adjustable input thresholds (see Table 1). The threshold voltage at each adjustable IN_{_} input is typically 0.394V (TOL = GND) or 0.372 (TOL = VCC). To monitor a voltage V_{INTH}, connect a resistive-divider network to the circuit as shown in Figure 10.

$$V_{INTH} = V_{TH} \left(\frac{R1}{R2} + 1 \right)$$

$$R1 = R2 \left(\frac{V_{INTH}}{V_{TH}} - 1 \right)$$

Large resistors can be used to minimize current through the external resistors. For greater accuracy, use lower-value resistors.

Unused Inputs

Connect any unused IN_{_} inputs to a voltage above its threshold.

OUT_{_} Outputs (MAX16000/MAX16001/MAX16003/ MAX16004/MAX16006)

The OUT_{_} outputs go low when their respective IN_{_} inputs drop below their specified thresholds. The output is open drain with a 30μA internal pullup to VCC. For many applications, no external pullup resistor is required to interface with other logic devices. An external pullup resistor to any voltage from 0 to 5.5V overrides the internal pullup if interfacing to different logic supply voltages. Internal circuitry prevents reverse current flow from the external pullup voltage to VCC (Figure 11).

Low-Voltage, Quad-/Hex-/Octal-Voltage μ P Supervisors

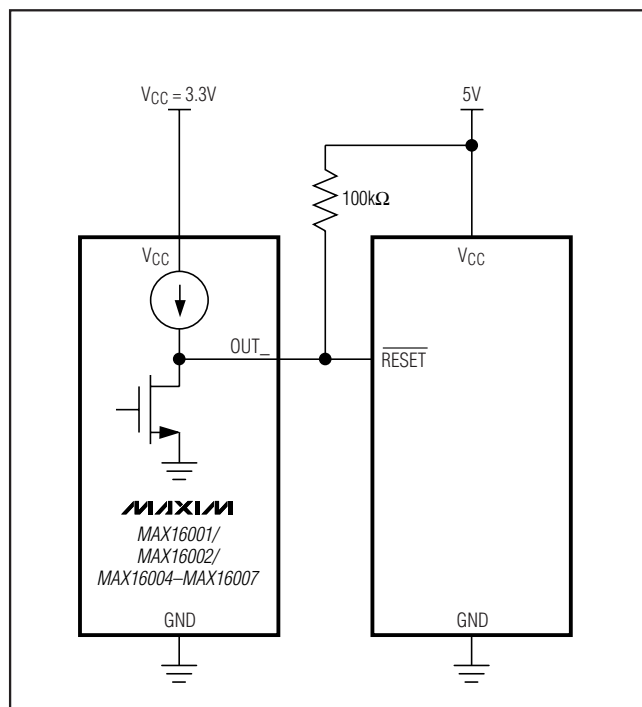


Figure 11. Interfacing to a Different Logic Supply Voltage

RESET Output (MAX16001/MAX16002/ MAX16004-MAX16007)

$\overline{\text{RESET}}$ asserts low when any of the monitored voltages fall below their respective thresholds or $\overline{\text{MR}}$ is asserted. $\overline{\text{RESET}}$ remains asserted for the reset timeout period after all monitored voltages exceed their respective thresholds and $\overline{\text{MR}}$ is deasserted (see Figure 12). This open-drain output has a 30 μ A internal pullup. An external pullup resistor to any voltage from 0 to 5.5V overrides the internal pullup if interfacing to different logic supply voltages. Internal circuitry prevents reverse current flow from the external pullup voltage to V_{CC} (Figure 11).

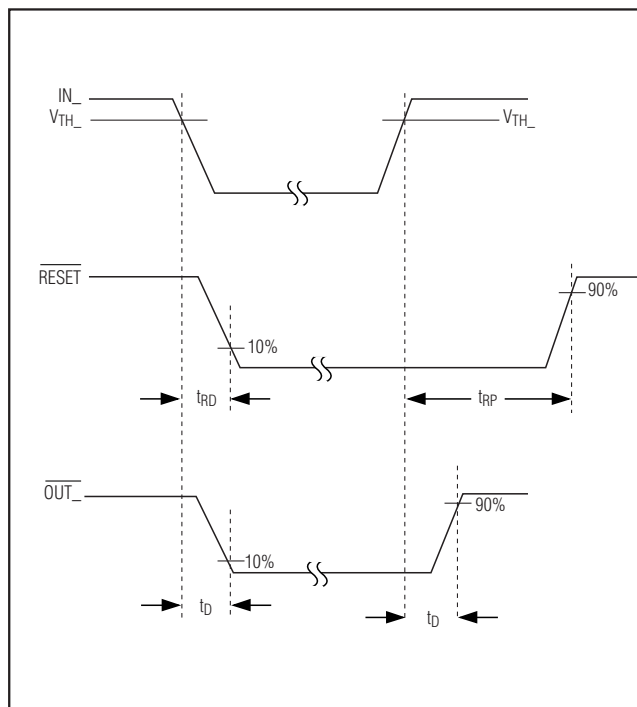


Figure 12. Output Timing Diagram

WDO (MAX16005 Only)

$\overline{\text{WDO}}$ asserts and stays low whenever any of the IN_n inputs fall below their respective thresholds. $\overline{\text{WDO}}$ deasserts without a timeout delay when all the IN_n inputs rise above their thresholds. When all the IN_n inputs rise above their thresholds, $\overline{\text{WDO}}$ asserts low whenever the watchdog timer times out. $\overline{\text{WDO}}$ deasserts after a valid WDI transition or if $\overline{\text{MR}}$ is pulled low. The watchdog timer begins counting after the reset timeout period once $\overline{\text{MR}}$ goes high. Pull $\overline{\text{MARGIN}}$ low to deassert $\overline{\text{WDO}}$ regardless of any other condition. The watchdog timer continues to run when $\overline{\text{MARGIN}}$ is low and if a timeout occurs. $\overline{\text{WDO}}$ will assert $\overline{\text{MR}}$ after $\overline{\text{MARGIN}}$ is deasserted. This open-drain output has a 30 μ A internal pullup. An external pullup resistor to any voltage from 0 to 5.5V overrides the internal pullup if interfacing to different logic supply voltages. Internal circuitry prevents reverse current flow from the external pullup voltage to V_{CC} (Figure 11).

Low-Voltage, Quad-/Hex-/Octal-Voltage μ P Supervisors

MAX16000-MAX16007

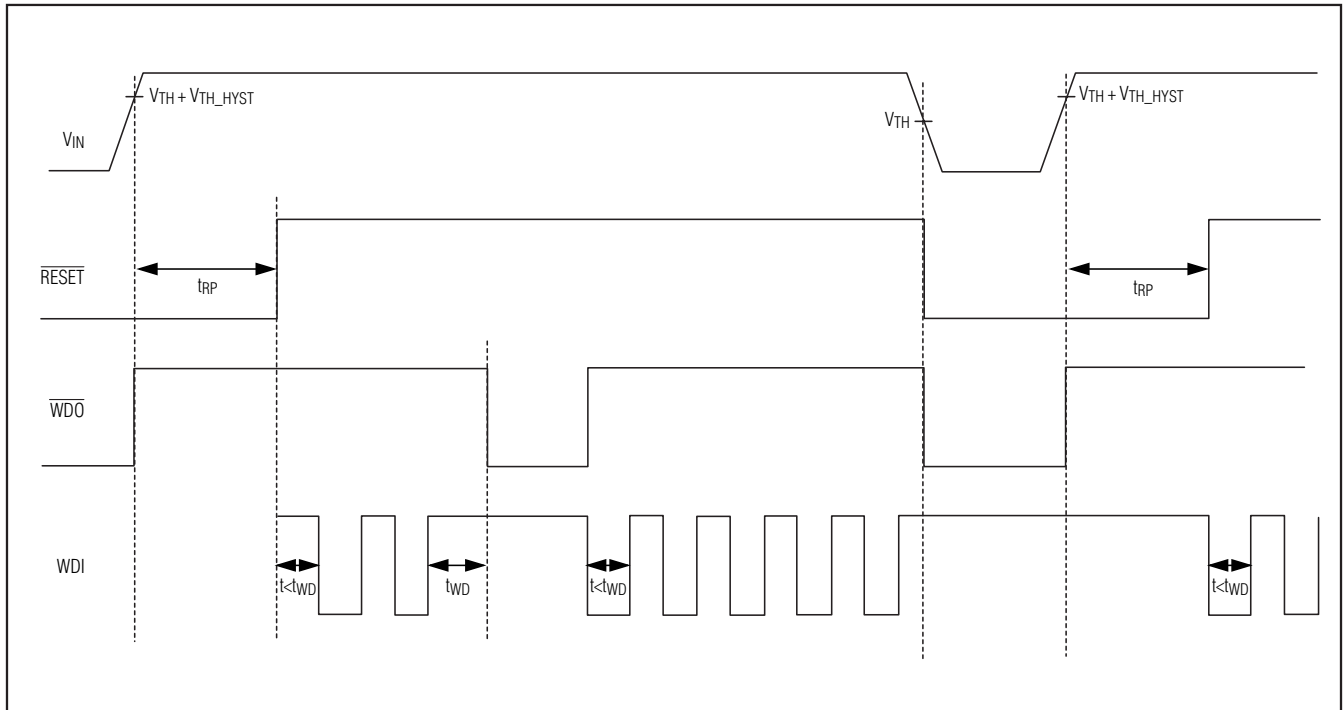


Figure 13. \overline{WDO} Timing Related to V_{TH} and t_{RP}

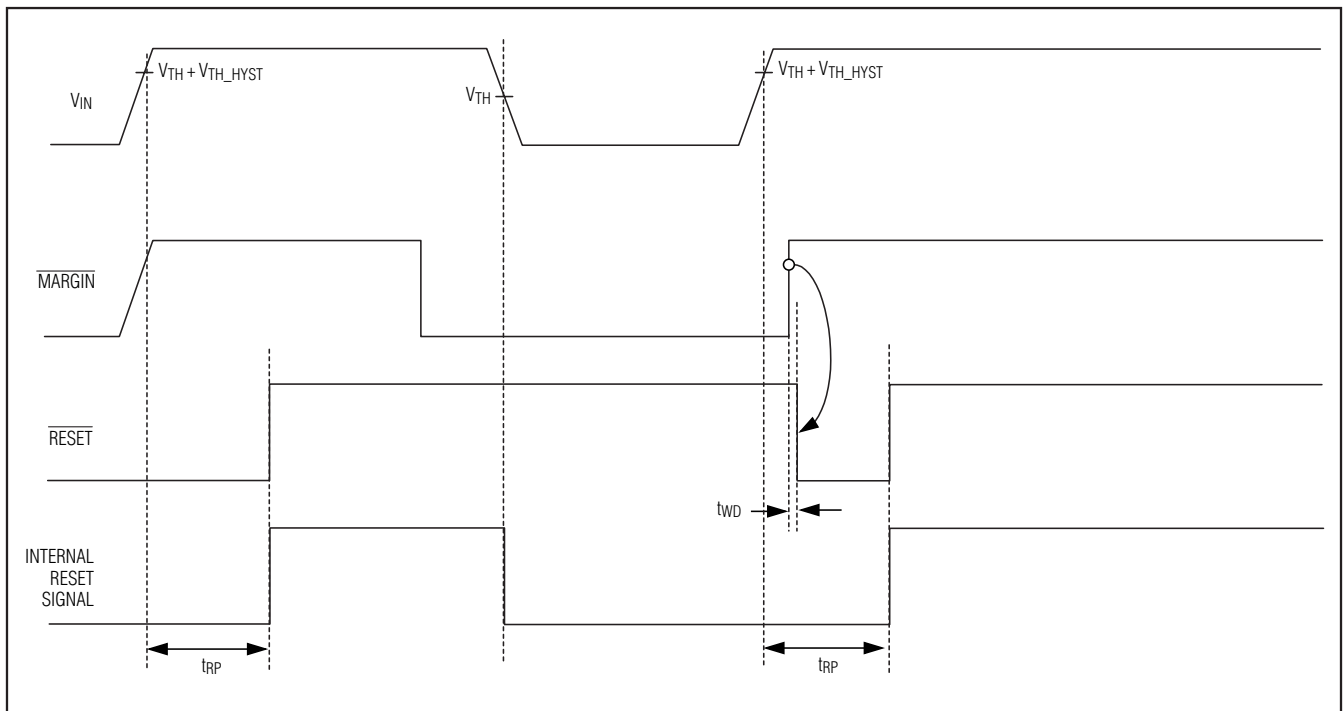


Figure 14. Margin Output Disable (\overline{MARGIN}) Affect on \overline{RESET} within t_{RP}

Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

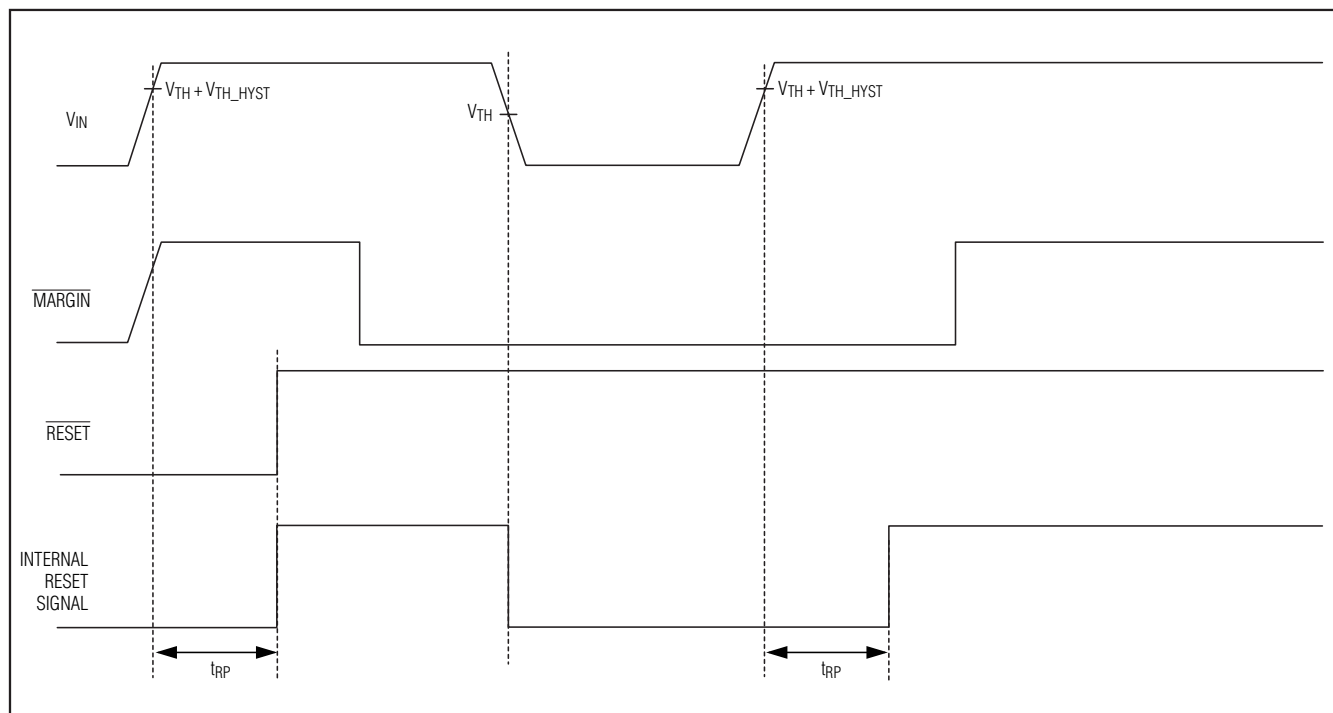


Figure 15. Margin Output Disable ($\overline{\text{MARGIN}}$) Affect on $\overline{\text{RESET}}$ Outside t_{RP}

Reset Timeout Capacitor

The reset timeout period can be adjusted to accommodate a variety of μP applications from 50 μs to 1.12s. Adjust the reset timeout period (t_{RP}) by connecting a capacitor (C_{SRT}) between SRT and GND. Calculate the reset timeout capacitor as follows:

$$C_{SRT} (\text{F}) = \frac{t_{RP} (\text{s}) \times I_{SRT}}{V_{TH_SRT}}$$

Connect SRT to V_{CC} for a factory-programmed reset timeout of 140ms (min).

Manual Reset Input (MR) (MAX16001/MAX16002/ MAX16004-MAX16007)

Many μP -based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic-low on $\overline{\text{MR}}$ asserts $\overline{\text{RESET}}$ low. $\overline{\text{RESET}}$ remains asserted while $\overline{\text{MR}}$ is low, and during the reset timeout period (140ms min) after $\overline{\text{MR}}$ returns high. The $\overline{\text{MR}}$ input has an internal 20k Ω pullup resistor to V_{CC} , so it can be left unconnected if not used. $\overline{\text{MR}}$ can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from

$\overline{\text{MR}}$ to GND to create a manual reset function. External debounce circuitry is not required. If $\overline{\text{MR}}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1 μF capacitor from $\overline{\text{MR}}$ to GND provides additional noise immunity.

Margin Output Disable ($\overline{\text{MARGIN}}$)

$\overline{\text{MARGIN}}$ allows system-level testing while power supplies are adjusted from their nominal voltages. Drive $\overline{\text{MARGIN}}$ low to force $\overline{\text{RESET}}$, $\overline{\text{WDO}}$, and $\overline{\text{OUT}}$ high, regardless of the voltage at any monitored input. The state of each output does not change while $\overline{\text{MARGIN}}$ = GND. The watchdog timer continues to run when $\overline{\text{MARGIN}}$ is low, and if a timeout occurs, $\overline{\text{WDO/RESET}}$ will assert t_{MD} after $\overline{\text{MARGIN}}$ is deasserted.

The $\overline{\text{MARGIN}}$ input is internally pulled up to V_{CC} . Leave $\overline{\text{MARGIN}}$ unconnected or connect to V_{CC} if unused.

Power-Supply Bypassing

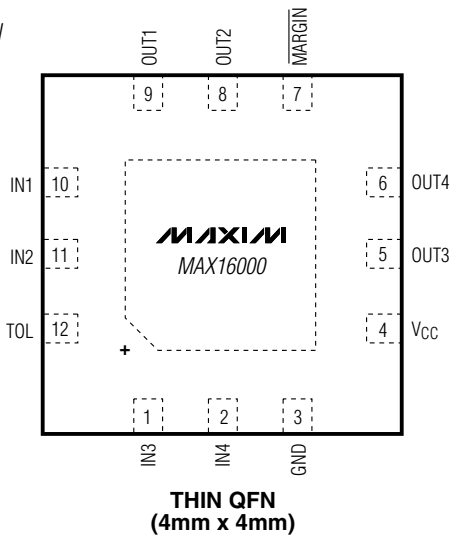
The MAX16000-MAX16007 operate from a 2.0V to 5.5V supply. An undervoltage lockout ensures that the outputs are in the correct states when the UVLO is exceeded. In noisy applications, bypass V_{CC} to ground with a 0.1 μF capacitor as close to the device as possible. The additional capacitor improves transient immunity. For fast-rising V_{CC} transients, additional capacitance may be required.

Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

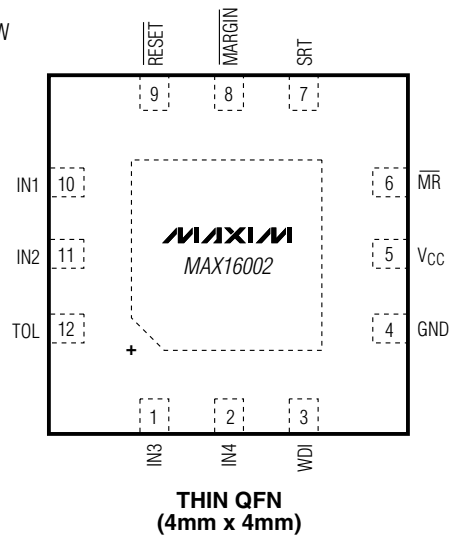
Pin Configurations

MAX16000-MAX16007

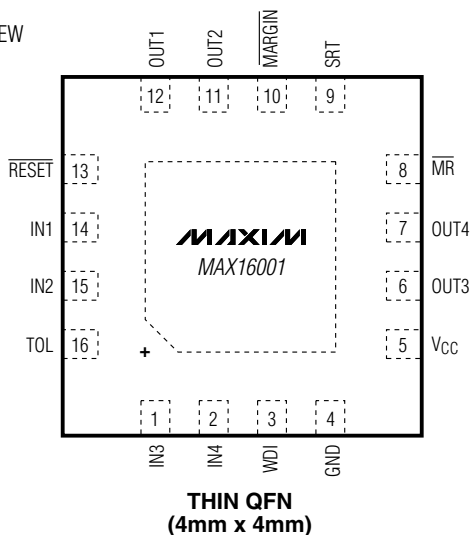
TOP VIEW



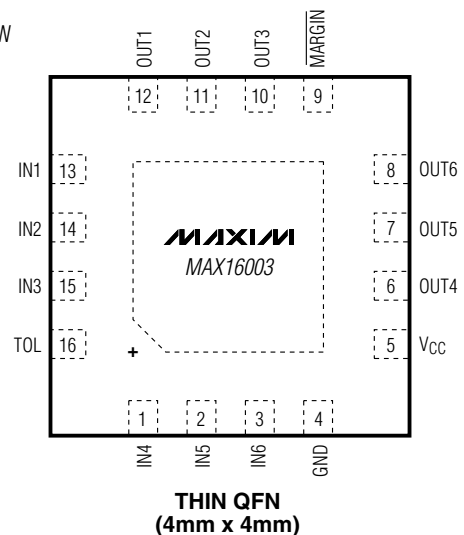
TOP VIEW



TOP VIEW

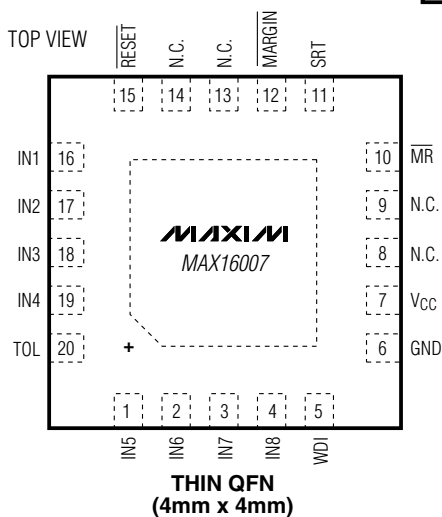
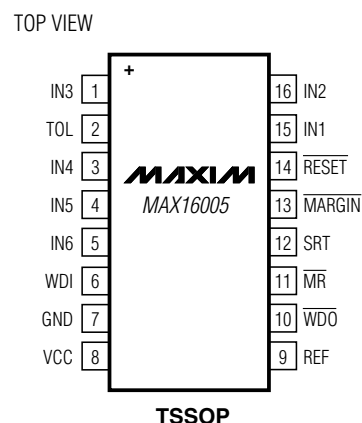
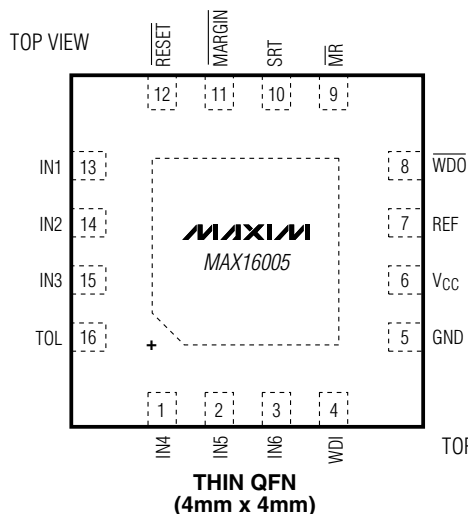
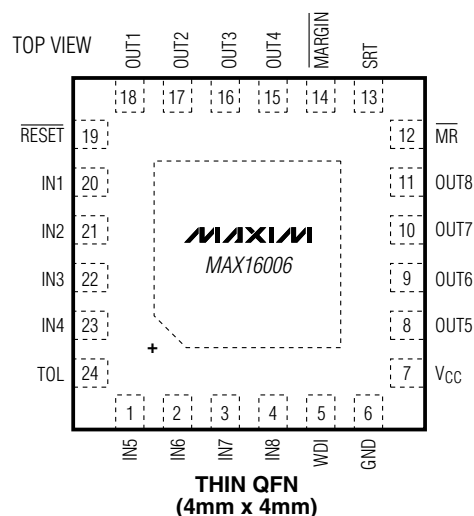
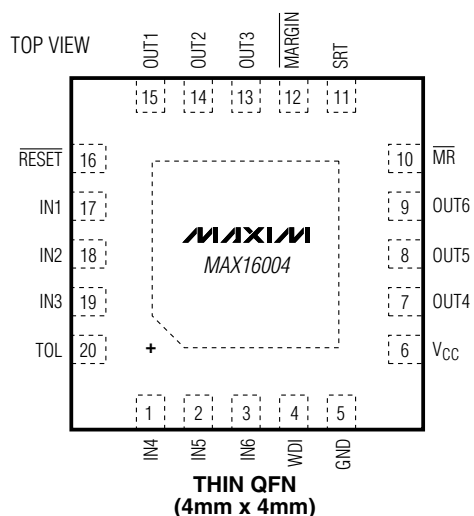


TOP VIEW



Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

Pin Configurations (continued)



Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

MAX16000-MAX16007

Ordering Information (continued)

| PART | TEMP RANGE | PIN-PACKAGE |
|--------------|-----------------|-------------|
| MAX16001_TE+ | -40°C to +125°C | 16 TQFN-EP* |
| MAX16002_TC+ | -40°C to +125°C | 12 TQFN-EP* |
| MAX16003_TE+ | -40°C to +125°C | 16 TQFN-EP* |
| MAX16004_TP+ | -40°C to +125°C | 20 TQFN-EP* |
| MAX16005_TE+ | -40°C to +125°C | 16 TQFN-EP* |
| MAX16005_UE+ | -40°C to +125°C | 16 TSSOP |
| MAX16006_TG+ | -40°C to +125°C | 24 TQFN-EP* |
| MAX16007_TP+ | -40°C to +125°C | 20 TQFN-EP* |

Note: The “_” is a placeholder for the input voltage threshold.
See Table 1.

+Denotes lead(Pb)-free/RoHS-compliant package.

For tape-and-reel, add a “T” after the “+.” Tape-and-reel are offered in 2.5k increments.

*EP = Exposed pad.

PROCESS: BiCMOS

Chip Information

Selector Guide

| PART | MONITORED VOLTAGES | INDEPENDENT OUTPUTS | RESET | WDI/WDO | MR | ADJUSTABLE RESET TIMEOUT |
|----------|--------------------|---------------------|-------|---------|----|--------------------------|
| MAX16000 | 4 | 4 | — | — | — | — |
| MAX16001 | 4 | 4 | ✓ | WDI | ✓ | ✓ |
| MAX16002 | 4 | — | ✓ | WDI | ✓ | ✓ |
| MAX16003 | 6 | 6 | — | — | — | — |
| MAX16004 | 6 | 6 | ✓ | WDI | ✓ | ✓ |
| MAX16005 | 6 | — | ✓ | WDI/WDO | ✓ | ✓ |
| MAX16006 | 8 | 8 | ✓ | WDI | ✓ | ✓ |
| MAX16007 | 8 | — | ✓ | WDI | ✓ | ✓ |

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|--------------|--------------|-------------------------|
| 12 TQFN | T1244-4 | 21-0139 |
| 16 TSSOP | U16-2 | 21-0108 |
| 16 TQFN | T1644-4 | 21-0139 |
| 20 TQFN | T2044-3 | 21-0139 |
| 24 TQFN | T2444-4 | 21-0139 |

Low-Voltage, Quad-/Hex-/Octal-Voltage μP Supervisors

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|--------------------|------------------|--|-----------------------------|
| 0 | 12/05 | Initial release | — |
| 1 | 1/06 | Released MAX16003 and MAX16004. | 20, 21 |
| 2 | 7/06 | Released MAX16005. Updated <i>Pin Description</i> and <i>Detailed Description</i> . | 1, 4, 7, 9, 10, 20, 21 |
| 3 | 12/08 | Added the MAX16005 TSSOP package. Modified the <i>Detailed Description</i> , and added Figures 13, 14, and 15. | 1, 2, 7, 8, 9, 10, 20–26 |

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

26 **Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600**