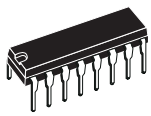
M74HC4538

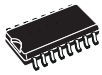
Dual retriggerable monostable multivibrator

Features

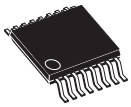
- High speed:
  t_{PD} = 25 ns (typ.) at V_{CC} = 6 V
- Low power dissipation
  standby state:
  I_{CC} = 4 µA (max.) at T_A = 25 °C
  active state:
  I_{CC} = 200 µA (max.) at V_{CC} = 6 V
- High noise immunity:
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (min.)
- Symmetrical output impedance:
  $|I_{OH}| = I_{OL}$ = 4 mA (min.)
- Balanced propagation delays:
  $t_{PLH} \cong t_{PHL}$
- Wide operating voltage range:
  V_{CC} (opr) = 2 to 6 V
- Wide output pulse width range:
  t_{WOUT} = 120 ns ~ 60 s over at V_{CC} = 4.5 V
- Pin and function compatible with
  74 series 4538



DIP-16



SO-16



TSSOP16

Description

The M74HC4538 is a high speed CMOS monostable multivibrator fabricated with silicon gate C^2MOS technology.

Each multivibrator features both a negative A, and a positive B, edge triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The monostable multivibrators are retriggerable. That is, they may be triggered repeatedly while their outputs are generating a pulse and the pulse will be extended. Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques.

The output pulse equation is simply: PW = 0.7 (R)(C) where PW is in seconds, R in Omhs and C is in Farads.

All the inputs are equipped with protection circuits against static discharge and transient excess voltage.

Table 1. Device summary

Order code	Package	Packaging
M74HC4538B1R	DIP-16	Tube
M74HC4538RM13TR	SO-16	Tape and reel
M74HC4538TTR	TSSOP16	Tape and reel

1 Pin connection and IEC logic symbols

Figure 1. Pin connections and IEC logic symbols

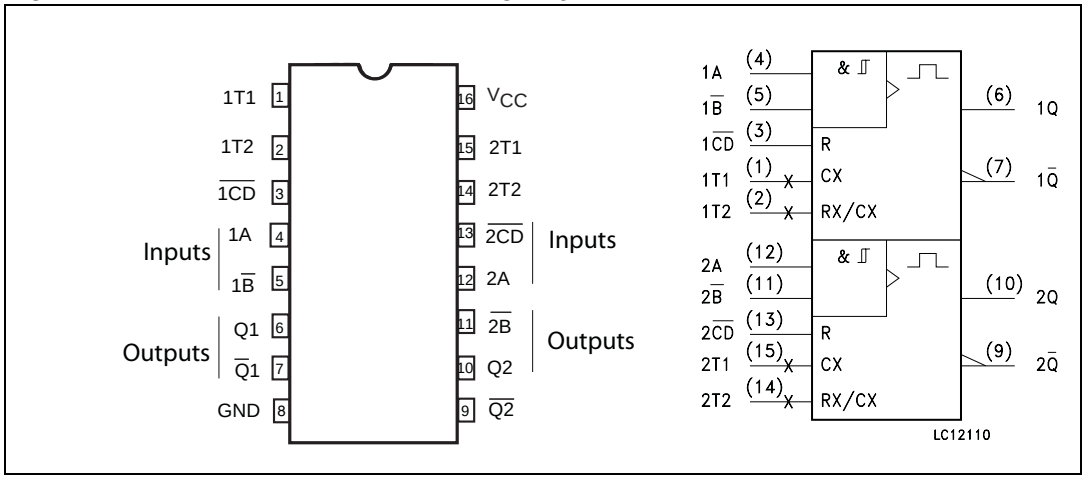


Table 2. Pin description

Pin number	Symbol	Name and function
1, 15	1T1, 2T1	External capacitor connections
2, 14	1T2, 2T2	External resistor, capacitor connections
3, 13	$1\overline{CD}$, $2\overline{CD}$	Direct reset inputs (active low)
4, 12	1A, 2A	Trigger inputs (low to high, edge-triggered)
5, 11	$\overline{1B}$, $\overline{2B}$	Trigger inputs (high to low, edge-triggered)
6, 10	Q1, Q2	Pulse outputs
7, 9	$\overline{Q1}$, $\overline{Q2}$	Complementary pulse outputs
8	GND	Ground (0 V)
16	V_{CC}	Positive supply voltage

Figure 2. Input and output equivalent circuit

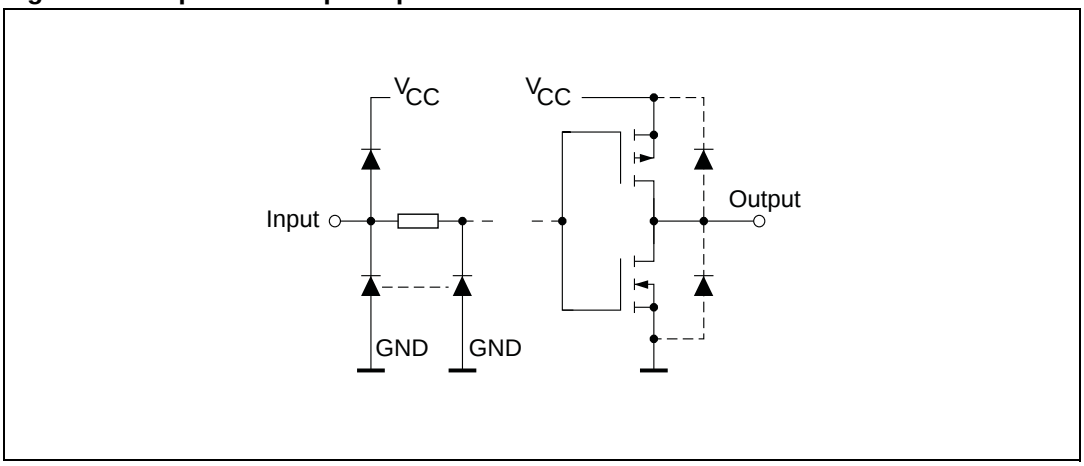


Table 3. Truth table

Inputs			Outputs		Note
A	$\overline{B}$	$\overline{CD}$	Q	$\overline{Q}$	
⌐	H	H	⌐¬	¬⌐	Output enable
X	L	H	L	H	Inhibit
H	X	H	L	H	Inhibit
L	¬	H	⌐¬	¬⌐	Output enable
X	X	L	L	H	Inhibit

Figure 3. System diagram

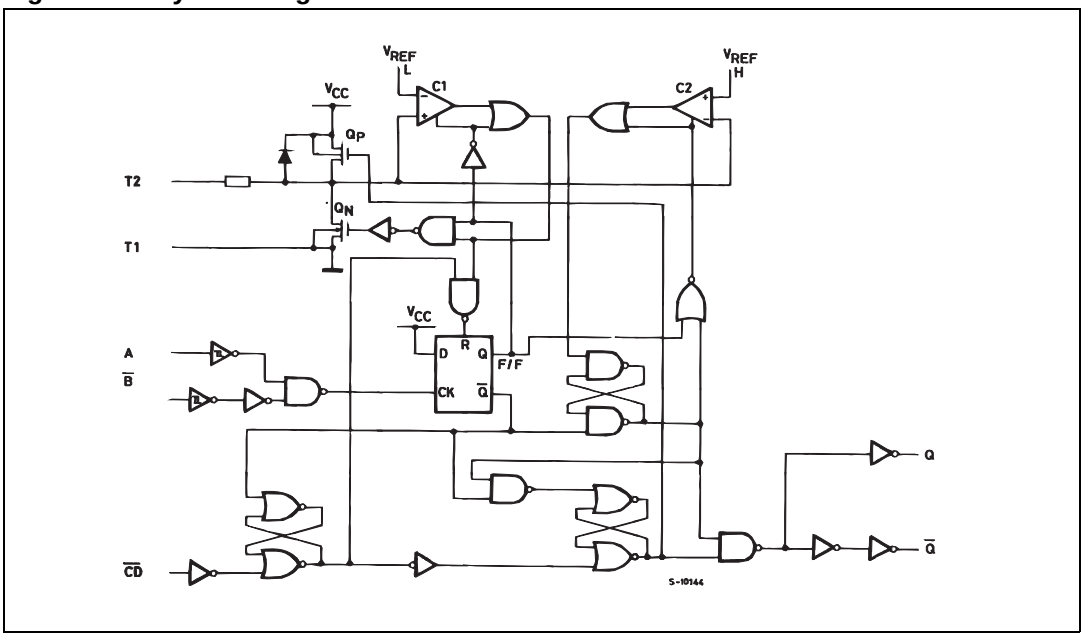


Figure 4. Timing chart

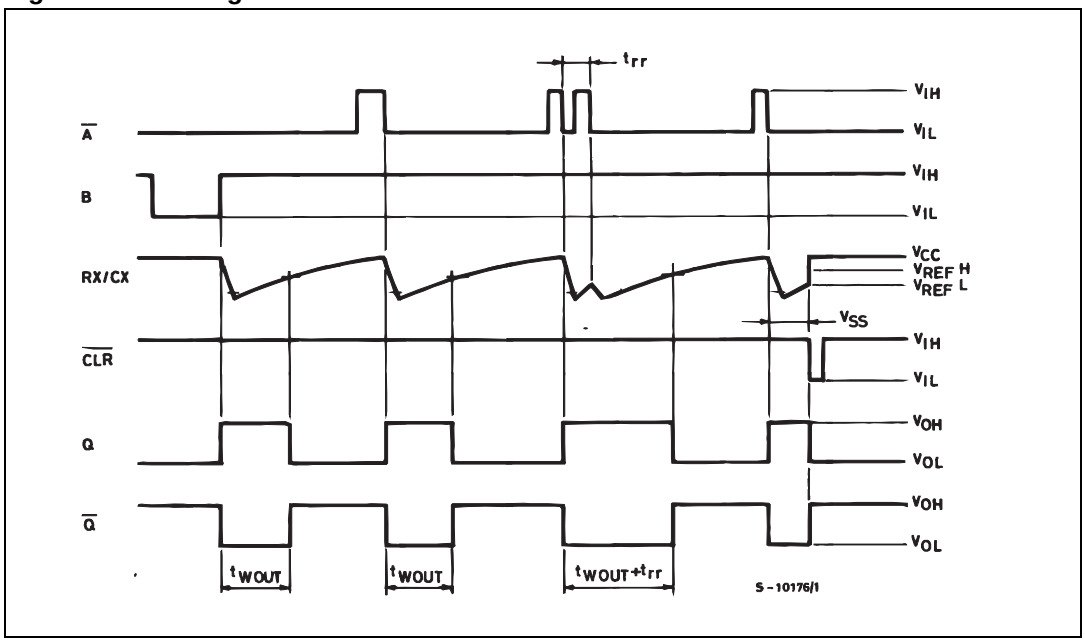
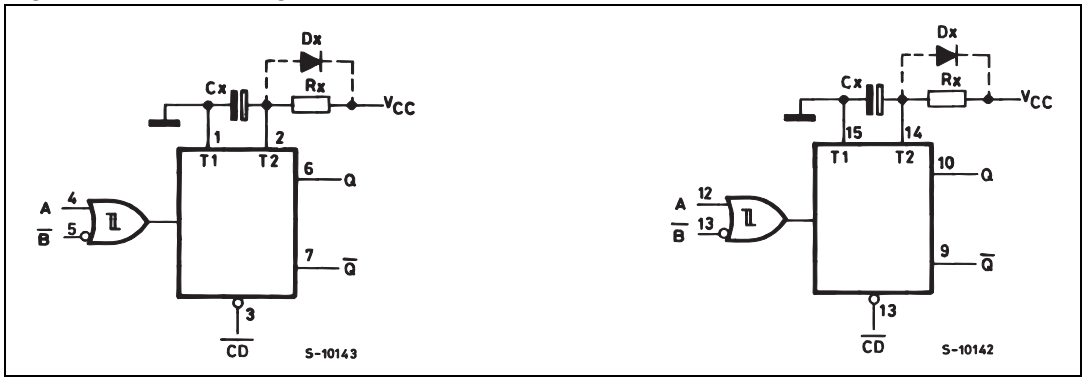


Figure 5. Block diagram



1. Cx, Rx, Dx are external components.
2. Dx is a clamping diode.
   The external capacitor is charged to V_{CC} in the standby state, i.e. no trigger. When the supply voltage is turned off Cx is discharged mainly through an internal parasitic diode (see figures). If Cx is sufficiently large and V_{CC} decreases rapidly, there will be some possibility of damaging the IC with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decreases slowly, the surge current is automatically limited and damage to the IC is avoided. The maximum forward current of the parasitic diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows: $t_f \geq (V_{CC} - 0.7) \times Cx/20$ mA.
   In cases where t_f is too short an external clamping diode is required to protect the IC from the surge current.

2 Functional description

Standby state

The external capacitor Cx, is fully charged to V_{CC} in the standby state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned-off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

Trigger operation

Triggering occurs when:

- A is low and B has a falling edge
- B is high and A has a rising edge

After the multivibrator has been retriggered, the comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node Rx/Cx external falls.

When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn resets the flip-flop and Qn is turned off.

At this point C1 stops functioning but C2 continues to operate.

The voltage at R/C external begins to rise with a time constant set by the external components Rx and Cx.

Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH} . At this point C2 output goes low and G goes low. C2 stops operating. That means that after triggering when the voltage R/C external returns to V_{REFH} the multivibrator has returned to its monostable state. In the case where Rx · Cx are large enough and the discharge time of the capacitor and the delay time in the IC can be ignored, the width of the output pulse $t_{w(out)}$ is as follows:

$$t_{W(OUT)} = 0.72Cx \bullet Rx$$

Re-triggered operation

When a second triggered pulse follows the first, its effect will depend on the state of the multivibrator. If the capacitor Cx is being charged, the voltage level of Rx/Cx external falls to V_{REFL} again and Q remains high i.e. the retrigger pulse arrives in a time shorter than the period Rx · Cx seconds, the capacitor charging time constant. If the second trigger pulse is very close to the initial trigger pulse it is ineffective; i.e. the second trigger must arrive in the capacitor discharge cycle to be ineffective; hence the minimum time for a second trigger to be effective, t_{rr} (min.) depends on V_{CC} and Cx.

Reset operation

CD is normally high. If CD is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset. Also transistor Op is turned on and Cx is charged quickly to V_{CC}. Then, if CD input goes low the IC becomes waiting state both in operating and non operating state.

3 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7	V
V_I	DC input voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC input diode current	±20	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±25	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±50	mA
P_D	Power dissipation	500(1)	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	300	°C

1. 500 mW at 65 °C; derate to 300 mW by 10 mW/ °C from 65° C to 85° C

3.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		2 to 6	V
V_I	Input voltage		0 to V_{CC}	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-55 to 125	°C
t_r, t_f	Input rise and fall time ($\overline{CD}$ only)	V_{CC} = 2.0 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	ns
		V_{CC} = 6.0 V	0 to 400	ns
Cx	External capacitor		No limitation	pF
Rx	External resistor	$V_{CC} \leq$3.0 V	5 K to 1 M	Ω
		$V_{CC} \geq$ 3.0 V	1 K to 1 M	

4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High level input voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low level input voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High level output voltage	2.0	I_O = -20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O = -20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O = -20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O = -4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O = -5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low level output voltage	2.0	I_O = 20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O = 20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O = 20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O = 4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O = 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input leakage current	6.0	V_I = V_{CC} or GND			±0.1		±1		±1	µA
I_I	Input leakage current	6.0	V_I = V_{CC} or GND Rext/Cext			±0.1		±1		±1	µA
I_{CC}	Quiescent supply current	6.0	V_I = V_{CC} or GND			4		40		80	µA
I_{CC}	Quiescent supply current	2.0	V_I = V_{CC} or GND Pin 2 or 14 V_{IN} = V_{CC}/2		40	120		160		200	µA
		4.5			0.2	0.3		0.4		0.6	mA
		6.0			0.3	0.6		0.8		1.0	mA

Table 7. AC electrical characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test condition			Value							Unit
		V_{CC} (V)			T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min	Typ	Max	Min	Max	Min	Max	
t_{TLH} t_{THL}	Output transition time	2.0				30	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_{PLH} t_{PHL}	Propagation delay time (A, $\overline{B}$ - Q, $\overline{Q}$)	2.0				120	250		315		375	ns
		4.5				30	50		63		75	
		6.0				25	43		54		64	
t_{PLH} t_{PHL}	Propagation delay time ($\overline{CD}$ - Q, $\overline{Q}$)	2.0				100	195		245		295	ns
		4.5				25	39		49		59	
		6.0				20	33		42		50	
t_{WOUT}	Output pulse width	2.0	Cx=0	Rx = 5 KΩ		540	1200		1500		1800	ns
		4.5		Rx = 1 KΩ		180	250		320		375	
		6.0		Rx = 1 KΩ		150	200		260		320	
		2.0	Cx = 0.01 µF Rx = 10 KΩ		70	83	96	70	96	70	96	µs
		4.5			69	77	85	69	85	69	85	
		6.0			69	77	85	69	85	69	85	
		2.0	Cx = 0.1 µF Rx = 10 KΩ		0.67	0.75	0.83	0.67	0.83	0.67	0.9	ms
		4.5			0.67	0.73	0.77	0.67	0.77	0.67	0.8	
		6.0			0.67	0.73	0.77	0.67	0.77	0.67	0.8	
Δt_{WOUT}	Output pulse width error between circuits in same package					±1						%
$t_{W(H)}$ $t_{W(L)}$	Minimum pulse width (A,$\overline{B}$)	2.0				30	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
$t_{W(L)}$	Minimum pulse width ($\overline{CD}$)	2.0				30	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_{REM}	Minimum clear removal time	2.0				0	15		15		20	ns
		4.5				0	5		5		7	
		6.0				0	5		5			

Table 7. AC electrical characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns) (continued)

Symbol	Parameter	Test condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min	Max	
t_{rr}	Minimum retrigger time	2.0	Cx = 0.1 µF Rx = 1KΩ		380						ns
		4.5			92						
		6.0			72						
		2.0	Cx = 0.01µF Rx = 1KΩ		6						µs
		4.5			1.4						
		6.0			1.2						

Table 8. Capacitive characteristics

Symbol	Parameter	Test condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min	Max	
C_{IN}	Input capacitance	5.0			5	10		10		10	pF
C_{PD}	Power dissipation capacitance (1)	5.0			70						pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$' Duty/100 + Ic/2(per monostable) (I_{cc}' : Active Supply current) (Duty : %)

Figure 6. Test circuit

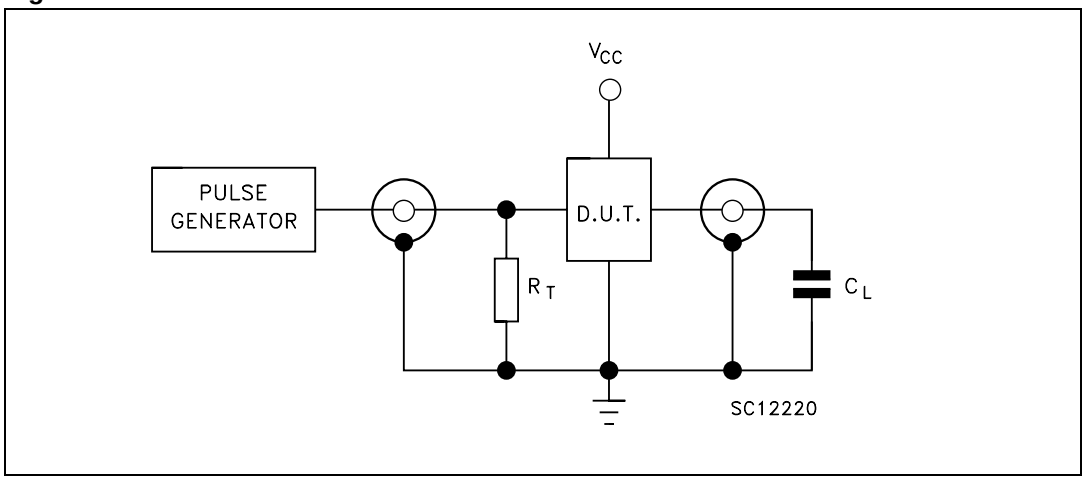
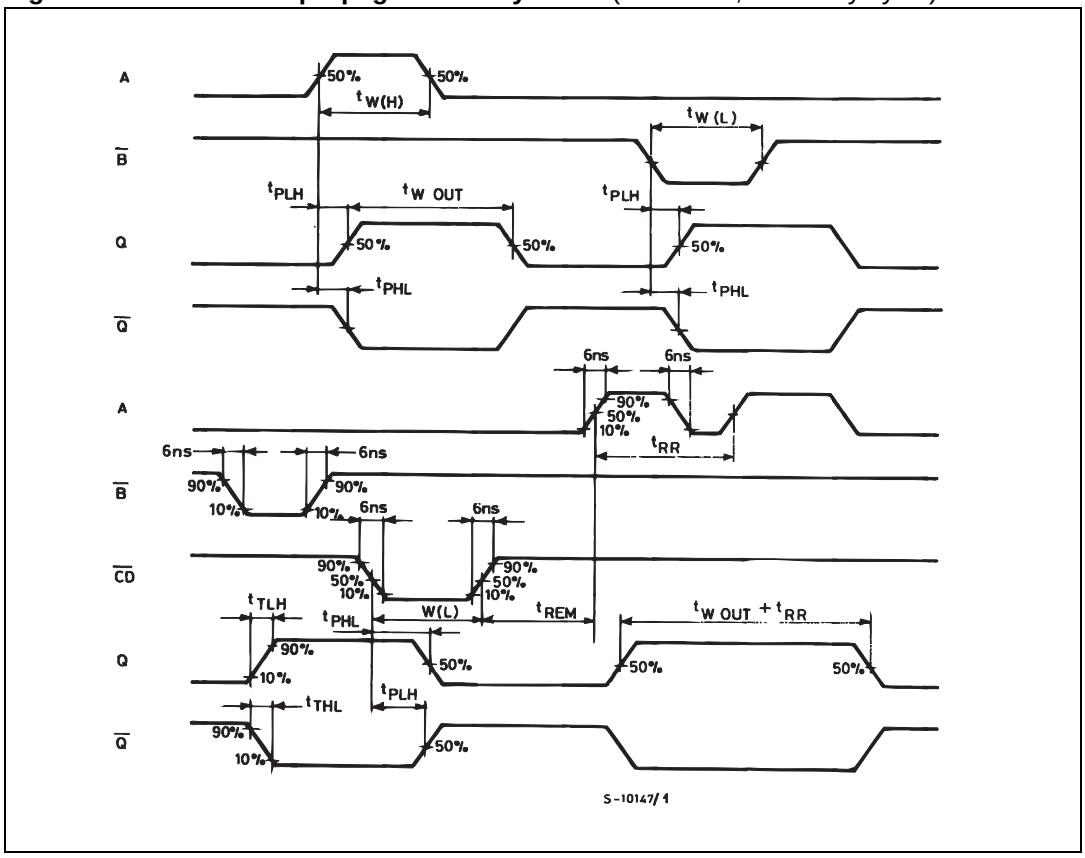


Figure 7. Waveform: propagation delay times (f = 1 MHz; 50% duty cycle)

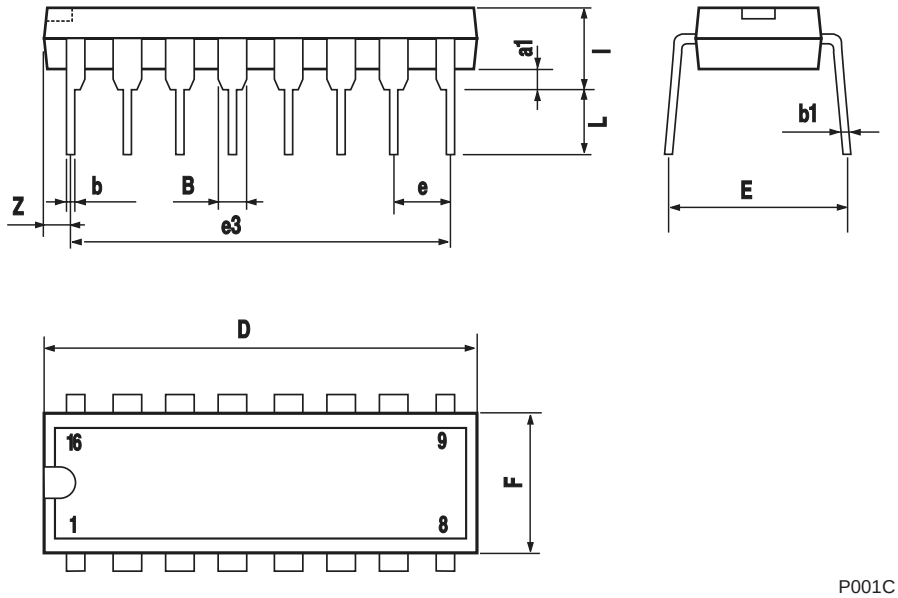


5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Plastic DIP-16 (0.25) MECHANICAL DATA

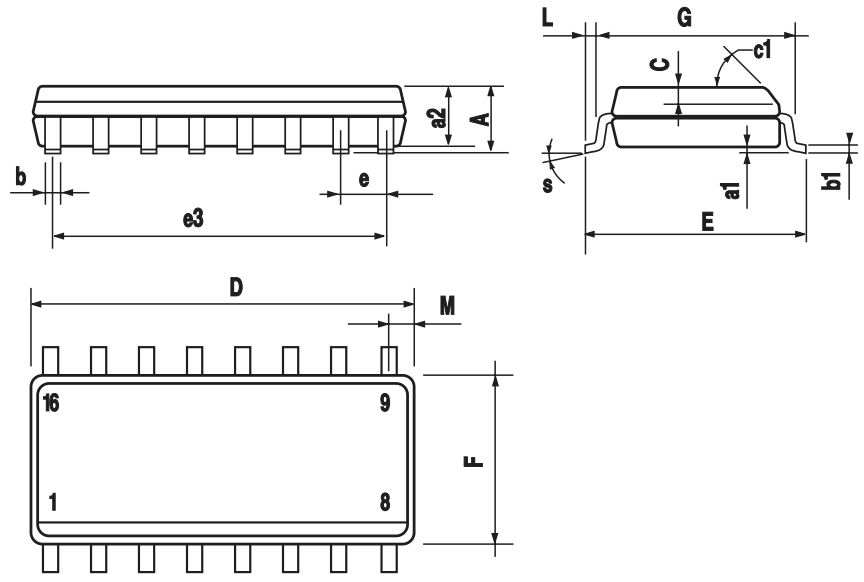
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

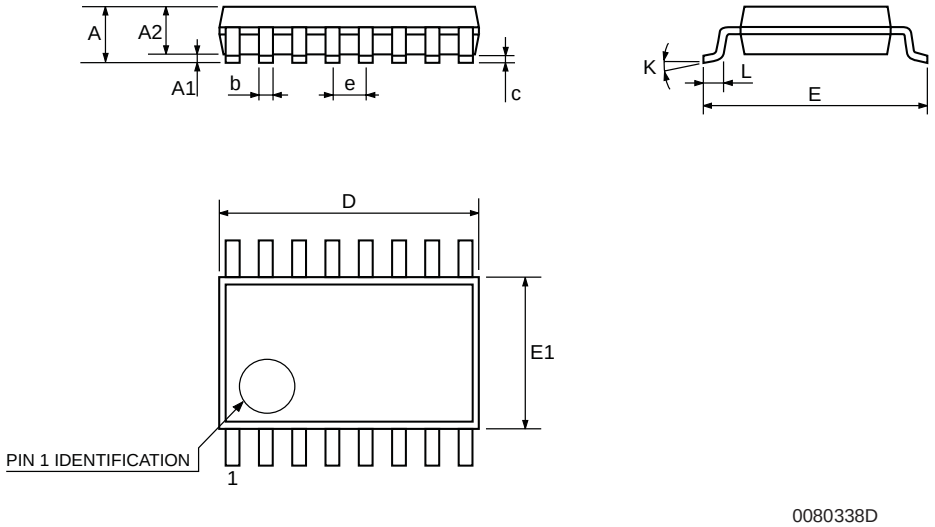
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



0016020D

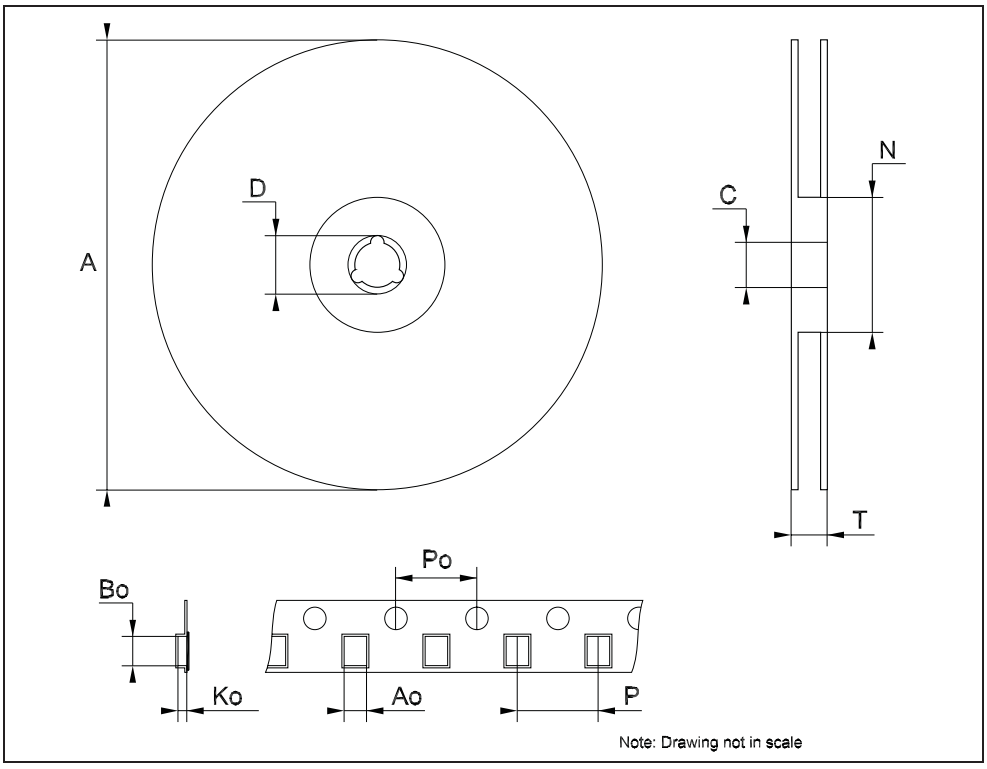
TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

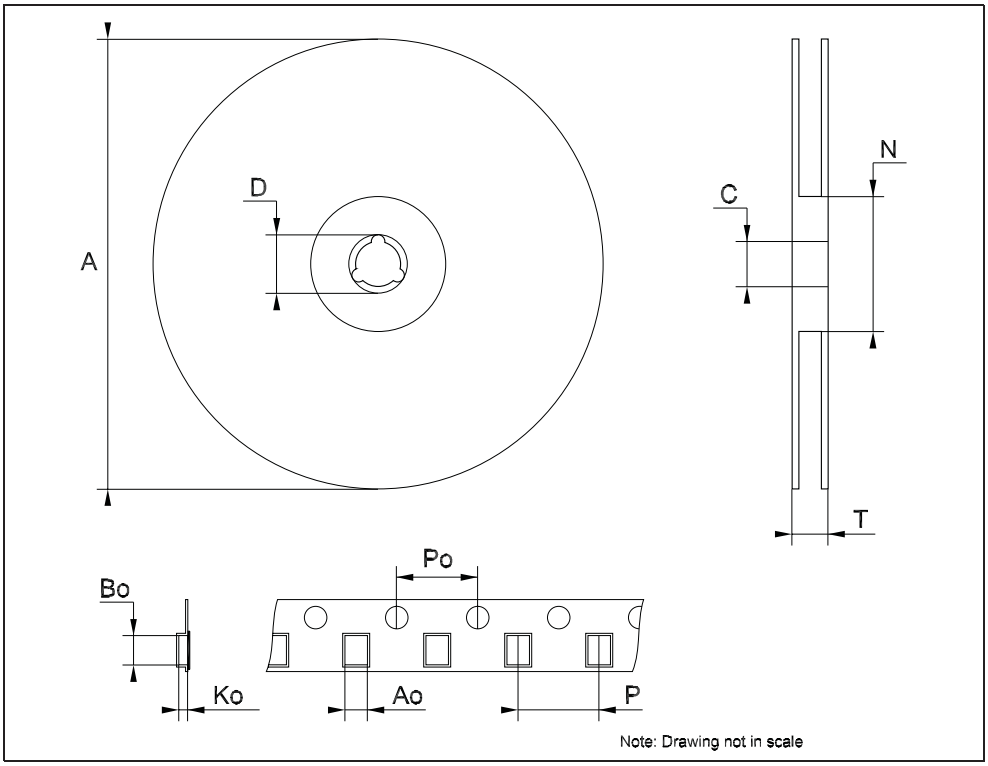


Tape & Reel SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.45		6.65	0.254		0.262
Bo	10.3		10.5	0.406		0.414
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Tape & Reel TSSOP16 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
01-Jul-2001	1	Initial release.
26-May-2008	2	Document converted and restructured to new template. Removed: M74HC4538M1R order code. Minor text changes. Added: SO-16 and TSSOP16 tape and reel specifications.

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