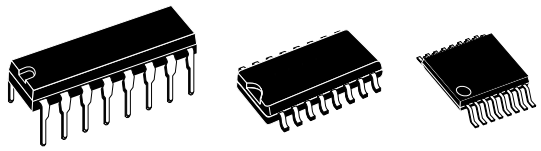
M74HC4060

14-stage binary counter/oscillator

Datasheet - production data



PDIP-16 SO-16 TSSOP-16

Features

- High speed:
  f_{max} = 65 MHz (typ.) at V_{CC} = 6 V
- Low power dissipation:
  I_{CC} = 4 A (max.) at T_A = 25 °C
- High noise immunity:
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min.)
- Symmetrical output impedance:
  $|I_{OH}| = I_{OL}$ = 4 mA (min.)
- Balanced propagation delays: $T_{PLH} \cong T_{PHL}$
- Wide operating voltage range:
  V_{CC} (opr.) = 2 V to 6 V
- Pin and function compatible with 74 series 4060

Applications

- Automotive
- Industrial
- Computer
- Consumer

Description

The M74HC4060 device is a high speed CMOS 14-stage binary counter/oscillator fabricated with silicon gate C^2MOS technology.

The oscillator configuration allows design of either RC or crystal oscillator circuits. A high level on the CLEAR accomplishes the reset function, i.e. all counter outputs are made low and the oscillator is disabled.

A negative transition on the clock input increments the counter. Ten kinds of divided output are provided; 4 to 10 and 12 to 14 stage inclusive. The maximum division available at Q12 is 1/16384 of the oscillator frequency.

The $\overline{\varnothing}$I input and the CLEAR input are equipped with protection circuits against static discharge and transient excess voltage.

Table 1. Device summary

Ordering code	Temperature range	Package	Marking
M74HC4060B1R	-55 °C to +125 °C	PDIP-16	M74HC4060B1
M74HC4060RM13TR	-55 °C to +125 °C	SO-16	74HC4060
M74HC4060YRM13TR(1)	-40 °C to +125 °C	SO-16 (automotive version)	74HC4060Y
M74HC4060TTR	-55 °C to +125 °C	TSSOP-16	HC4060
M74HC4060YTTR(1)	-40 °C to +125 °C	TSSOP-16 (automotive version)	HC4060Y

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

Contents

1 Pin description

Figure 1. Pin connection and IEC logic symbols

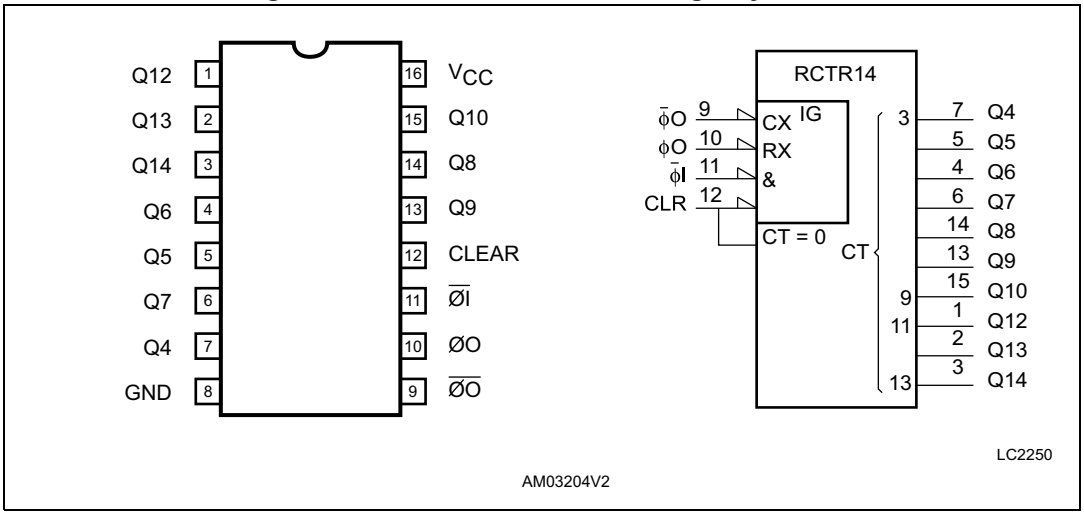


Figure 2. Input and output equivalent circuit

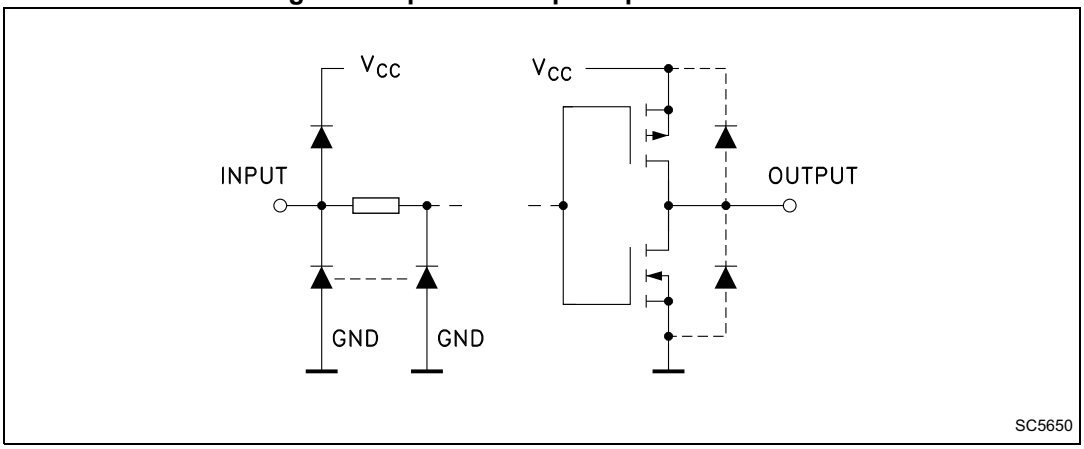
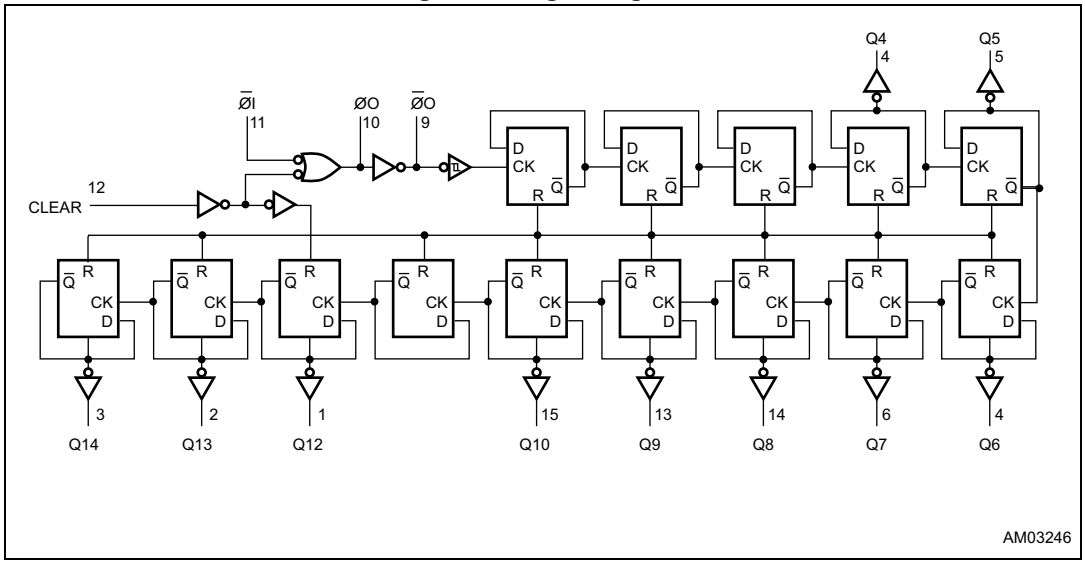


Table 2. Pin description

Pin no	Symbol	Name and function
1, 2, 3	Q12 to Q14	Counter outputs
7, 5, 4, 6, 14, 13, 15	Q4 to Q10	Counter outputs
9	$\overline{\varnothing}\overline{O}$	External capacitor connection
10	$\varnothing O$	External resistor connection
11	$\overline{\varnothing}\overline{I}$	Clock input / oscillator pin
12	CLEAR	Master reset
8	GND	Ground (0 V)
16	V_{CC}	Positive supply voltage

2 Functional description

Figure 3. Logic diagram



1. This logic diagram has not be used to estimate propagation delays.

Table 3. Truth table

$\overline{\varnothing I}$	CLEAR	Function
X(1)	H	Counter is reset to zero state ∅O output goes to high level $\overline{\varnothing O}$ output goes to low level
↓	L	Count up one step
↑	L	No change

1. X: don't care.

3 Maximum ratings

Table 4. Absolute maximum ratings(1)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7	V
V_I	DC Input voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC input diode current	20	mA
I_{OK}	DC output diode current	20	mA
I_O	DC output current	25	mA
I_{CC} or I_{GND}	DC VCC or ground current	50	mA
P_D	Power dissipation	500(2)	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec.)	300	°C

1. Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
2. 500 mW at 65 °C; derate to 300 mW by 10 mW/ C from 65 °C to 85 °C.

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_C	Supply voltage		2 to 6	V
V_I	Input voltage		0 to V_{CC}	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-55 to 125	°C
t_r, t_f	Input rise and fall time	V_{CC} = 2.0 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	ns
		V_{CC} = 6.0 V	0 to 400	ns

4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85 °C		-55 to 125 °C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High level input voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low level input voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High level output voltage (Q output)	2.0	I_O = -20 A	1.9	2.0		1.9		1.9		V
		4.5	I_O = -20 A	4.4	4.5		4.4		4.4		
		6.0	I_O = -20 A	5.9	6.0		5.9		5.9		
		4.5	I_O = -4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O = -5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low level output voltage (Q output)	2.0	I_O = 20 A		0.0	0.1		0.1		0.1	V
		4.5	I_O = 20 A		0.0	0.1		0.1		0.1	
		6.0	I_O = 20 A		0.0	0.1		0.1		0.1	
		4.5	I_O = 4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O = 5.2 mA		0.18	0.26		0.33		0.40	
V_{OH}	High level output voltage (∅O, $\overline{\varnothing O}$ output)	2.0	I_O =-20 A	1.8	2.0		1.8		1.8	2.0	V
		4.5	I_O = -20 A	4.4	4.5		4.0		4.0		
		6.0	I_O = -20 A	5.5	5.9		5.5		5.5		
V_{OL}	Low level output voltage (∅O, $\overline{\varnothing O}$ output)	2.0	I_O = -20 A		0.0	0.2		0.2		0.2	V
		4.5	I_O = -20 A		0.0	0.5		0.5		0.5	
		6.0	I_O = -20 A		0.1	0.5		0.5		0.5	
I_I	Input leakage current	6.0	V_I = V_{CC} or GND			0.1		±1		±1	µA
I_{CC}	Quiescent supply current	6.0	V_I = V_{CC} or GND			4		40		80	µA

Table 7. AC electrical characteristics (C_L = 50 pF, input $t_r = t_f$ = 6 ns)

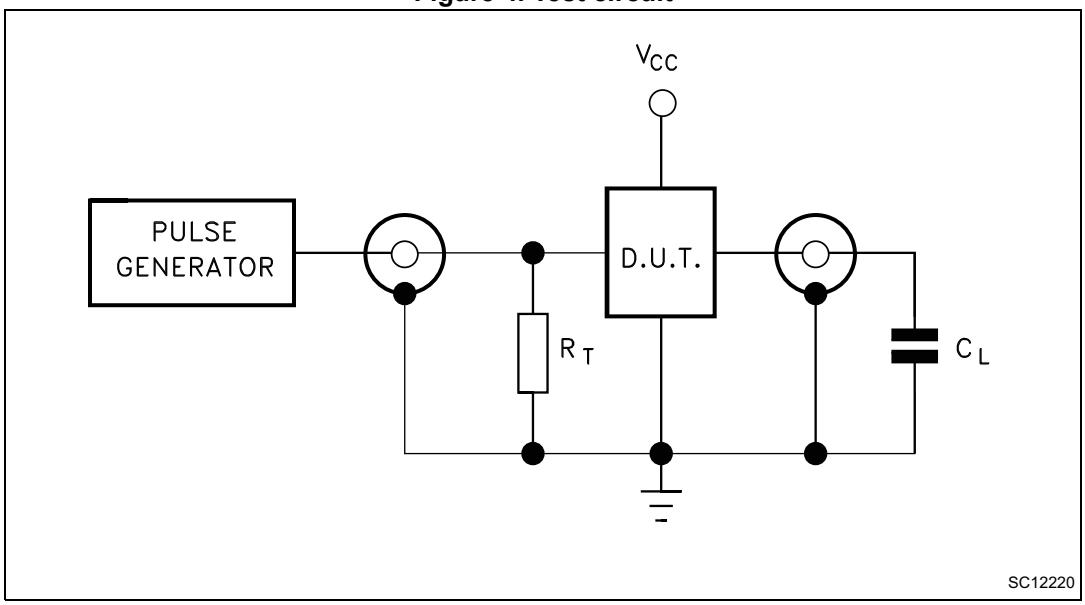
Symbol	Parameter	Test condition	Value							Unit
		V_{CC} (V)	T_A = 25 °C			-40 to 85 °C		-55 to 125 °C		
			Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output transition time	2.0		30	75		95		110	ns
		4.5		8	15		19		22	
		6.0		7	13		16		19	
t_{PLH} t_{PHL}	Propagation delay time ($\overline{\varnothing}$I - $\overline{Q4}$)	2.0		170	300		375		450	ns
		4.5		41	60		75		90	
		6.0		30	51		64		76	
t_{PD}	Propagation delay time difference (Qn - Qn+1)	2.0		32	75		95		110	ns
		4.5		7	15		19		22	
		6.0		5	13		16		19	
t_{PHL}	Propagation delay time (CLEAR - Qn)	2.0		85	195		245		295	ns
		4.5		23	39		49		59	
		6.0		17	33		42		50	
f_{MAX}	Maximum clock frequency	2.0	6	12		5		4		MHz
		4.5	30	50		24		20		
		6.0	35	65		28		24		
$t_{W(H)}$, $t_{W(L)}$	Minimum pulse width ($\overline{\varnothing}$I)	2.0		30	75		95		110	ns
		4.5		8	15		19		22	
		6.0		7	13		16		19	
$t_{W(H)}$	Minimum pulse width (CLEAR)	2.0		30	75		95		110	ns
		4.5		8	15		19		22	
		6.0		7	13		16		19	
t_{REM}	Minimum removal time	2.0		40	100		125		150	ns
		4.5		10	20		25		30	
		6.0		9	17		21		26	

Table 8. Capacitive characteristics

Symbol	Parameter	Test condition	Value							Unit
		V_{CC} (V)	T_A = 25 °C			-40 to 85 °C		-55 to 125 °C		
			Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input capacitance	5.0	5	10		10		10		pF
C_{PD}	Power dissipation capacitance(1)	5.0		27						pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to *Figure 4: Test circuit*). Average operating current can be obtained by the following equation. $I_{CC}(opr.) = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$.

Figure 4. Test circuit



1. C_L = 50 pF or equivalent (includes jig and probe capacitance)
$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω).

5 Waveforms

Figure 5. Waveform 1: propagation delay times, minimum pulse width ($\overline{\varnothing I}$) (f = 1 MHz; 50% duty cycle)

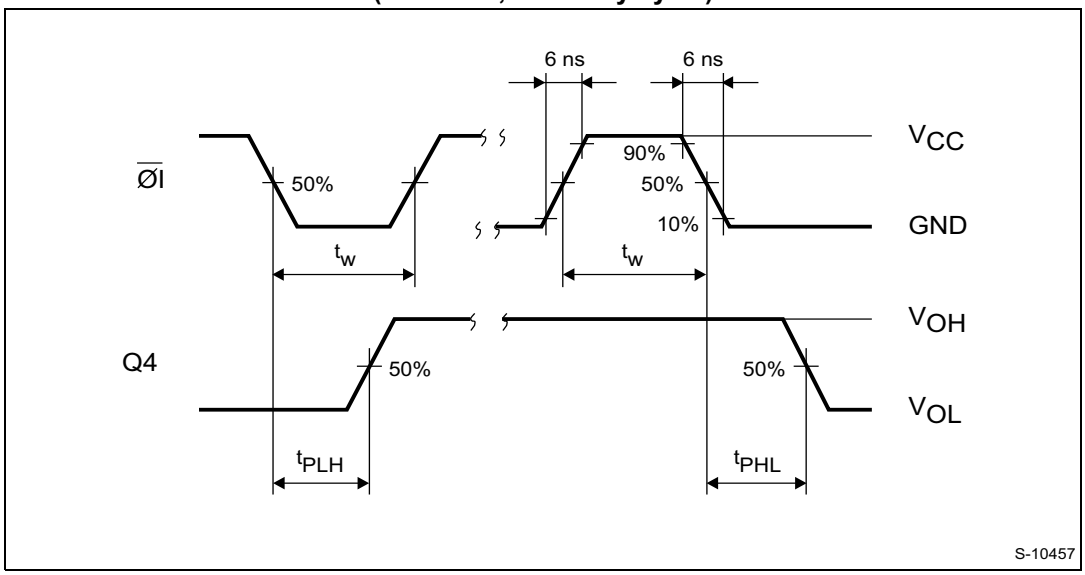


Figure 6. Waveform 2: propagation delay times, minimum pulse width (CLEAR) (f = 1 MHz; 50% duty cycle)

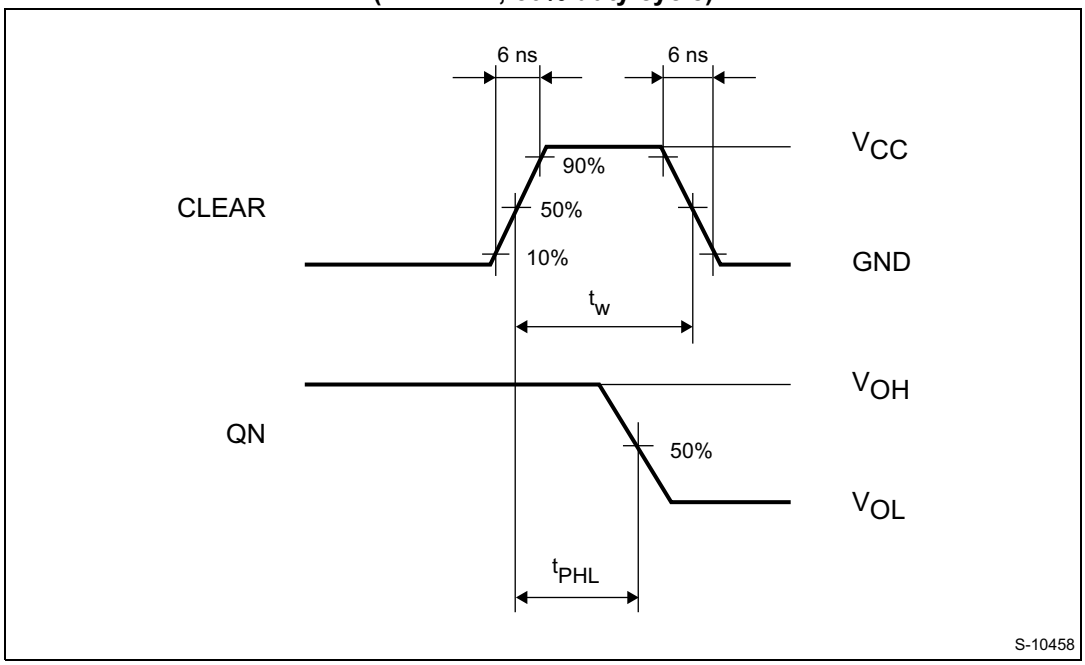


Figure 7. Waveform 3:propagation delay times (f = 1 MHz; 50% duty cycle)

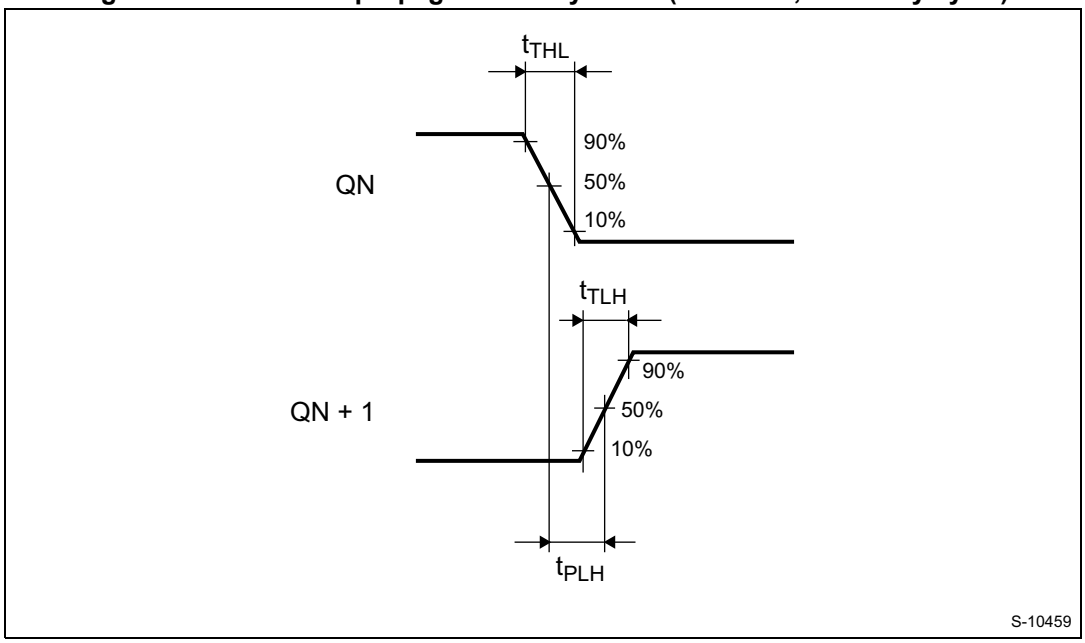


Figure 8. Waveform 4: propagation delay times (f = 1 MHz; 50% duty cycle)

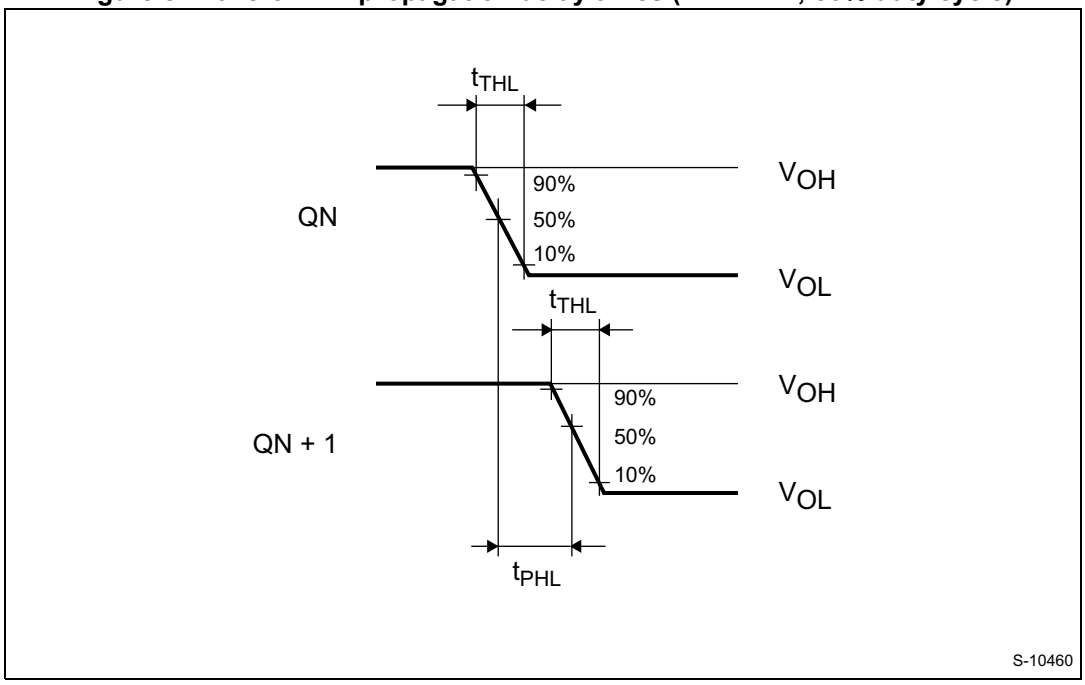
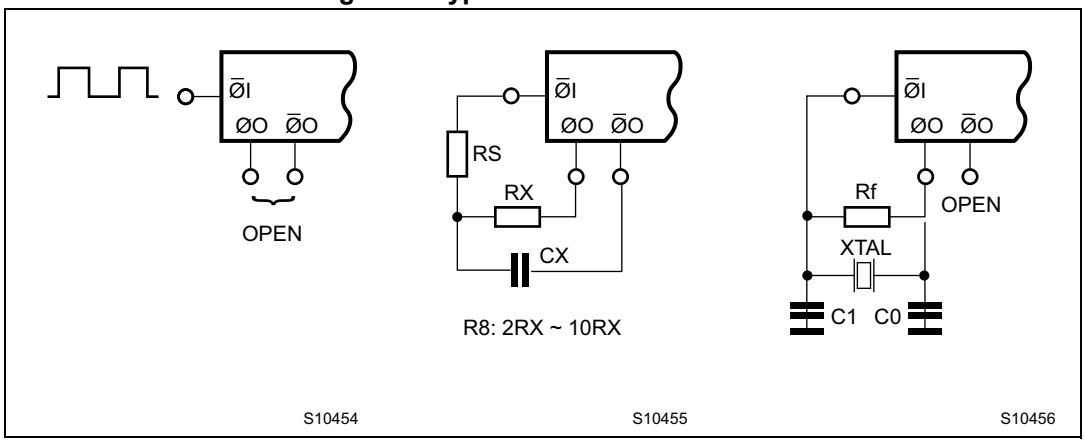


Figure 9. Typical clock drive circuits



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 10. Plastic DIP-16 package outline

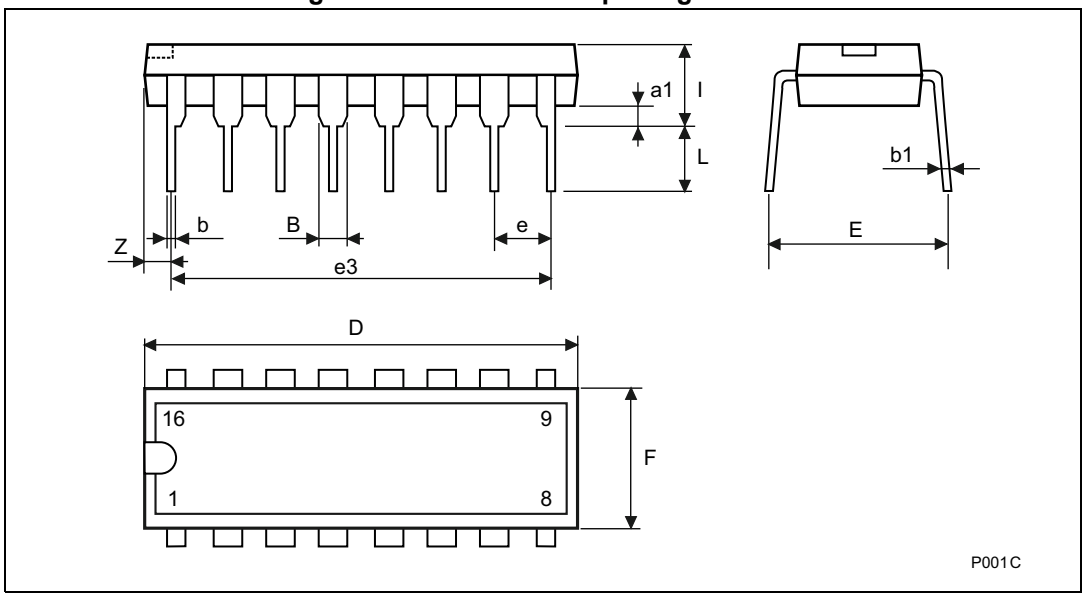


Table 9. Plastic DIP-16 (0.25) package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

Figure 11. SO-16 package outline

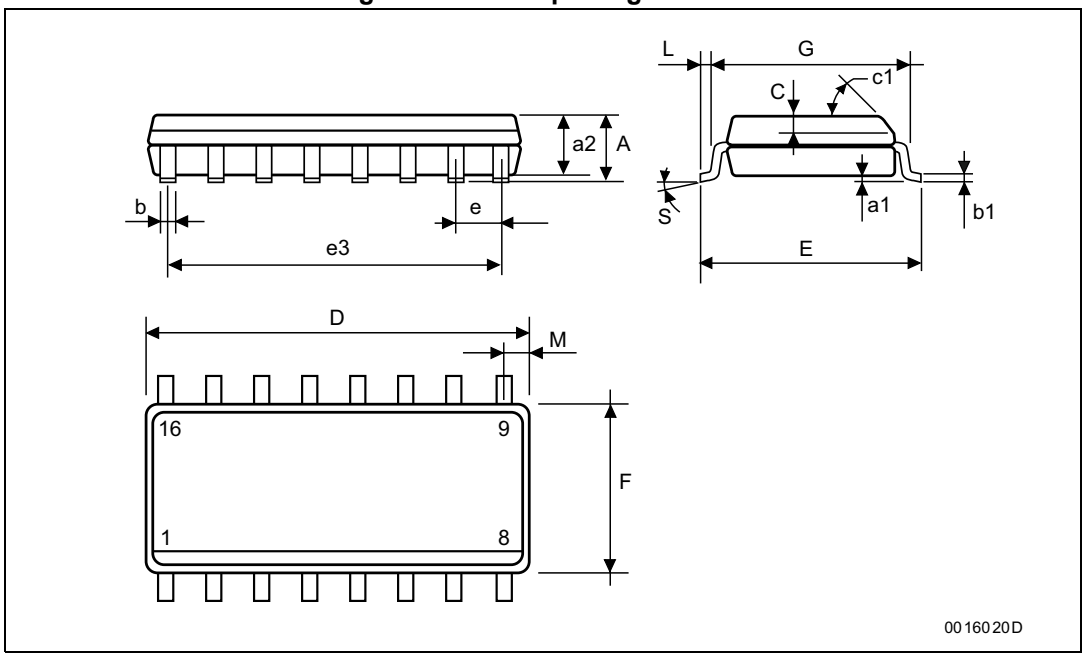


Table 10. SO-16 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					

Figure 12. TSSOP-16 package outline

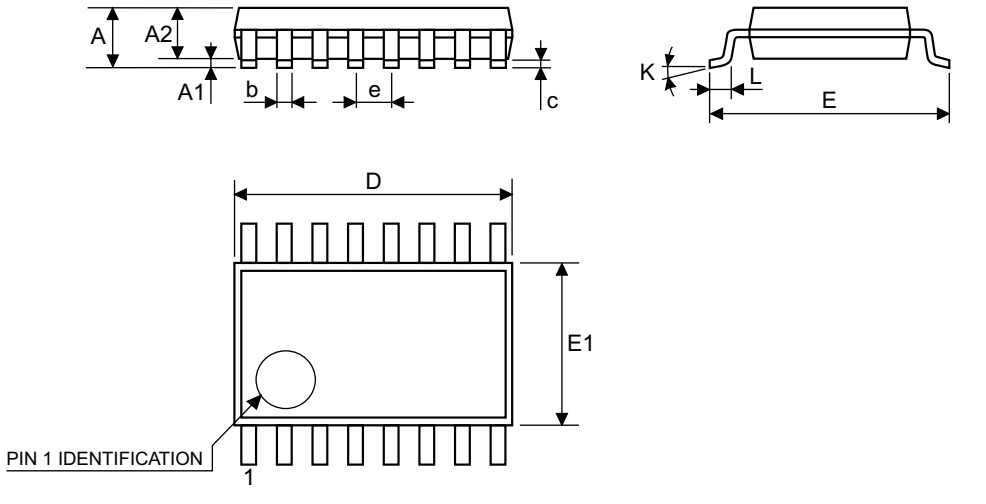


Table 11. TSSOP-16 mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

7 Revision history

Table 12. Document revision history

Date	Revision	Changes
1-Feb-2008	1	Initial release.
15-May-2013	2	Added *Applications* on page 1. Corrected *Description* (replaced “The maximum division available at Q12 is 1/16384 f oscillator.” by “The maximum division available at Q12 is 1/16384 of the oscillator frequency.”). Updated *Table 1* (added order codes, temperature range, updated package, added marking). Moved *Figure 1* to page 3. Redrawn *Figure 1*, *Figure 3*, *Figure 5* to *Figure 9*. Added *Contents*. Added titles to *Section 1: Pin description* to *Section 7: Revision history*. Added numbers to *Table 1* to *Table 12* and *Figure 1* to *Figure 12*. Updated *Section 6: Package information* (added ECOPACK text, reversed order of *Figure 10* to *Figure 12* and *Table 10* to *Table 11*). Minor corrections throughout document.

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