Complete SO-8, 12-Bit, 200ksps ADC with Shutdown

FEATURES

- **Complete 12-Bit ADC with Reference in SO-8**
- **Single Supply 3V Operation**
- **Sample Rate: 200ksps**
- Power Dissipation: 15mW (Typ)
- 68dB S/(N + D) and – 72dB THD at 50kHz
- No Missing Codes Over Temperature
- Nap Mode with Instant Wake-Up: 1.5mW
- Sleep Mode: 19.5µW
- Shutdown Mode: 13.5µW
- High Impedance Analog Input
- Input Range (0.5mV/LSB): 0V to 2.048V
- Internal Reference Can Be Overdriven Externally
- 3-Wire Interface to DSPs and Processors (SPI and MICROWIRE™ Compatible)

APPLICATIONS

- Low Power and Battery-Operated Systems
- Handheld or Portable Instruments
- High Speed Data Acquisition
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Telecommunication
- Digital Radio
- Spectrum Analysis

DESCRIPTION

The LTC®1401 is a complete 200ksps, 12-bit A/D converter that converts 0V to 2.048V unipolar input and draws only 15mW from a single 3V supply. This easy-to-use device comes complete with a 315ns sample-and-hold and a precision reference. Maximum DC specifications include ±1LSB INL, ±1LSB DNL and 45ppm/°C full-scale drift over temperature.

The LTC1401 has three power saving modes: Nap and Sleep, through the serial interface and Shutdown by setting the $\overline{SHDN}$ pin to zero. In Nap mode, it consumes only 1.5mW of power and can wake up and convert immediately. In Sleep (Shutdown) mode, it consumes 19.5µW (13.5µW) of power typically. Upon power-up from Sleep or Shutdown mode, a reference ready (REFRDY) signal is available in the serial word to indicate that the reference has settled and the chip is ready to convert.

The 3-wire serial port allows compact and efficient data transfer to a wide range of microprocessors, microcontrollers and DSPs.

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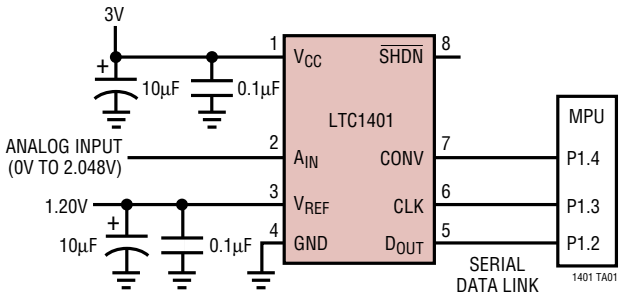
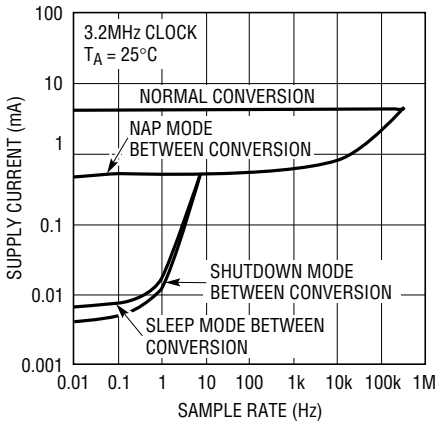
MICROWIRE is a trademark of National Semiconductor Corporation.

TYPICAL APPLICATION

Single 3V Supply, 200kHz, 12-Bit Sampling A/D Converter



Power Consumption vs Sample Rate

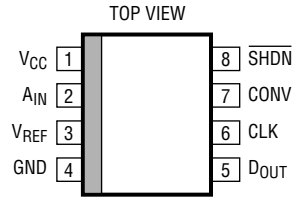


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) 7V
Analog Input Voltage (Note 3) ..... –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage (Note 4) .....–0.3V to 12V
Digital Output Voltage ..... –0.3V to (V_{CC} + 0.3V)
Power Dissipation 300mW
Operating Ambient Temperature Range
LTC1401C..... 0°C to 70°C
LTC1401I..... –40°C to 85°C
Operating Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1401CS8 LTC1401IS8
S8 PART MARKING
1401 1401I

Consult factory for PDIP packages and Military grade parts.

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage			2.7	3.0	3.6	V
I_{CC}	Supply Current	f_{SAMPLE} = 200ksps	●		5	10	mA
		Nap Mode	●		0.5	1.0	mA
		Sleep Mode	●		6.5	15	µA
		Shutdown Mode	●		4.5	10	µA
P_D	Power Dissipation	f_{SAMPLE} = 200ksps	●		15	30	mW
		Nap Mode	●		1.5	3.0	mW
		Sleep Mode	●		19.5	45	µW
		Shutdown Mode	●		13.5	30	µW

ANALOG INPUT (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range		●		0 to 2.048		V
I_{IN}	Analog Input Leakage Current	During Conversions (Hold Mode)	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode)			45		pF
		During Conversions (Hold Mode)			5		pF

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		1.180	1.200	1.220	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±10	±45	ppm/°C
V_{REF} Line Regulation	2.7V ≤ V_{CC} ≤ 3.6V			0.01		LSB/V
V_{REF} Load Regulation	0 ≤ $\lvert I_{OUT} \rvert$ ≤ 1mA			2		LSB/mA
V_{REF} Wake-Up Time from Sleep or Shutdown Mode	C_{VREF} = 10µF			3		ms

CONVERTER CHARACTERISTICS With internal reference (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 7)	●			±1	LSB
Differential Linearity Error		●			±1	LSB
Offset Error		 ●			±6 ±8	LSB LSB
Full-Scale Error					±15	LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0	●		±10	±45	ppm/°C

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	50kHz Input Signal 100kHz Input Signal	●	65	68 65		dB dB
THD	Total Harmonic Distortion Up to 5th Harmonic	50kHz Input Signal 100kHz Input Signal	●		–72 –66	–65	dB dB
	Peak Harmonic or Spurious Noise	50kHz Input Signal 100kHz Input Signal	●		–74 –67	–65	dB dB
IMD	Intermodulation Distortion	f_{IN1} = 49.853kHz, f_{IN2} = 53.076kHz			–69		dB
	Full Power Bandwidth				2		MHz
	Full Linear Bandwidth (S/(N + D) ≥ 68dB)				50		kHz

DIGITAL INPUTS AND OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{CC}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{CC} = 2.7V, I_O = –10µA V_{CC} = 2.7V, I_O = –200µA	● ●	2.40 2.25	2.64 2.50		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 2.7V, I_O = 400µA	●		0.13	0.4	V
I_{OZ}	Hi-Z Output Leakage D_{OUT}	V_{OUT} = 0V to V_{CC}	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D_{OUT}				15		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0			–5		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			10		mA

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	200			kHz
t_{CONV}	Conversion Time	f_{CLK} = 3.2MHz	●			4.1	µs
t_{ACQ}	Acquisition Time				315		ns
f_{CLK}	CLK Frequency		●	0.1		3.2	MHz
t_{CLK}	CLK Pulse Width	(Note 6)	●	60			ns
$t_{WK(NAP)}$	Time to Wake Up from Nap Mode				350		ns
t_1	CLK Pulse Width to Return to Active Mode		●	60			ns
t_2	CONV↑ to CLK↑ Setup Time		●	100			ns
t_3	CONV↑ After Leading CLK↑		●	0			ns
t_4	CONV Pulse Width	(Note 8)	●	50			ns
t_5	Time from CLK↑ to Sample Mode				80		ns
t_6	Aperture Delay of Sample-and-Hold	Jitter < 50ps			45		ns
t_7	Minimum Delay Between Conversion	(Note 6)	●		350	550	ns
t_8	Delay Time, CLK↑ to D_{OUT} Valid	C_{LOAD} = 20pF	●		60	120	ns
t_9	Delay Time, CLK↑ to D_{OUT} Hi-Z	C_{LOAD} = 20pF	●		60	120	ns
t_{10}	Time from Previous Data Remains Valid After CLK↑	C_{LOAD} = 20pF	●	15	50		ns

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals apply to T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: When these pin voltages are taken below GND or above V_{CC}, they will be clamped by internal diodes. This product can handle input currents greater than 40mA without latch-up if the pin is driven below GND or above V_{CC}.

Note 4: When these pin voltages are taken below GND, they will be clamped by internal diodes. This product can handle input currents greater than 40mA without latch-up if the pin is driven below GND. These pins are not clamped to V_{CC}.

Note 5: V_{CC} = 3V, f_{SAMPLE} = 200kHz, $t_r = t_f$ = 5ns unless otherwise specified.

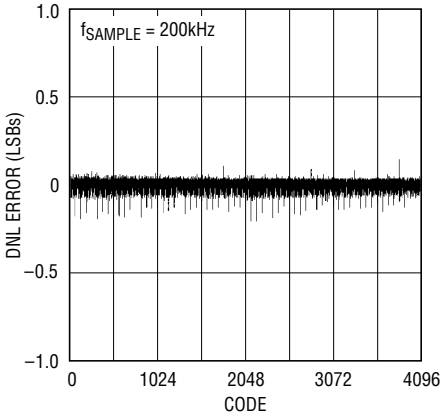
Note 6: Guaranteed by design, not subject to test.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: The rising edge of CONV starts a conversion. If CONV returns low at a bit decision point during the conversion, it can create small errors. For best performance, ensure that CONV returns low either within 120ns after the conversion starts (i.e., before the first bit decision) or after the 14 clock cycles. (Figure 13 Timing Diagram).

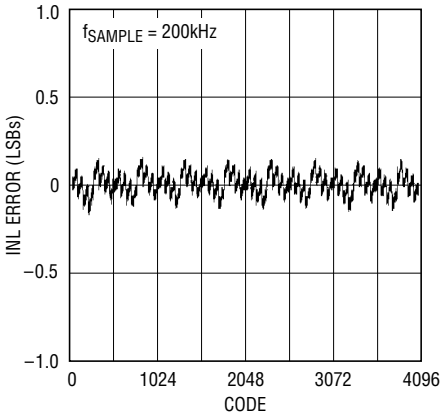
TYPICAL PERFORMANCE CHARACTERISTICS

Differential Nonlinearity vs Output Code



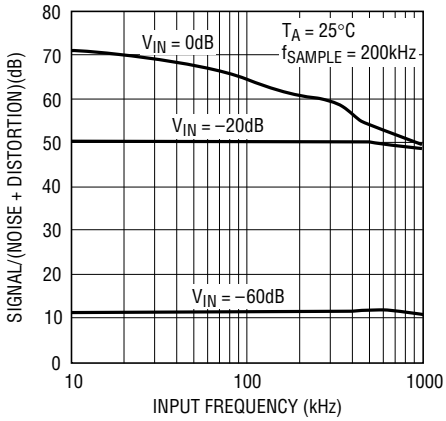
LTC1401 • TPC01

Integral Nonlinearity vs Output Code



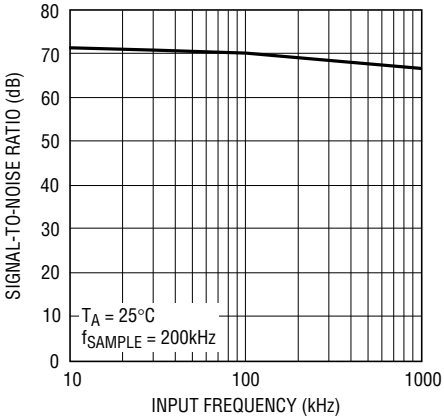
LTC1401 • TPC02

S/(N + D) vs Input Frequency and Amplitude



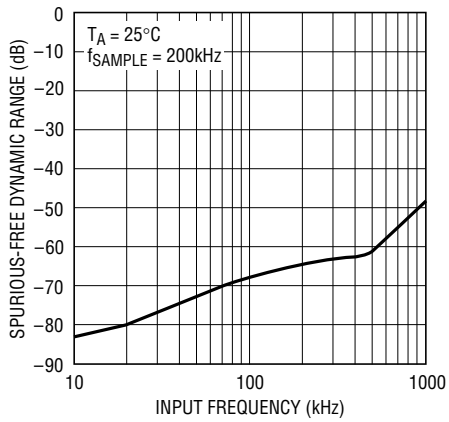
LTC1401 • TPC03

Signal-to-Noise Ratio (Without Harmonics) vs Input Frequency



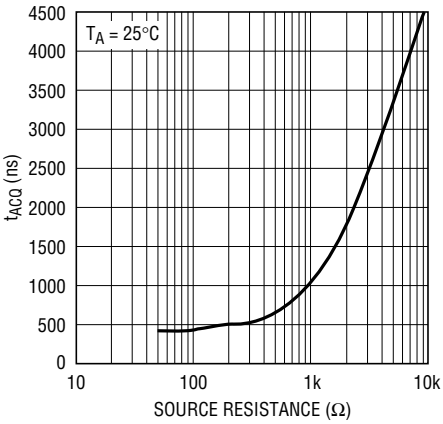
LTC1401 • TPC04

Peak Harmonic or Spurious Noise vs Input Frequency



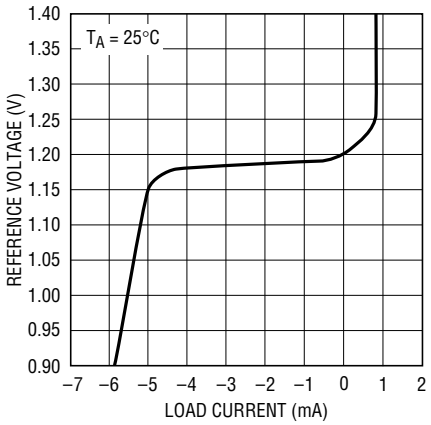
LTC1401 • TPC05

Acquisition Time vs Source Impedance



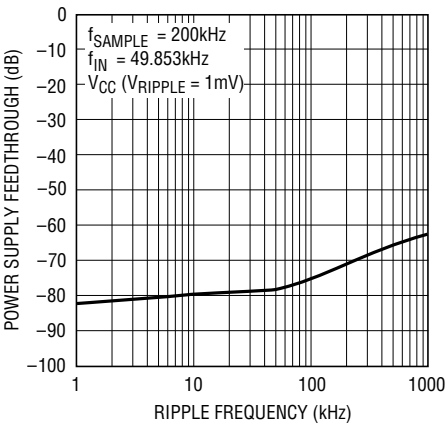
LTC1401 • TPC06

Reference Voltage vs Load Current



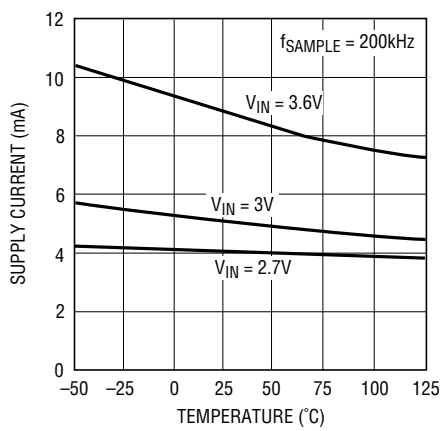
LTC1401 • TPC07

Power Supply Feedthrough vs Ripple Frequency



LTC1401 • TPC08

Supply Current vs Temperature



LTC1401 • TPC09

PIN FUNCTIONS

V_{CC} (Pin 1): Positive Supply, 3V. Bypass to GND (10µF tantalum in parallel with 0.1µF ceramic).

A_{IN} (Pin 2): Analog Input. 0V to 2.048V.

V_{REF} (Pin 3): 1.2V Reference Output. Bypass to GND (10µF tantalum in parallel with 0.1µF ceramic).

GND (Pin 4): Ground. GND should be tied directly to an analog ground plane.

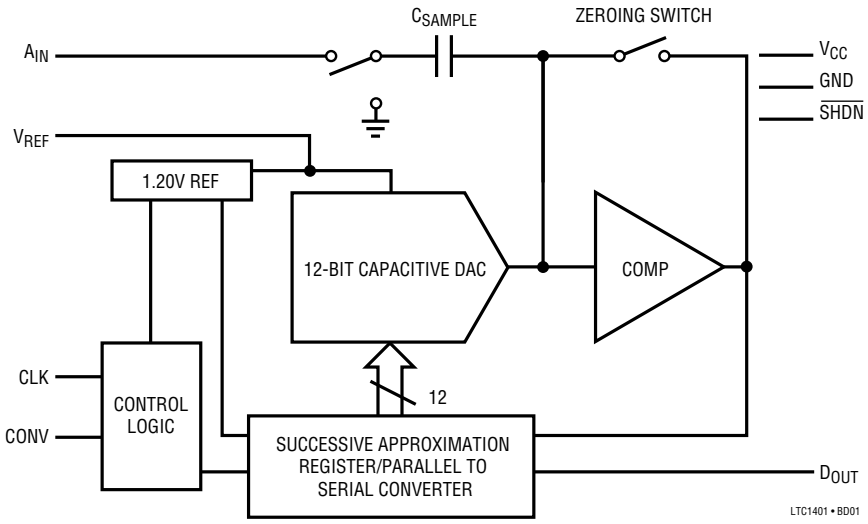
D_{OUT} (Pin 5): The A/D conversion result is shifted out from this pin.

CLK (Pin 6): Clock. This clock synchronizes the serial data transfer. A minimum CLK pulse of 60ns signals the ADC to wake up from Nap or Sleep mode.

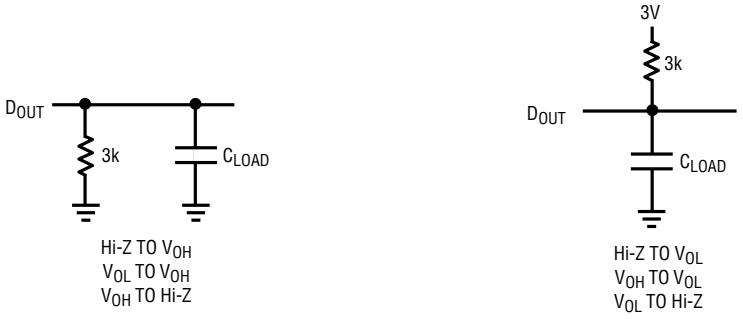
CONV (Pin 7): Conversion Start Signal. This active high signal starts a conversion on its rising edge. Keeping CLK low and pulsing CONV two/four times will put the ADC into Nap/Sleep mode.

$\overline{SHDN}$ (Pin 8): Shutdown Input. Pull this pin Low to put the ADC in Shutdown mode and save power (REFRDY will go Low). The device will draw 4.5µA in this mode.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS



APPLICATIONS INFORMATION

Conversion Details

The LTC1401 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit serial output based on a precision internal reference. The control logic provides an easy interface to microprocessors and DSPs through serial 3-wire connections.

A rising edge on the CONV input starts a conversion. At the start of a conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun, it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN} input connects to the sample-and-hold capacitor during the acquire phase and the comparator offset is nulled by the feedback switch. In this acquire phase, it typically takes 315ns for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the comparator feedback switch opens, putting the comparator into the compare mode. The input switches C_{SAMPLE} to ground, injecting the analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the A_{IN} input charge. The SAR contents (a 12-bit data word) which represent the input voltage, are presented through the serial pin D_{OUT}.

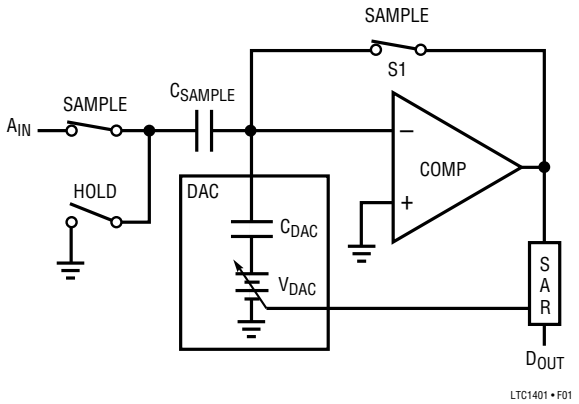


Figure 1. A_{IN} Input

Dynamic Performance

The LTC1401 has excellent high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2a shows a typical LTC1401 FFT plot.

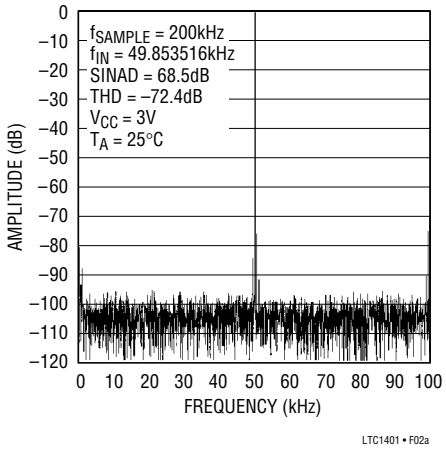


Figure 2a. LTC1401 Nonaveraged, 4096 Point FFT Plot with 50kHz Input Frequency

Signal-to-Noise Ratio

The signal-to-noise plus distortion ratio [S/(N+D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from DC to half the sampling frequency. Figure 2a shows a typical spectral content with a 200kHz sampling rate and a 50kHz input. The dynamic performance is excellent for input frequencies up to the Nyquist limit of 100kHz as shown in Figure 2b.

APPLICATIONS INFORMATION

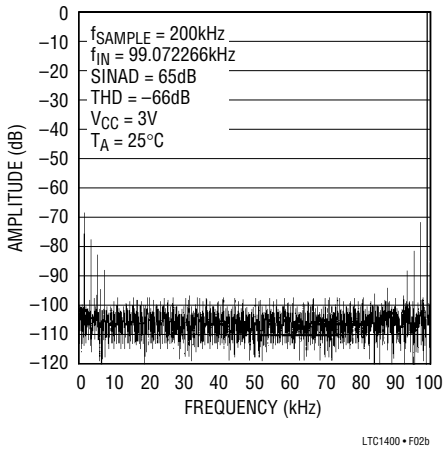


Figure 2b. LTC1401 Nonaveraged, 4096 Point FFT Plot with 100kHz Input Frequency

Effective Number of Bits

The effective number of bits (ENOBs) is a measurement of the effective resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = \frac{S/(N+D) - 1.76}{6.02}$$

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. Figure 3 shows ENOBs vs Input Frequency.

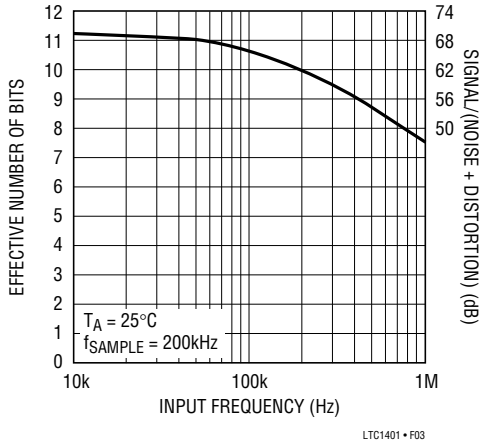


Figure 3. Effective Bits and Signal-to-Noise + Distortion vs Input Frequency

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half of the sampling frequency. THD is expressed as:

$$THD = 20\log \frac{\sqrt{V2^2 + V3^2 + ...Vn^2}}{V1}$$

Where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. THD vs input frequency is shown in Figure 4. The LTC1401 has good distortion performance up to the Nyquist frequency and beyond.

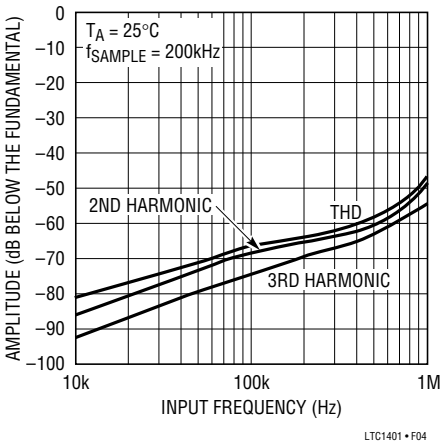


Figure 4. Distortion vs Input Frequency

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and differ-

APPLICATIONS INFORMATION

ence frequencies of mfa ±nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb) and (fa – fb) while 3rd order IMD terms includes (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula.

$$IMD(fa \pm fb) = 20\log\frac{\text{Amplitude at } (fa \pm fb)}{\text{Amplitude at fa}}$$

Figure 5 shows the IMD performance at a 50kHz input.

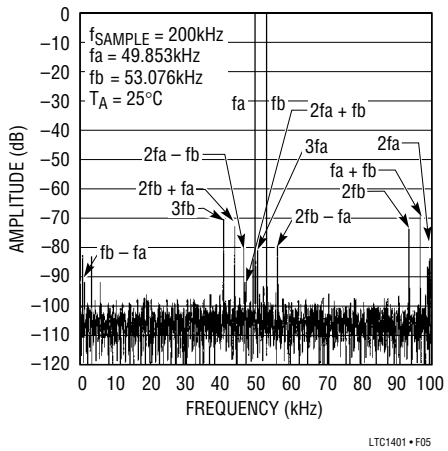


Figure 5. Intermodulation Distortion Plot

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

Full Power and Full Linear Bandwidth

The full power bandwidth is the input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal.

The full linear bandwidth is the input frequency at which the S/(N+D) has dropped to 68dB (11 effective bits).

Driving the Analog Input

The analog input of the LTC1401 is easy to drive. It draws only one small current spike while charging the sample-and-hold capacitor at the end of a conversion. During conversion, the analog input draws only a small leakage current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Any op amp that settles in 315ns to small load current transients will allow maximum speed operation. If a slower op amp is used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC's A_{IN} input include the LT®1498 and the LT1630 op amps.

The following list is a summary of the op amps that are suitable for driving the LTC1401, more detailed information is available in the Linear Technology databooks and the LinearView™ CD-ROM.

LT1215/LT1216: Dual and quad 23MHz, 50V/µs single supply op amps. Single 5V to ±15V supplies, 6.6mA specifications, 90ns settling to 0.5LSB.

LT1229/LT1230: Dual and quad 100MHz current feedback amplifiers. ±2V to ±15V supplies, 6mA supply current each amplifier. Low noise. Good AC specs.

LT1498/LT1499: Dual or quad 10MHz, 6V/µs, single 2.2V to ±15V supplies, 1.7mA supply current per amplifier, input/output swings rail-to-rail. Excellent AC and DC specs.

LT1630: Dual or quad 30MHz, 10V/µs, single 2.7V to ±15V supplies, 3.5mA supply current per amplifier, input/output swings rail-to-rail. Good AC and DC specs.

Internal Reference

The LTC1401 has an on-chip, temperature compensated, curvature corrected, bandgap reference, which is factory trimmed to 1.20V. It is internally connected to the DAC and

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APPLICATIONS INFORMATION

is available at Pin 3 to provide up to 1mA current to an external load. For minimum code transition noise, the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10uF tantalum in parallel with a 0.1uF ceramic is recommended). The V_{REF} pin can be driven with a DAC or other means to provide input span adjustment. The V_{REF} pin must be driven to at least 1.25V to prevent conflict with the internal reference. The reference should not be driven to more than 3V.

Figure 6 shows an LT1360 op amp driving the reference pin. Figure 7 shows a typical reference (LT1634-1.25) connected to the LTC1401. This will provide improved drift (equal to the maximum 25ppm/°C of the LT1634-1.25) and a 2.1338V full scale.

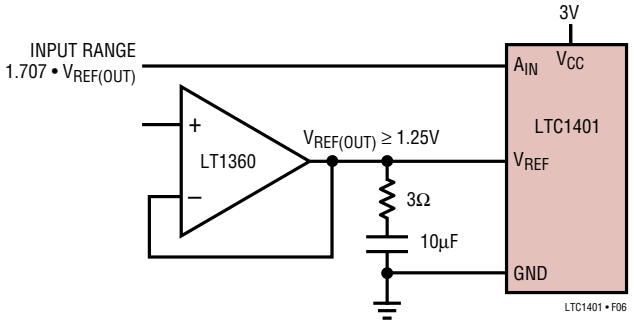


Figure 6. Driving the V_{REF} with the LT1360 Op Amp

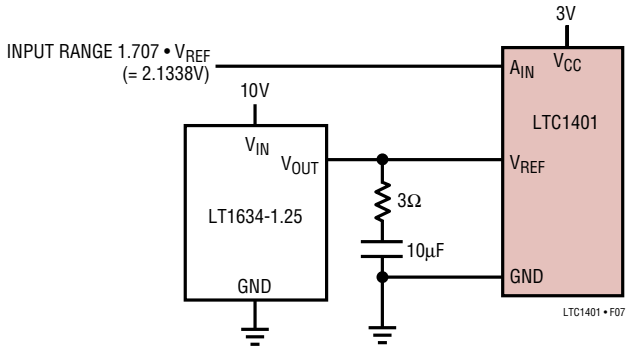


Figure 7. Supplying a 2.5V Reference Voltage to the LTC1401 with the LT1634-1.25

UNIPOLAR OPERATION AND ADJUSTMENT

Figure 8 shows the ideal input/output characteristics for the LTC1401. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, ... FS – 1.5LSB). The output code is natural binary with 1LSB = 2.048/4096 = 0.5mV.

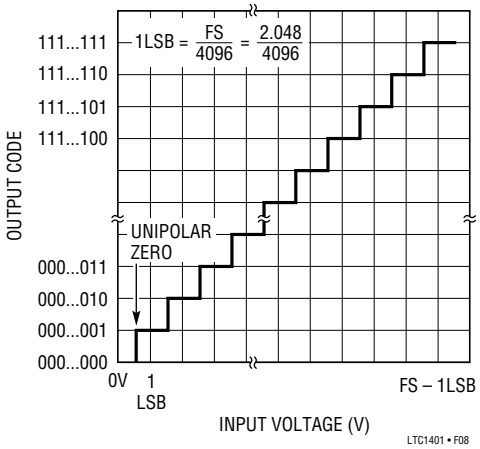


Figure 8. LTC1401 Unipolar Transfer Characteristics

Unipolar Offset and Full-Scale Error Adjustments

In applications where absolute accuracy is important, the offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 9a shows the extra components required for full scale error adjustment. If both offset and full-scale adjustments are needed, the circuit in Figure 9b can be used. For zero offset error, apply 0.25mV (i.e., 0.5LSB) at the input and adjust the offset trim until the LTC1401 output code flickers between 0000 0000 0000 and 0000 0000 0001. For zero full-scale error, apply an analog input of 2.04725V (FS – 1.5LSB or last code transition) at the input and adjust R5 until the LTC1401 output code flickers between 1111 1111 1110 and 1111 1111 1111.

APPLICATIONS INFORMATION

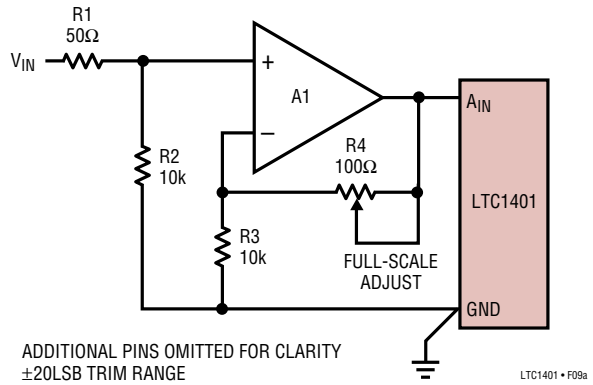


Figure 9a. LTC1401 Full-Scale Adjust Circuit

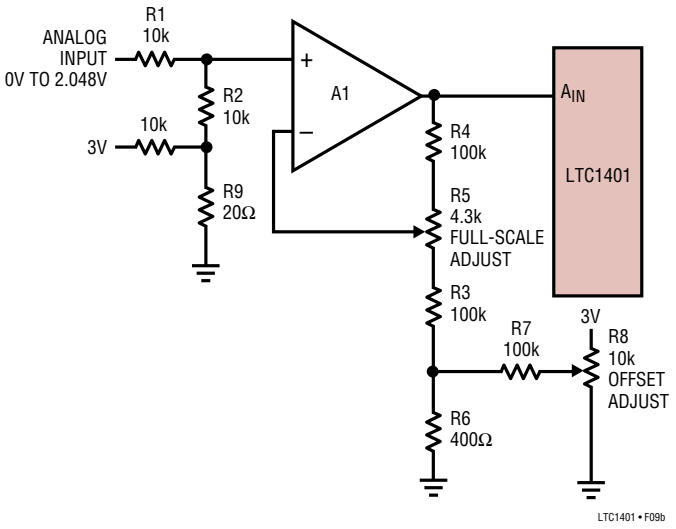


Figure 9b. LTC1401 Offset and Full-Scale Adjust Circuit

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1401, a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital traces alongside an analog signal trace or underneath the ADC. The analog input should be screened by GND.

High quality tantalum and ceramic bypass capacitors should be used at the V_{CC} and V_{REF} pins as shown in the Typical Application on the first page of this datasheet. For optimum performance, a 10µF surface mount AVX capacitor in parallel with a 0.1µF ceramic is recommended for the V_{CC} and V_{REF} pins. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Input signal leads to A_{IN} and signal return leads from GND (Pin 4) should be kept as short as possible to minimize noise coupling. In applications where this is not possible, a shielded cable between the analog input signal and the ADC is recommended. Also, any potential difference in grounds between the analog signal and the ADC appears as an error voltage in series with the analog input signal. Attention should be paid to reducing the ground circuit impedance as much as possible.

Figure 10 shows the recommended system ground connections. All analog circuitry grounds should be terminated at the LTC1401 GND pin. The ground return to the power supply from Pin 4 should be low impedance for noise free operation. Digital circuitry grounds must be connected to the digital supply common.

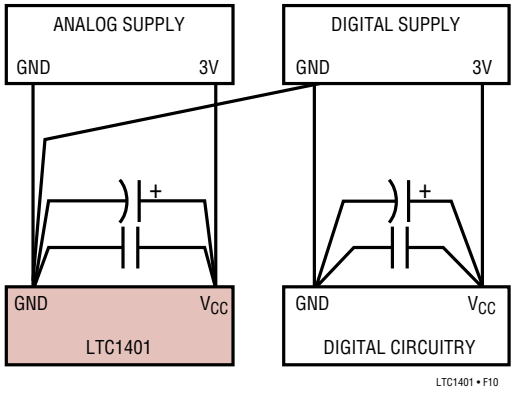


Figure 10. Power Supply Connection

Power-Down Mode

Upon power up, the LTC1401 is initialized to the active state and is ready for conversion. However, the chip can be easily placed into Nap or Sleep mode by exercising the right combination of CLK and CONV signals. In Nap mode, all power is off except the internal reference which remains active and provides 1.20V output voltage to the other

APPLICATIONS INFORMATION

circuitry. In this mode, the ADC draws only 1.5mW of power instead of 15mW (for minimum power, the logic inputs must be within 500mV of the supply rails). The wake-up time from Nap mode to active mode is 350ns. In Sleep mode, power consumption is reduced to 19.5µW by cutting off the supply to the comparator and reference. Figure 11 illustrates power-down methods for the LTC1401. The chip enters Nap mode by keeping the CLK signal low and pulsing the CONV signal twice. For Sleep mode operation, CONV signal should be pulsed four times while CLK is kept low. NAP and SLEEP modes are activated on the falling edge of the CONV pulse. By pulling $\overline{SHDN}$ low, the LTC1401 enters Shutdown mode and power consumption drops to 13.5µW.

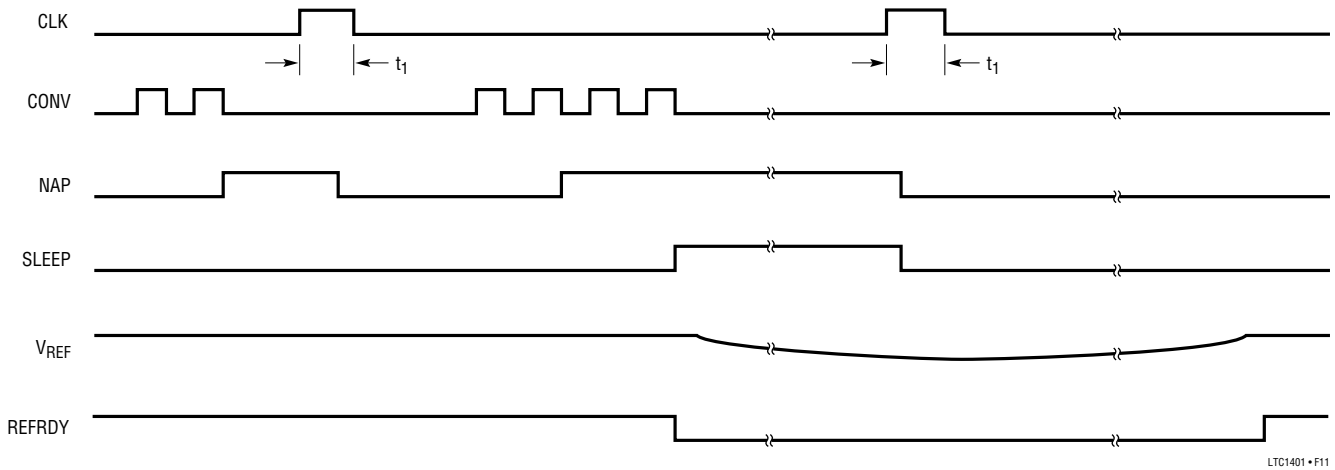
Once $\overline{SHDN}$ goes high, the LTC1401 returns to active mode or the LTC1401 returns to active mode by pulsing the CLK signal if the device has entered Nap/Sleep mode. During the transistion from Sleep mode to active mode, the V_{REF} voltage ramp-up time is a function of its loading conditions. With a 10µF bypass capacitor, the wake-up time from Sleep mode is typically 3ms. A REFRDY signal is activated once the reference has settled and is ready for an A/D conversion. This REFRDY bit is sent to the D_{OUT} pin as the first bit followed by the 12-bit data word (refer to Figure 12).

DIGITAL INTERFACE

The digital interface requires only three digital lines. CLK and CONV are both inputs, and the D_{OUT} output provides the conversion result in serial form.

Figures 12 and 13 show the digital timing waveform of the LTC1401 during the Analog to Digital Conversion. The CONV rising edge starts the conversion. Once initiated, it can not be restarted until the conversion is completed. If the time from the CONV signal to the CLK rising edge is less than t_2, the digital output will be delayed by one clock cycle.

The digital output data is updated on the rising edge of the CLK line. The digital output data consists of a REFRDY bit followed by the valid 12-bit data word. D_{OUT} data should be captured by the receiving system on the rising CLK edge. Data remains valid for a minimum time of t_{10} after the rising CLK edge to allow capture to occur.



NOTE: NAP AND SLEEP ARE INTERNAL SIGNALS. REFRDY APPEARS AS THE FIRST BIT IN THE D_{OUT} WORD.

Figure 11. Nap Mode and Sleep Mode Waveforms

APPLICATIONS INFORMATION

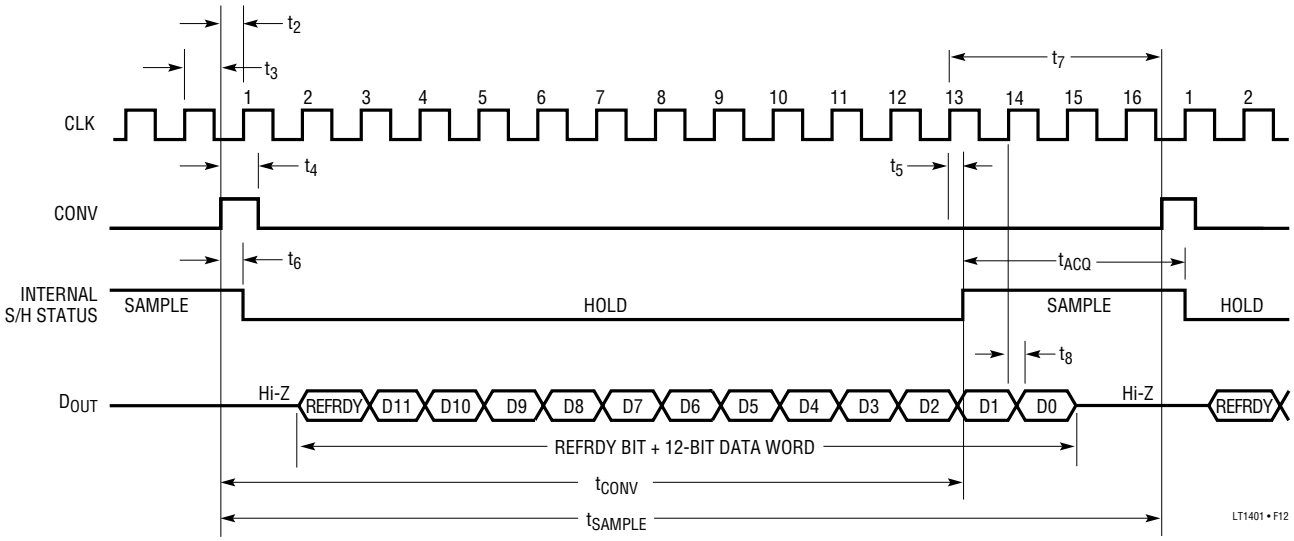


Figure 12. ADC Digital Timing Waveform

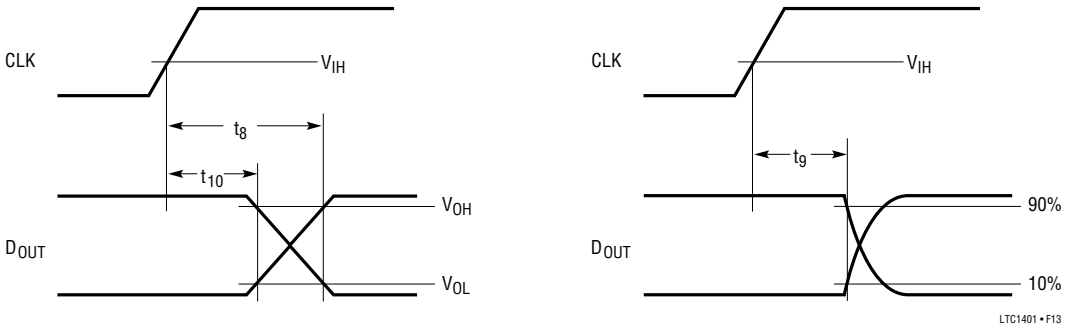
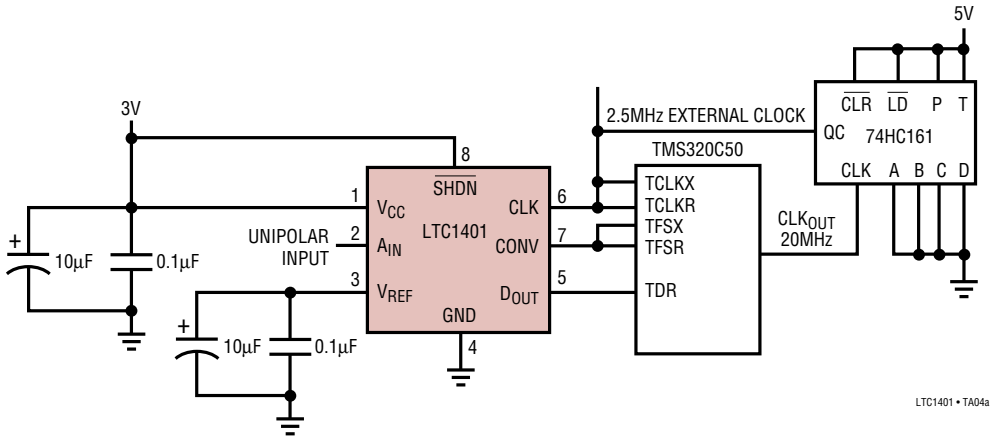


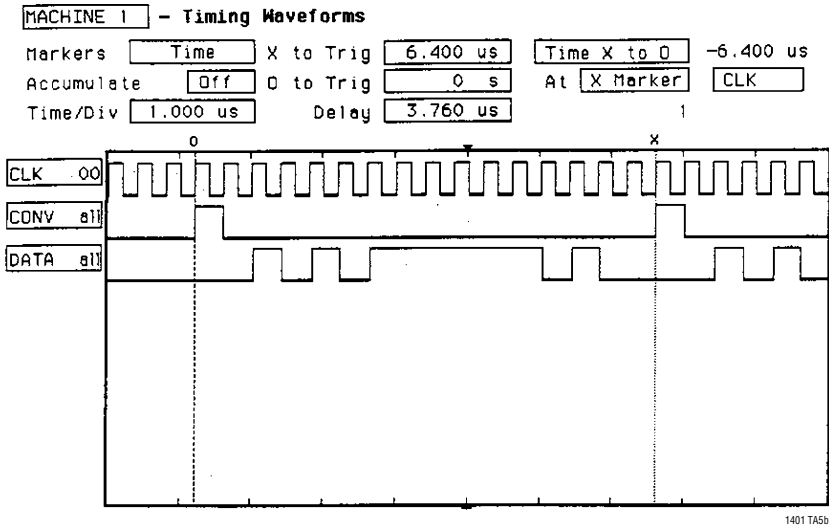
Figure 13. CLK to D_{OUT} Delay

TYPICAL APPLICATIONS

Interface to the TMS320C50's TDM Serial Port (Frame Sync is Generated from TFSX)



Logic Analyzer Waveforms Show 6.4µs Throughput Rate (Input Voltage = 0.765V, Output Code = 0101 1111 1010 = 1530_{10})



Data from the LTC1401 Loaded into the TMS320C50's TRCV Register

X	RDY	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X

1401 TA4c

Data Stored in the TMS320C50's Memory (in Right Justified Format)

0	0	0	RDY	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

1401 TA4d

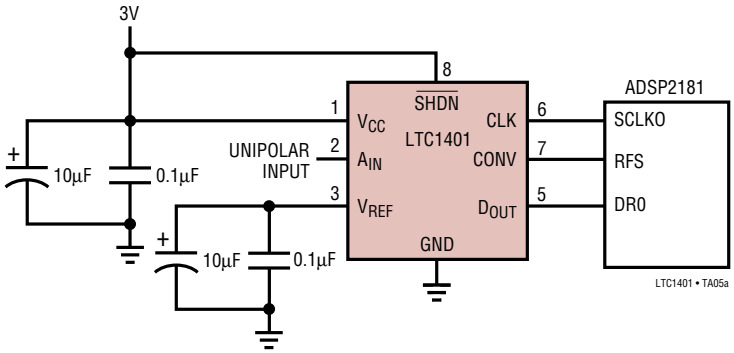
TYPICAL APPLICATIONS

TMS320C50 Code for Circuit

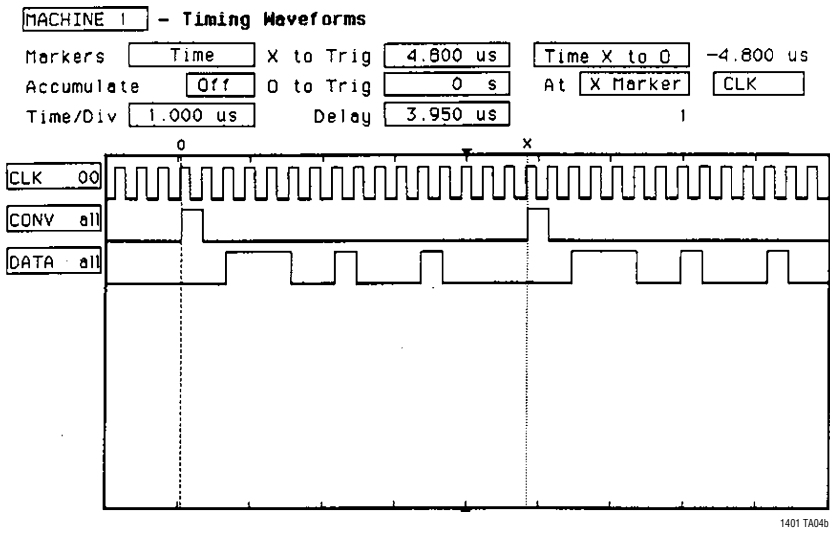
```
*************************************************************
**THIS PROGRAM DEMONSTRATES THE LTC1401 INTERFACE TO THE**
**TMS320C50. FRAME SYNC PULSE IS GENERATED FROM TFSX.**
**DATA SHIFT CLOCK IS DERIVED FROM CLKOUT.**
*************************************************************
*Initialization*
    .mmregs                     ; Defines global symbolic names
;- - Initialized data memory to zero
          .ds       0F00h       ; Initialize data to zero
DATA0     .word     0           ; Begin sample data location
DATA1     .word     0           ; .
DATA2     .word     0           ; Location of data
DATA3     .word     0           ; .
DATA4     .word     0           ; .
DATA5     .word     0           ; End sample data location
;- - Set up the ISR vector
          .ps       080Ah       ; Serial ports interrupts
rint :    B         RECEIVE     ; 0A;
xint :    B         TRANSMIT    ; 0C;
trnt :    B         TREC        ; 0E;
txnt :    B         TTRANX      ; 10;
;- - Setup the reset vector
    .ps 0A00h
    .entry
START:
*************************************************************
*TMS320C50 Initialization*
    SETC  INTM              ; Temporarily disable all interrupts
    LDP   #0                ; Set data page pointer to zero
    OPL   #0834h, PMST      ; Set up the PMST status and control register
    LACC  #0
    SAMM  CWSR              ; Set software wait state to 0
    SAMM  PDWSR             ;
*************************************************************
*Configure Serial Port*
    SPLK  #0028h, TSPC      ; Set TDM Serial Port
                            ; TDM = 0 Stand Alone mode
                            ; DLB = 0 Not loop back
                            ; FO = 0 16 Bits
                            ; FSM = 1 Burst Mode
                            ; MCM = 0 CLKR is generated externally
                            ; TXM = 1 FSX as output pin
                            ; Put serial port into reset
                            ; (XRST = RRST = 0)
    SPLK  #00E8h, TSPC      ; Take Serial Port out of reset
                            ; (XRST = RRST = 1)
    SPLK  #0FFFFh, IFR      ; Clear all the pending interrupts
*************************************************************
*Start Serial Communication*
    SACL  TDXR              ; Generate frame sync pulse
    SPLK  #040h, IMR        ; Turn on TRNT receiver interrupt
    CLRC  INTM              ; Enable interrupt
    CLRC  SXM               ; For Unipolar input, set for right shift
                            ; with no sign extension
    MAR   *AR7              ; Load the auxiliary register pointer with seven
    LAR   AR7, #0F00h       ; Load the auxiliary register seven with #0F00h
                            ; as the begin address for data storage
WAIT:     NOP               ; Wait for a receive interrupt
          NOP               ;
          NOP               ;
    SACL  TDXR              ; !! Regenerate the frame sync pulse
    B     WAIT              ;
; - - - - - - - end of main program - - - - - - - - - - ;
*************************************************************
*Receiver Interrupt Service Routine*
TREC:
    LAMM  TRCV              ; Load the data received from LTC1401
    SFR                     ; Shift right two times
    SFR                     ;
    AND   #1FFFh, 0         ; ANDed with #1FFFh
                            ; For converting the data to right
                            ; justified format
                            ;
    SACL  *+, 0             ; Write to data memory pointed by AR7 and
                            ; Increase the memory address by one
    LACC  AR7               ;
    SUB   #0F05h,0          ; Compare to end sample address #0F05h
    BCND  END_TRCV, GEQ     ; If the end sample address has exceeded jump
                            to END_TRCV
                            ;
    SPLK  #040h, IMR        ; Else re-enable the TRNT receive interrupt
    RETE                    ; Return to main program and enable interrupt
*************************************************************
*After Obtained the Data from LTC1401, Program Jump to END_TRCV*
END_TRCV:
    SPLK  #002h, IMR        ; Enable INT2 for program to halt
    CLRC  INTM
SUCCESS:
    B     SUCCESS
*************************************************************
*Fill the unused interrupt with RETE, to avoid program get "lost"*
TTRANX:
    RETE
RECEIVE:
    RETE
TRANSMIT:
    RETE
INT2:
    B halt                  ; Halts the running CPU
*************************************************************
```

TYPICAL APPLICATIONS

LTC1401 Interface to the ADSP2181's SPORT0 (Frame Sync is Generated from RFS)



Logic Analyzer Waveforms Show 4.8µs Throughput Rate (Input Voltage = 1.604V, Output Code = 1100 1000 1000 = 3208_{10})



Data from the LTC1401 (Normal Mode)

X	RDY	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X

LTC1401 • TA05c

Data Stored in the ADSP2181's Memory (Normal Mode, SLEN = D)

0	0	0	RDY	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

LTC1401 • TA05d

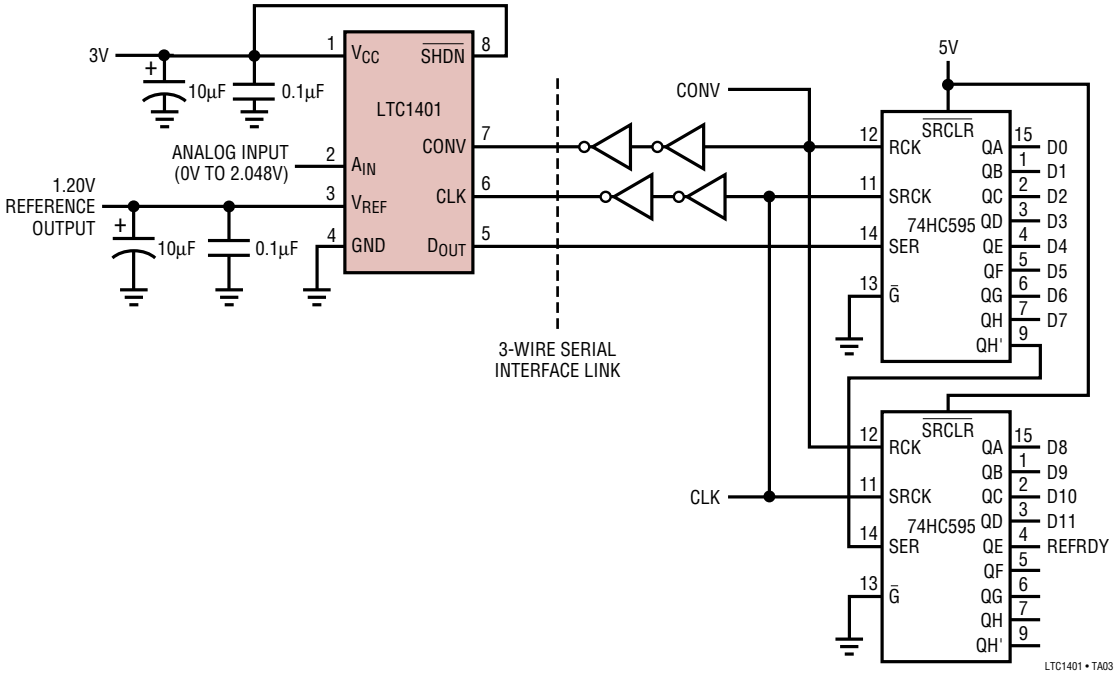
TYPICAL APPLICATIONS

ADSP2181 Code for Circuit

```
THIS PROGRAM DEMONSTRATES THE LTC1401 INTERFACE TO THE
ADSP-2181. FRAME SYNC PULSE IS GENERATED FROM RFS.
DATA SHIFT CLOCK IS INTERNALLY GENERATED.

/*Section 1: Initialization*/
.module/ram/abs = 0 adspltc;    /*define the program module*/
    jump start;             /*jump over interrupt vectors*/
    nop; nop; nop;
    rti; rti; rti; rti;     /*code vectors here upon IRQ2 int*/
    rti; rti; rti; rti;     /*code vectors here upon IRQL1 int*/
    rti; rti; rti; rti;     /*code vectors here upon IRQL0 int*/
    rti; rti; rti; rti;     /*code vectors here upon SPORT0 TX int*/
    ax0 = rx0;              /*Section 5*/
    dm (0x2000) = ax0;      /*begin of SPORT0 receive interrupt*/
    rti;                    /* */
                            /* */
                            /*end of SPORT0 receive interrupt*/
    rti; rti; rti; rti;     /*code vectors here upon /IRQE int*/
    rti; rti; rti; rti;     /*code vectors here upon BDMA interrupt*/
    rti; rti; rti; rti;     /*code vectors here upon SPORT1 TX (IRQ1) int*/
    rti; rti; rti; rti;     /*code vectors here upon SPORT1 RX (IRQ0) int*/
    rti; rti; rti; rti;     /*code vectors here upon TIMER int*/
    rti; rti; rti; rti;     /*code vectors here upon POWER DOWN int*/

/*Section 2: Configure SPORT0*/
start:
/*to configure SPORT0 control reg*/
                            /*SPORT0 address = 0x3FF6*/
                            /*RFS is used for frame sync generation*/
                            /*RFS is internal, TFS is not used*/
                            /*bit 0-3 = Slen*/
                            /*F = 15 = 1111*/
                            /*E = 14 = 1110*/
                            /*D = 13 = 1101*/
                            /*bit 4,5 data type right justified zero filled MSB*/
                            /*bit 6 INVRFS = 0*/
                            /*bit 7 INVTFS = 0*/
                            /*bit 8 IRFS=1 receive internal frame sync*/
                            /*bit 9,10,11 are for TFS (don't care)*/
                            /*bit 12 RFSW=0 receive is normal mode*/
                            /*bit 13 RTFS=1 receive is framed mode*/
                            /*bit 14 ISCLK = 1 clock is internal*/
                            /*bit 15 multichannel mode = 0*/
    ax0 = 0x6F0D;

    dm (0x3FF6) =ax0;

/*Section 3: configure CLKDIV and RFSDIV, setup interrupts*/
/*to configure CLKDIV reg*/
    ax0= 4;
    dm(0x3FF5) =ax0;        /*set the serial clock divide modulus reg
                            SCLKDIV*/
                            /*the input clock frequency = 16.67MHz*/
                            /*CLKOUT frequency = 2x = 33MHz*/
                            /*SCLK= 1/2*CLKOUT*1/(SCLKDIV+1)*/
                            /*for SCLKDIV = 4, SCLK = 33/10 = 3.3MHz*/
/*to Configure RFSDIV*/
    ax0 = 15;               /*set the RFSDIV reg = 15*/
                            /*=> the frame sync pulse for every 16 SCLK*/
                            /*if frame sync pulse in every 15 SCLK, ax0=14*/
    dm(0x3FF4) =ax0;
/*to setup interrupt*/
    ifc= 0x0066;            /*clear any extraneous SPORT interrupts*/
    icntl= 0;               /*IRQXB = level sensitivity*/
                            /*disable nesting interrupt*/
    imask= 0x0020;          /*bit 0 = timer int = 0*/
                            /*bit 1 = SPORT1 or IRQ0B int = 0*/
                            /*bit 2 = SPORT1 or IRQ1B int = 0*/
                            /*bit 3 = BDMA int = 0*/
                            /*bit 4 = IRQEB int = 0*/
                            /*bit 5 = SPORT0 receive int = 1*/
                            /*bit 6 = SPORT0 transmit int = 0*/
                            /*bit 7 = IRQ2B int = 0*/
                            /*enable SPORT0 receive interrupt*/

/*Section 4: Configure System Control Register and Start Communication*/
/*to configure system control reg*/
    ax0 = dm(0x3FFF);       /*read the system control reg*/
    ay0 = 0xFFF0;
    ar = ax0 AND ay0;       /*set wait state to zero*/
    ay0 = 0x1000;
    ar = ar OR ay0;         /*bit 12 = 1, enable SPORT0*/
    dm(0x3FFF) = ar;
/*frame sync pulse regenerated automatically*/
    cntr = 5000;
do waitloop until ce;
    nop;
    nop;
    nop;
    nop;
    nop;
    nop;
waitloop: nop;
    rts;
.endmod;
```

TYPICAL APPLICATIONS

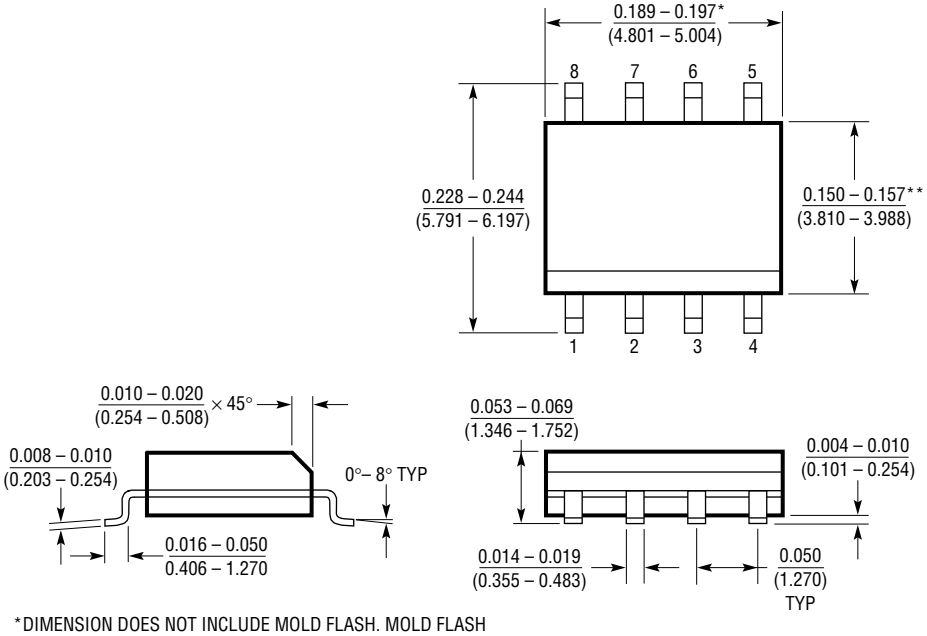
Quick Look Circuit for Converting Data to Parallel Format



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

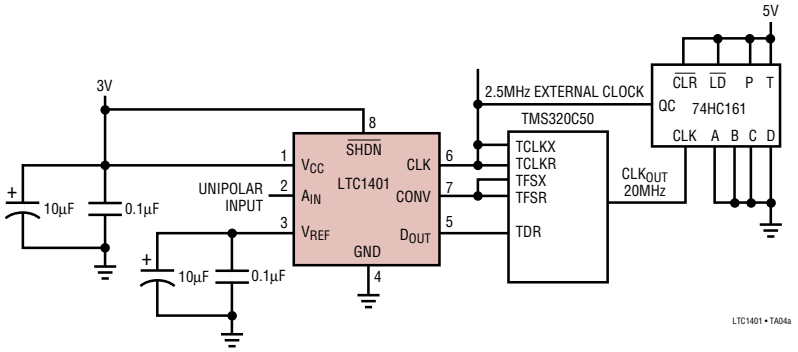
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 0996

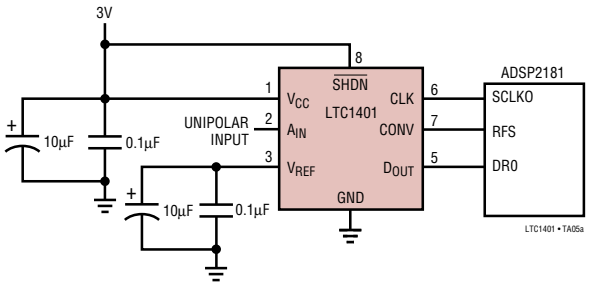
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATIONS

Interface to the TMS320C50's TDM Serial Port (Frame Sync is Generated from TFSX)



LTC1401 Interface to the ADSP2181's SPORT0 (Frame Sync is Generated from RFS)



RELATED PARTS

12-Bit Parallel Output ADCs

PART NUMBER	DESCRIPTION	COMMENTS
LTC1273/LTC1275/LTC1276	Complete 5V Sampling 12-Bit ADCs with 70dB SINAD at Niquist	Lower Power and Cost Effective for $f_{SAMPLE} \leq 300$ksps
LTC1274/LTC1277	Low Power 12-Bit ADCs with Nap and Sleep Mode Shutdown	Lowest Power (10mW) $f_{SAMPLE} \leq 100$ksps
LTC1278/LTC1279	High Speed Sampling 12-Bit ADCs with Shutdown	Cost Effective 12-Bit ADCs with Convert Start Input Best for 300ksps < $f_{SAMPLE} \leq 600$ksps
LTC1282	Complete 3V 12-Bit ADCs with 12mW Power Dissipation	Fully Specified for 3V Powered Applications, $f_{SAMPLE} \leq 140$ksps
LTC1409	Low Power 12-Bit, 800ksps Sampling ADC	Best Dynamic Performance $f_{SAMPLE} \leq 800$ksps, 80mW Dissipation
LTC1410	12-Bit, 1.25Msps Sampling ADC with Shutdown	Best Dynamic Performance, THD = –84dB and SINAD = 71dB at Nyquist

12-Bit Serial Output ADCs

PART NUMBER	V_{CC}	SAMPLE RATE	POWER DISSIPATION	DESCRIPTION
LTC1285/LTC1288	3V	7.5/6.6ksps	0.48mW	3V, One or Two Input, Micropower, SO-8
LTC1286/LTC1298	5V	12.5/11.1ksps	1.25mV	One or Two Input, Micropower, SO-8
LTC1290	5/±5V	50ksps	30mW	8 Input, Full-Duplex Serial I/O
LTC1296	5/±5V	46.5ksps	30mW	8 Input, Half-Duplex Serial I/O, Power Shutdown Output
LTC1400	5/±5V	400ksps	75mW	Complete 12-Bit, 400ksps, SO-8 ADC with Shutdown
LTC1404	5/±5V	600ksps	75mW	Complete 12-Bit, 600ksps, SO-8 ADC with Shutdown

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