RELIABILITY REPORT

FOR

LMX321AxK

PLASTIC ENCAPSULATED DEVICES

May 26, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Written by

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Conclusion

The LMX321 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The LMX321 is a single, low-cost, low-voltage, pin-to-pin compatible upgrade to the LMV321 general-purpose op amp. This device offers Rail-to-Rail® outputs and an input common-mode range that extends below ground. This op amp draws only $105\mu\text{A}$ of quiescent current per amplifier, operates from a single +2.3V to +7V supply, and drives $2k\Omega$ resistive loads to within 40mV of either rail. The LMX321 is unity-gain stable with a 1.3MHz gain-bandwidth product capable of driving capacitive loads up to 400pF. The combination of low voltage, low cost, and small package size makes this amplifier ideal for portable/battery-powered equipment.

The LMX321 single op amp is available in ultra-small 5-pin SC70 and space-saving 5-pin SOT23 packages.

B. Absolute Maximum Ratings

<u>ltem</u>	Rating
Supply Voltage (V _{CC} to V _{EE}) Differential Input Voltage (VIN+ - VIN-) OUT_ to VEE Short-Circuit Duration (OUT_ shorted to VCC or VEE)	-0.3V to +8V VEE to VCC -0.3V to (VCC + 0.3V) Continuous
Continuous Power Dissapation ($T_A = +70^{\circ}C$) Storage Temp.	-65°C to +150°C
Junction Temperature	+150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
5 Lead SOT23	571mW
5 Lead SC70	247mW
Derates above +70°C	
5 Lead SOT-23	7.1mW/°C
5 Lead SC70	3.1mW/°C

II. Manufacturing Information

A. Description/Function: Single, General Purpose, Low-Voltage, Rail-to-Rail Op Amp

B. Process: CB20 (High Speed Complementary Bipolar Process)

C. Number of Device Transistors: 88

D. Fabrication Location: Oregon, USA

E. Assembly Location: Philippines, Malaysia or Thailand

F. Date of Initial Production: July, 2001

III. Packaging Information

A. Package Type: 5 Lead SOT-23 5-Lead SC70

B. Lead Frame: Copper Alloy 42

C. Lead Finish: Solder Plate Solder Plate

D. Die Attach: Silver-filled Epoxy Silver-filled Epoxy

E. Bondwire: Gold (1 mil dia.) Gold (1 mil dia.)

F. Mold Material: Epoxy with silica filler Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-2501-0167 Buildsheet # 05-2501-0168

H. Flammability Rating: Class UL94-V0 Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 31 x 30 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Gold

D. Backside Metallization: None

E. Minimum Metal Width: 2 microns (as drawn)

F. Minimum Metal Spacing: 2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 79 \times 2} \text{(Chi square value for MTTF upper limit)}$$

$$\frac{1}{\text{Temperature Acceleration factor assuming an activation energy of } 0.8eV$$

$$\lambda = 13.76 \times 10^{-9}$$

 λ = 13.76 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5662) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1L).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85° C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The OX63 die type has been found to have all pins able to withstand a transient pulse of ± 25000 V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA.

Table 1Reliability Evaluation Test Results

LMX321AxK

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		79	0
Moisture Testin	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SC70 SOT23	77 99	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the package.

Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/2/

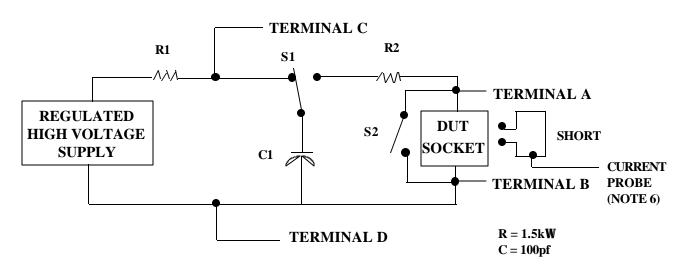
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- $\overline{3/}$ Repeat pin combination I for each named Power supply and for ground

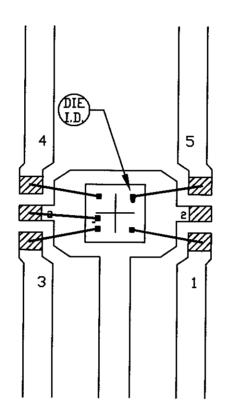
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., \(\mathbb{L}_{S1} \), or \(\mathbb{L}_{S2} \) or \(\mathbb{L}_{S3} \) or \(\mathbb{L}_{C1} \), or \(\mathbb{L}_{C2} \)) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



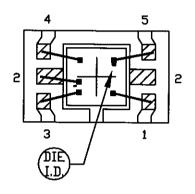
Mil Std 883D Method 3015.7 Notice 8



Ø- BONDING AREA

NOTE: CAVITY DOWN

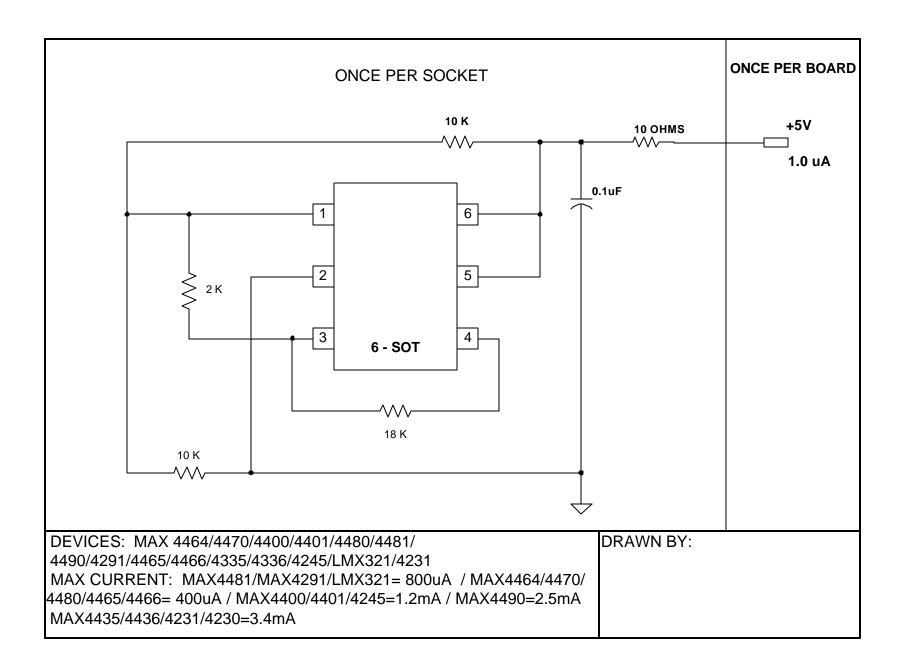
PKG. CODE: U5-1		SIGNATURES	DATE	CONFIDENTIAL & PROPRIE	
CAV./PAD SIZE:	PKG.			BOND DIAGRAM #:	REV:
64X45	DESIGN	•		05-2501-0167	Α



☑ BONDABLE AREA

NOTE: CAVITY DOWN

PKG. CODE: X5-1		SIGNATURES	DATE	CONFIDENTIAL & PROPRIE	
CAV./PAD SIZE:	PKG.	···		BOND DIAGRAM #:	REV:
35×34	DESIGN			05-2501-0168	Α



DOCUMENT I.D. 06-5662	REVISION E	MAXIM TITLE: BI Circuit	PAGE 2 OF 3	
		(MAX4464/4470/4465/4466/4400/4401/4480/4481/4490/4291/4335/4336/4245/LMX321/		
		4231/4230)		