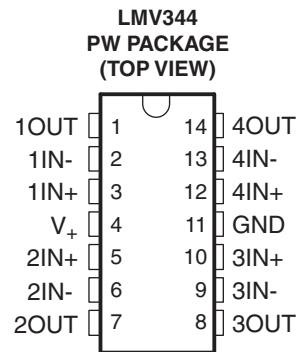
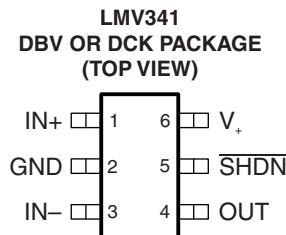


RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS

FEATURES

- Qualified for Automotive Applications
- 2.7-V and 5-V Performance
- Rail-to-Rail Output Swing
- Input Bias Current: 1 pA Typ
- Input Offset Voltage: 0.25 mV Typ
- Low Supply Current: 100 μ A Typ
- Gain Bandwidth: 1 MHz Typ
- Slew Rate: 1 V/ μ s Typ
- Turn-On Time From Shutdown: 5 μ s Typ
- Input Referred Voltage Noise (at 10 kHz): 20 nV/ $\sqrt{\text{Hz}}$



DESCRIPTION/ORDERING INFORMATION

The LMV341 and LMV344 devices are single and quad CMOS operational amplifiers, respectively, with low voltage, low power, and rail-to-rail output swing capabilities. The PMOS input stage offers an ultra-low input bias current of 1 pA (typ) and an offset voltage of 0.25 mV (typ). The single supply amplifier is designed specifically for low-voltage (2.7 V to 5 V) operation, with a wide common-mode input voltage range that typically extends from -0.2 V to 0.8 V from the positive supply rail. Additional features are a 20-nV/ $\sqrt{\text{Hz}}$ voltage noise at 10 kHz, 1-MHz unity-gain bandwidth, 1-V/ μ s slew rate, and 100- μ A current consumption per channel.

An extended industrial temperature range from -40°C to 125°C makes this device suitable for automotive applications.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
-40°C to 125°C	SC-70 – DCK	Reel of 3000	LMV341QDCKRQ1	RR_
	SOT-23 – DBV	Reel of 3000	LMV341QDBVRQ1	RCH_
	TSSOP – PW	Reel of 2000	LMV344IPWRQ1	LMV344Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

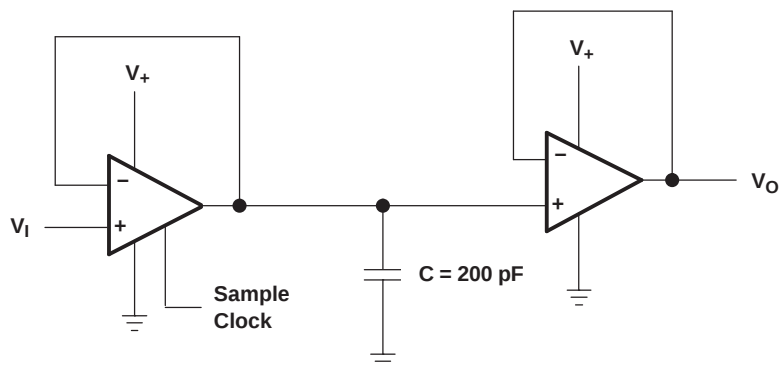
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) DBV/DCK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

APPLICATION CIRCUIT: SAMPLE-AND-HOLD CIRCUIT



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

V ₊	Supply voltage ⁽²⁾		5.5 V
V _{ID}	Differential input voltage ⁽³⁾		±5.5 V
V _I	Input voltage range (either input)		0 to 5.5 V
θ _{JA}	Package thermal impedance ⁽⁴⁾⁽⁵⁾	DBV package	165°C/W
		DCK package	259°C/W
		PW package	113°C/W
T _J	Operating virtual junction temperature		150°C
T _{stg}	Storage temperature range		–65°C to 150°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V₊ specified for the measurement of I_{OQ}) are with respect to the network GND.
- (3) Differential voltages are at IN+ with respect to IN–.
- (4) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) – T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (5) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V ₊	Supply voltage (single-supply operation)	2.5	5.5	V
T _A	Operating free-air temperature	−40	125	°C

ESD PROTECTION

TEST CONDITIONS	TYP	UNIT
Human-Body Model (HBM)	2000	V
Machine Model (MM)	200	V

ELECTRICAL CHARACTERISTICS

 $V_+ = 2.7\text{ V}$, $\text{GND} = 0\text{ V}$, $V_{IC} = V_O = V_+/2$, $R_L > 1\text{ M}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A	LMV341			LMV344			UNIT
					MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
V _{IO}	Input offset voltage			25°C	0.25		4	0.25		4	mV
				Full range	4.5		4.5				
α _{VIO}	Average temperature coefficient of input offset voltage			Full range	1.7			1.7		μV/°C	
I _{IB}	Input bias current			25°C	1	120	1		120	pA	
				–40°C to 85°C	250		250				
				–40°C to 125°C	3		3		nA		
I _{IO}	Input offset current			25°C	6.6		6.6		fA		
CMRR	Common-mode rejection ratio	0 ≤ V _{ICR} ≤ 1.7 V	25°C	40	80	56		80	dB		
		0 ≤ V _{ICR} ≤ 1.6 V	Full range	36	50						
k _{SVR}	Supply-voltage rejection ratio	2.7 V ≤ V ₊ ≤ 5 V		25°C	45	82	65		82	dB	
				Full range	60	60					
V _{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	0	–0.2 to 1.9	1.7	0	–0.2 to 1.9	1.7	V
A _V	Large-signal voltage gain ⁽²⁾	R _L = 10 kΩ to 1.35 V		25°C	73	113	78		113	dB	
				Full range	66	70					
		R _L = 2 kΩ to 1.35 V		25°C	70	103	72		103		
				Full range	63	64					
V _O	Output swing (delta from supply rails)	R _L = 2 kΩ to 1.35 V	Low level	25°C	24	60	24		60	mV	
				Full range	95		95				
			High level	25°C	26	60	26		60		
				Full range	95		95				
		R _L = 10 kΩ to 1.35 V	Low level	25°C	5	30	5		30		
				Full range	40		40				
			High level	25°C	5.3	30	5.3		30		
				Full range	40		40				
I _{CC}	Supply current (per channel)			25°C	100	170	100		170	μA	
				Full range	230		230				
I _{OS}	Output short- circuit current	Sourcing		25°C	20	32	18		24	mA	
		Sinking			15	24	15		24		
SR	Slew rate	R _L = 10 kΩ ⁽³⁾		25°C	1		1		V/μs		
GBM	Unity-gain bandwidth	R _L = 10 kΩ, C _L = 200 pF		25°C	1		1		MHz		
Φ _m	Phase margin	R _L = 100 kΩ		25°C	72		72		deg		
G _m	Gain margin	R _L = 100 kΩ		25°C	20		20		dB		
V _n	Equivalent input noise voltage	f = 1 kHz		25°C	40		40		nV/√Hz		
I _n	Equivalent input noise current	f = 1 kHz		25°C	0.001		0.001		pA/√Hz		
THD	Total harmonic distortion	f = 1 kHz, A _V = 1, R _L = 600 Ω, V _I = 1 V _{PP}		25°C	0.017		0.017		%		

(1) Typical values represent the most likely parametric norm.

(2) $\text{GND} + 0.2\text{ V} \leq V_O \leq V_+ - 0.2\text{ V}$

(3) Connected as voltage follower with $2\text{-}V_{PP}$ step input. Number specified is the slower of the positive and negative slew rates.

SHUTDOWN CHARACTERISTICS

$V_+ = 2.7\text{ V}$, $\text{GND} = 0\text{ V}$, $V_{\text{IC}} = V_{\text{O}} = V_+/2$, $R_{\text{L}} > 1\text{ M}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_{A}	MIN	TYP	MAX	UNIT
$I_{\text{CC(SHDN)}}$	Supply current in shutdown mode (per channel)	$V_{\text{SD}} = 0\text{ V}$	25°C		0.045	1000	nA
			Full range			1.5	μA
$t_{\text{(on)}}$	Amplifier turn-on time		25°C		5		μs
V_{SD}	Shutdown pin voltage range	ON mode	25°C	1.7 to 2.7	2.4 to 2.7		V
		Shutdown mode		0 to 1	0 to 0.8		

ELECTRICAL CHARACTERISTICS

 $V_+ = 5\text{ V}$, $\text{GND} = 0\text{ V}$, $V_{IC} = V_O = V_+/2$, $R_L > 1\text{ M}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A	LMV341			LMV344			UNIT
					MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
V _{IO}	Input offset voltage			25°C	0.25		4	0.25		4	mV
				Full range	4.5		4.5				
α _{VIO}	Average temperature coefficient of input offset voltage			Full range	1.9			1.9			μV/°C
I _{IB}	Input bias current			25°C	1	200		1	200		pA
				−40°C to 85°C	375		375				
				−40°C to 125°C	5		5		nA		
I _{IO}	Input offset current			25°C	6.6			6.6			fA
CMRR	Common-mode rejection ratio	0 ≤ V _{ICR} ≤ 4 V		25°C	46	86		56	86		dB
		0 ≤ V _{ICR} ≤ 3.9 V		Full range	47		50				
k _{SVR}	Supply-voltage rejection ratio	2.7 V ≤ V ₊ ≤ 5 V		25°C	45	82		65	82		dB
				Full range	44		60				
V _{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	0	−0.2 to 4.2	4	0	−0.2 to 4.2	4	V
A _V	Large-signal voltage gain ⁽²⁾	R _L = 10 kΩ to 2.5 V		25°C	78	116		78	116		dB
				Full range	70		70				
		R _L = 2 kΩ to 2.5 V		25°C	72	107		72	107		
				Full range	64		64				
V _O	Output swing (delta from supply rails)	R _L = 2 kΩ to 2.5 V	Low level	25°C	32	67		32	60		mV
				Full range		95		95			
			High level	25°C	34	60		34	60		
				Full range		95		95			
		R _L = 10 kΩ to 2.5 V	Low level	25°C	7	30		7	30		
				Full range		45		40			
			High level	25°C	7	30		7	30		
				Full range		40		40			
I _{CC}	Supply current (per channel)			25°C	107	200		107	200		μA
				Full range		260		260			
I _{OS}	Output short-circuit current	Sourcing		25°C	85	113		70	90		mA
		Sinking			50	75		50	75		
SR	Slew rate	R _L = 10 kΩ ⁽³⁾		25°C	1			1			V/μs
GBM	Unity-gain bandwidth	R _L = 10 kΩ, C _L = 200 pF		25°C	1			1			MHz
Φ _m	Phase margin	R _L = 100 kΩ		25°C	70			70			deg
G _m	Gain margin	R _L = 100 kΩ		25°C	20			20			dB
V _n	Equivalent input noise voltage	f = 1 kHz		25°C	39			39			nV/√Hz
I _n	Equivalent input noise current	f = 1 kHz		25°C	0.001			0.001			pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A _V = 1, R _L = 600 Ω, V _I = 1 V _{PP}		25°C	0.012			0.012			%

(1) Typical values represent the most likely parametric norm.

(2) $\text{GND} + 0.2\text{ V} \leq V_O \leq V_+ - 0.2\text{ V}$

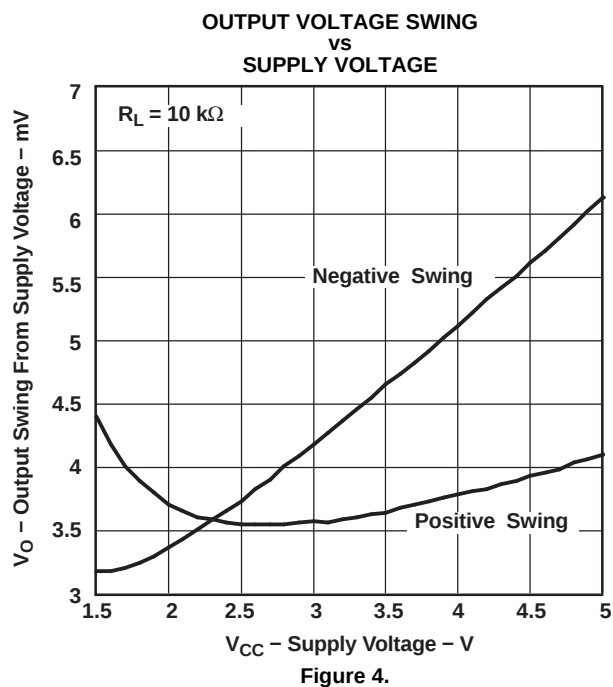
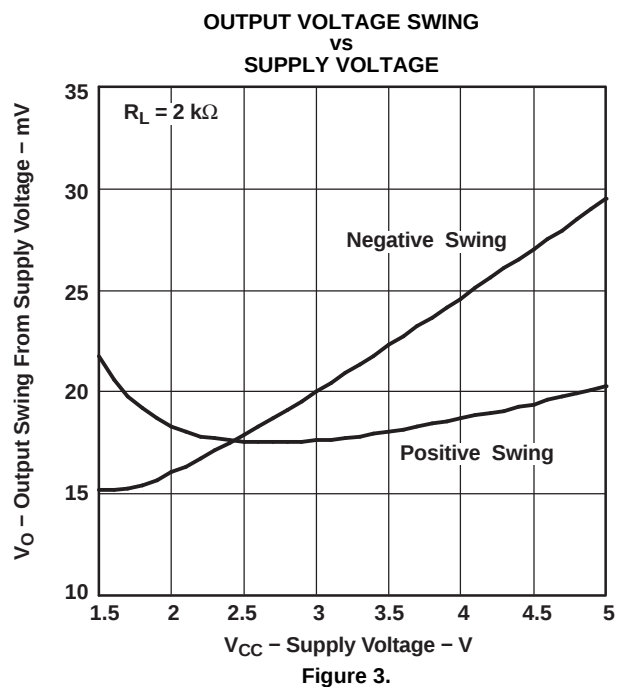
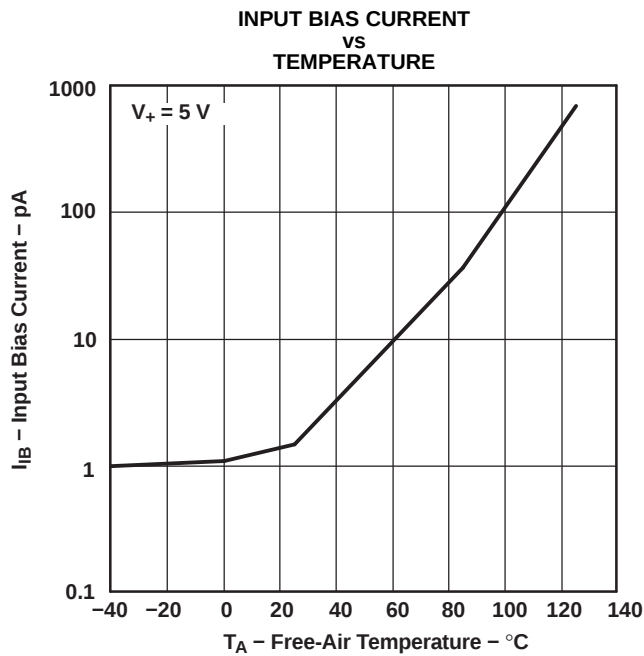
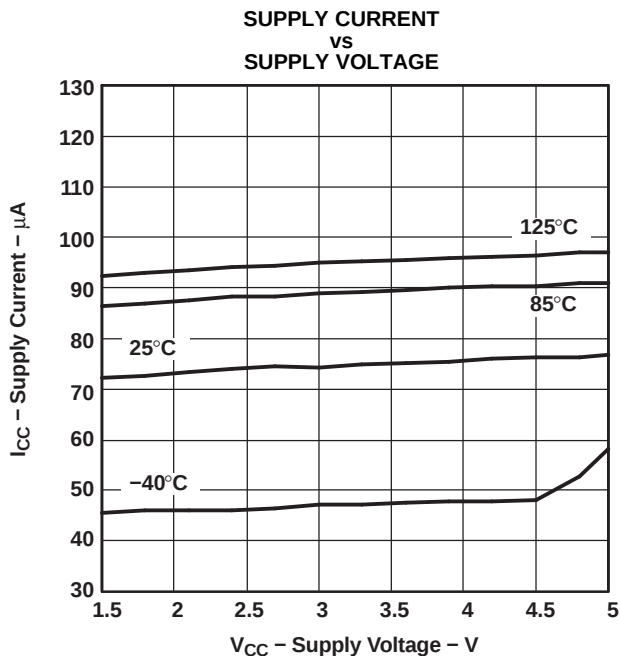
(3) Connected as voltage follower with 2- V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

SHUTDOWN CHARACTERISTICS

$V_+ = 5\text{ V}$, $GND = 0\text{ V}$, $V_{IC} = V_O = V_+/2$, $R_L > 1\text{ M}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode (per channel)	$V_{SD} = 0\text{ V}$	25°C		0.033	1	μA
			Full range			1.5	
$t_{(on)}$	Amplifier turn-on time		25°C		5		μs
V_{SD}	Shutdown pin voltage range	ON mode	25°C		3.1 to 5	4.5 to 5	V
		Shutdown mode			0 to 1	0 to 0.8	

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

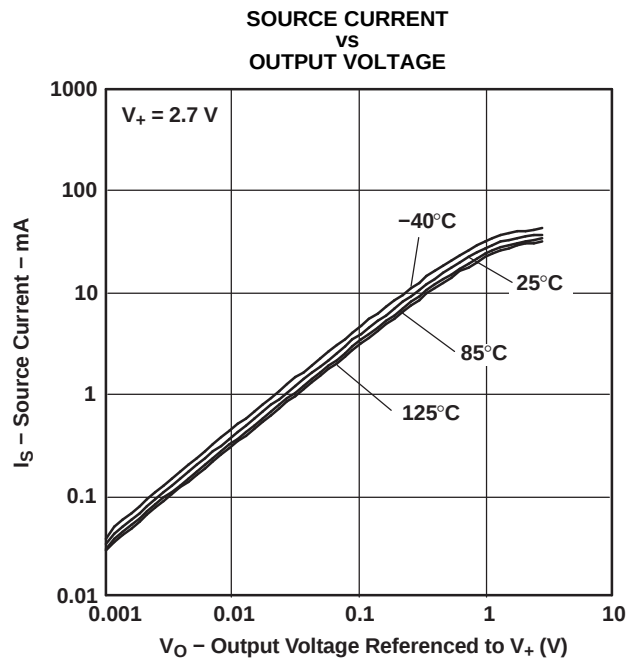


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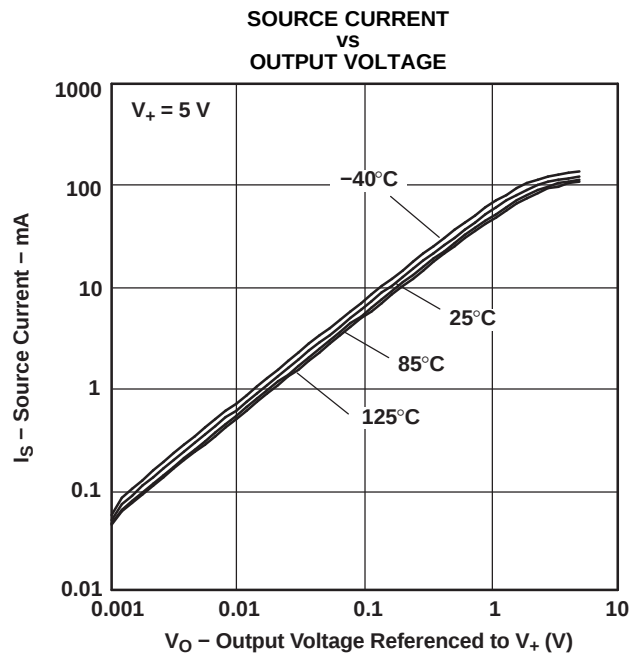


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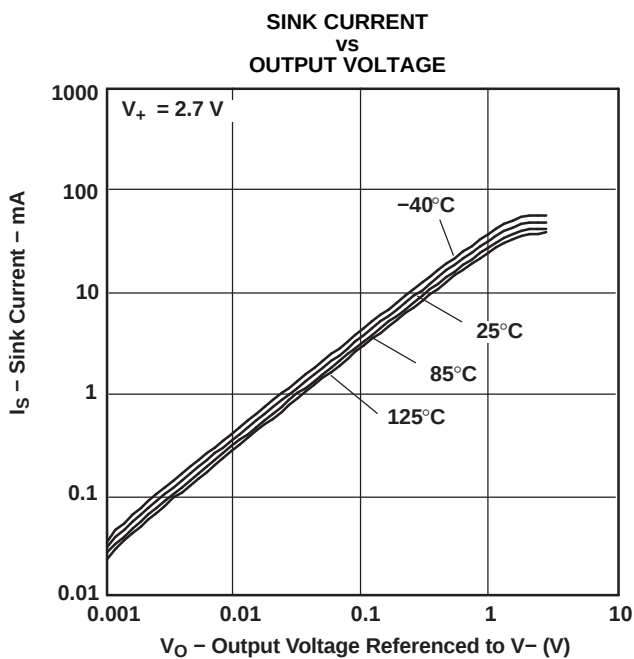


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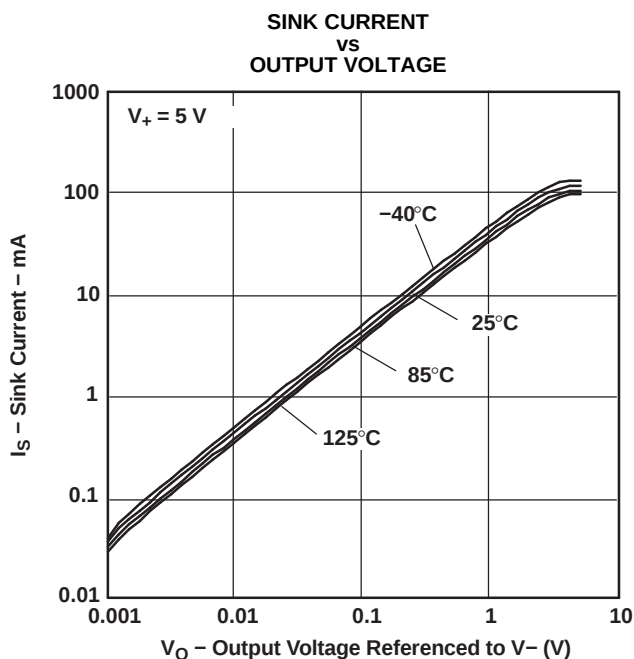


Figure 8.

TYPICAL CHARACTERISTICS (continued)

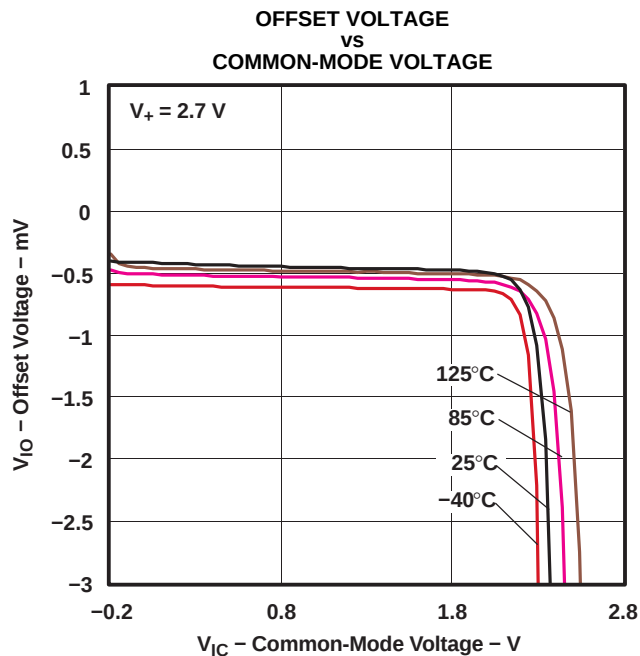


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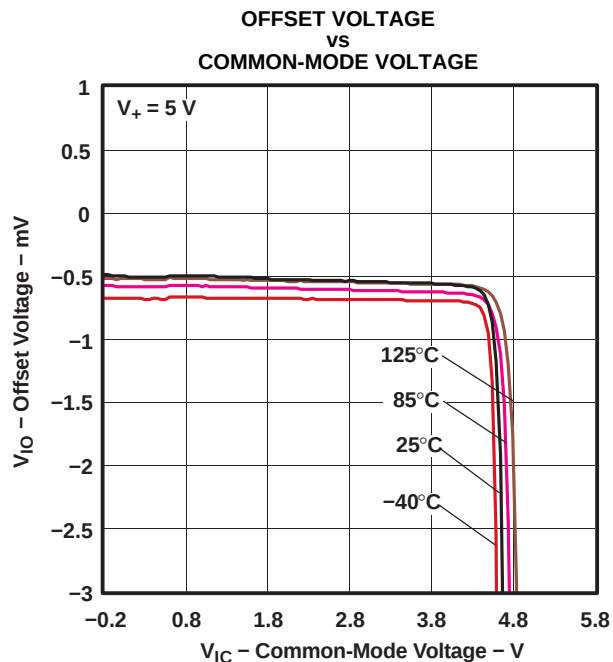


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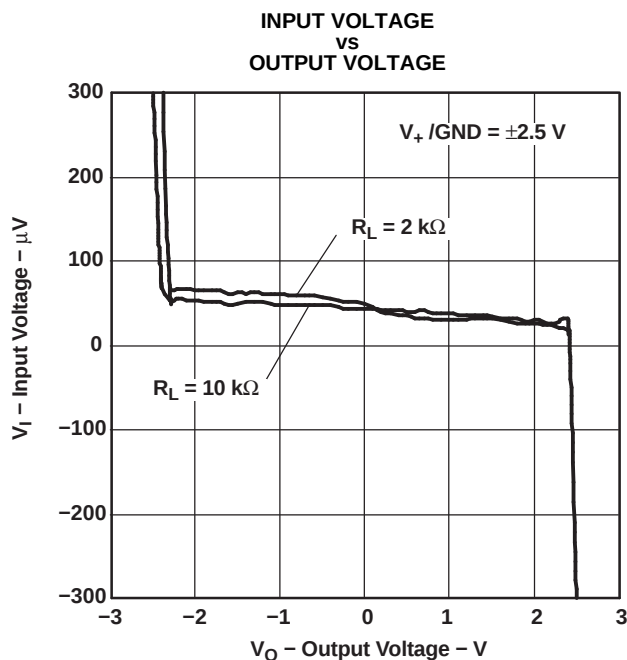


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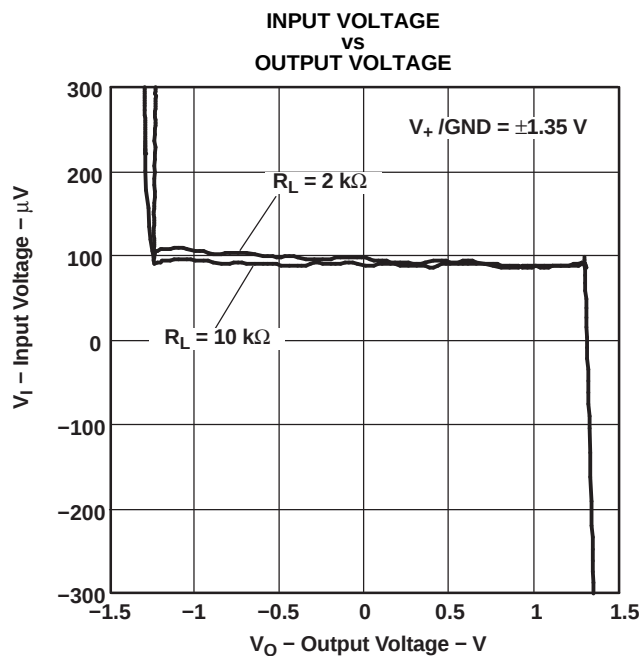


Figure 12.

TYPICAL CHARACTERISTICS (continued)

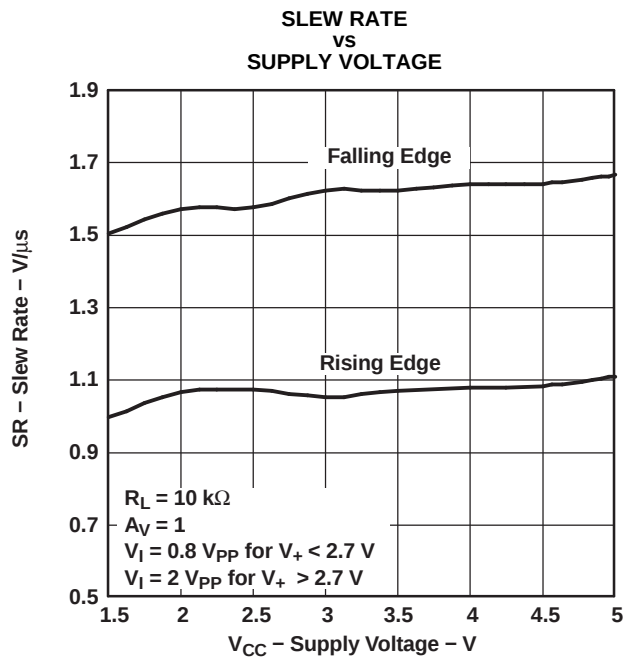


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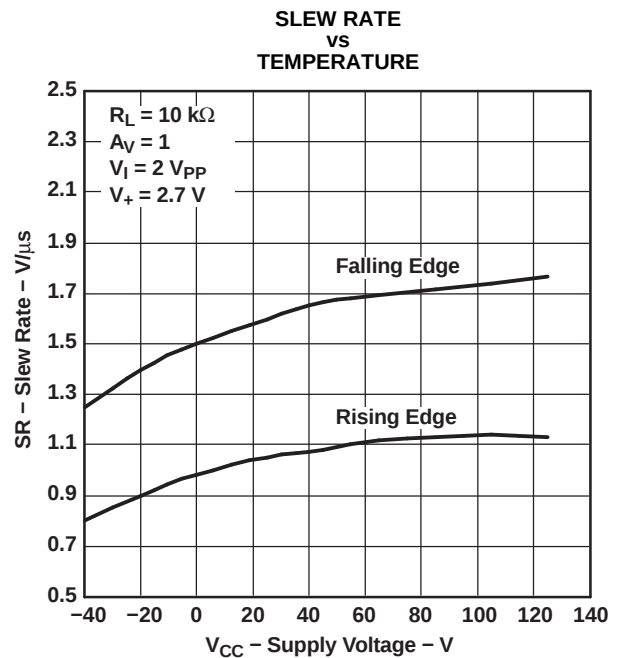


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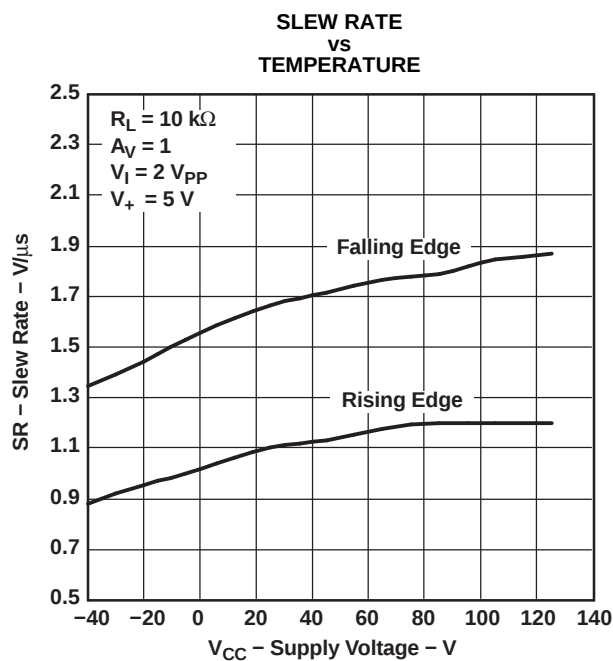


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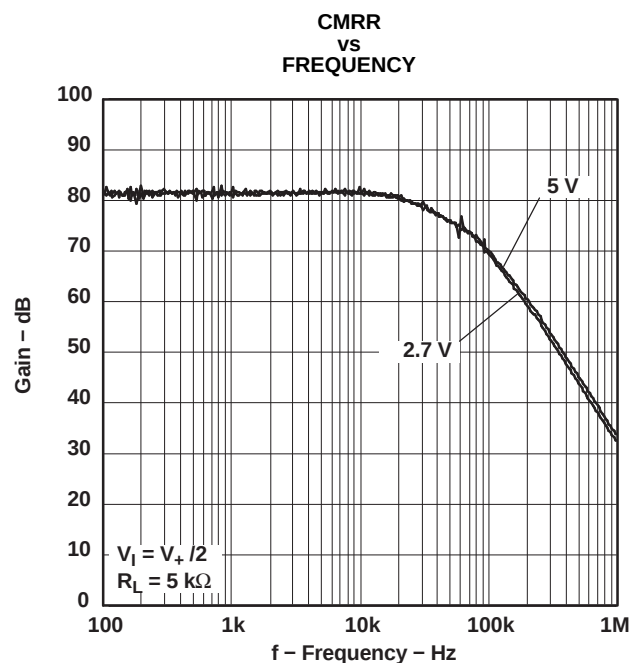


Figure 16.

TYPICAL CHARACTERISTICS (continued)

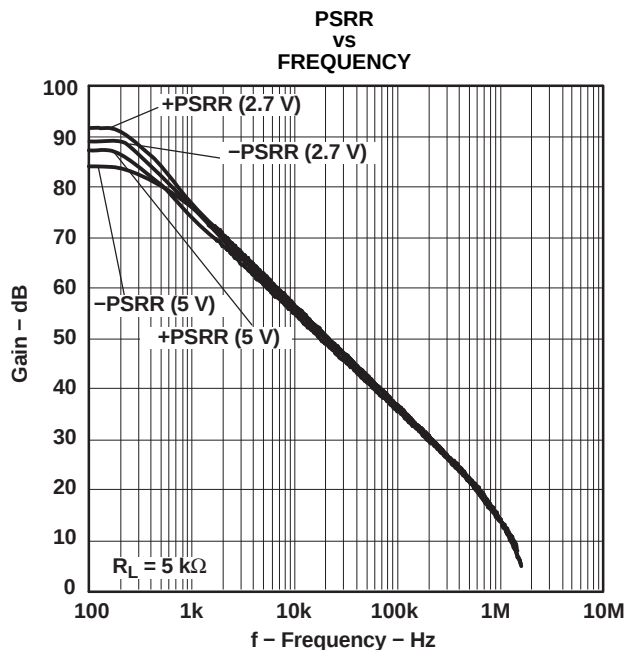


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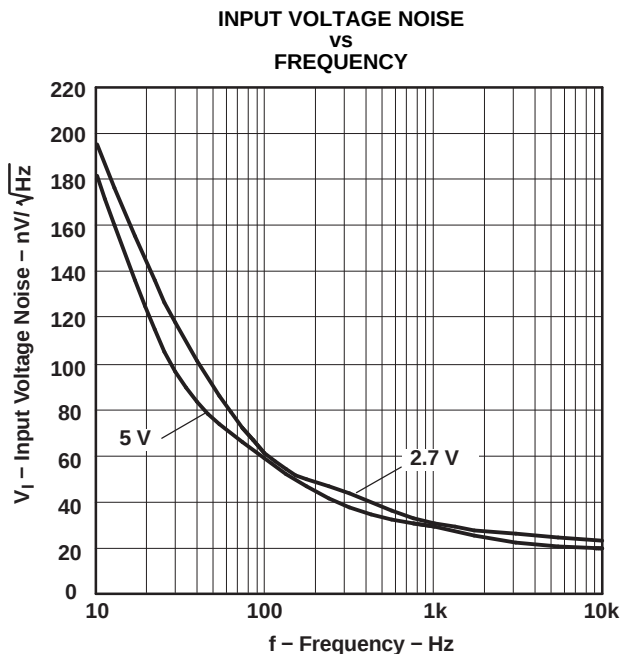


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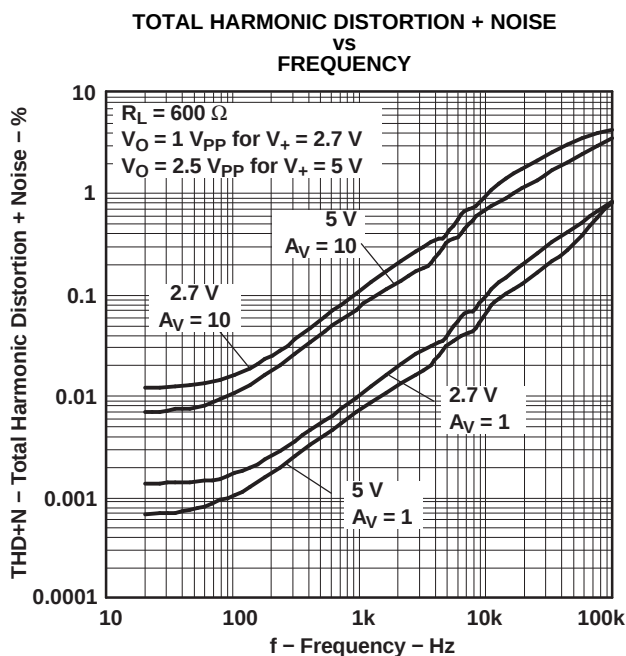


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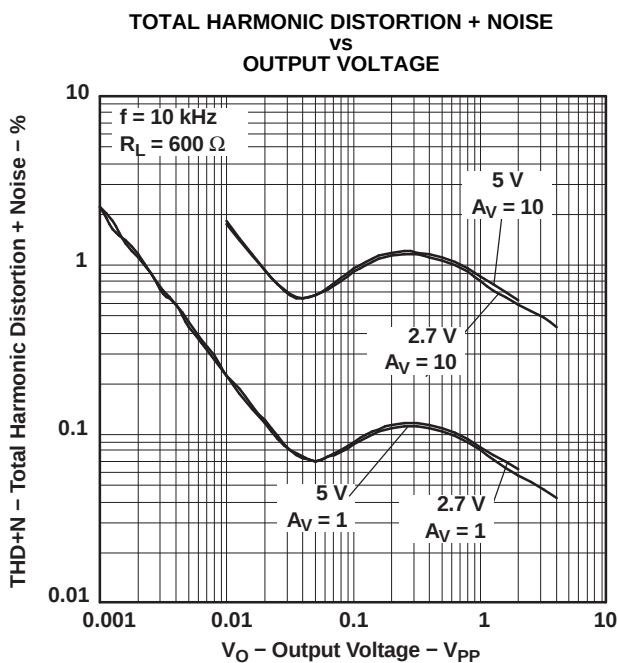
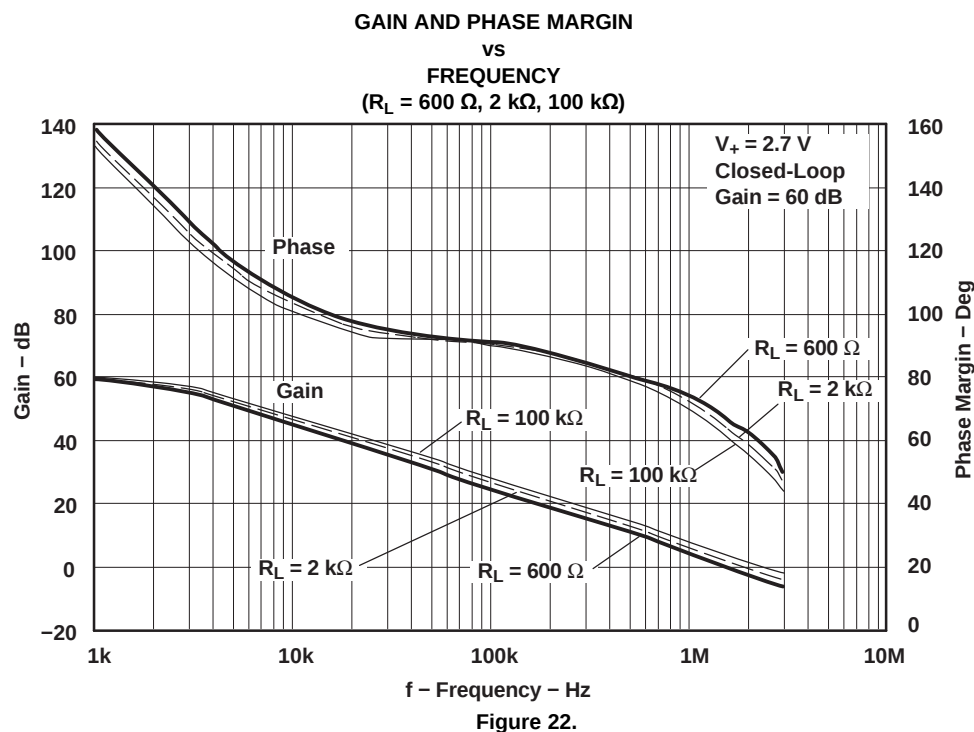
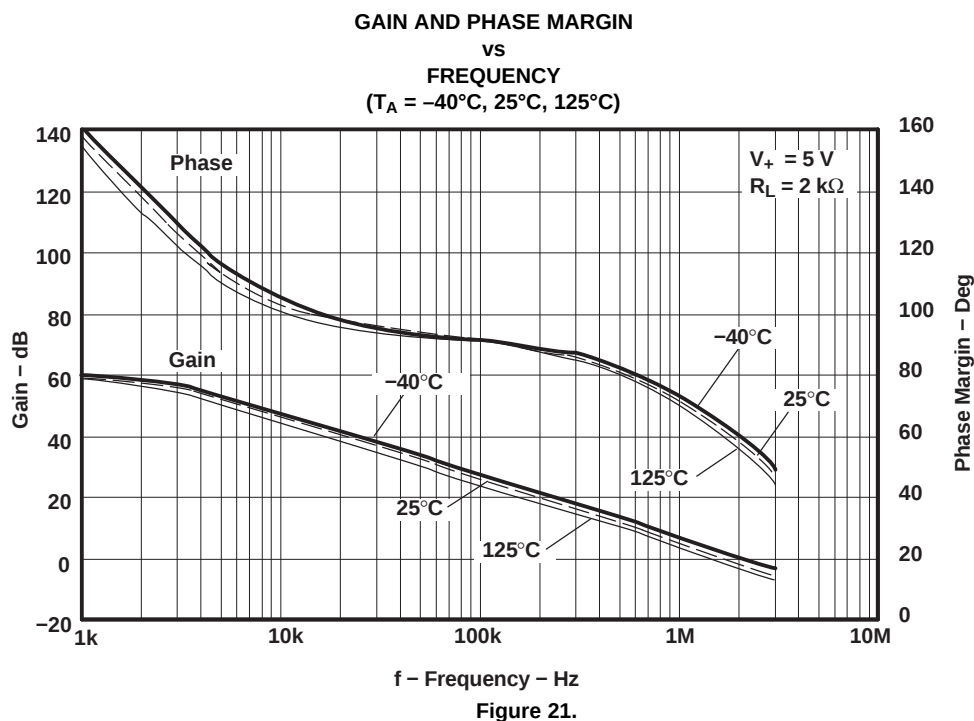


Figure 20.

TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

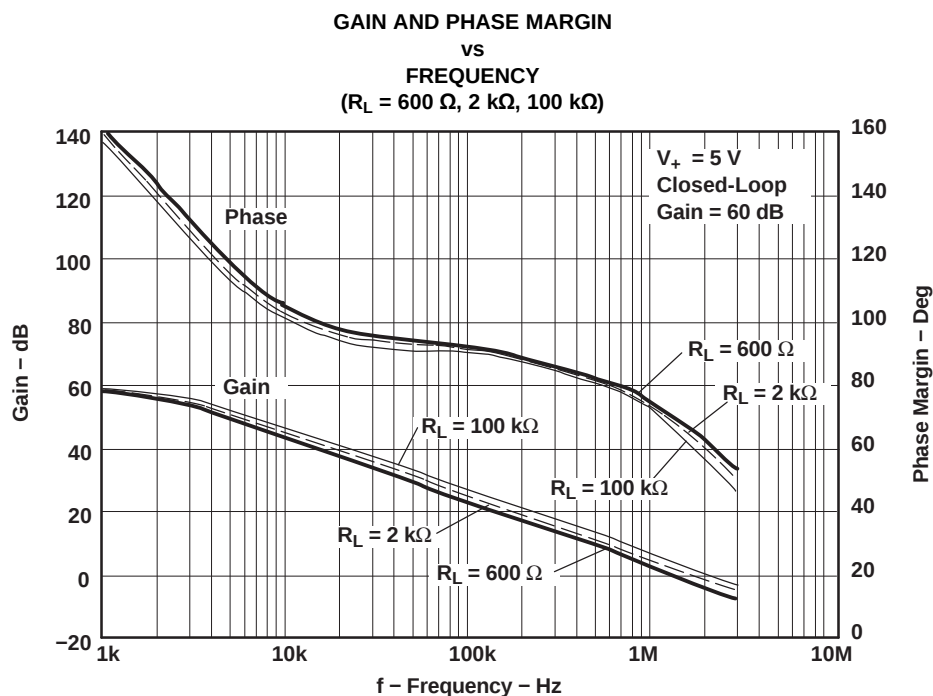


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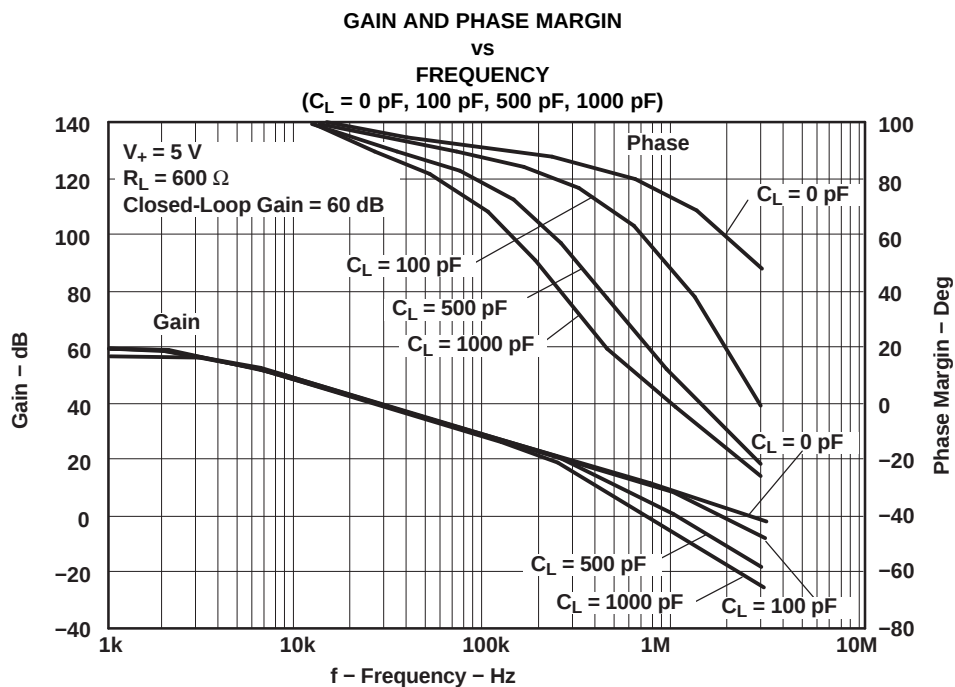


Figure 24.

TYPICAL CHARACTERISTICS (continued)

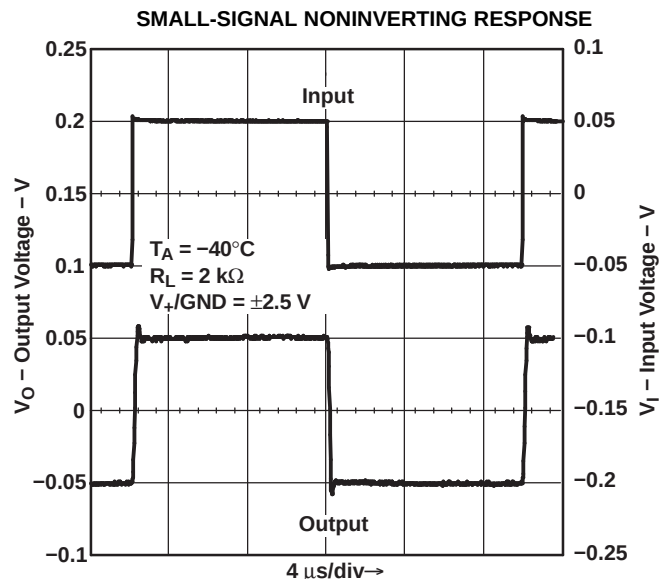


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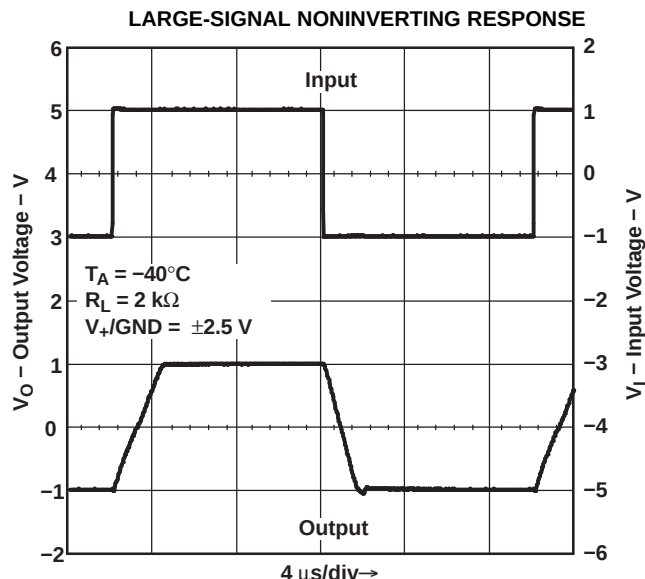


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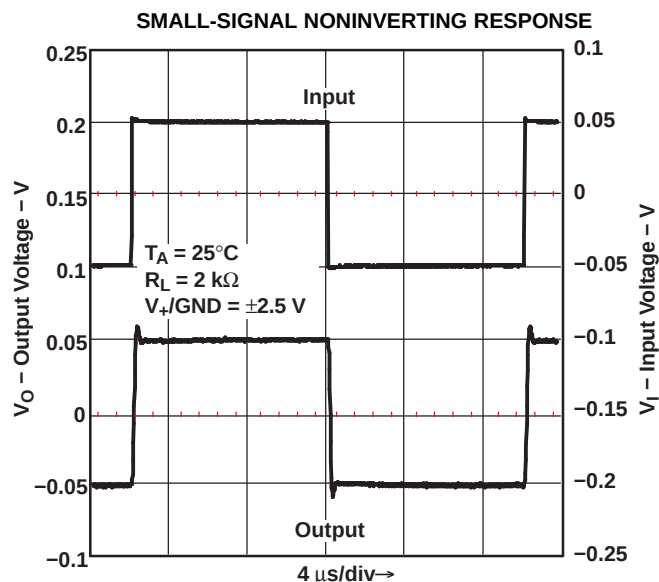


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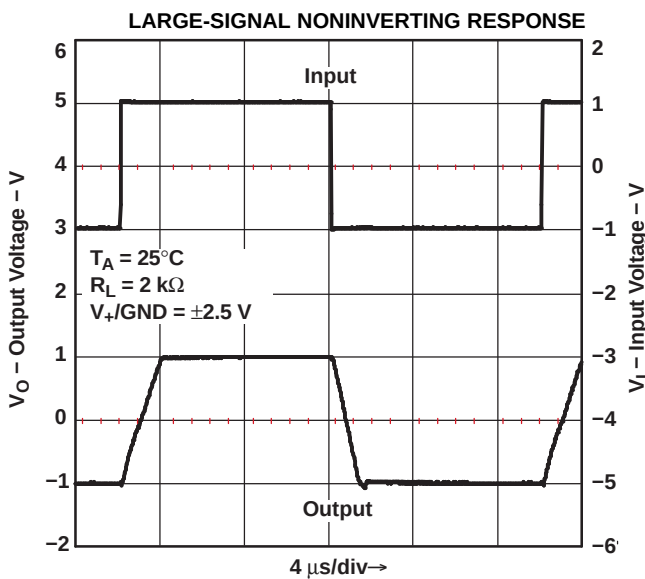


Figure 28.

TYPICAL CHARACTERISTICS (continued)

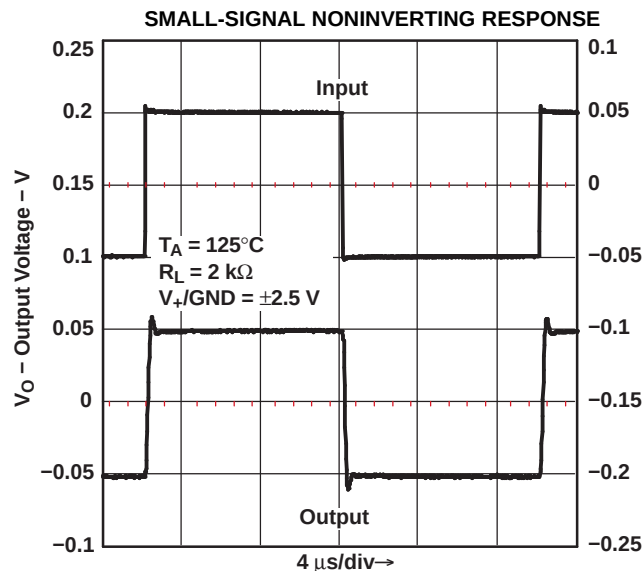


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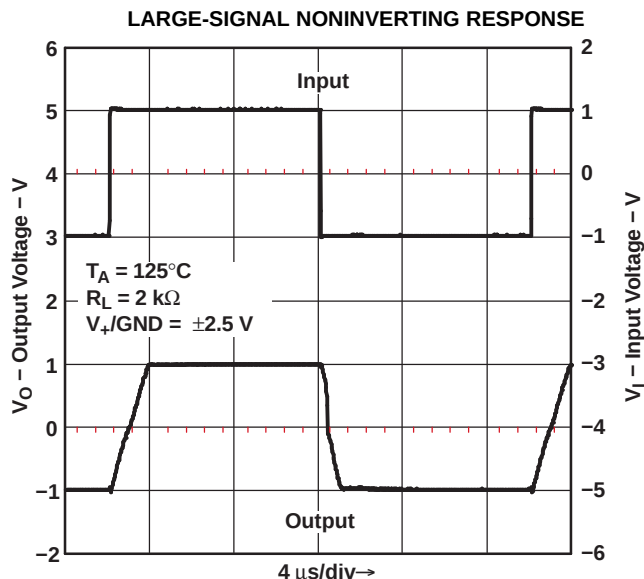


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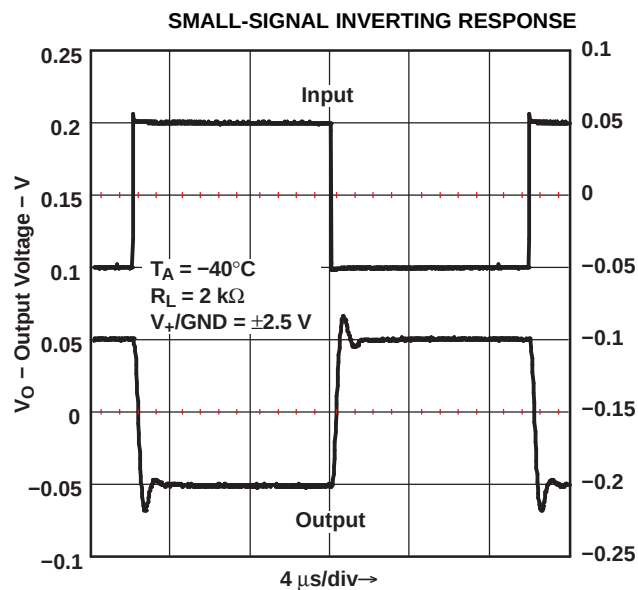


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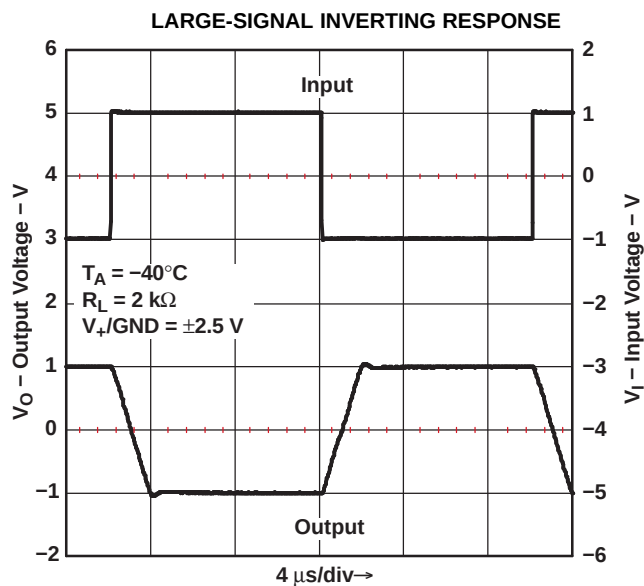


Figure 32.

TYPICAL CHARACTERISTICS (continued)

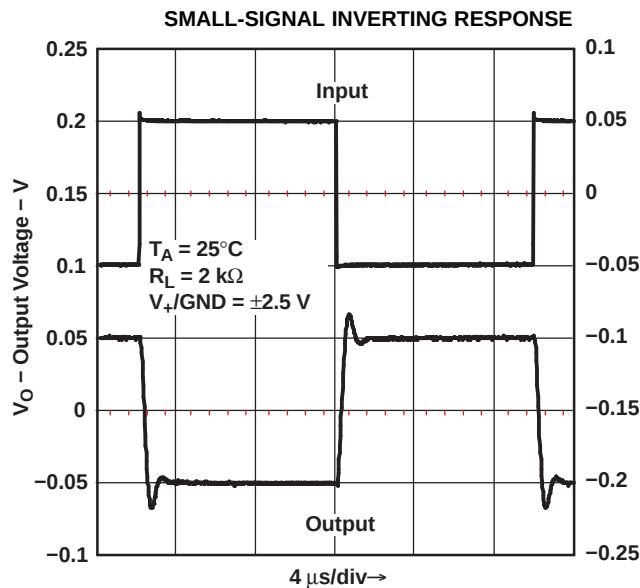


Figure 33.

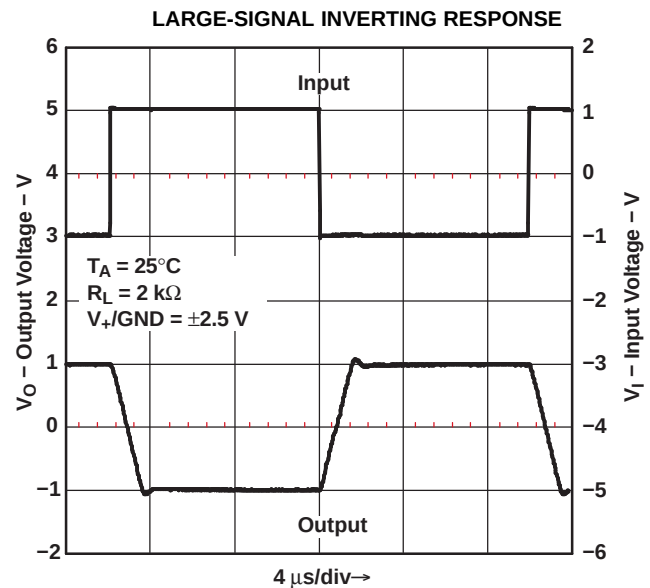


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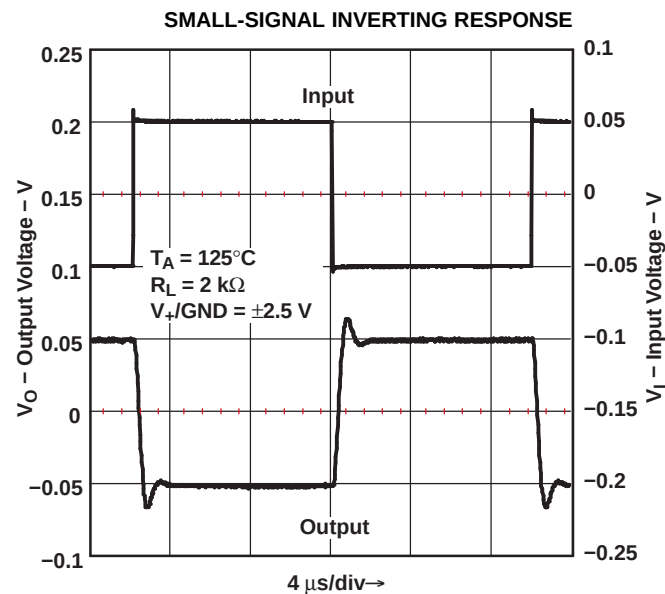


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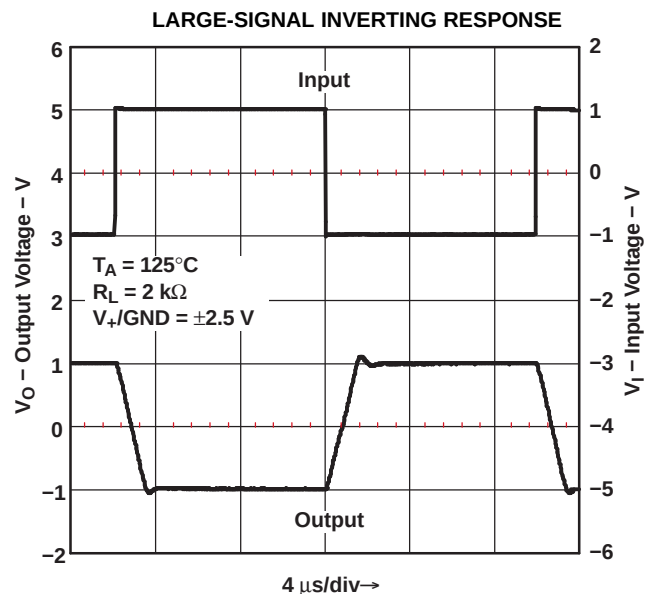


Figure 36.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
LMV341QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV341QDCKRQ1	ACTIVE	SC70	DK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV344IPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF LMV341-Q1, LMV344-Q1 :

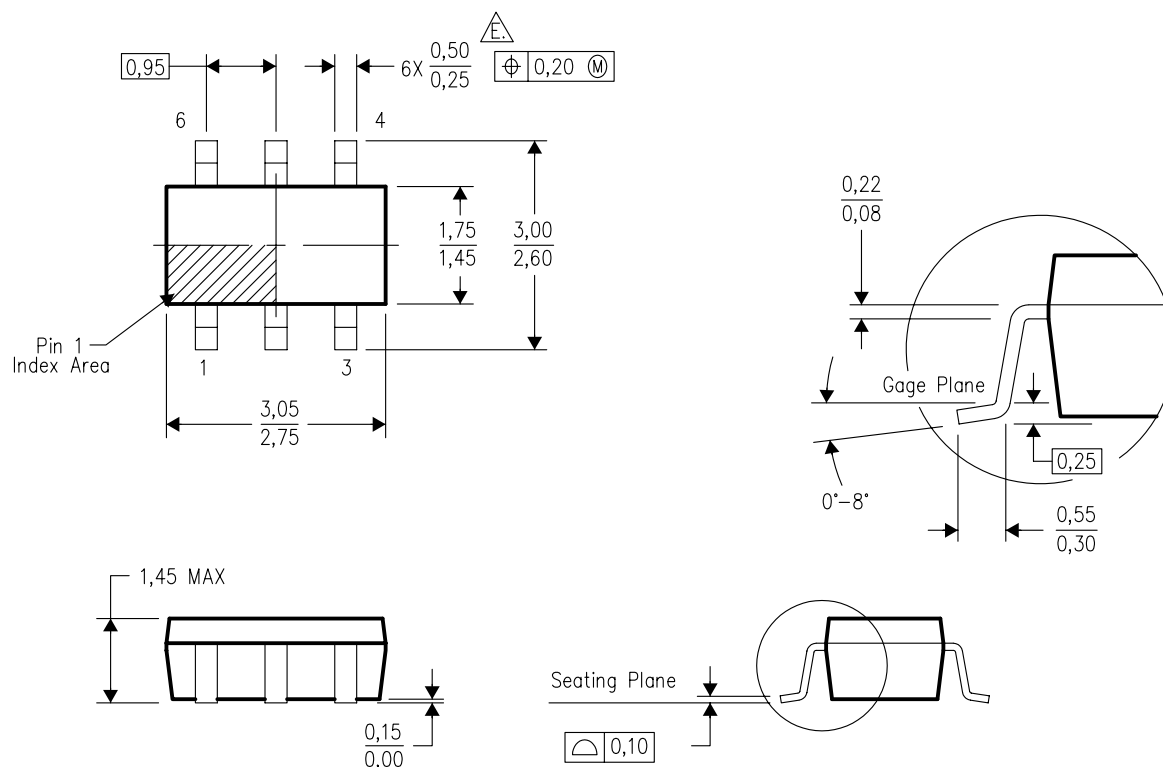
- Catalog: [LMV341](#), [LMV344](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

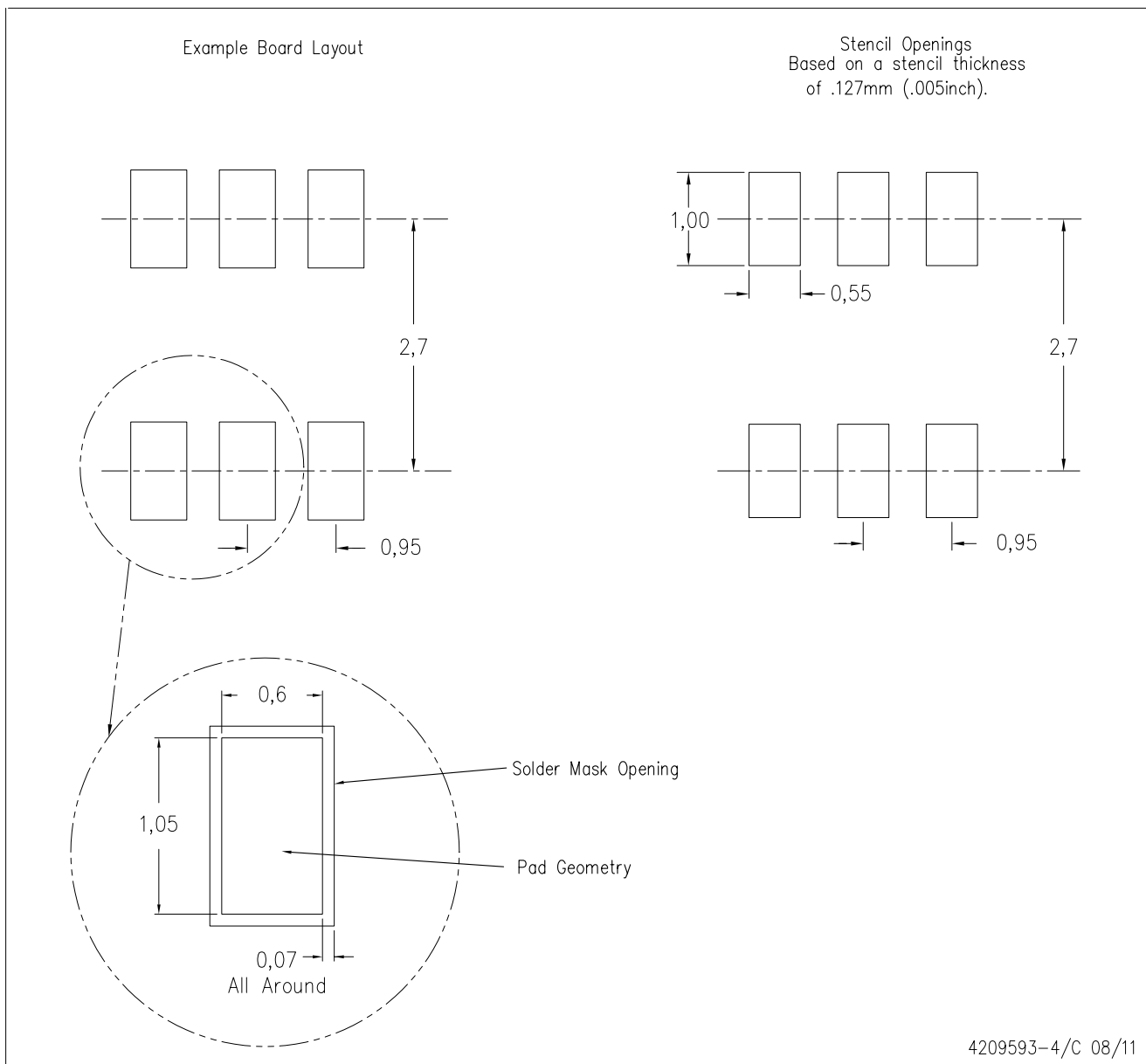


4073253-5/K 03/2006

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
-  Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

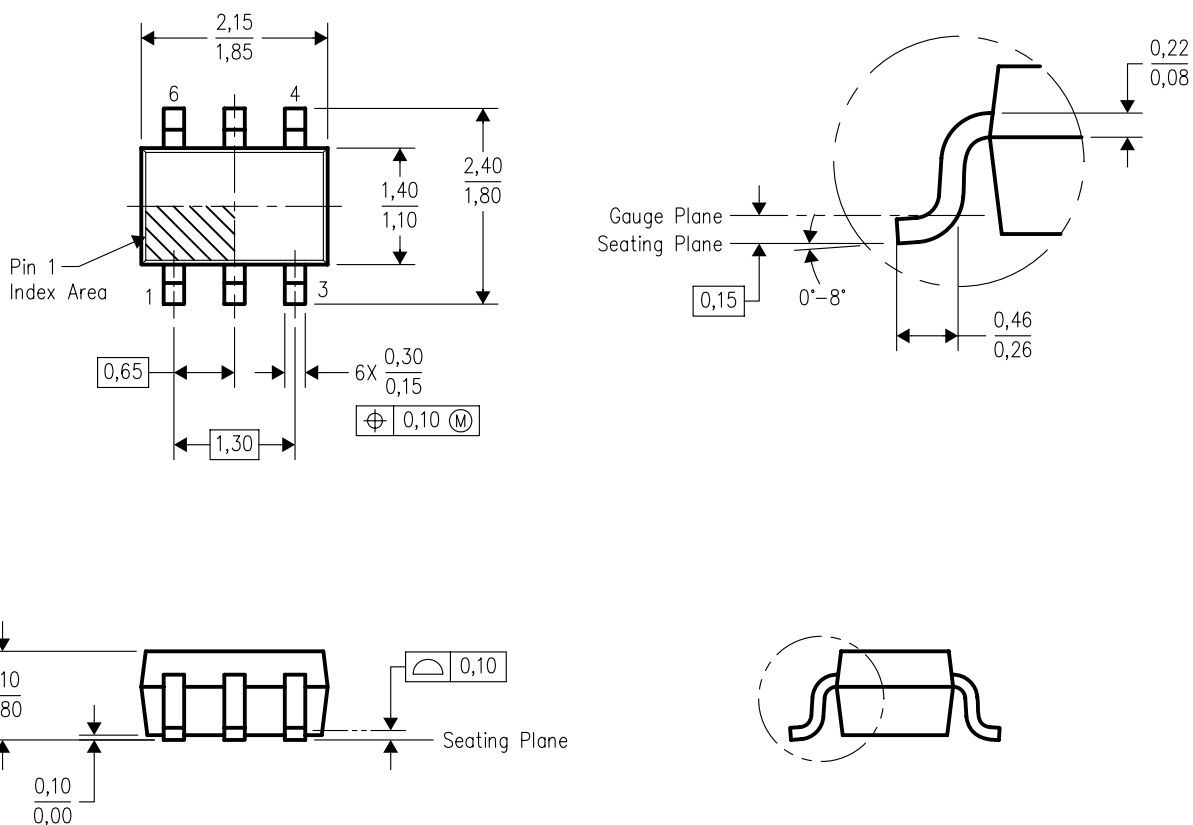
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

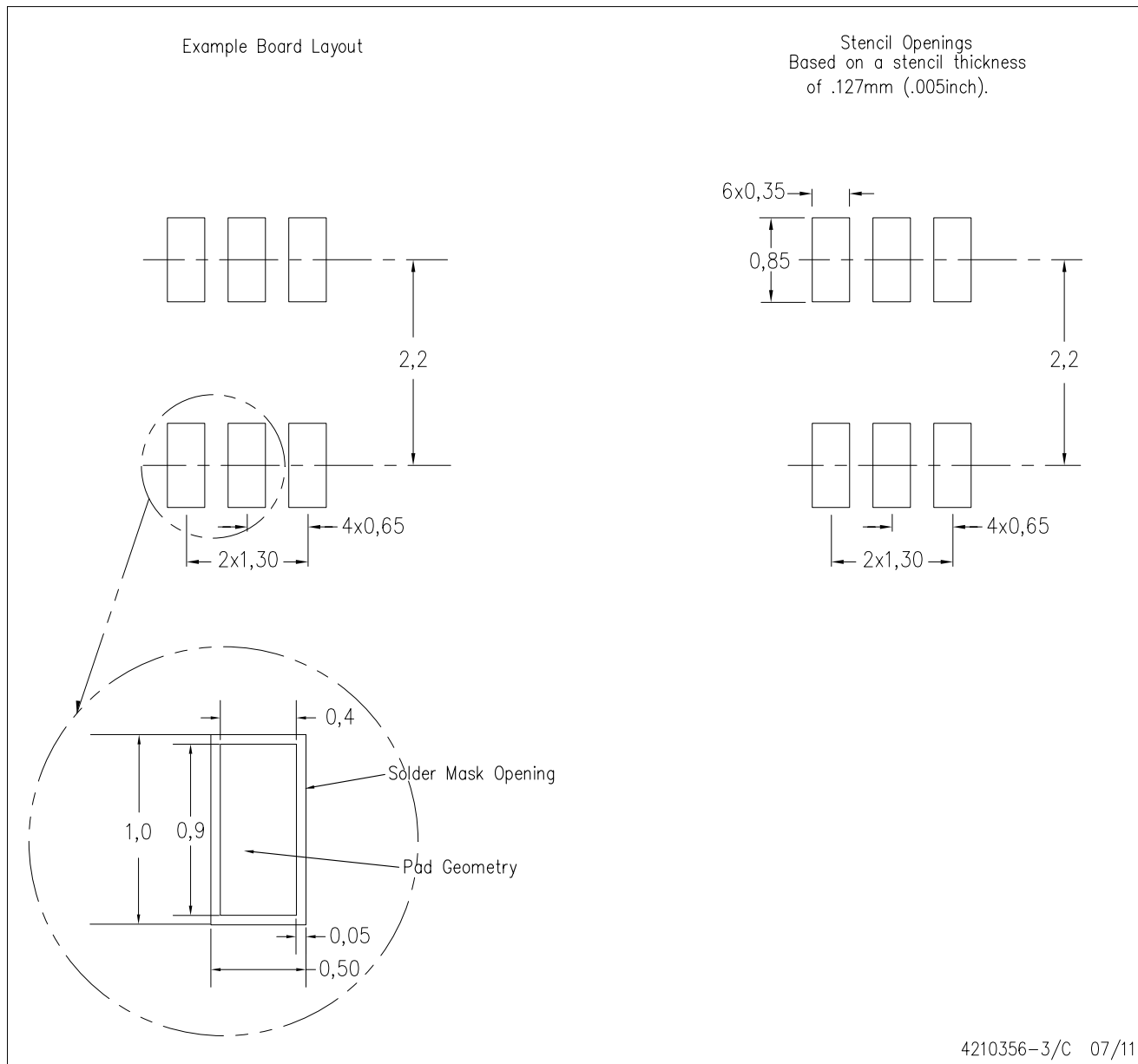


4093553-4/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

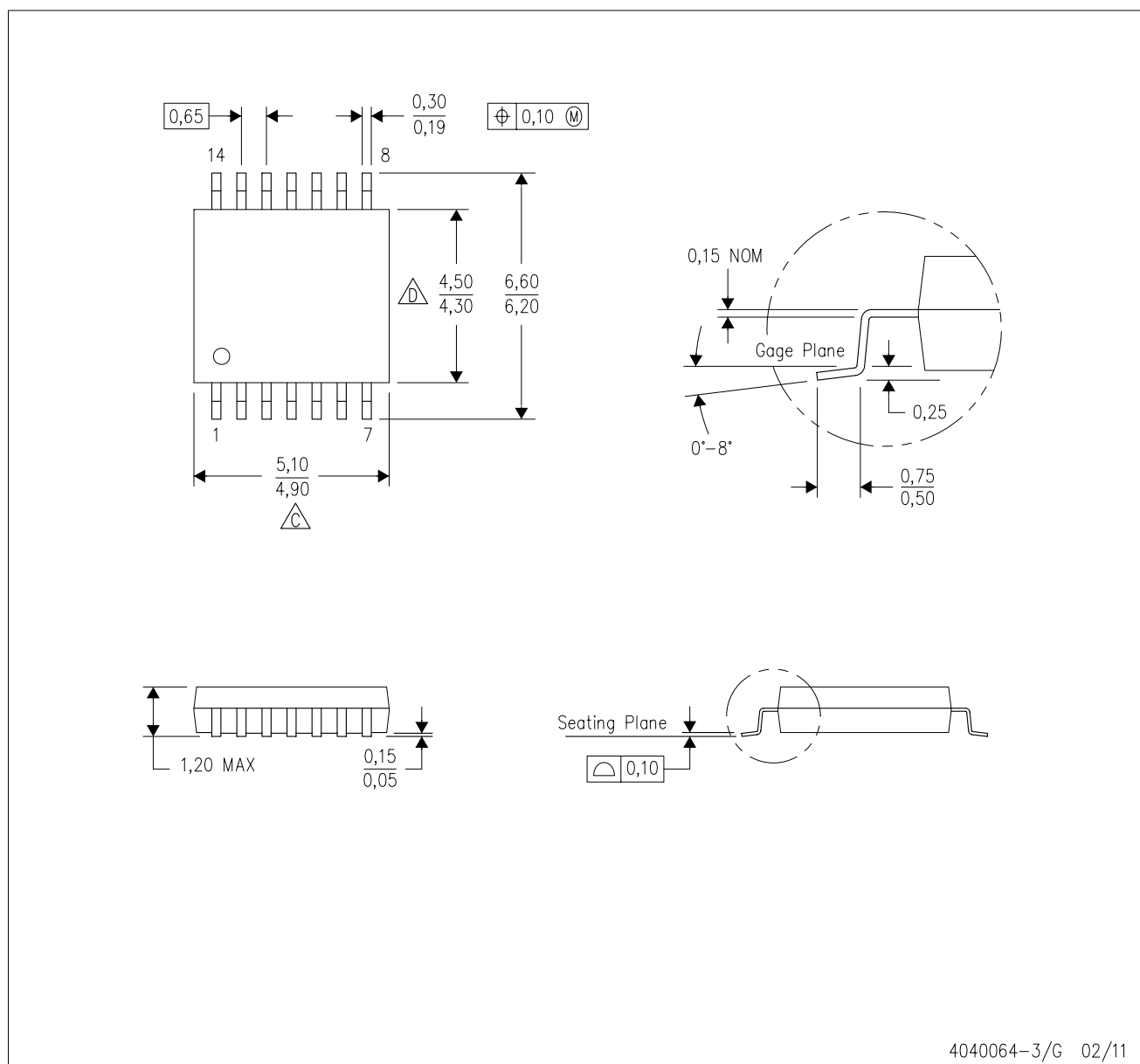
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

PW (R-PDSO-G14)

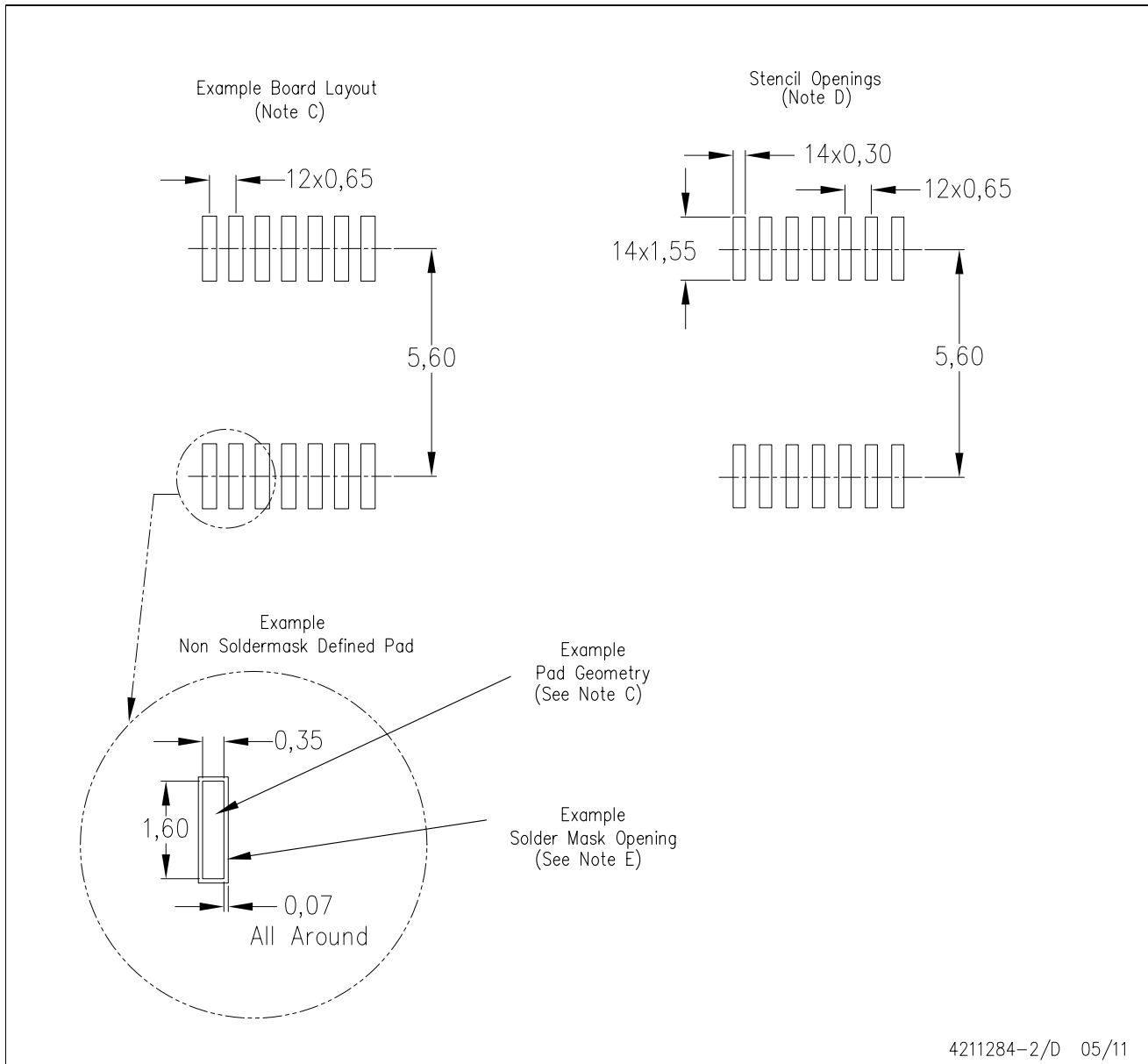
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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