LMK1C110x 1.8-V, 2.5-V, and 3.3-V LVCMOS Clock Buffer Family

1 Features

- High-performance 1:6 and 1:8 LVCMOS clock buffer
- Very low output skew < 55 ps
- Extremely low additive jitter < 25-fs nominal
  - 12-fs typical at V_{DD} = 3.3 V
  - 15-fs typical at V_{DD} = 2.5 V
  - 28-fs typical at V_{DD} = 1.8 V
- Very low propagation delay < 3 ns
- Synchronous output enable
- Supply voltage: 3.3 V, 2.5 V, or 1.8 V
  - 3.3-V tolerant input at all supply voltages
- Industry high ESD rating of 9000 V HBM
- f_{max} = 250 MHz for 3.3 V
  f_{max} = 200-MHz for 2.5 V and 1.8 V
- Operating temperature range: –40 °C to 125 °C
- Available in 14-pin and 16-pin TSSOP package

2 Applications

- Factory automation & control
- Telecommunications equipment
- Data center & enterprise computing
- Grid infrastructure
- Motor drives
- Medical imaging

3 Description

The LMK1C110x is a modular, high-performance, low-skew, general-purpose clock buffer family from Texas Instruments.

The entire family is designed with a modular approach in mind. Five different fan-out variations, 1:2, 1:3, 1:4, 1:6 and 1:8 are available.

All of the devices within this family are pin-compatible to each other and backwards compatible to the CDCLVC110x family for easy handling.

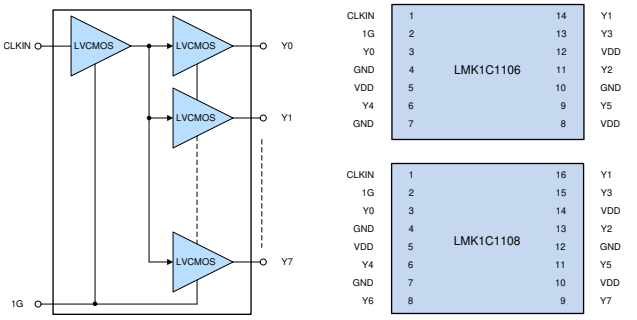
All family members share the same high performing characteristics such as low additive jitter, low skew, and wide operating temperature range.

The LMK1C110x supports a synchronous output enable control (1G) which switches the outputs into a low state when 1G is low.

The LMK1C110x family operates in a 1.8-V, 2.5-V and 3.3-V environment and are characterized for operation from – 40 °C to 125 °C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMK1C1106	TSSOP (14)	5.00 mm x 4.40 mm
LMK1C1108	TSSOP (16)	5.00 mm x 4.40 mm



Functional Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2020	*	Initial Release

5 Pin Configuration and Functions

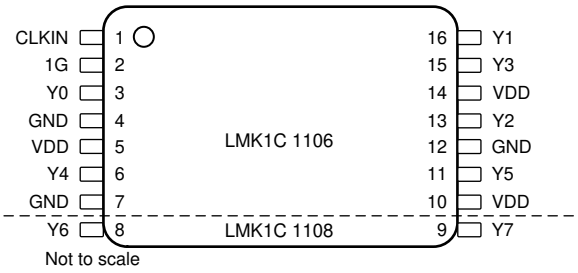


Figure 5-1. LMK1C1106 and LMK1C1108 PW Package 14-Pin TSSOP and 16-Pin TSSOP Top View

Table 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	LMK1C 1106	LMK1C 1108		
LVCMOS CLOCK INPUT				
CLKIN	1	1	Input	Single-ended clock input with internal 300-kΩ (typical) pulldown resistor to GND. Typically connected to a single-ended clock input.
CLOCK OUTPUT ENABLE				
1G	2	2	Input	Global Output Enable with internal 300k-Ohm (typ) pulldown resistor to GND. Typically connected to VDD with external pullup resistor. HIGH: outputs enabled LOW: outputs disabled
LVCMOS CLOCK OUTPUT				
Y0	3	3	Output	LVCMOS output. Typically connected to a receiver. Unused outputs can be left floating.
Y1	14	16		
Y2	11	13		
Y3	13	15		
Y4	6	6		
Y5	9	11		
Y6	–	8		
Y7	–	9		
SUPPLY VOLTAGE				
VDD	5	5	Power	Power supply terminal. Typically connected to a 3.3-V, 2.5-V, or 1.8-V supply. The VDD pin is typically connected to an external 0.1-µF capacitor near the pin.
	8	10		
	12	14		
GROUND				
GND	4	4	GND	Device ground.
	7	7		
	10	12		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.5	3.6	V
V_{CLKIN}	Input voltage (CLKIN)			
V_{IN}	Input voltage (1G)			
V_{Yn}	Output pins (Yn)	–0.5	V_{DD} + 0.3	
I_{IN}	Input current	–20	20	mA
I_O	Continuous output current	–50	50	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±9000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Core supply voltage	3.3-V supply	3.135	3.3	3.465	V
		2.5-V supply	2.375	2.5	2.625	
		1.8-V supply	1.71	1.8	1.89	
T_A	Operating free-air temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMK1C1106 PW (TSSOP) 14 PINS	LMK1C1108 PW(TSSOP) 16 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	114.4	123.4	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	45.2	53.1	°C/W
R_{qJB}	Junction-to-board thermal resistance	60.6	66.4	°C/W
Y_{JT}	Junction-to-top characterization parameter	5.9	8.9	°C/W
Y_{JB}	Junction-to-board characterization parameter	60	65.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

VDD = 3.3 V ± 5 %, –40°C ≤ TA ≤ 125°C. Typical values are at VDD = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION						
I_{DD}	Core supply current, static	All-outputs disabled, f_{IN} = 0 V		25	45	µA
I_{DD}	Core supply current	All-outputs disabled, f_{IN} = 100 MHz, V_{DD} = 1.8 V		2	6	mA
I_{DD}	Core supply current	All-outputs disabled, f_{IN} = 100 MHz, V_{DD} = 2.5 V		6.5	10	mA
I_{DD}	Core supply current	All-outputs disabled, f_{IN} = 100 MHz, V_{DD} = 3.3 V		15	21	mA
I_{DD}	Output current	Per output, f_{IN} = 100 MHz, C_L = 5pF, V_{DD} = 1.8 V		3.2	3.5	
		Per output, f_{IN} = 100 MHz, C_L = 5pF, V_{DD} = 2.5 V		4.6	5.5	
		Per output, f_{IN} = 100 MHz, C_L = 5pF, V_{DD} = 3.3 V		6	7	
CLOCK INPUT						
f_{IN_SE}	Input frequency	V_{DD} = 3.3 V	DC		250	MHz
		V_{DD} = 2.5 V and 1.8 V	DC		200	
V_{IH}	Input high voltage		0.7 x V_{DD}			V
V_{IL}	Input low voltage				0.3 x V_{DD}	
dV_{IN}/dt	Input slew rate	20% - 80% of input swing	0.1			V/ns
I_{IN_LEAK}	Input leakage current		–50		50	uA
C_{IN_SE}	Input capacitance	at 25°C		7		pF
CLOCK OUTPUT FOR ALL V_{DD} LEVELS						
f_{OUT}	Output frequency	V_{DD} = 3.3 V			250	MHz
		V_{DD} = 2.5 V and 1.8 V			200	
ODC	Output duty cycle	With 50% duty cycle input	45		55	%
t_{1G_ON}	Output enable time	See (1)			5	cycles
t_{1G_OFF}	Output disable time	See (2)			5	cycles
CLOCK OUTPUT FOR V_{DD} = 3.3 V ± 5%						
V_{OH}	Output high voltage	I_{OH} = 1 mA	2.8			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.2	
$t_{RISE-FALL}$	Output rise and fall time	20/80%, C_L= 5 pF, fIN = 156.25 MHz		0.3	0.7	ns
$t_{OUTPUT-SKEW}$	Output-output skew	See (3)		35	55	ps
$t_{PART-SKEW}$	Part-to-part skew				950	
$t_{PROP-DELAY}$	Propagation delay	See (4)		1.3	2.2	ns
$t_{JITTER-ADD}$	Additive Jitter	f_{IN} = 156.25 MHz, Input slew rate = 1.6 V/ns, Integration range = 12 kHz - 20 MHz		12	20	fs, RMS
R_{OUT}	Output impedance			50		Ω
CLOCK OUTPUT FOR V_{DD} = 2.5 V ± 5%						
V_{OH}	Output high voltage	I_{OH} = 1 mA	0.8 x V_{DD}			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.2 x V_{DD}	
$t_{RISE-FALL}$	Output rise and fall time	20/80%, C_L= 5 pF, f_{IN} = 156.25 MHz		0.33	0.8	ns
$t_{OUTPUT-SKEW}$	Output-output skew	See (3)			55	ps
$t_{PART-SKEW}$	Part-to-part skew				450	
$t_{PROP-DELAY}$	Propagation delay	See (4)		1.5	2.5	ns

VDD = 3.3 V ± 5 %, –40°C ≤ TA ≤ 125°C. Typical values are at VDD = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{JITTER-ADD}$	Additive Jitter	f_{IN} = 156.25 MHz, Input slew rate = 1.2 V/ns, Integration range = 12 kHz - 20 MHz		15	27	fs, RMS
R_{OUT}	Output impedance			55		Ω
CLOCK OUTPUT FOR V_{DD} = 1.8 V ± 5%						
V_{OH}	Output high voltage	I_{OH} = 1 mA	0.8 x V_{DD}			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.2 x V_{DD}	V
$t_{RISE-FALL}$	Output rise and fall time	20/80%, C_L= 5 pF, f_{IN} = 156.25 MHz		0.38	1	ns
$t_{OUTPUT-SKEW}$	Output-output skew	See (3)			55	ps
$t_{PART-SKEW}$	Part-to-part skew				930	ps
$t_{PROP-DELAY}$	Propagation delay	See (4)		1.5	3	ns
$t_{JITTER-ADD}$	Additive Jitter	f_{IN} = 156.25 MHz, Input slew rate = 1.2 V/ns, Integration range = 12 kHz - 20 MHz		28	60	fs, RMS
R_{OUT}	Output impedance			64		Ω
GENERAL PURPOSE INPUT (1G)						
V_{IH}	High-level input voltage		0.75 x V_{DD}			V
V_{IL}	Low-level input voltage				0.25 x V_{DD}	V
I_{IH}	Input high-level current	V_{IH} = V_{DD_REF}	–50		50	µA
I_{IL}	Input low-level current	V_{IL} = GND	–50		50	µA

(1) Measured from 1G rising edge crossing VIH to first rising edge of Yn.
(2) Measured from 1G falling edge crossing VIL to last falling edge of Yn.
(3) Measured from rising edge of any Yn output to any other Ym output.
(4) Measured from rising edge of CLKIN to any Yn output.

6.6 Timing Requirements

VDD = 3.3 V ± 5 %, –40°C ≤ TA ≤ 125°C

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
V/t_{RAMP}	V_{DD} ramp rate		0.1		50	V/ms

6.7 Typical Characteristics

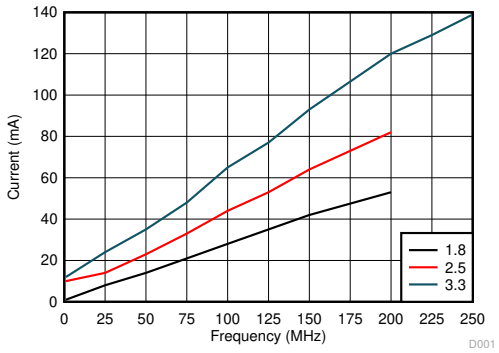


Figure 6-1. Device Power Consumption vs Clock Frequency (Load 5 pF)

7 Parameter Measurement Information

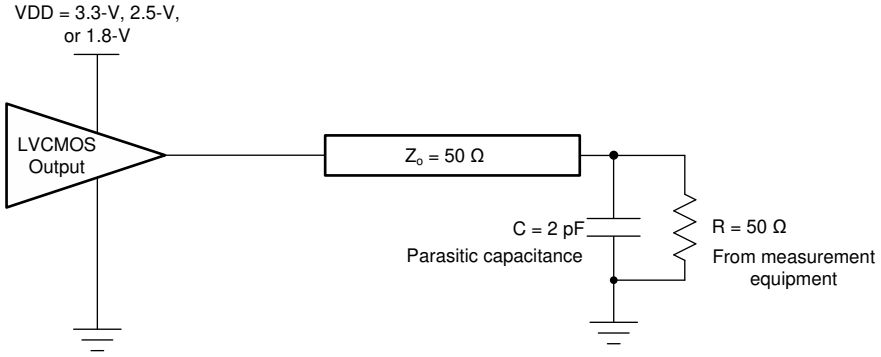


Figure 7-1. Test Load Circuit

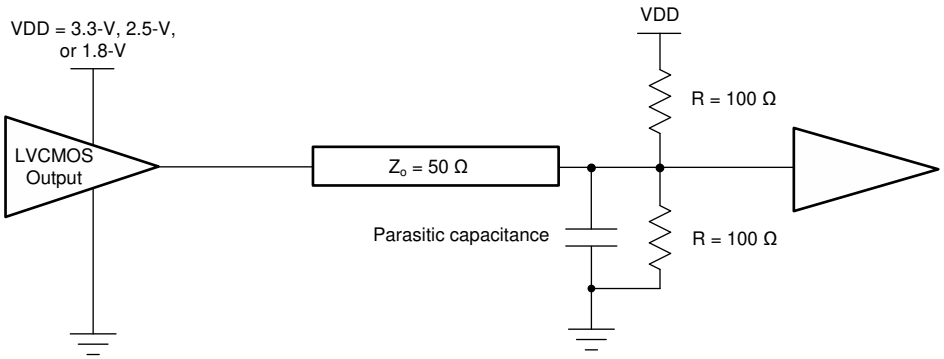


Figure 7-2. Application Load With 50-Ω Termination

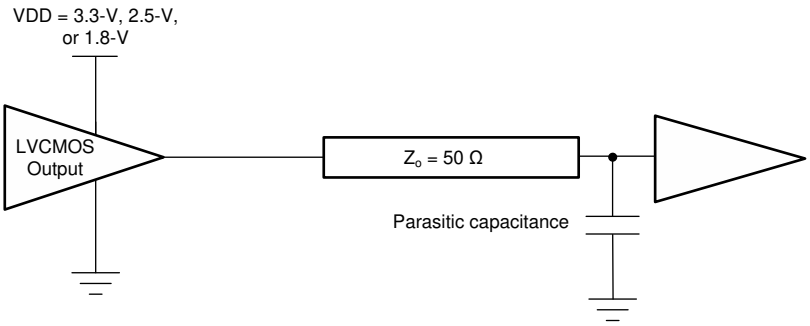


Figure 7-3. Application Load With Termination

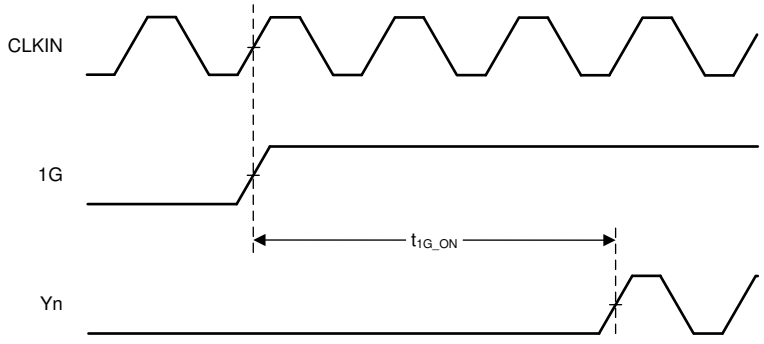


Figure 7-4. t_{1G_ON} Output Enable Time

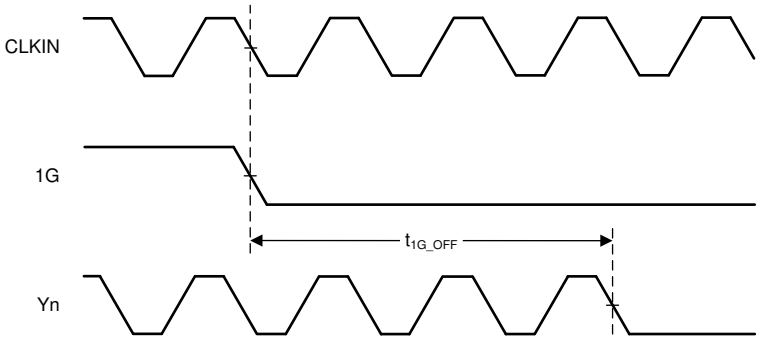


Figure 7-5. t_{1G_OFF} Output Disable Time

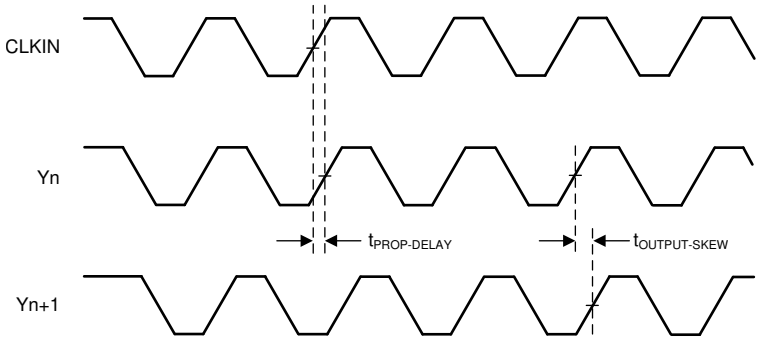


Figure 7-6. Propagation Delay $t_{PROP-DELAY}$ and Output Skew $t_{OUTPUT-SKEW}$

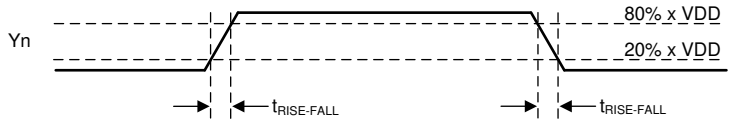


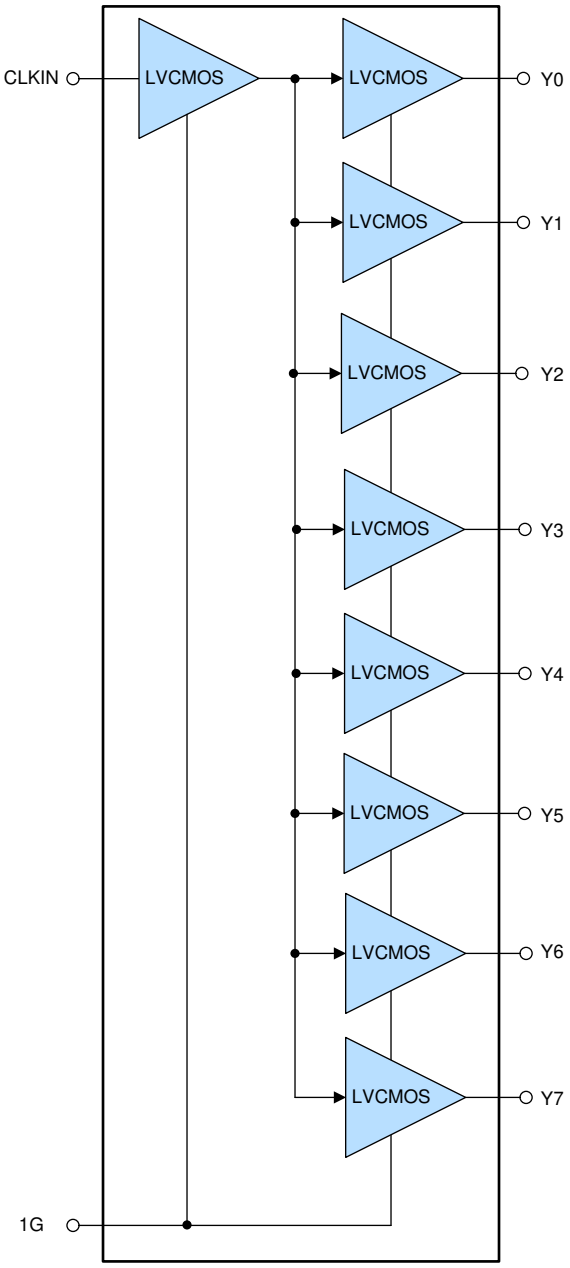
Figure 7-7. Rise and Fall Time $t_{RISE-FALL}$

8 Detailed Description

8.1 Overview

The LMK1C110x family of devices is part of a low-jitter and low-skew LVCMOS fan-out buffer solution. For best signal integrity, it is important to match the characteristic impedance of the LMK1C110x's output driver with that of the transmission line.

8.2 Functional Block Diagram



8.3 Feature Description

The outputs of the LMK1C110x can be disabled by driving the synchronous output enable pin (1G) low. Unused output can be left floating to reduce overall system component cost. Supply and ground pins must be connected to V_{DD} and GND, respectively.

8.4 Device Functional Modes

The LMK1C110x operates from 1.8-V, 2.5-V, or 3.3-V supplies. Table 8-1 shows the output logics of the LMK1C110x.

Table 8-1. Output Logic Table

INPUTS		OUTPUTS
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMK1C110x family is a low additive jitter LVCMOS buffer solution that can operate up to 250-MHz at V_{DD} = 3.3 V and 200 MHz at V_{DD} = 2.5 V to 1.8 V. Low output skew as well as the ability for synchronous output enable is featured to simultaneously enable or disable buffered clock outputs as necessary in the application.

9.2 Typical Application

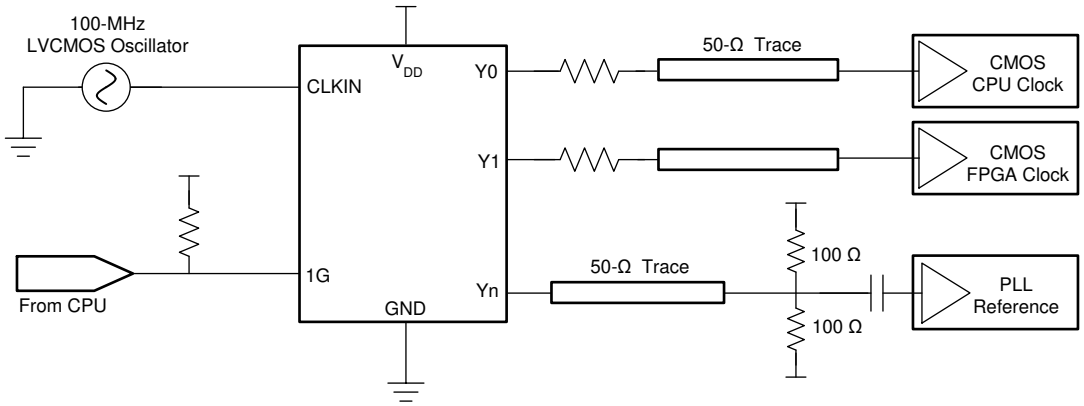


Figure 9-1. System Configuration Example

9.2.1 Design Requirements

The LMK1C110x shown in Figure 9-1 is configured to fan out a 100-MHz signal from a local LVCMOS oscillator. The CPU is configured to control the output state through 1G.

The configuration example is driving three LVCMOS receivers in a backplane application with the following properties:

- The CPU clock can accept a full swing DC-coupled LVCMOS signal. A series resistor is placed near the LMK1C110x to closely match the characteristic impedance of the trace to minimize reflections.
- The FPGA clock is similarly DC-coupled with an appropriate series resistor placed near the LMK1C110x.
- The PLL in this example can accept a lower amplitude signal, so a Thevenin's equivalent termination is used. The PLL receiver features internal biasing, so AC coupling can be used when common-mode voltage is mismatched.

9.2.2 Detailed Design Procedure

Unused outputs can be left floating. See Section 10 for recommended filtering techniques.

9.2.3 Application Curves

The low additive jitter of the LMK1C110x is shown in Figure 9-2.

Figure 9-3 shows the low-noise 156.25-MHz reference source with 24.8-fs RMS jitter driving the LMK1C110x, resulting in 27.3-fs RMS jitter when integrated from 12 kHz to 20 MHz at 3.3-V supply. The resultant additive jitter measured is a low 11.4-fs RMS for this configuration.

Figure 9-4 shows the low-noise 156.25-MHz reference source with 24.8-fs RMS jitter driving the LMK1C110x, resulting in 29-fs RMS jitter when integrated from 12 kHz to 20 MHz at 2.5-V supply. The resultant additive jitter measured is a low 15-fs RMS for this configuration.

Figure 9-5 shows the low-noise 156.25-MHz reference source with 24.8-fs RMS jitter driving the LMK1C110x, resulting in 34-fs RMS jitter when integrated from 12 kHz to 20 MHz at 1.8-V supply. The resultant additive jitter measured is a low 23.25-fs RMS for this configuration.

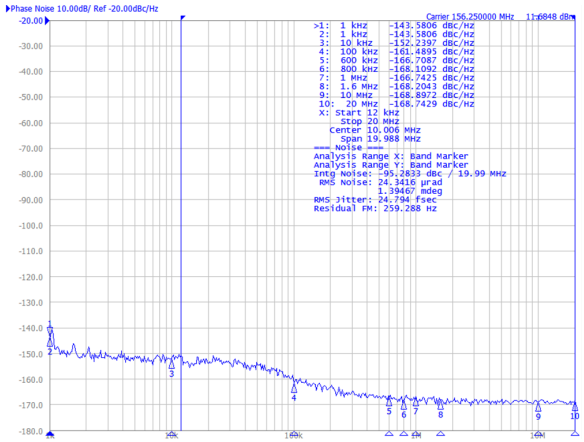


Figure 9-2. LMK1C110x Reference Phase Noise 24.8-fs (12 kHz to 20 MHz)

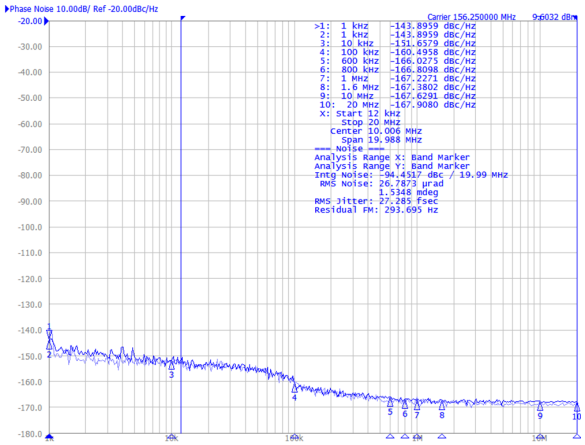


Figure 9-3. LMK1C110x 3.3-V Output Phase Noise 27.3-fs (12 kHz to 20 MHz)

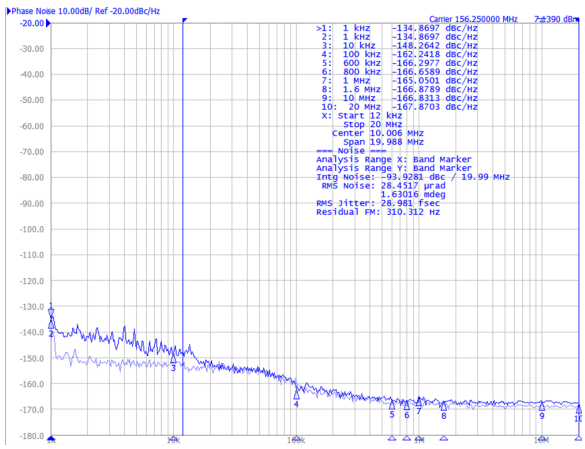


Figure 9-4. LMK1C110x 2.5-V Output Phase Noise 29-fs (12 kHz to 20 MHz)

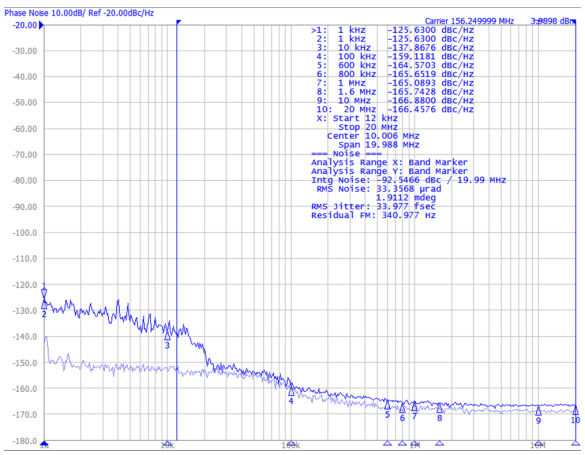


Figure 9-5. LMK1C110x 1.8-V Output Phase Noise 34-fs (12 kHz to 20 MHz)

10 Power Supply Recommendations

High-performance clock buffers can be sensitive to noise on the power supply, which may dramatically increase the additive jitter of the buffer. Thus, it is essential to manage any excessive noise from the system power supply, especially for applications where the jitter and phase noise performance is critical.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly bypass the supply, the decoupling capacitors must be placed very close to the power-supply terminals, be connected directly to the ground plane, and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1 µF) bypass capacitors, as there are supply terminals in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 10-1 shows this recommended power supply decoupling method.

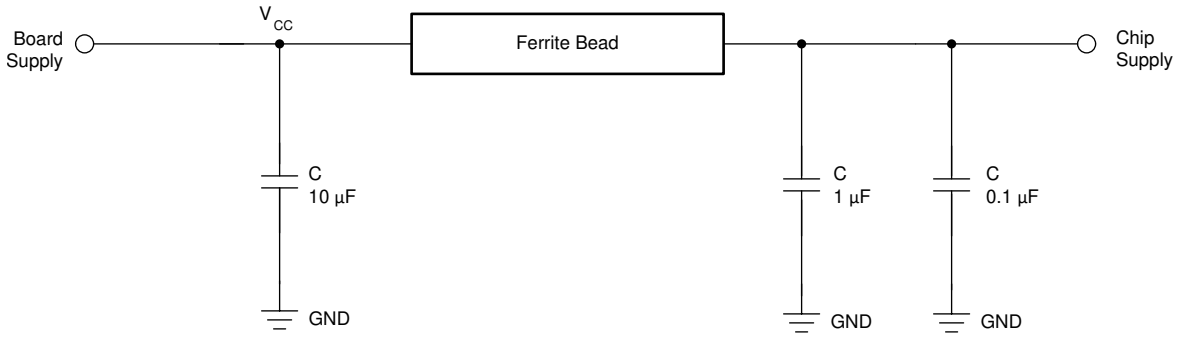


Figure 10-1. Power Supply Decoupling

11 Layout

11.1 Layout Guidelines

Figure 11-1 shows a conceptual layout detailing recommended placement of power supply bypass capacitors. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

11.2 Layout Example

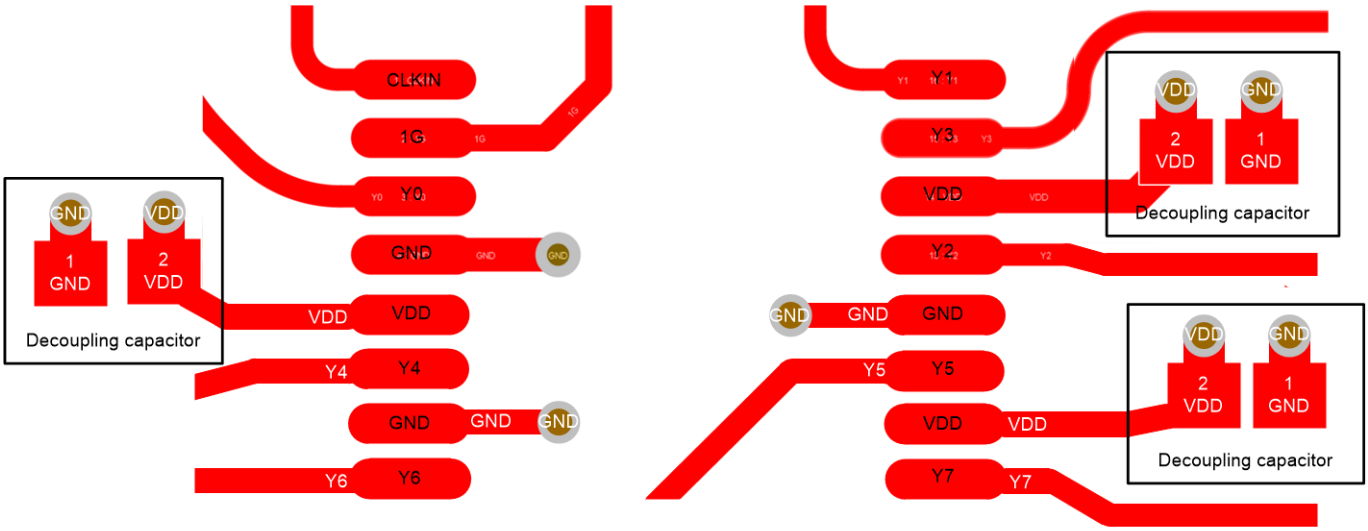


Figure 11-1. PCB Conceptual Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

LMK1C1108EVM User Guide

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK1C1106PWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1C6	Samples
LMK1C1108PWR	ACTIVE	TSSOP	PW	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1C8	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

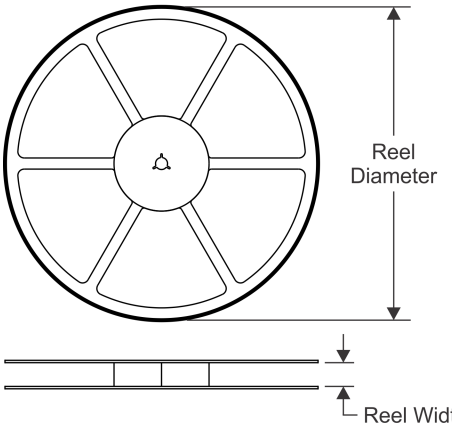
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

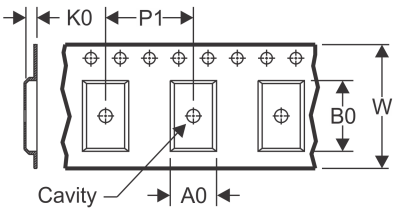
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

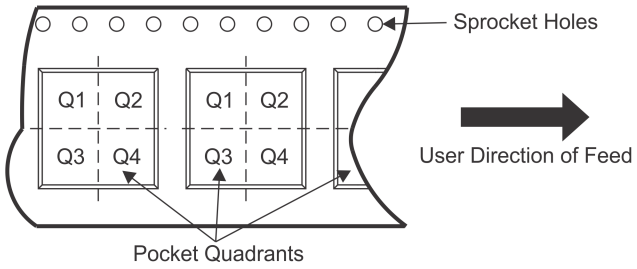


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

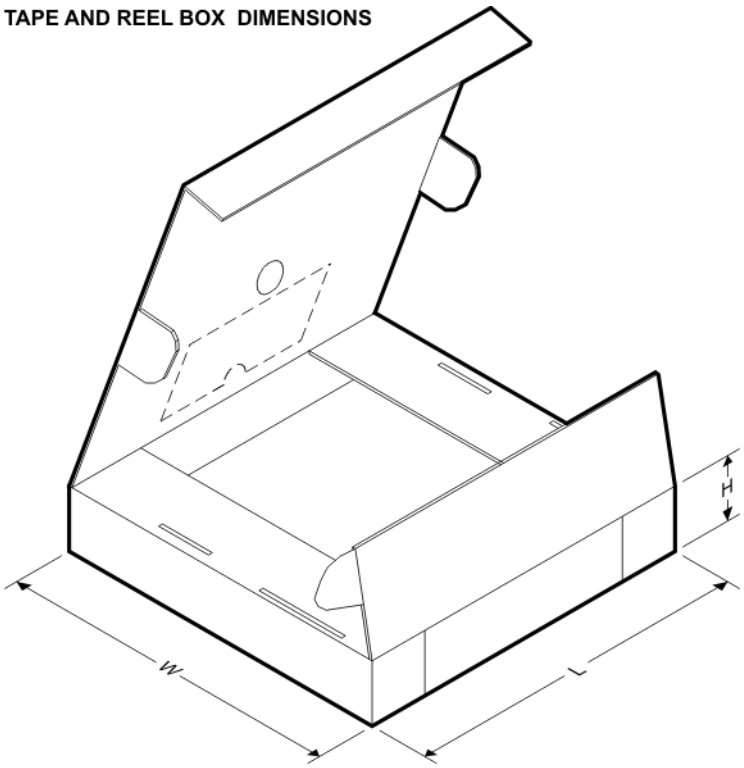
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK1C1106PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMK1C1108PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

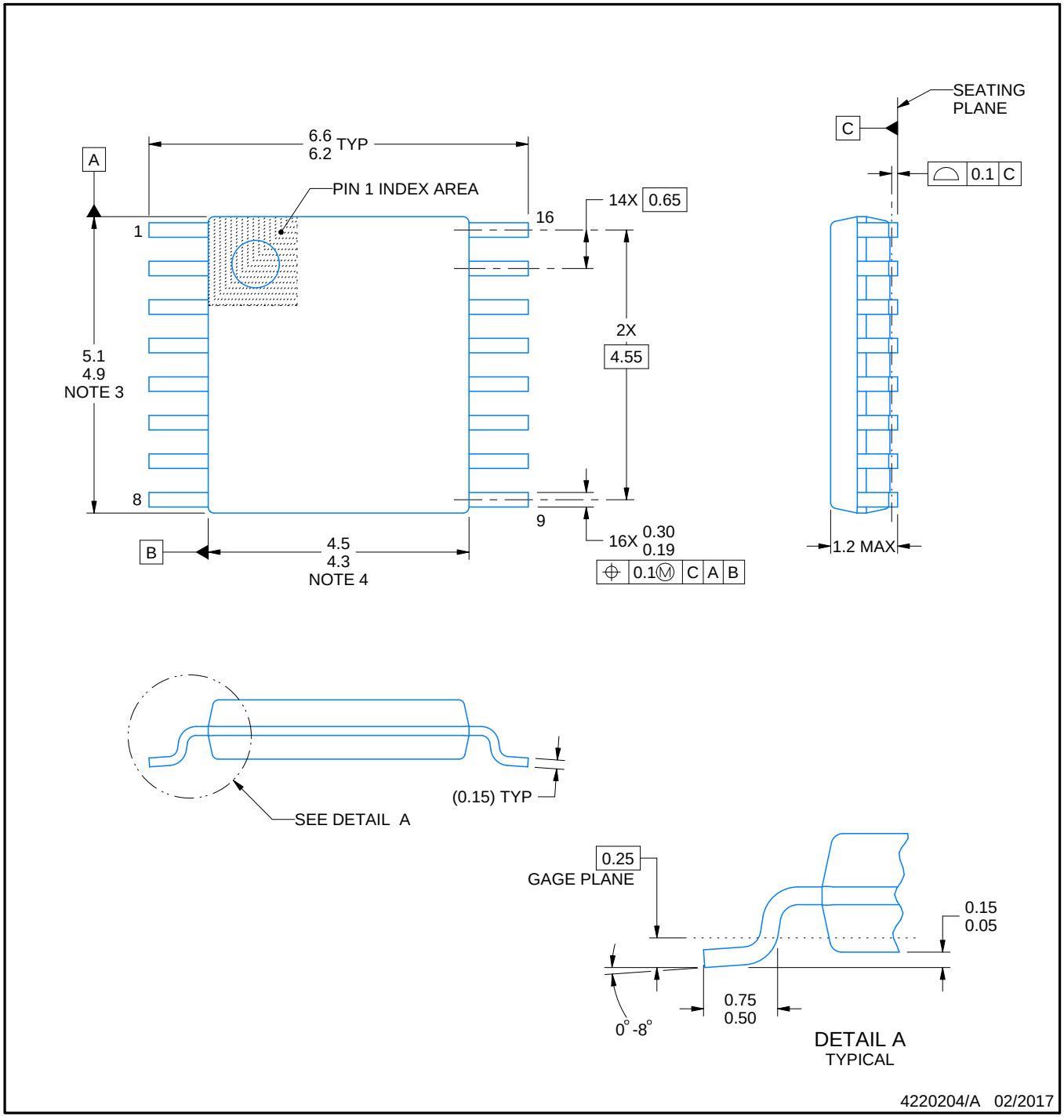
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK1C1106PWR	TSSOP	PW	14	3000	853.0	449.0	35.0
LMK1C1108PWR	TSSOP	PW	16	3000	853.0	449.0	35.0

PACKAGE OUTLINE

PW0016A

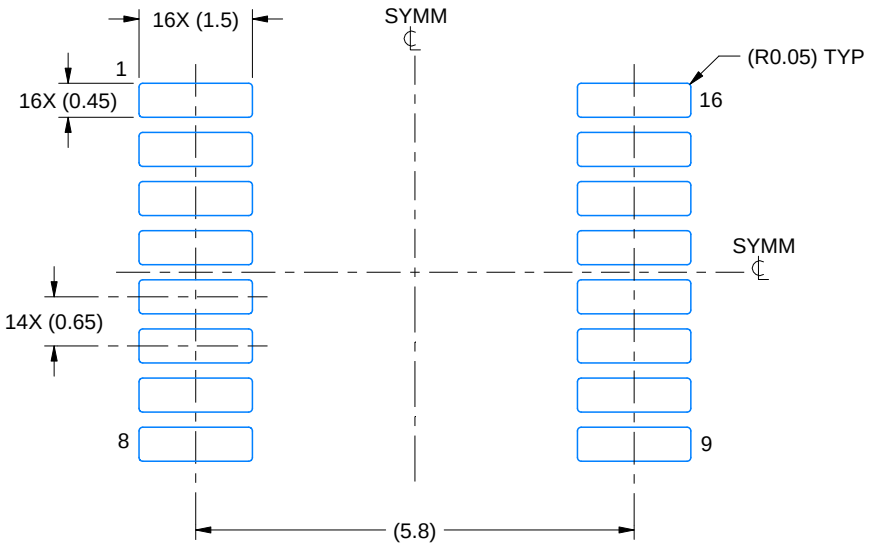
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

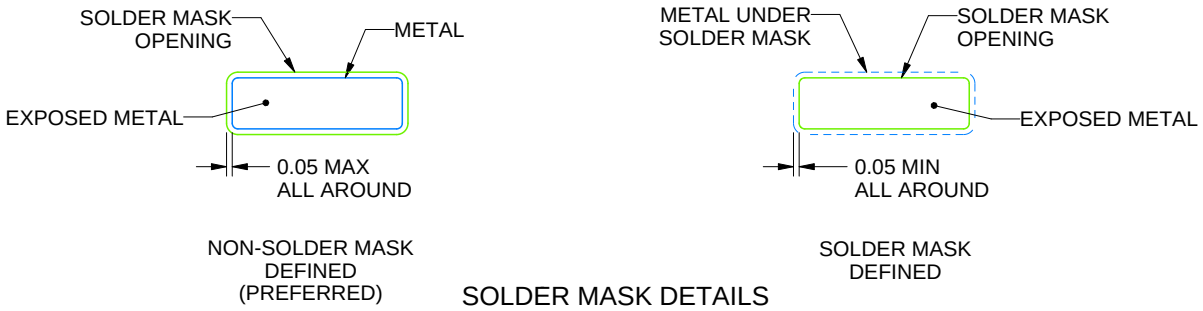


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

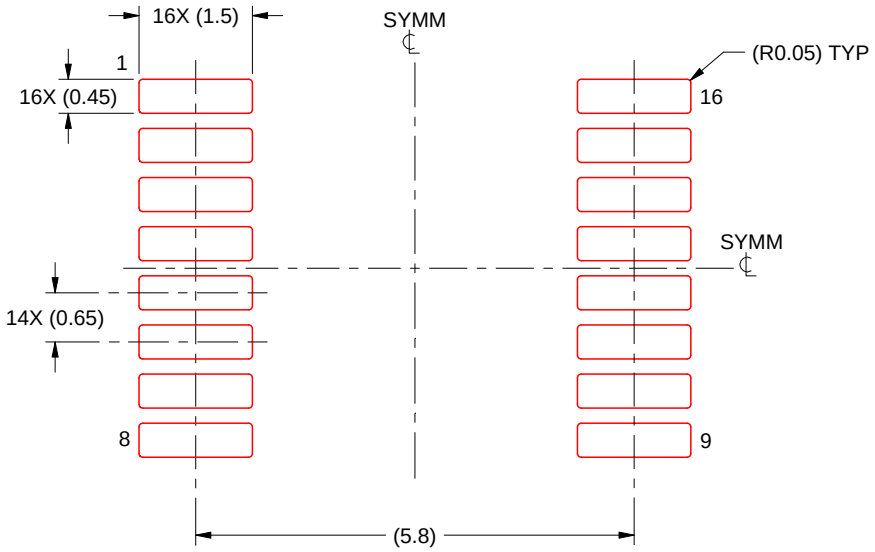


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



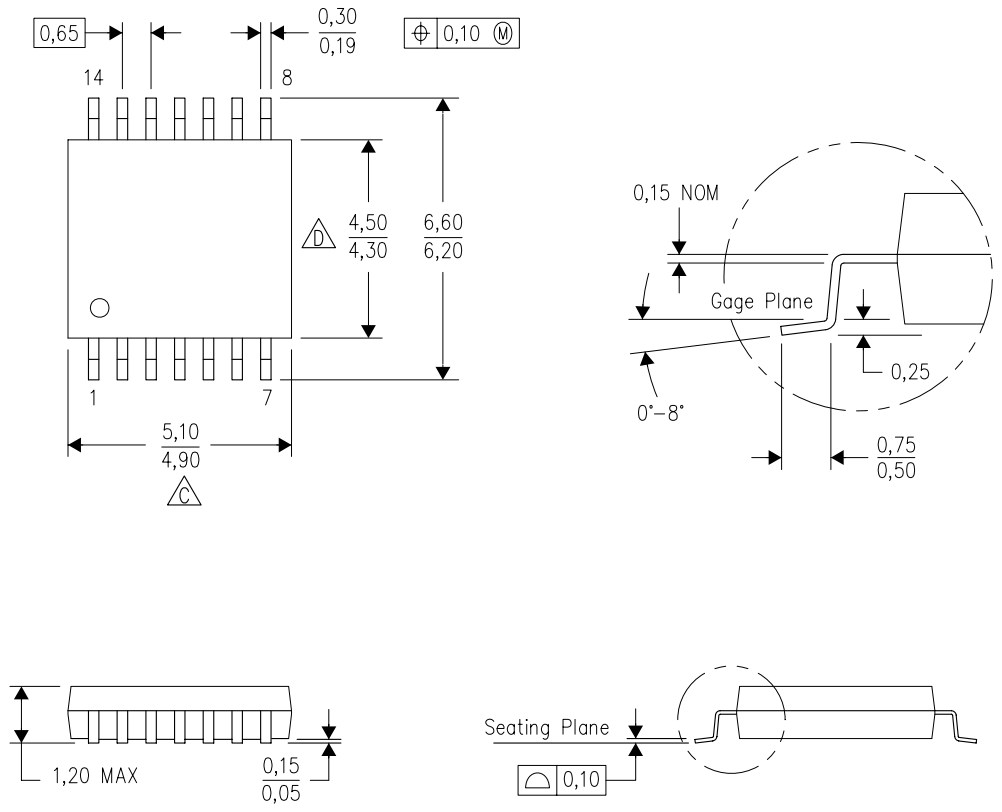
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

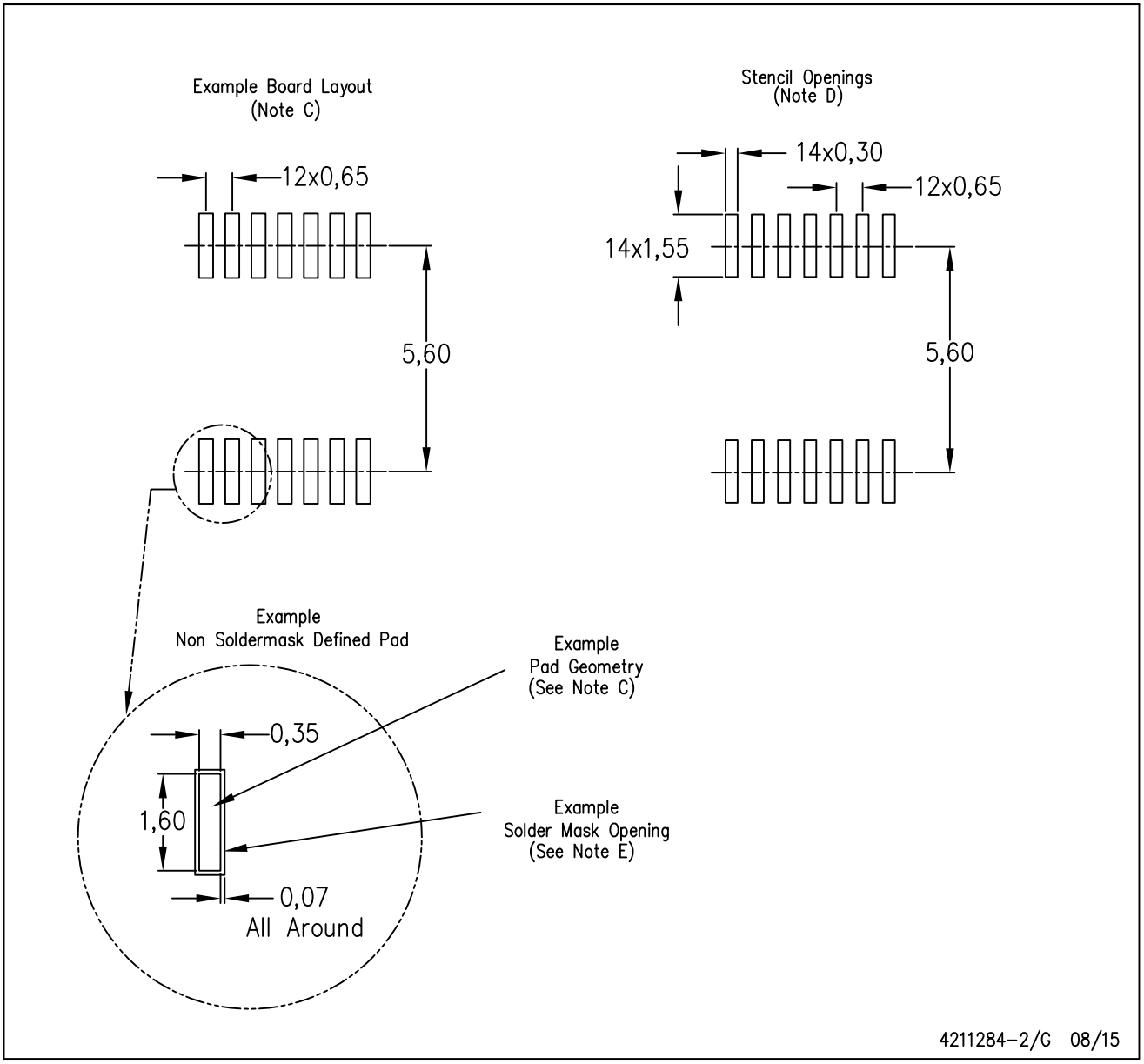
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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