National Semiconductor

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LMH0384

3 Gbps HD/SD SDI Extended Reach and Configurable Adaptive Cable Equalizer

General Description

The LMH0384 3 Gbps HD/SD SDI Extended Reach and Configurable Adaptive Cable Equalizer is designed to equalize data transmitted over cable (or any media with similar dispersive loss characteristics). The equalizer operates over a wide range of data rates from 125 Mbps to 2.97 Gbps and supports SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M standards.

The LMH0384 includes active sensing features and design enhancements including longer cable equalization, lower output jitter, configurable pin mode and SPI modes, a power-saving sleep mode, and programmable output common mode voltage and swing. The LMH0384 implements DC restoration to correctly handle pathological data conditions.

The LMH0384 includes an auto sleep mode to power down the device when no input signal is detected. Other features include separate carrier detect and output mute pins which may be tied together to mute the output when no input signal is present, and a programmable mute reference which may be used to mute the output at a selectable level of signal degradation.

The LMH0384 supports two modes of operation. In pin mode (non-SPI mode) the LMH0384 is footprint compatible with the LMH0344 and legacy SDI equalizers. In the optional SPI mode, the LMH0384 provides register access to all of its features along with a cable length indicator, programmable output common mode voltage and swing, and launch amplitude optimization.

The device is available in a 16-pin LLP package.

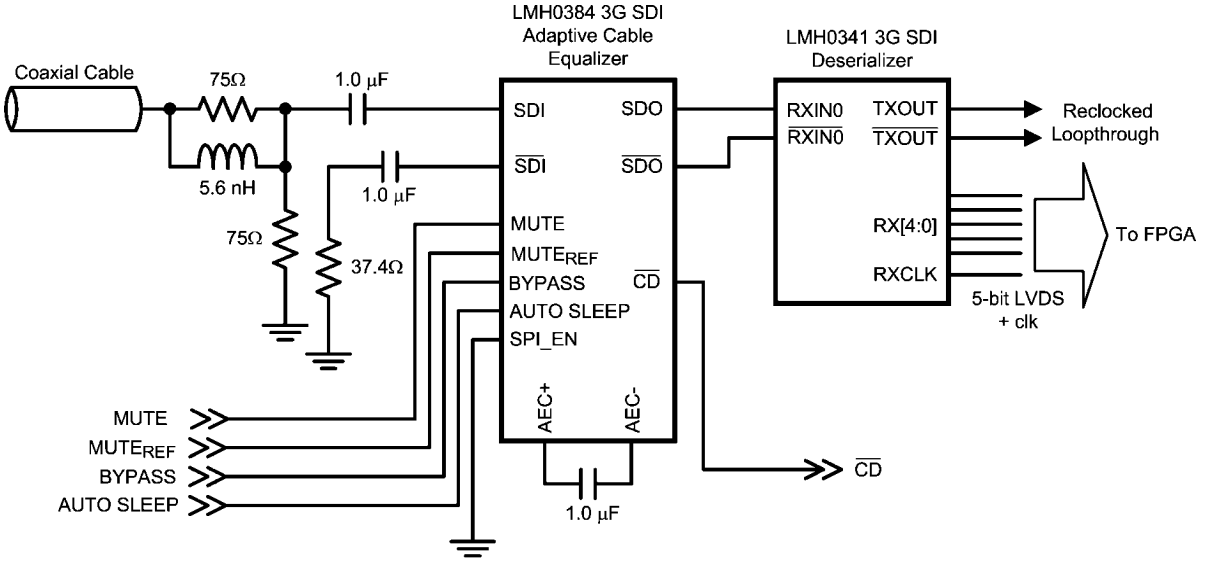
Features

- SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M compliant
- Supports DVB-ASI at 270 Mbps
- Wide range of data rates: 125 Mbps to 2.97 Gbps
- Equalizes up to 140 meters of Belden 1694A at 2.97 Gbps, up to 200 meters of Belden 1694A at 1.485 Gbps, or up to 400 meters of Belden 1694A at 270 Mbps
- Power save mode with auto sleep control (35 mW typical power consumption in power save mode)
- Optional SPI register access
- Manual bypass and output mute with a programmable threshold
- Internally terminated 100Ω LVDS outputs with SPI programmable output common mode voltage and swing
- Programmable launch amplitude optimization in SPI mode
- Cable length indicator in SPI mode
- Single 3.3V supply operation
- 16-pin LLP package
- Industrial temperature range: –40°C to +85°C
- Footprint compatible with the LMH0344, LMH0044, and LMH0074 in pin mode.

Applications

- SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M serial digital interfaces
- Serial digital data equalization and reception
- Data recovery equalization

Typical Application (Pin Mode)



Absolute Maximum Ratings (Note 1)

Supply Voltage	4.0V
Input Voltage (all inputs)	−0.3V to V_{CC}+0.3V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+125°C
Package Thermal Resistance	
θ_{JA} 16-pin LLP	+40°C/W
θ_{JC} 16-pin LLP	+6°C/W
ESD Rating (HBM)	≥±6.5 kV
ESD Rating (MM)	≥±400V
ESD Rating (CDM)	≥±2 kV

Recommended Operating Conditions

Supply Voltage (V_{CC} – V_{EE})	3.3V ±5%
Input Coupling Capacitance	1.0 µF
AEC Capacitor (Connected between AEC+ and AEC-)	1.0 µF
Operating Free Air Temperature (T_A)	−40°C to +85°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2, 3).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{IH}	Input Voltage High Level		Logic Inputs	2.0		V_{CC}	V
V_{IL}	Input Voltage Low Level			V_{EE}		0.8	V
V_{SDI}	Input Voltage Swing	0m cable length, (Note 5)	SDI, $\overline{SDI}$	720	800	950	mV_{P-P}
V_{CMIN}	Input Common Mode Voltage				1.75		V
V_{SSP-P}	Differential Output Voltage, P-P	100Ω load, default values (Note 6), *Figure 1*	SDO, $\overline{SDO}$	500	700	900	mV_{P-P}
V_{OD}	Differential Output Voltage			250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States					50	mV
V_{OS}	Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States					50	mV
I_{OS}	Output Short Circuit Current					30	mA
	$MUTE_{REF}$ DC Voltage (floating)		$MUTE_{REF}$		1.3		V
	$MUTE_{REF}$ Range				0.8		V
V_{OH}	Output Voltage High Level	I_{OH} = -2 mA	$\overline{CD}$, MISO	2.4			V
V_{OL}	Output Voltage Low Level	I_{OL} = +2 mA				0.4	V
I_{CC}	Supply Curren	Normal operation, equalizing cable < 140m (Belden 1694A), (Note 7)			70	85	mA
		Normal operation, equalizing cable > 140m (Belden 1694A)			90	110	mA
		Power save mode			10	14	mA

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 3).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
BR_{MIN}	Minimum Input Data Rate		SDI, $\overline{SDI}$		125		Mbps
BR_{MAX}	Maximum Input Data Rate					2970	Mbps
	Jitter for Various Cable Lengths	270 Mbps, Belden 1694A, 0-350 meters (Note 8)				0.2	UI
		270 Mbps, Belden 1694A, 350-400 meters			0.2		UI
		1.485 Gbps, Belden 1694A, 0-170 meters (Note 8)				0.25	UI
		1.485 Gbps, Belden 1694A, 170-200 meters			0.3		UI
		2.97 Gbps, Belden 1694A, 0-110 meters (Note 8)				0.3	UI
		2.97 Gbps, Belden 1694A, 110-140 meters			0.35		UI
t_r,t_f	Output Rise Time, Fall Time	20% – 80%, 100Ω load, (Note 4), *Figure 1*	SDO, $\overline{SDO}$		80	130	ps
	Mismatch in Rise/Fall Time	(Note 4)			2	15	ps
t_{OS}	Output Overshoot	(Note 4)			1	5	%
RL_{IN}	Input Return Loss	5 MHz - 1.5 GHz, (Note 9)	SDI, $\overline{SDI}$	15			dB
		1.5 GHz - 3.0 GHz, (Note 9)		10			dB
R_{IN}	Input Resistance	single-ended			1.3		kΩ
C_{IN}	Input Capacitance	single-ended			0.7		pF

SPI Interface AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 3).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
Recommended Input Timing Requirements							
f_{SCK}	SCK Frequency		SCK			20	MHz
t_{PH}	SCK Pulse Width High	*Figures 2, 3*		40			% SCK period
t_{PL}	SCK Pulse Width Low			40			% SCK period
t_{SU}	MOSI Setup Time	*Figures 2, 3*	MOSI	4			ns
t_H	MOSI Hold Time			4			ns
t_{SSSU}	$\overline{SS}$ Setup Time	*Figures 2, 3*	$\overline{SS}$	4			ns
t_{SSH}	$\overline{SS}$ Hold Time			4			ns
t_{SSOF}	$\overline{SS}$ Off Time			10			ns
Switching Characteristics							
t_{ODZ}	MISO Driven-to-Tristate Time	*Figure 3*	MISO			15	ns
t_{OZD}	MISO Tristate-to-Driven Time					15	ns
t_{OD}	MISO Output Delay Time					15	ns

Note 1: "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be guaranteed. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

Note 2: Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.

Note 3: Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.

Note 4: Specification is guaranteed by characterization.

Note 5: The LMH0384 can be optimized for different launch amplitudes via the SPI.

Note 6: The differential output voltage and offset voltage are adjustable via the SPI.

Note 7: The equalizer automatically shifts equalization stages at cable lengths less than 140m (Belden 1694A) to reduce power consumption. This power savings is also achieved by setting Extended 3G Reach Mode = 1 via the SPI.

Note 8: Based on design and characterization data over the full range of recommended operating conditions of the device. Jitter is measured in accordance with SMPTE RP 184, SMPTE RP 192, and the applicable serial data transmission standard: SMPTE 424M, SMPTE 292M, or SMPTE 259M.

Note 9: Input return loss is dependent on board design. The LMH0384 exceeds this specification on the SD384 evaluation board with a return loss network consisting of a 5.6 nH inductor in parallel with the 75Ω series resistor on the input.

Timing Diagrams

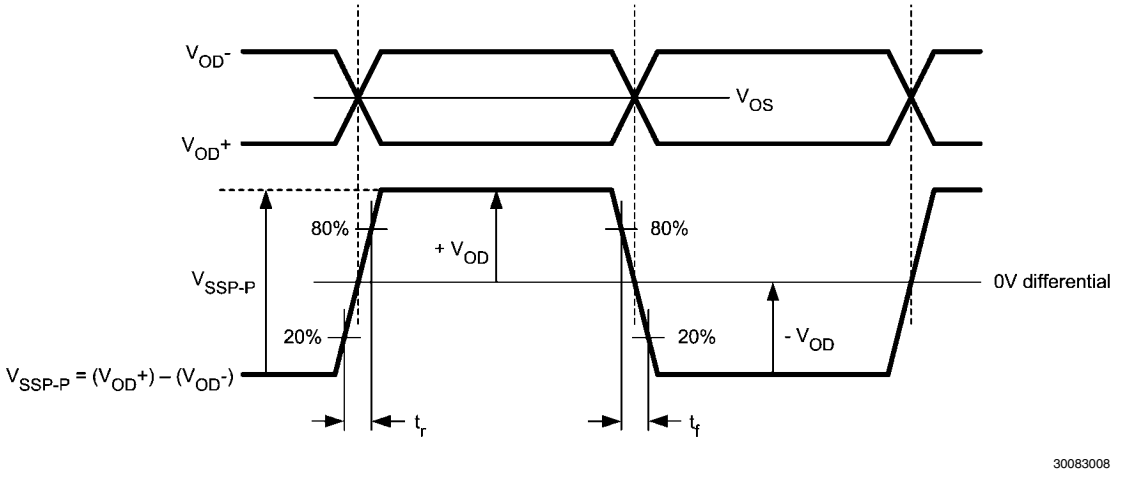


FIGURE 1. LVDS Output Voltage, Offset, and Timing Parameters

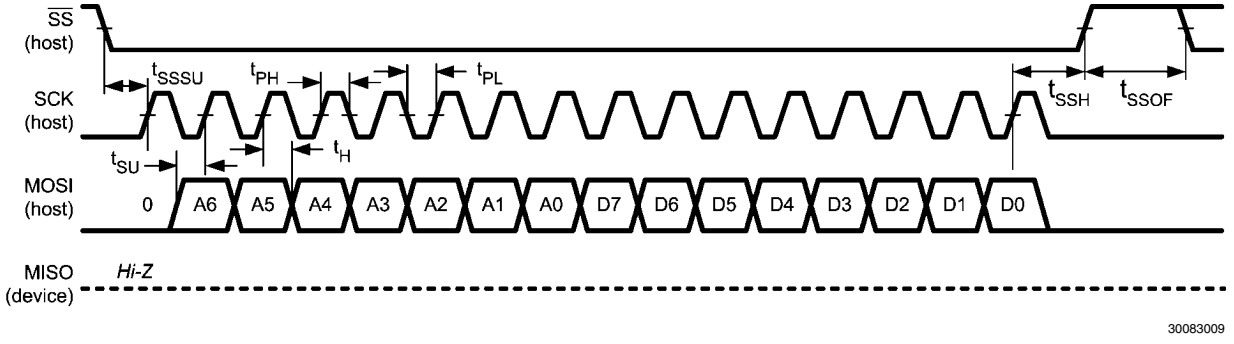


FIGURE 2. SPI Write

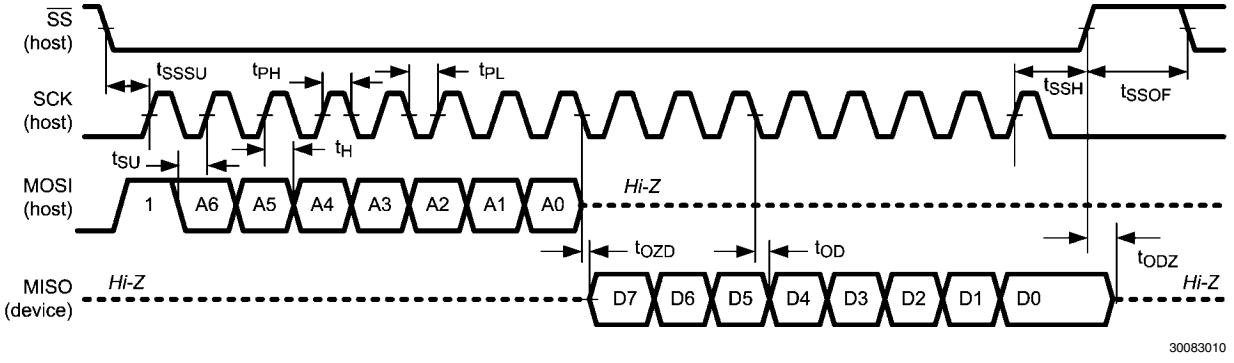
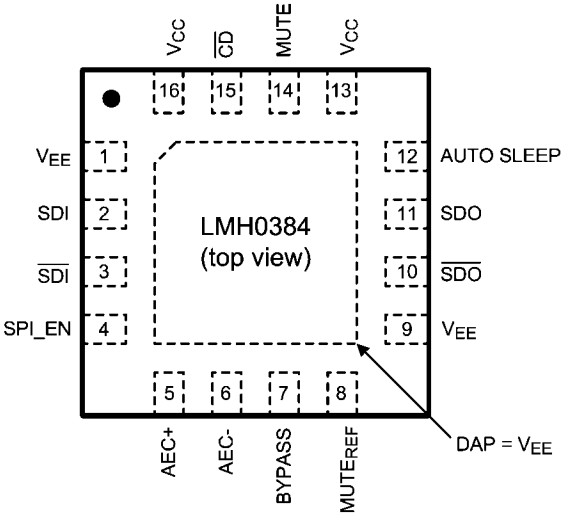


FIGURE 3. SPI Read

Connection Diagrams

Pin Mode (non-SPI) / SPI_EN = GND / LMH0344 Compatible



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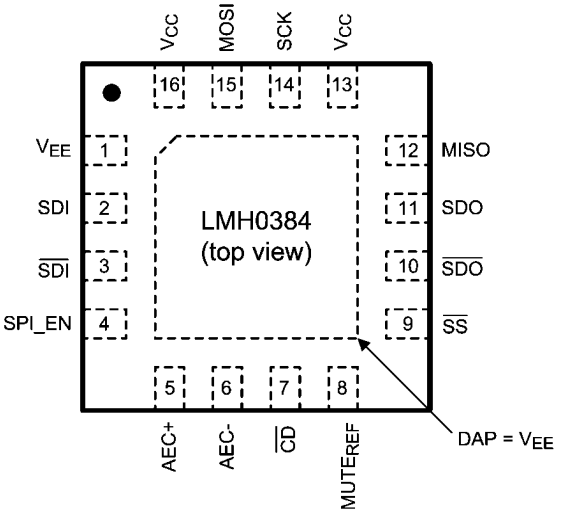
SPI Mode / SPI_EN = V_{CC}



30083007

The exposed die attach pad is a negative electrical terminal for this device. It should be connected to the negative power supply voltage.

16-Pin LLP
Order Number LMH0384SQ
See NS Package Number SQB16A

Pin Descriptions – Pin Mode (non-SPI) / SPI_EN = GND / LMH0344 Compatible

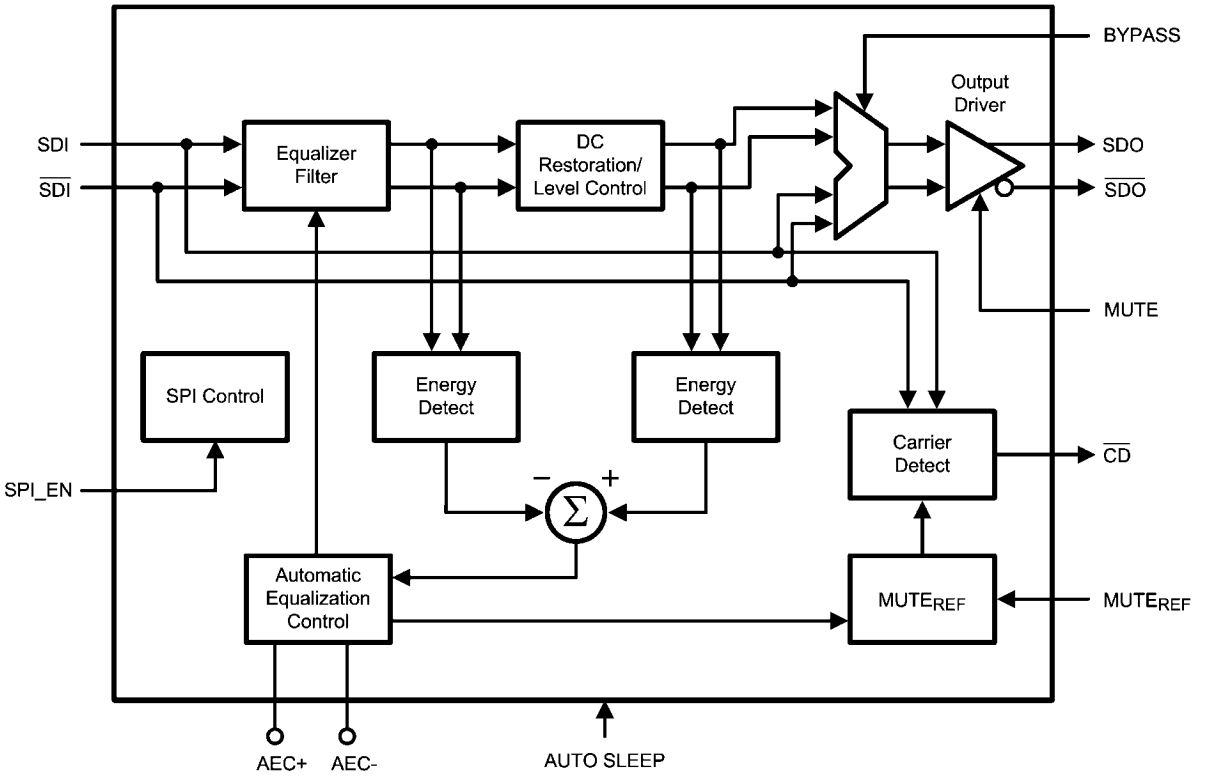
Pin	Name	I/O, Type	Description
1	V_{EE}	Ground	Negative power supply (ground).
2	SDI	I, SDI	Serial data true input.
3	$\overline{SDI}$	I, SDI	Serial data complement input.
4	SPI_EN	I, LVCMOS	SPI register access enable. This pin has an internal pulldown. H = SPI register access mode. L = Pin mode.
5	AEC+	I/O, Analog	AEC loop filter external capacitor (1µF) positive connection.
6	AEC-	I/O, Analog	AEC loop filter external capacitor (1µF) negative connection.

Pin	Name	I/O, Type	Description
7	BYPASS	I, LVCMOS	Equalization bypass. This pin has an internal pulldown. H = Equalization is bypassed (no equalization occurs). L = Normal operation.
8	$MUTE_{REF}$	I, Analog	Mute reference input. Sets the threshold for $\overline{CD}$ and (with $\overline{CD}$ tied to MUTE) determines the maximum cable to be equalized before muting. $MUTE_{REF}$ may be either unconnected or connected to ground for normal $\overline{CD}$ operation.
9	V_{EE}	I, LVCMOS	Connect this pin to ground or drive it logic low.
10	$\overline{SDO}$	O, LVDS	Serial data complement output.
11	SDO	O, LVDS	Serial data true output.
12	AUTO SLEEP	I, LVCMOS	Auto Sleep. AUTO SLEEP has precedence over MUTE and BYPASS. This pin has an internal pullup. H = Device will power down when no input is detected. L = Normal operation (device will not enter auto power down).
13	V_{CC}	Power	Positive power supply (+3.3V).
14	MUTE	I, LVCMOS	Output mute. $\overline{CD}$ may be tied to this pin to inhibit the output when no input signal is present. MUTE has precedence over BYPASS. This pin has an internal pulldown. H = Outputs forced to a muted state. L = Outputs enabled.
15	$\overline{CD}$	O, LVCMOS	Carrier detect. H = No input signal detected. L = Input signal detected.
16	V_{CC}	Power	Positive power supply (+3.3V).
DAP	V_{EE}	Ground	Connect exposed DAP to negative power supply (ground).

Pin Descriptions – SPI Mode / SPI_EN = V_{CC}

Pin	Name	I/O, Type	Description
1	V_{EE}	Ground	Negative power supply (ground).
2	SDI	I, SDI	Serial data true input.
3	$\overline{SDI}$	I, SDI	Serial data complement input.
4	SPI_EN	I, LVCMOS	SPI register access enable. This pin has an internal pulldown. H = SPI register access mode. L = Pin mode.
5	AEC+	I/O, Analog	AEC loop filter external capacitor (1µF) positive connection.
6	AEC-	I/O, Analog	AEC loop filter external capacitor (1µF) negative connection.
7	$\overline{CD}$	O, LVCMOS	Carrier detect. H = No input signal detected. L = Input signal detected.
8	$MUTE_{REF}$	I, Analog	Mute reference input. Sets the threshold for $\overline{CD}$ and (with $\overline{CD}$ tied to MUTE) determines the maximum cable to be equalized before muting. $MUTE_{REF}$ may be either unconnected or connected to ground for normal $\overline{CD}$ operation.
9	$\overline{SS}$ (SPI)	I, LVCMOS	SPI slave select. This pin has an internal pullup.
10	$\overline{SDO}$	O, LVDS	Serial data complement output.
11	SDO	O, LVDS	Serial data true output.
12	MISO (SPI)	O, LVCMOS	SPI Master Input / Slave Output. LMH0384 data transmit.
13	V_{CC}	Power	Positive power supply (+3.3V).
14	SCK (SPI)	I, LVCMOS	SPI serial clock input.
15	MOSI (SPI)	I, LVCMOS	SPI Master Output / Slave Input. LMH0384 data receive.
16	V_{CC}	Power	Positive power supply (+3.3V).
DAP	V_{EE}	Ground	Connect exposed DAP to negative power supply (ground).

Block Diagram (Pin Mode)



Device Operation

BLOCK DESCRIPTION

The **Equalizer Filter** block is a multi-stage adaptive filter. If Bypass is high, the equalizer filter is disabled.

The **DC Restoration / Level Control** block receives the differential signals from the equalizer filter block. This block incorporates a self-biasing DC restoration circuit to fully DC restore the signals. If Bypass is high, this function is disabled.

The signals before and after the DC Restoration / Level Control block are used to generate the **Automatic Equalization Control (AEC)** signal. This control signal sets the gain and bandwidth of the equalizer filter. The loop response in the AEC block is controlled by an external 1µF capacitor placed across the AEC+ and AEC- pins.

The **Carrier Detect** block generates the carrier detect signal based on the SDI input and an adjustment from the **Mute Reference** block.

The **SPI Control** block uses the MOSI, MISO, SCK, and $\overline{SS}$ signals in SPI mode to control the SPI registers. SPI_EN selects between SPI mode and pin mode. In pin mode, SPI_EN is driven logic low.

The **Output Driver** produces SDO and $\overline{SDO}$.

MUTE REFERENCE ($MUTE_{REF}$)

The mute reference sets the threshold for $\overline{CD}$ and (with $\overline{CD}$ tied to MUTE) determines the amount of cable to equalize before automatically muting the outputs. This is set by applying a voltage inversely proportional to the length of cable to equalize. The applied voltage must be greater than the $MUTE_{REF}$ floating voltage (typically 1.3V) in order to change the $\overline{CD}$ threshold. As the applied $MUTE_{REF}$ voltage is increased, the amount of cable that can be equalized before carrier detect is de-asserted and the outputs are muted is decreased. $MUTE_{REF}$ may be left unconnected or connected to ground for normal $\overline{CD}$ operation.

CARRIER DETECT ($\overline{CD}$) AND MUTE

Carrier detect $\overline{CD}$ indicates if a valid signal is present at the LMH0384 input. If $MUTE_{REF}$ is used, the carrier detect threshold will be altered accordingly. $\overline{CD}$ provides a high voltage when no signal is present at the LMH0384 input. $\overline{CD}$ is low when a valid input signal is detected.

MUTE can be used to manually mute or enable SDO and $\overline{SDO}$. Applying a high input to MUTE will mute the LMH0384 outputs by forcing the output to a logic zero. Applying a low input will force the outputs to be active.

$\overline{CD}$ and MUTE may be tied together to automatically mute the output when no input signal is present.

AUTO SLEEP

The auto sleep mode allows the LMH0384 to power down when no input signal is detected. If the AUTO SLEEP pin is set high, the LMH0384 goes into a deep power save mode when no signal is detected. The device powers on again once an input signal is detected. The auto sleep functionality can be turned off by setting AUTO SLEEP low or tying this pin to ground. An additional auto sleep setting available in SPI mode can be used to force the equalizer to power down regardless of whether there is an input signal or not. Auto sleep has precedence over mute and bypass modes.

In auto sleep mode, the time to power down the equalizer when the input signal is removed is less than 200 µs and

should not have any impact on the system timing requirements. The device will wake up automatically once an input signal is detected, and the delay between signal detection and full functionality of the equalizer is negligible (about 1 µs). The overall system will be limited only by the settling time constant of the equalizer adaptation loop.

INPUT INTERFACING

The LMH0384 accepts either differential or single-ended input. The input must be AC coupled. The *Typical Application (Pin Mode)* diagram on the front page shows the typical configuration for a single-ended input. The unused input must be properly terminated as shown.

The LMH0384 can be optimized for different launch amplitudes via the SPI (see *LAUNCH AMPLITUDE OPTIMIZATION* in the *SPI Register Access* section).

The LMH0384 correctly handles equalizer pathological signals for standard definition and high definition serial digital video, as described in SMPTE RP 178 and RP 198, respectively.

OUTPUT INTERFACING

SDO and $\overline{\text{SDO}}$ together are internally terminated 100Ω LVDS outputs. These outputs can be DC coupled to most common differential receivers.

The default output common mode voltage (V_{OS}) is 1.25V. The output common mode voltage may be adjusted via the SPI in 200 mV increments, from 1.05V to 1.85V (see *OUTPUT DRIVER ADJUSTMENTS* in the *SPI Register Access* section). This adjustable output common mode voltage offers flexibility for interfacing to many types of receivers.

The default differential output swing (V_{SSP-P}) is 700 mV_{P-P}. The differential output swing may be adjusted via the SPI in 100 mV increments from 400 mV_{P-P} to 800 mV_{P-P} (see *OUTPUT DRIVER ADJUSTMENTS* in the *SPI Register Access* section).

The LMH0384 output should be DC coupled to the input of the receiving device as long as the common mode ranges of both devices are compatible. 100Ω differential transmission lines should be used to connect between the LMH0384 outputs and the input of the receiving device where possible. *Figure 4* shows an example of a DC-coupled interface between the LMH0384 and LMH0346 SDI reclocker. All that is required is the 100Ω differential termination as shown. The resistor should be placed as close as possible to the LMH0346 input. If desired, this network may be terminated with two 50Ω resistors and a center tap capacitor to ground in place of the signal 100Ω resistor.

Figure 5 shows an example of a DC-coupled interface between the LMH0384 and LMH0356 SDI reclocker. The LMH0356 inputs have 50Ω internal terminations (100Ω differential) to terminate the transmission line, so no additional components are required.

The LMH0384 allows flexibility when interfacing to low voltage crosspoint switches (i.e. 1.8V) and other devices with limited input ranges. The LMH0384 outputs can be DC coupled to these devices in most cases, avoiding the need to AC couple.

The LMH0384 may be AC coupled to the receiving device when necessary. For example, the LMH0384 outputs are not strictly compatible with 3.3V CML and thus should not be connected via 50Ω resistors to 3.3V. If the input common mode range of the receiving device is not compatible with the output common mode range of the LMH0384, then AC coupling is required. Following the AC coupling capacitors, the signal may have to be biased at the input of the receiving device.

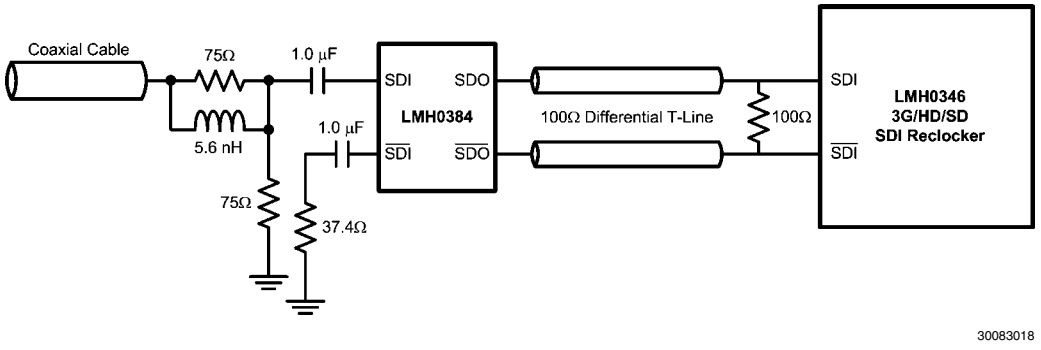


FIGURE 4. DC Output Interface to LMH0346 Reclocker

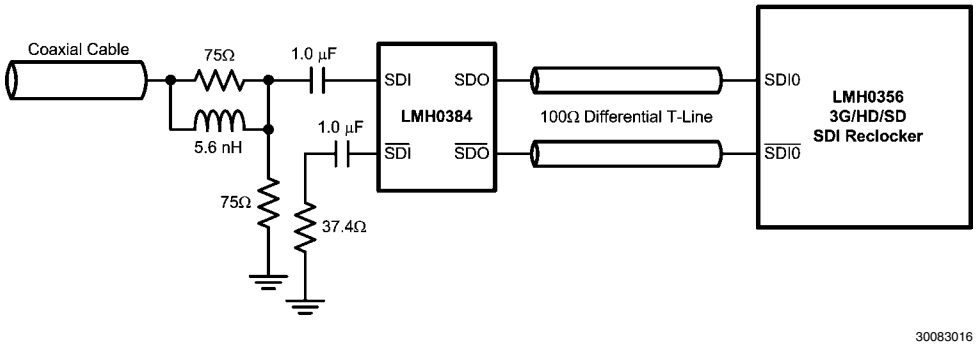


FIGURE 5. DC Output Interface to LMH0356 Reclocker

SPI Register Access

Setting SPI_EN high enables the optional SPI register access mode. In SPI mode, the LMH0384 provides register access to all of its features along with a cable length indicator, programmable output common mode voltage and swing, and launch amplitude optimization. There are five supported 8-bit registers in the device (see *Table 1*). With SPI_EN set low, the device operates in pin mode and is footprint compatible with the LMH0344, LMH0044, and LMH0074.

SPI WRITE

The SPI write is shown in *Figure 2*. The MOSI payload consists of a "0" (write command), seven address bits, and eight data bits. The $\overline{SS}$ signal is driven low, and the 16 bits are sent to the LMH0384's MOSI input. Data is latched on the rising edge of SCK. The MISO output is normally tri-stated during this operation. After the SPI write, $\overline{SS}$ must return high.

SPI READ

The SPI read is shown in *Figure 3*. The MOSI payload consists of a "1" (read command) and seven address bits. The $\overline{SS}$ signal is driven low, and the eight bits are sent to the LMH0384's MOSI input. The addressed location is accessed immediately after the rising edge of the 8th clock and the eight data bits are shifted out on MISO starting with the falling edge of the 8th clock. MOSI must be tri-stated immediately after the rising edge of the 8th clock. After the SPI read, $\overline{SS}$ must return high.

OUTPUT DRIVER ADJUSTMENTS

The output driver swing (amplitude) and offset voltage (common mode voltage) are adjustable via SPI register 01h.

The output swing is adjustable via bits [7:5] of SPI register 01h. The default value for these register bits is "011" for a peak to peak differential output voltage of 700 mV_{P-P}. The output swing can be adjusted in 100 mV increments from 400 mV_{P-P} to 800 mV_{P-P}.

The offset voltage is adjustable via bits [4:2] of SPI register 01h. The default value for these register bits is "001" for an output offset of 1.25V. The output common mode voltage may be adjusted in 200 mV increments, from 1.05V to 1.85V. It can also be set to "101" for the maximum offset voltage. At this maximum offset voltage setting, the outputs are referenced to the positive supply and the offset voltage is around 2.1V.

LAUNCH AMPLITUDE OPTIMIZATION

The LMH0384 can compensate for attenuation of the input signal prior to the equalizer. This compensation is useful for applications with a passive splitter at the equalizer input or a non-ideal input termination network, and is controlled by SPI register 02h.

Bit 7 of SPI register 02h is used for coarse control of the launch amplitude setting. At the default setting of "0", the LMH0384 operates normally and expects a launch amplitude of 800 mV_{P-P}. Bit 7 may be set to "1" to optimize the LMH0384 for input signals with 6 dB of attenuation (400 mV_{P-P}).

Once the coarse control is set, the LMH0384 input compensation may be further fine tuned by bits [6:3] of SPI register 02h. These bits may be used to tweak the input gain stage -22% to +40% around the coarse control setting.

CABLE LENGTH INDICATOR (CLI)

The Cable Length Indicator (CLI) provides an indication of the length of cable attached to the input. CLI is accessible via bits [7:3] of SPI register 03h. The 5-bit CLI ranges in decimal value from 0 to 25 ("00000" to "11001" binary) and increases as the cable length is increased. *Figure 6* shows typical CLI values vs. Belden 1694A cable length. CLI is valid for Belden 1694A cable lengths of 0-140m at 2.97 Gbps, 0-200m at 1.485 Gbps, and 0-400m at 270 Mbps.

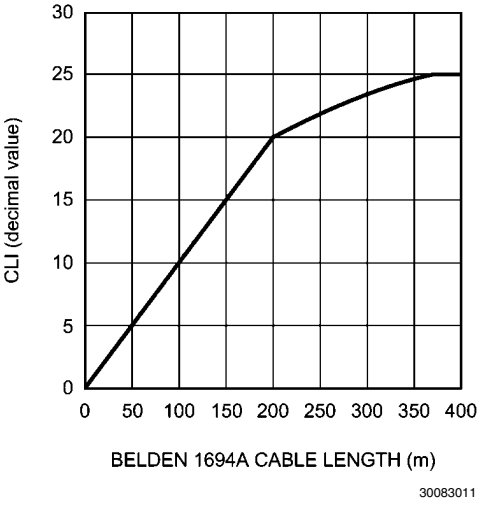


FIGURE 6. CLI vs. Belden 1694A Cable Length

APPLICATION OF CLI: EXTENDING 3G REACH

An application of CLI is to extend the 3G reach in systems which have margin in the jitter budget. This allows for additional cable reach at 2.97 Gbps at the expense of slightly higher output jitter. The extended 3G reach mode provides 15m of additional Belden 1694A cable reach, with an increase of output jitter at this longer cable length of 0.05 to 0.1 UI.

The extended 3G reach mode is accessible via bit 2 of SPI register 00h. In order to achieve longer 3G cable reach while still maintaining the performance at HD and SD data rates, a state machine can be implemented as shown in *Figure 7*. (Note: If this procedure is not followed, the maximum equalizable cable lengths for HD and SD data rates will be limited to less than what can be achieved in normal mode).

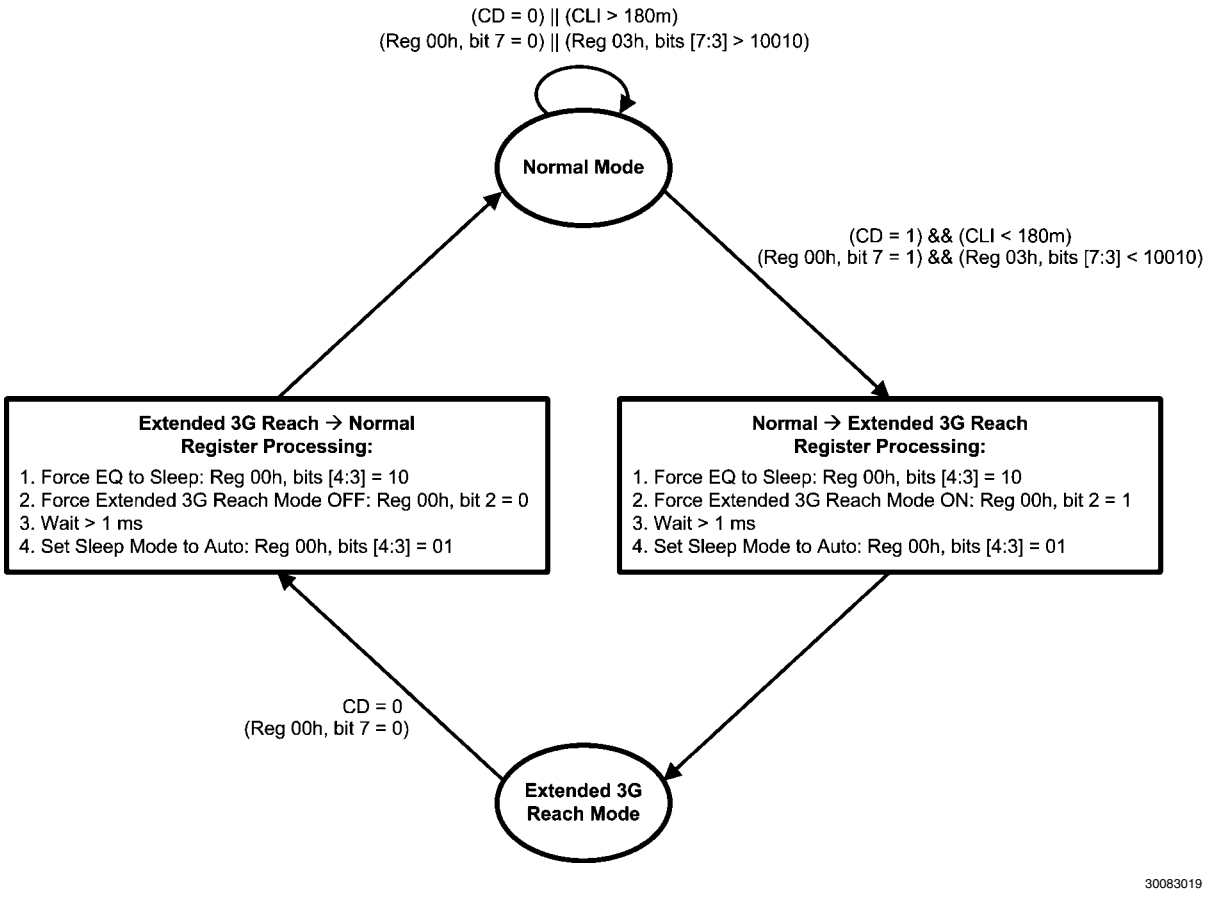


FIGURE 7. Extended 3G Reach Mode State Machine Example

EXPLANATION OF EXTENDED 3G REACH MODE STATE MACHINE (*Figure 7*)

When the LMH0384 is powered on, it will be in normal mode. If there is no input signal (register 00h, bit 7 = 0) or if the input cable is longer than a user programmable cable length (i.e. 180m, which means register 03h, bits [7:3] > 10010), then the device should remain in normal mode.

Once an input signal is detected (register 00h, bit 7 = 1) AND the detected cable length is shorter than the user programmed cable length of 180m (register 03h, bits [7:3] < 10010), then the equalizer can enter the extended 3G reach mode to allow for longer cable lengths at 2.97 Gbps. This requires the following procedure:

1. Force the equalizer to sleep by writing “10” to bits [4:3] of register 00h.
2. Turn on the extended 3G reach mode by writing “1” to bit 2 of register 00h.
3. Wait at least 1ms.
4. Set the sleep mode to auto by writing “01” to bits [4:3] of register 00h. Alternately, sleep mode may be set to off by writing “00” to bits [4:3] of register 00h.

The equalizer remains in extended 3G reach mode until the cable length is changed. If the cable length is changed, the input signal drops out momentarily. Once this happens (register 00h, bit 7 = 0), then the following procedure must be used to set the device back to normal mode:

1. Force the equalizer to sleep by writing “10” to bits [4:3] of register 00h.
2. Turn off the extended 3G reach mode by writing “0” to bit 2 of register 00h.
3. Wait at least 1ms.
4. Set the sleep mode to auto by writing “01” to bits [4:3] of register 00h. Alternately, sleep mode may be set to off by writing “00” to bits [4:3] of register 00h.

Application Information

APPLICATION CIRCUIT (SPI MODE)

Figure 8 shows the application circuit for the LMH0384 in SPI mode.

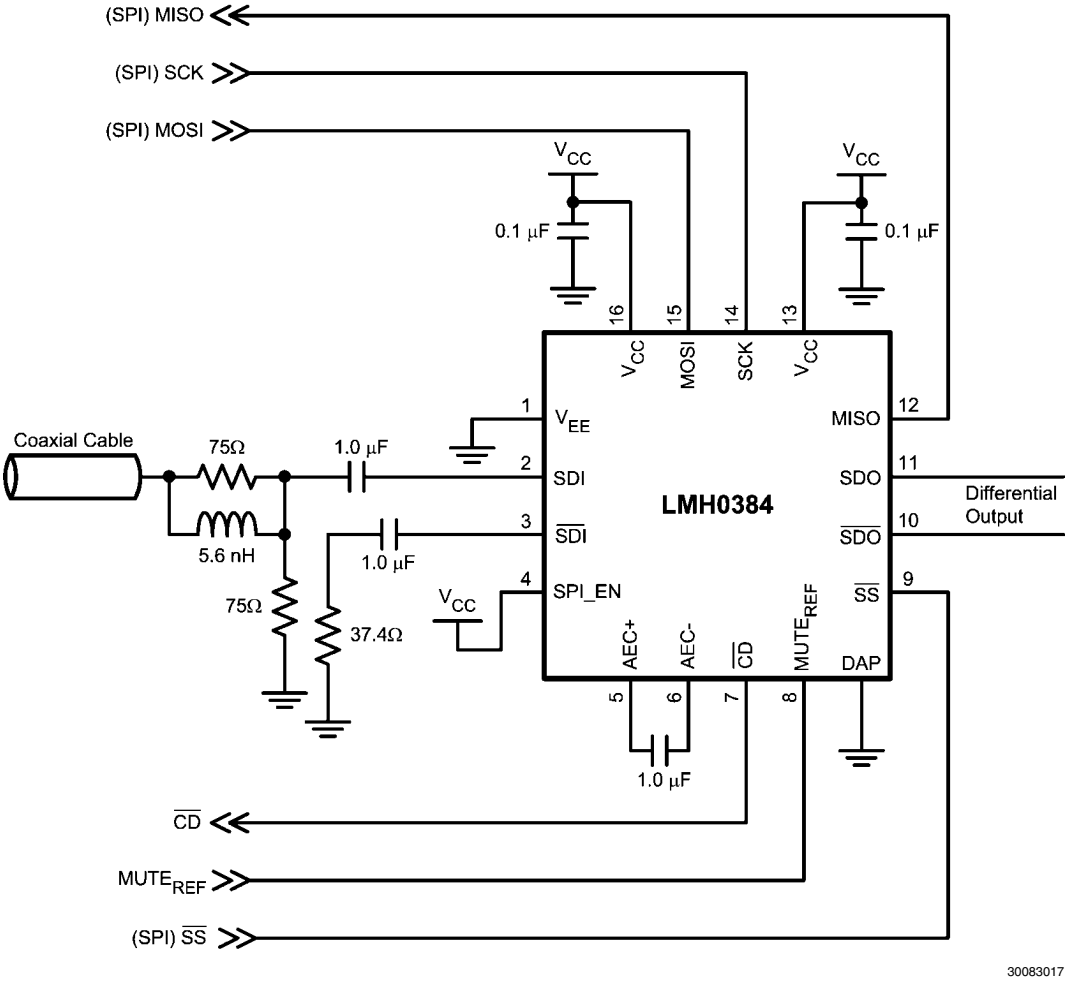


FIGURE 8. Application Circuit (SPI Mode)

REPLACING THE LMH0344

In pin mode, the LMH0384 is a drop-in replacement for the LMH0344SQ SDI cable equalizer. When replacing an LMH0344 with an LMH0384, it is important to consider the following points:

1. The LMH0384 auto sleep function is mapped to pin 12 which is a ground pin on the LMH0344SQ. When this pin is grounded on the LMH0384, the auto sleep function is disabled. To enable auto sleep mode on the LMH0384, pin 12 must be pulled high.
2. Pin 4 and pin 9 on the LMH0344SQ are true ground pins. For the LMH0384, pin 4 and pin 9 may be driven logic low in pin mode (they do not require a true ground connection).
3. The LMH0384 has lower input capacitance than the LMH0344 which allows for improved input return loss. The input return loss network may need to be modified. In most cases, the LMH0384 should provide superior input return loss.
4. The LMH0384 default output common mode voltage is different than that of the LMH0344. In most cases, this should not cause an issue. The LMH0384 and LMH0344 outputs can both be DC coupled to National's SDI reclockers and cable drivers. In addition, the LMH0384 output can be DC coupled to LVDS and other inputs that require lower input common mode voltages than the LMH0344. The LMH0384 output common mode voltage is adjustable via the SPI.

PCB LAYOUT RECOMMENDATIONS

For information on layout and soldering of the LLP package, pease refer to the following application note: **AN-1187, "Leadless Leadframe Package (LLP)."**

The SMPTE 424M, 292M, and 259M standards have stringent requirements for the input return loss of receivers, which essentially specify how closely the input must resemble a 75Ω network. Any non-idealities in the network between the BNC and the equalizer will degrade the input return loss. Care must be taken to minimize impedance discontinuities be-

tween the BNC and the equalizer to ensure that the characteristic impedance of this trace is 75Ω. Please consider the following PCB recommendations:

- Use surface mount components, and use the smallest components available. In addition, use the smallest size component pads.
- Select trace widths that minimize the impedance mismatch between the BNC and the equalizer.
- Select a board stack up that supports both 75Ω single-ended traces and 100Ω loosely-coupled differential traces.
- Place return loss components closest to the equalizer input pins.
- Maintain symmetry on the complimentary signals.
- Route 100Ω traces uniformly (keep trace widths and trace spacing uniform along the trace).
- Avoid sharp bends in the signal path; use 45° or radial bends.
- Place bypass capacitors close to each power pin, and use the shortest path to connect equalizer power and ground pins to the respective power or ground planes.

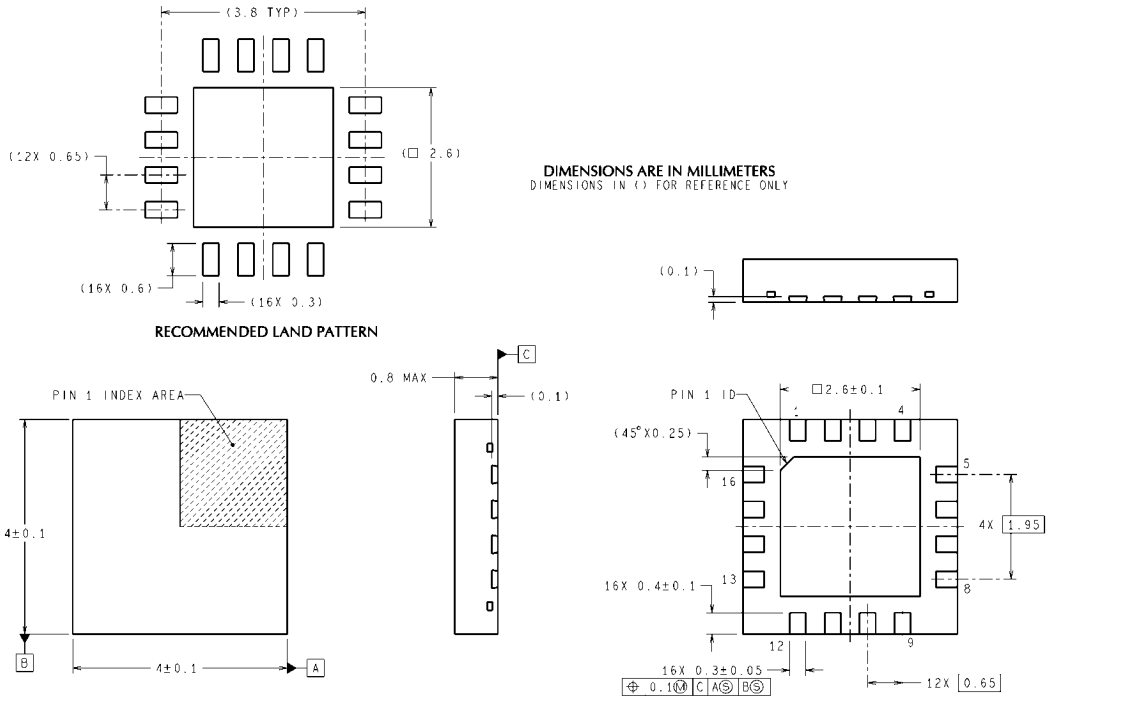
SPI Registers

TABLE 1. SPI Registers

Address	R/W	Name	Bits	Field	Default	Description
00h	R/W	General Control	7	Carrier Detect		0: No carrier detected. 1: Carrier detected.
			6	Mute	0	Mute has precedence over Bypass. 0: Normal operation. 1: Outputs muted.
			5	Bypass	0	0: Normal operation. 1: Equalizer bypassed.
			4:3	Sleep Mode	01	Sleep mode control. Sleep has precedence over Mute and Bypass. 00: Disable sleep mode (force equalizer to stay enabled). 01: Sleep mode active when no input signal detected. 10: Force equalizer into sleep mode (powered down) regardless of whether there is an input signal or not. 11: Reserved.
			2	Extended 3G Reach Mode	0	Extended 3G reach mode to extend the cable length for 2.97 Gbps applications. 0: Normal operation. 1: Extended 3G reach mode.
			1:0	Reserved	00	Reserved as 00. Always write 00 to these bits.
01h	R/W	Output Driver	7:5	Output Swing	011	Output driver swing (V_{SSP-P}). 000: V_{SSP-P} = 400 mV_{P-P}. 001: V_{SSP-P} = 500 mV_{P-P}. 010: V_{SSP-P} = 600 mV_{P-P}. 011: V_{SSP-P} = 700 mV_{P-P}. 100: V_{SSP-P} = 800 mV_{P-P}. 101, 110, 111: Reserved.
			4:2	Offset Voltage	001	Output driver offset voltage (common mode voltage). 000: V_{OS} = 1.05V. 001: V_{OS} = 1.25V. 010: V_{OS} = 1.45V. 011: V_{OS} = 1.65V. 100: V_{OS} = 1.85V. 101: V_{OS} referenced to positive supply. 110, 111: Reserved.
			1:0	Reserved	00	Reserved as 00. Always write 00 to these bits.

Address	R/W	Name	Bits	Field	Default	Description
02h	R/W	Launch Amplitude	7	Coarse Control	0	Coarse launch amplitude optimization. 0: Normal optimization with no external attenuation (800 mV_{P-P} launch amplitude). 1: Optimized for 6 dB external attenuation (400 mV_{P-P} launch amplitude).
			6:3	Fine Control	0000	Launch amplitude optimization fine tuning. 0000: Nominal. 0001: -4% from nominal. 0010: -8% from nominal. 0011: -11% from nominal. 0100: -14% from nominal. 0101: -17% from nominal. 0110: -20% from nominal. 0111: -22% from nominal. 1000: Nominal. 1001: +4% from nominal. 1010: +9% from nominal. 1011: +14% from nominal. 1100: +20% from nominal. 1101: +26% from nominal. 1110: +33% from nominal. 1111: +40% from nominal.
			2:0	Reserved	000	Reserved as 000. Always write 000 to these bits.
03h	R	CLI	7:3	CLI		Cable Length Indicator. Provides an indication of the length of cable attached to the input. CLI increases as the cable length increases.
			2:0	Reserved	000	Reserved.
04h	R	Device ID	7:0	Die Revision	00000010	Die revision.

Physical Dimensions inches (millimeters) unless otherwise noted



SQB16A (Rev A)

16-Pin LLP
Order Number LMH0384SQ
NS Package Number SQB16A

Notes

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Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
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