LMG1205 100-V, 1.2-A, 5-A, Half-Bridge Gate Driver for Enhancement Mode GaN FETs

1 Features

- Independent High-Side and Low-Side TTL Logic Inputs
- 1.2-A Peak Source, 5-A Sink Current
- High-Side Floating Bias Voltage Rail Operates up to 100 VDC
- Internal Bootstrap Supply Voltage Clamping
- Split Outputs for Adjustable Turnon, Turnoff Strength
- 0.6-Ω Pulldown, 2.1-Ω Pullup Resistance
- Fast Propagation Times (35 ns Typical)
- Excellent Propagation Delay Matching (1.5 ns Typical)
- Supply Rail Undervoltage Lockout
- Low Power Consumption

2 Applications

- Current-Fed Push-Pull Converters
- Half and Full-Bridge Converters
- Synchronous Buck Converters
- Two-Switch Forward Converters
- Forward with Active Clamp Converters

3 Description

The LMG1205 is designed to drive both the high-side and the low-side enhancement mode Gallium Nitride (GaN) FETs in a synchronous buck, boost, or half-bridge configuration. The device has an integrated 100-V bootstrap diode and independent inputs for the high-side and low-side outputs for maximum control flexibility. The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5 V, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of enhancement mode GaN FETs. The inputs of the LMG1205 are TTL logic compatible and can withstand input voltages up to 14 V regardless of the VDD voltage. The LMG1205 has split-gate outputs, providing flexibility to adjust the turnon and turnoff strength independently.

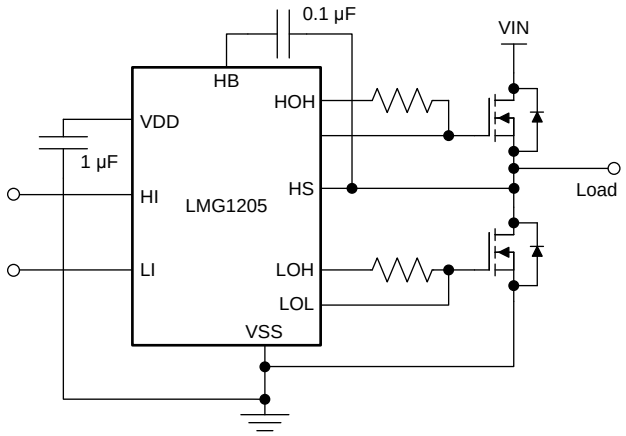
In addition, the strong sink capability of the LMG1205 maintains the gate in the low state, preventing unintended turnon during switching. The LMG1205 can operate up to several MHz. The LMG1205 is available in a 12-pin DSBGA package that offers a compact footprint and minimized package inductance.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMG1205	DSBGA (12)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



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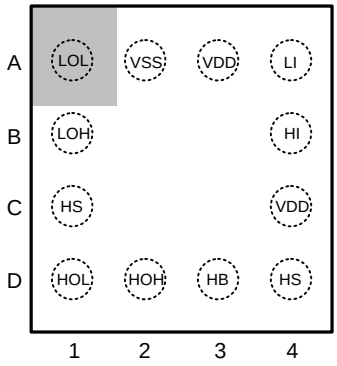
4 Revision History

DATE	REVISION	NOTES
March 2017	*	Initial release.

5 Pin Configuration and Functions

YFX Package
12-Pin DSBGA
Top View



Pin Functions

PIN		TYPE (1)	DESCRIPTION
NUMBER	NAME		
A1	LOL	O	Low-side gate driver sink-current output: connect to the gate of the low-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turnoff speed.
A2	VSS	G	Ground return: all signals are referenced to this ground.
A3, C4 (2)	VDD	P	5-V positive gate drive supply: locally decouple to VSS using low ESR/ESL capacitor located as close as possible to the IC.
A4	LI	I	Low-side driver control input. The LMG1205 inputs have TTL type thresholds. Unused inputs must be tied to ground and not left open.
B1	LOH	O	Low-side gate driver source-current output: connect to the gate of high-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turnon speed.
B4	HI	I	High-side driver control input. The LMG1205 inputs have TTL type thresholds. Unused inputs must be tied to ground and not left open.
C1, D4 (2)	HS	P	High-side GaN FET source connection: connect to the bootstrap capacitor negative terminal and the source of the high-side GaN FET.
D1	HOL	O	High-side gate driver turnoff output: connect to the gate of high-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turnoff speed.
D2	HOH	O	High-side gate driver turnon output: connect to the gate of high-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turnon speed.
D3	HB	P	High-side gate driver bootstrap rail: connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The bootstrap capacitor must be placed as close as possible to the IC.

(1) I = Input, O = Output, G = Ground, P = Power
(2) A3 and C4, C1 and D4 are internally connected

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VDD to VSS	–0.3	7	V
HB to HS	–0.3	7	V
LI or HI input	–0.3	15	V
LOH, LOL output	–0.3	VDD +0.3	V
HOH, HOL output	V_{HS} – 0.3	V_{HB} +0.3	V
HS to VSS	–5	93	V
HB to VSS	0	100	V
Operating junction temperature		150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VDD	4.5		5.5	V
LI or HI input	0		14	V
HS	–5		90	V
HB	V_{HS} + 4		V_{HS} + 5.5	V
HS slew rate			50	V/ns
Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMG1205 YFX (DSBGA) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Specifications are T_J = 25°C. Unless otherwise specified: V_{DD} = V_{HB} = 5 V, V_{SS} = V_{HS} = 0 V.
No load on LOL and HOL or HOH and HOL(1).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENTS							
I_{DD}	VDD quiescent current	LI = HI = 0 V, V_{DD} = V_{HB} = 4 V	T_J = 25°C		0.09		mA
			T_J = –40°C to 125°C			0.12	
I_{DDO}	VDD operating current	f = 500 kHz	T_J = 25°C		2		mA
			T_J = –40°C to 125°C			3	
I_{HB}	Total HB quiescent current	LI = HI = 0 V, V_{DD} = V_{HB} = 4 V	T_J = 25°C		0.10		mA
			T_J = –40°C to 125°C			0.12	
I_{HBO}	Total HB operating current	f = 500 kHz	T_J = 25°C		1.5		mA
			T_J = –40°C to 125°C			2.5	
I_{HBS}	HB to VSS quiescent current	HS = HB = 80 V	T_J = 25°C		0.1		µA
			T_J = –40°C to 125°C			8	
I_{HBSO}	HB to VSS operating current	f = 500 kHz	T_J = 25°C		0.4		mA
			T_J = –40°C to 125°C			1	
INPUT PINS							
V_{IR}	Input voltage threshold	Rising edge	T_J = 25°C		2.06		V
			T_J = –40°C to 125°C	1.89		2.18	
V_{IF}	Input voltage threshold	Falling edge	T_J = 25°C		1.66		V
			T_J = –40°C to 125°C	1.48		1.76	
V_{IHYS}	Input voltage hysteresis				400		mV
R_I	Input pulldown resistance	T_J = 25°C			200		kΩ
		T_J = –40°C to 125°C		100		300	
UNDERVOLTAGE PROTECTION							
V_{DDR}	VDD rising threshold	T_J = 25°C			3.8		V
		T_J = –40°C to 125°C		3.2		4.5	
V_{DDH}	VDD threshold hysteresis				0.2		V
V_{HBR}	HB rising threshold	T_J = 25°C			3.2		V
		T_J = –40°C to 125°C		2.5		3.9	
V_{HBH}	HB threshold hysteresis				0.2		V
BOOTSTRAP DIODE AND CLAMP							
V_{DL}	Low-current forward voltage	I_{VDD-HB} = 100 µA	T_J = 25°C		0.45		V
			T_J = –40°C to 125°C			0.65	
V_{DH}	High-current forward voltage	I_{VDD-HB} = 100 mA	T_J = 25°C		0.9		V
			T_J = –40°C to 125°C			1	
R_D	Dynamic resistance	I_{VDD-HB} = 100 mA	T_J = 25°C		1.85		Ω
			T_J = –40°C to 125°C			3.6	
	HB-HS clamp regulation voltage		T_J = 25°C		5		V
			T_J = –40°C to 125°C	4.5		5.25	

(1) Parameters that show only a typical value are ensured by design and may not be tested in production.

Electrical Characteristics (continued)

Specifications are T_J = 25°C. Unless otherwise specified: V_{DD} = V_{HB} = 5 V, V_{SS} = V_{HS} = 0 V.
No load on LOL and HOL or HOH and HOL(1).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LOW- and HIGH-SIDE GATE DRIVER							
V_{OL}	Low-level output voltage	I_{HOL} = I_{LOL} = 100 mA	T_J = 25°C		0.06		V
			T_J = –40°C to 125°C			0.1	
V_{OH}	High-level output voltage V_{OH} = VDD – LOH or V_{OH} = HB – HOH	I_{HOH} = I_{LOH} = 100 mA	T_J = 25°C		0.21		V
			T_J = –40°C to 125°C			0.31	
I_{OHL}	Peak source current	HOH, LOH = 0 V			1.2		A
I_{OLL}	Peak sink current	HOL, LOL = 5 V			5		A

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{LPHL}	LO turnoff propagation delay	LI falling to LOL falling	T_J = 25°C		33.5		ns
			T_J = –40°C to 125°C			50	
t_{LPLH}	LO turnon propagation delay	LI rising to LOH rising	T_J = 25°C		35		ns
			T_J = –40°C to 125°C			50	
t_{HPHL}	HO turnoff propagation delay	HI falling to HOL falling	T_J = 25°C		33.5		ns
			T_J = –40°C to 125°C			50	
t_{HPLH}	HO turnon propagation delay	HI rising to HOH rising	T_J = 25°C		35		ns
			T_J = –40°C to 125°C			50	
t_{MON}	Delay matching LO on and HO off	T_J = 25°C			1.5		ns
		T_J = –40°C to 125°C				8	
t_{MOFF}	Delay matching LO off and HO on	T_J = 25°C			1.5		ns
		T_J = –40°C to 125°C				8	
t_{HRC}	HO rise time (0.5 V – 4.5 V)	C_L = 1000 pF			7		ns
t_{LRC}	LO rise time (0.5 V – 4.5 V)	C_L = 1000 pF			7		ns
t_{HFC}	HO fall time (0.5 V – 4.5 V)	C_L = 1000 pF			3.5		ns
t_{LFC}	LO fall time (0.5 V – 4.5 V)	C_L = 1000 pF			3.5		ns
t_{PW}	Minimum input pulse width that changes the output				10		ns
t_{BS}	Bootstrap diode reverse recovery time	I_F = 100 mA, I_R = 100 mA			40		ns

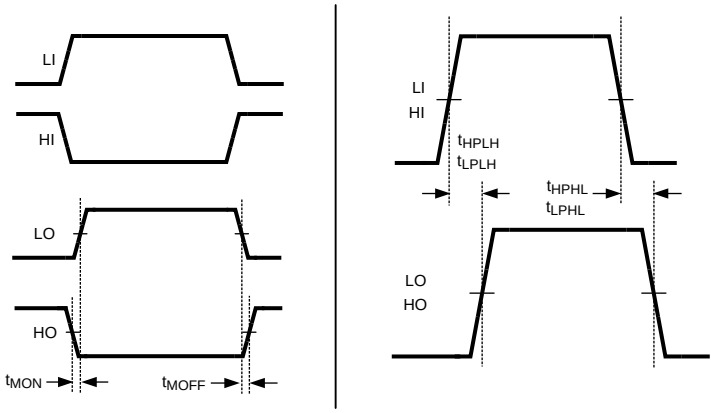


Figure 1. Timing Diagram

6.7 Typical Characteristics

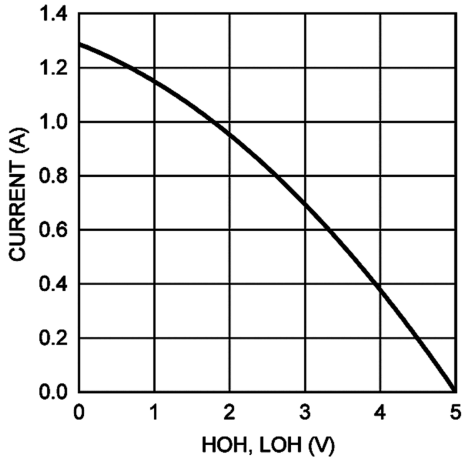


Figure 2. Peak Source Current vs Output Voltage

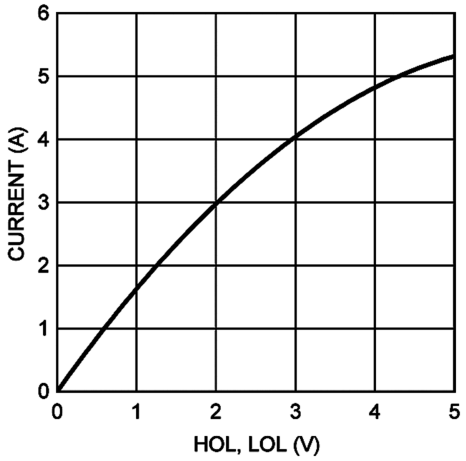


Figure 3. Peak Sink Current vs Output Voltage

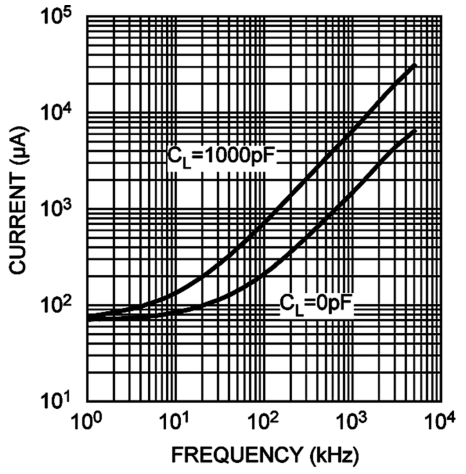


Figure 4. I_{DDO} vs Frequency

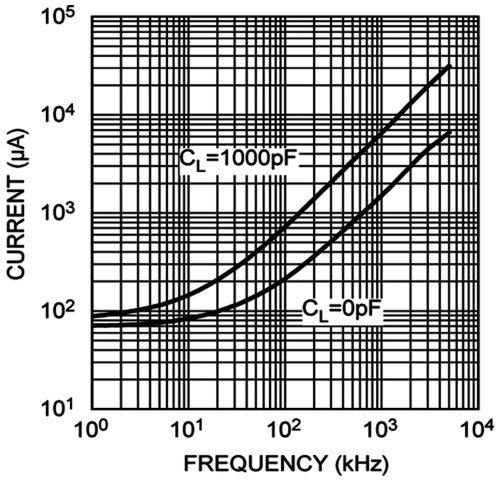


Figure 5. I_{HBO} vs Frequency

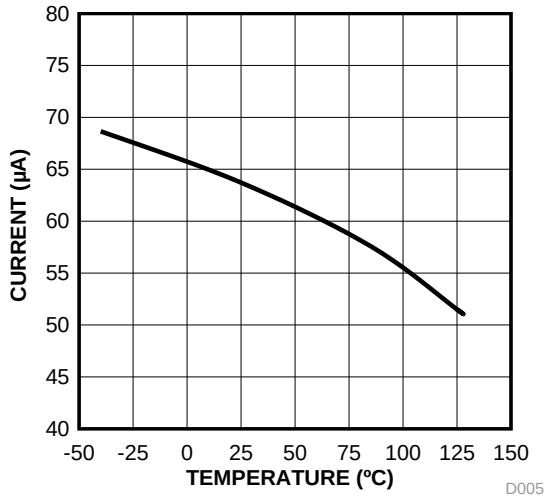


Figure 6. I_{DD} vs Temperature

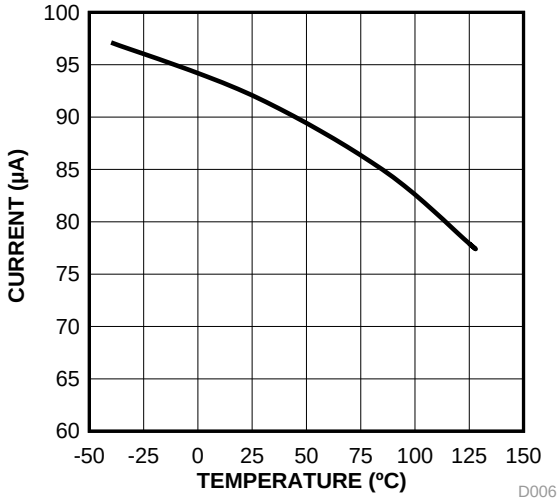


Figure 7. I_{HB} vs Temperature

Typical Characteristics (continued)

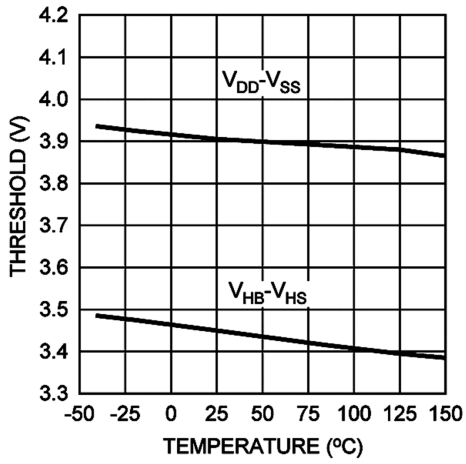


Figure 8. UVLO Rising Thresholds vs Temperature

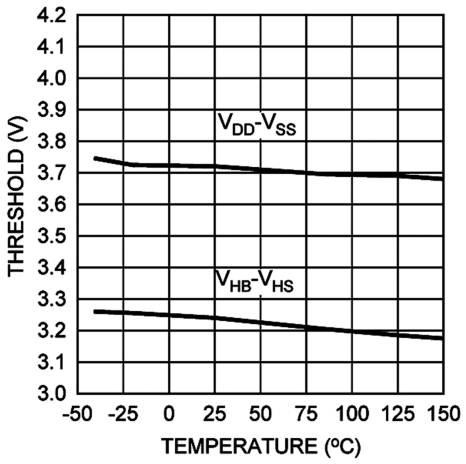


Figure 9. UVLO Falling Thresholds vs Temperature

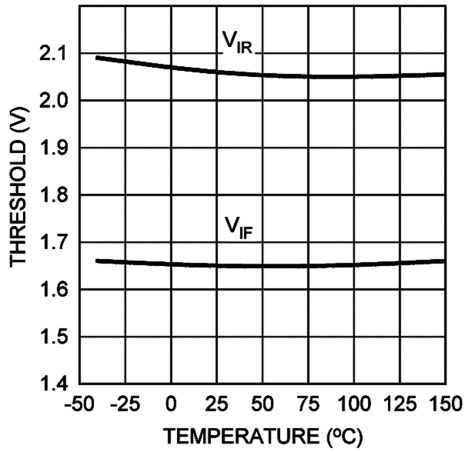


Figure 10. Input Thresholds vs Temperature

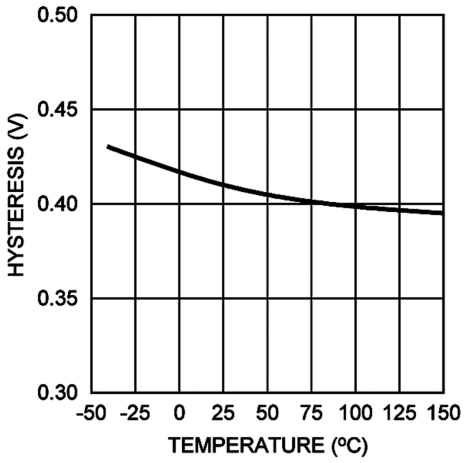


Figure 11. Input Threshold Hysteresis vs Temperature

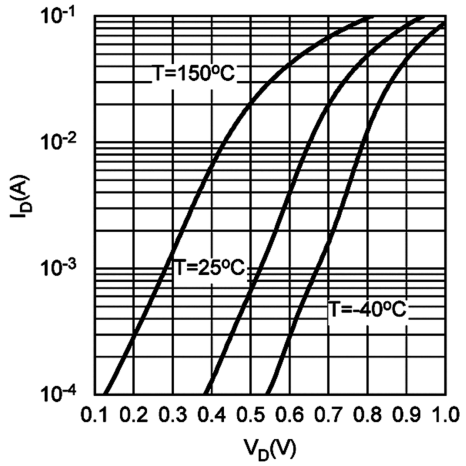


Figure 12. Bootstrap Diode Forward Voltage

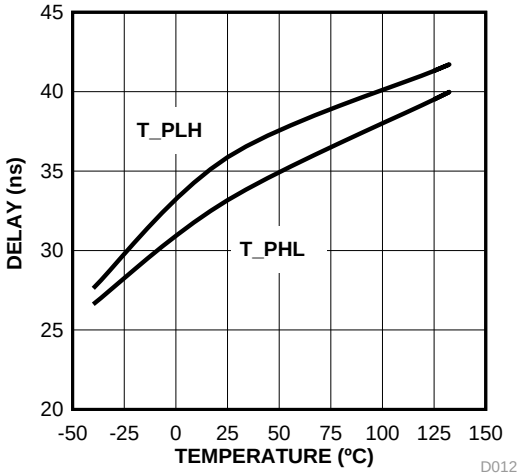


Figure 13. Propagation Delay vs Temperature

Typical Characteristics (continued)

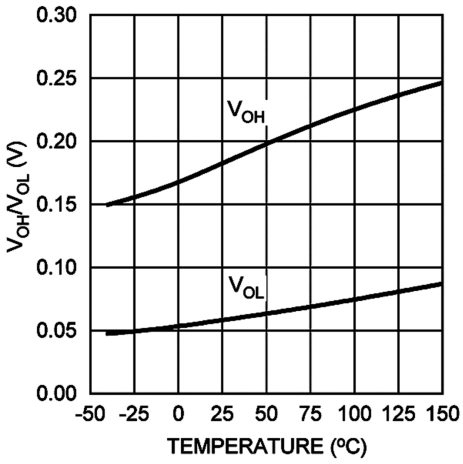


Figure 14. LO & HO Gate Drive – High/Low Level Output Voltage vs Temperature

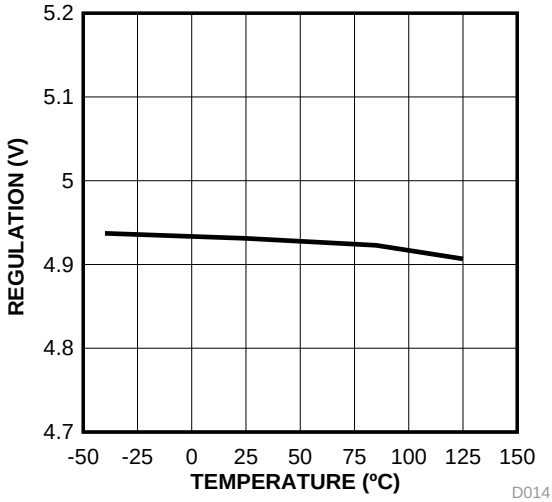


Figure 15. HB Regulation Voltage vs Temperature

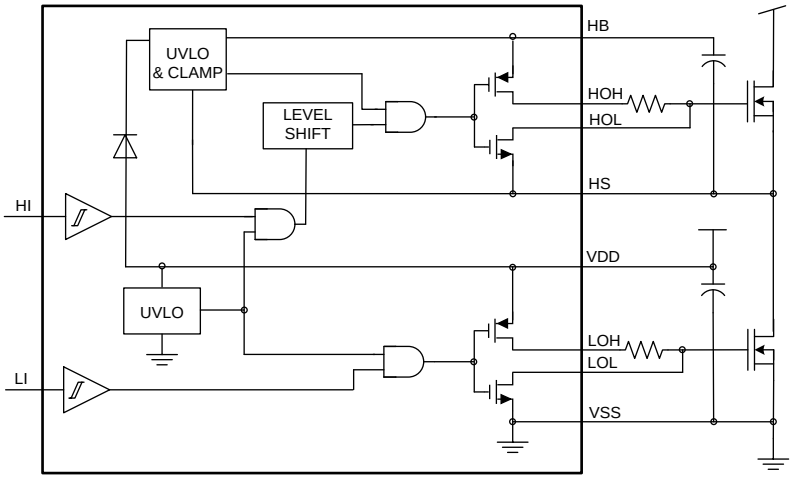
7 Detailed Description

7.1 Overview

The LMG1205 is a high frequency high- and low- side gate driver for enhancement mode Gallium Nitride (GaN) FETs in a synchronous buck, boost, or half-bridge configuration. The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5 V, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of enhancement mode GaN FETs. The LMG1205 has split-gate outputs with strong sink capability, providing flexibility to adjust the turnon and turnoff strength independently.

The LMG1205 can operate up to several MHz, and is available in a 12-pin DSBGA package that offers a compact footprint and minimized package inductance.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input and Output

The input pins of the LMG1205 are independently controlled with TTL input thresholds and can withstand voltages up to 12 V regardless of the VDD voltage. This allows the inputs to be directly connected to the outputs of an analog PWM controller with up to 12-V power supply, eliminating the need for a buffer stage.

The output pulldown and pullup resistance of LMG1205 is optimized for enhancement mode GaN FETs to achieve high frequency and efficient operation. The 0.6-Ω pulldown resistance provides a robust low impedance turnoff path necessary to eliminate undesired turnon induced by high dv/dt or high di/dt. The 2.1-Ω pullup resistance helps reduce the ringing and over-shoot of the switch node voltage. The split outputs of the LMG1205 offers flexibility to adjust the turnon and turnoff speed by independently adding additional impedance in either the turnon path and/or the turnoff path.

If the input signal for either of the the two channels, HI or LI, is not used, the control pin must be tied to either VDD or VSS. These inputs must not be left floating.

7.3.2 Start-up and UVLO

The LMG1205 has an undervoltage lockout (UVLO) on both the VDD and bootstrap supplies. When the VDD voltage is below the threshold voltage of 3.8 V, both the HI and LI inputs are ignored, to prevent the GaN FETs from being partially turned on. Also, if there is insufficient VDD voltage, the UVLO actively pulls the LOL and HOL low. When the VDD voltage is above its UVLO threshold, but the HB to HS bootstrap voltage is below the UVLO threshold of 3.2 V, only HOL is pulled low. Both UVLO threshold voltages have 200 mV of hysteresis to avoid chattering.

Feature Description (continued)

Table 1. VDD UVLO Feature Logic Operation

CONDITION (V_{HB-HS} > V_{HBR} for all cases below)	HI	LI	HO	LO
V_{DD} - V_{SS} < V_{DDR} during device start-up	H	L	L	L
V_{DD} - V_{SS} < V_{DDR} during device start-up	L	H	L	L
V_{DD} - V_{SS} < V_{DDR} during device start-up	H	H	L	L
V_{DD} - V_{SS} < V_{DDR} during device start-up	L	L	L	L
V_{DD} - V_{SS} < V_{DDR} - V_{DDH} after device start-up	H	L	L	L
V_{DD} - V_{SS} < V_{DDR} - V_{DDH} after device start-up	L	H	L	L
V_{DD} - V_{SS} < V_{DDR} - V_{DDH} after device start-up	H	H	L	L
V_{DD} - V_{SS} < V_{DDR} - V_{DDH} after device start-up	L	L	L	L

Table 2. V_{HB-HS} UVLO Feature Logic Operation

CONDITION (V_{DD} > V_{DDR} for all cases below)	HI	LI	HO	LO
V_{HB-HS} < V_{HBR} during device start-up	H	L	L	L
V_{HB-HS} < V_{HBR} during device start-up	L	H	L	H
V_{HB-HS} < V_{HBR} during device start-up	H	H	L	H
V_{HB-HS} < V_{HBR} during device start-up	L	L	L	L
V_{HB-HS} < V_{HBR} - V_{HBH} after device start-up	H	L	L	L
V_{HB-HS} < V_{HBR} - V_{HBH} after device start-up	L	H	L	H
V_{HB-HS} < V_{HBR} - V_{HBH} after device start-up	H	H	L	H
V_{HB-HS} < V_{HBR} - V_{HBH} after device start-up	L	L	L	L

7.3.3 HS Negative Voltage and Bootstrap Supply Voltage Clamping

Due to the intrinsic nature of enhancement mode GaN FETs, the source-to-drain voltage of the bottom switch is usually higher than a diode forward voltage drop when the gate is pulled low. This causes negative voltage on HS pin. Moreover, this negative voltage transient may become even more pronounced due to the effects of board layout and device drain/source parasitic inductances. With high-side driver using the floating bootstrap configuration, negative HS voltage can lead to an excessive bootstrap voltage, which can damage the high-side GaN FET. The LMG1205 solves this problem with an internal clamping circuit that prevents the bootstrap voltage from exceeding 5 V typical.

7.3.4 Level Shift

The level-shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output, which is referenced to the HS pin and provides excellent delay matching with the low-side driver. Typical delay matching between LO and HO is around 1.5 ns.

7.4 Device Functional Modes

Table 3 shows the device truth table.

Table 3. Truth Table

HI	LI	HOH	HOL	LOH	LOL
L	L	Open	L	Open	L
L	H	Open	L	H	Open
H	L	H	Open	Open	L
H	H	H	Open	H	Open

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

To operate GaN transistors at very high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the GaN transistor. Also, gate drivers are indispensable when the outputs of the PWM controller do not meet the voltage or current levels needed to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal, which cannot effectively turn on a power switch. A level-shift circuit is needed to boost the 3.3 V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses.

Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also address other needs such as minimizing the effect of high-frequency switching noise (by placing the high-current driver IC physically close to the power switch), driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

The LMG1205 is a MHz high- and low-side gate driver for enhancement mode GaN FETs in a synchronous buck, boost, or half-bridge configuration. The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5 V, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of enhancement mode GaN FETs. The LMG1205 has split-gate outputs with strong sink capability, providing flexibility to adjust the turnon and turnoff strength independently.

8.2 Typical Application

The circuit in Figure 16 shows a synchronous buck converter to evaluate LMG1205. Detailed synchronous buck converter specifications are listed in *Design Requirements*. Optimization of he power loop (loop impedance from VIN capacitor to PGND) is critical to the performance of the design. Having a high power loop inductance causes significant ringing in the SW node and also causes an associated power loss. For more information, please refer to *Related Documentation*.

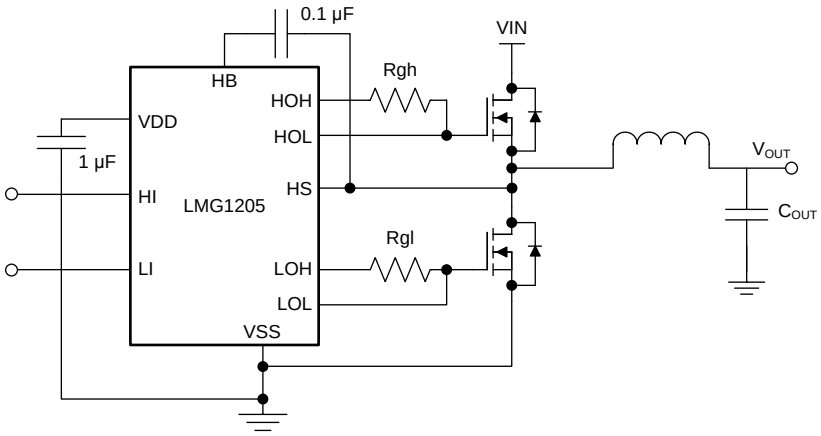


Figure 16. Application Circuit

8.2.1 Design Requirements

When designing a synchronous buck converter application that incorporates the LMG1205 gate driver and GaN power FETs, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are the input voltages, passive components, operating frequency, and controller selection. Table 4 shows some sample values for a typical application. See *Power Supply Recommendations*, *Layout*, and *Power Dissipation* for other key design considerations for the LMG1205.

Table 4. Design Parameters

PARAMETER	SAMPLE VALUE
Half-bridge input supply voltage, V_{IN}	48 V
Output voltage, V_{OUT}	12 V
Output current	8 A
Dead time	8 ns
Inductor	4.7 µH
Switching frequency	1 MHz

8.2.2 Detailed Design Procedure

This procedure outlines the design considerations of LMG1205 in a synchronous buck converter with enhancement mode GaN FET. For additional design help, see *Related Documentation*.

8.2.2.1 VDD Bypass Capacitor

The VDD bypass capacitor provides the gate charge for the low-side and high-side transistors and to absorb the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated with Equation 1.

$$C_{VDD} > \frac{Q_{gH} + Q_{gL} + Q_{rr}}{\Delta V}$$

where

- Q_{gH} and Q_{gL} are gate charge of the high-side and low-side transistors, respectively

- Q_{rr} is the reverse recovery charge of the bootstrap diode, which is typically around 4nC
- ΔV is the maximum allowable voltage drop across the bypass capacitor (1)

TI recommends a 0.1–µF or larger value, good-quality ceramic capacitor. The bypass capacitor must be placed as close as possible to the device pins to minimize the parasitic inductance.

8.2.2.2 Bootstrap Capacitor

The bootstrap capacitor provides the gate charge for the high-side switch, DC bias power for HB undervoltage lockout circuit, and the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated with Equation 2.

$$C_{BST} > \frac{Q_{gH} + I_{HB} \times t_{ON} + Q_{rr}}{\Delta V}$$

where

- I_{HB} is the quiescent current of the high-side driver
- t_{on} is the maximum on-time period of the high-side transistor (2)

A good-quality ceramic capacitor must be used for the bootstrap capacitor. TI recommends placing the bootstrap capacitor as close as possible to the HB and HS pins.

8.2.2.3 Power Dissipation

The power consumption of the driver is an important measure that determines the maximum achievable operating frequency of the driver. It must be kept below the maximum power dissipation limit of the package at the operating temperature. The total power dissipation of the LMG1205 is the sum of the gate driver losses and the bootstrap diode power loss.

The gate driver losses are incurred by charge and discharge of the capacitive load. It can be approximated as

$$P = \left(C_{LoadH} + C_{LoadL}\right) \times V_{DD}^2 \times f_{SW}$$

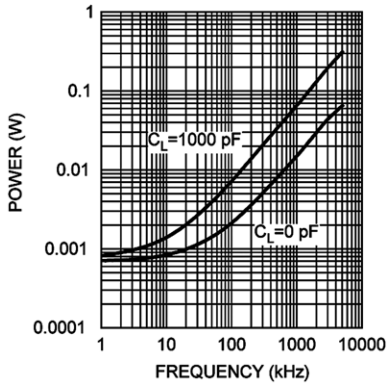
where

- C_{LoadH} and C_{LoadL} are the high-side and the low-side capacitive loads, respectively (3)

It can also be calculated with the total input gate charge of the high-side and the low-side transistors as

$$P = \left(Q_{gH} + Q_{gL}\right) \times V_{DD} \times f_{SW} \quad (4)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. Figure 17 shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equations. Figure 17 can be used to approximate the power losses due to the gate drivers.

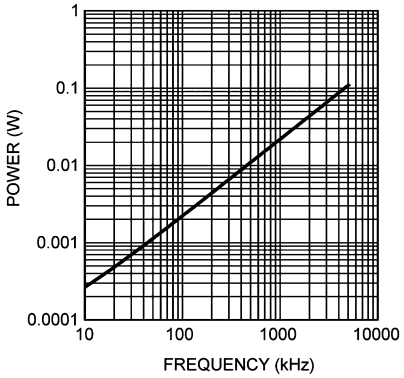


Gate driver power dissipation (LO+HO), VDD = 5 V

Figure 17. Neglecting Bootstrap Diode Losses

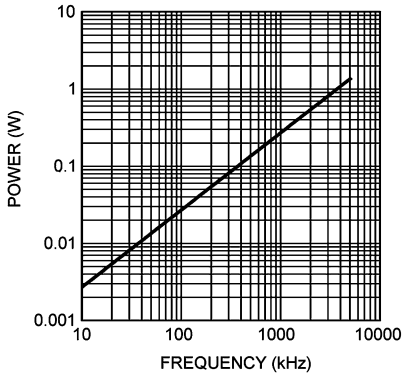
The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Because each of these events happens once per cycle, the diode power loss is proportional to the operating frequency. Larger capacitive loads require more energy to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge also result in higher reverse recovery losses.

Figure 18 and Figure 19the forward bias power loss and the reverse bias power loss of the bootstrap diode respectively. The plots are generated based on calculations and lab measurements of the diode reverse time and current under several operating conditions. Figure 18 and Figure 19 can be used to predict the bootstrap diode power loss under different operating conditions.



The load of high-side driver is a GaN FET with total gate charge of 10 nC.

Figure 18. Forward Bias Power Loss of Bootstrap Diode V_{IN} = 50 V



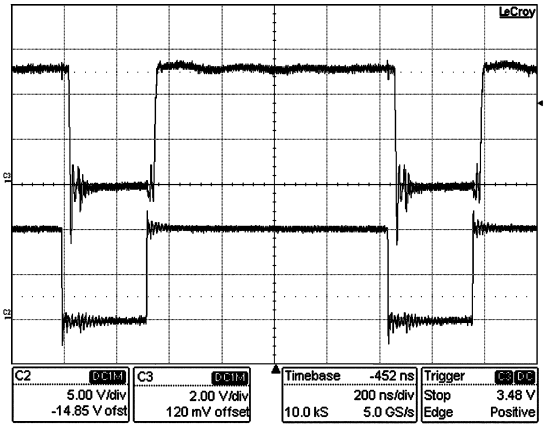
The load of high-side driver is a GaN FET with total gate charge of 10 nC.

Figure 19. Reverse Recovery Power Loss of Bootstrap Diode V_{IN} = 50 V

The sum of the driver loss and the bootstrap diode loss is the total power loss of the IC. For a given ambient temperature, the maximum allowable power loss of the IC can be defined as Equation 5.

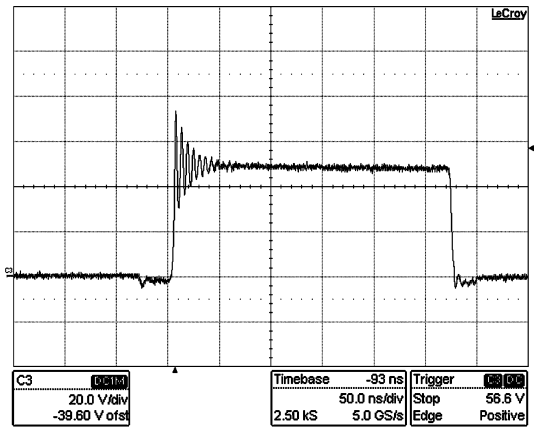
$$P = \frac{(T_J - T_A)}{\theta_{JA}} \quad (5)$$

8.2.3 Application Curves



Conditions:
Input Voltage = 48 V DC, Load Current = 5 A
Traces:
Top Trace: Gate of Low-Side eGaN FET, Volt/div = 2 V
Bottom Trace: LI of LMG1205, Volt/div = 5 V
Bandwidth Limit = 600 MHz
Horizontal Resolution = 0.2 µs/div

Figure 20. Low-Side Driver Input and Output



Conditions:
Input Voltage = 48 V DC,
Load Current = 10 A
Traces:
Trace: Switch-Node Voltage, Volts/div = 20 V
Bandwidth Limit = 600 MHz
Horizontal Resolution = 50 ns/div

Figure 21. Switch-Node Voltage

9 Power Supply Recommendations

The recommended bias supply voltage range for LMG1205 is from 4.5 V to 5.5 V. The lower end of this range is governed by the internal UVLO protection feature of the VDD supply circuit. TI recommends keeping proper margin to allow for transient voltage spikes while not violating the LMG1205 absolute maximum VDD voltage rating and the GaN transistor gate breakdown voltage limit.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the VDD voltage drops, the device continues to operate in normal mode as far as the voltage drop does not exceeds the hysteresis specification, VDDH. If the voltage drop is more than hysteresis specification, the device shuts down. Therefore, while operating at or near the 4.5-V range, the voltage ripple on the VDD power supply output must be smaller than the hysteresis specification of LMG1205 UVLO to avoid triggering device shutdown.

A local bypass capacitor must be placed between the VDD and VSS pins. This capacitor must be located as close as possible to the device. TI recommends a low-ESR, ceramic, surface-mount capacitor. TI also recommends using 2 capacitors across VDD and GND: a 100-nF ceramic surface-mount capacitor for high frequency filtering placed very close to VDD and GND pin, and another surface-mount capacitor, 220 nF to 10 µF, for IC bias requirements.

10 Layout

10.1 Layout Guidelines

Small gate capacitance and Miller capacitance enable enhancement mode GaN FETs to operate with fast switching speed. The induced high dv/dt and di/dt, coupled with a low gate threshold voltage and limited headroom of enhancement mode GaN FETs gate voltage, make the circuit layout crucial to the optimum performance. Following are some recommendations:

1. The first priority in designing the layout of the driver is to confine the high peak currents that charge and discharge the GaN FETs gate into a minimal physical area. This decreases the loop inductance and minimize noise issues on the gate terminal of the GaN FETs. The GaN FETs must be placed close to the driver.
2. The second high current path includes the bootstrap capacitor, the local ground referenced VDD bypass capacitor and low-side GaN FET. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
3. The parasitic inductance in series with the source of the high-side FET and the low-side FET can impose excessive negative voltage transients on the driver. TI recommends connecting the HS pin and VSS pin to the respective source of the high-side and low-side transistors with a short and low-inductance path.
4. The parasitic source inductance, along with the gate capacitor and the driver pull-down path, can form an LCR resonant tank, resulting in gate voltage oscillations. An optional resistor or ferrite bead can be used to damp the ringing.
5. Low ESR/ESL capacitors must be connected close to the IC, between VDD and VSS pins and between the HB and HS pins to support the high peak current being drawn from VDD during turnon of the FETs. Keeping bullet #1 (minimized GaN FETs gate driver loop) as the first priority, it is also desirable to place the VDD decoupling capacitor and the HB to HS bootstrap capacitor on the same side of the PC board as the driver. The inductance of vias can impose excessive ringing on the IC pins.
6. To prevent excessive ringing on the input power bus, good decoupling practices are required by placing low-ESR ceramic capacitors adjacent to the GaN FETs.

Figure 22 and Figure 23 show recommended layout patterns for the LMG1205. Two cases are considered: (1) without any gate resistors, and (2) with an optional turnon gate resistor. Note that 0402 surface mount package is assumed for the passive components in the drawings. For information on DSBGA package assembly, refer to *Related Documentation*.

10.2 Layout Examples

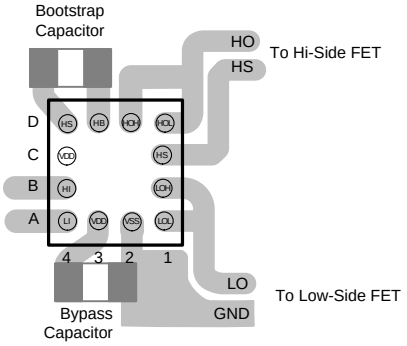


Figure 22. Layout Example Without Gate Resistors

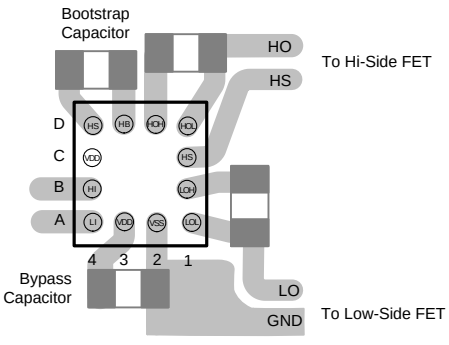


Figure 23. Layout Example with HOH and LOH Gate Resistors

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *AN-1112 DSBGA Wafer Level Chip Scale Package*
- *Using the LMG1205HBEVM GaN Half-Bridge EVM*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMG1205YFXR	ACTIVE	DSBGA	YFX	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1205	Samples
LMG1205YFXT	ACTIVE	DSBGA	YFX	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1205	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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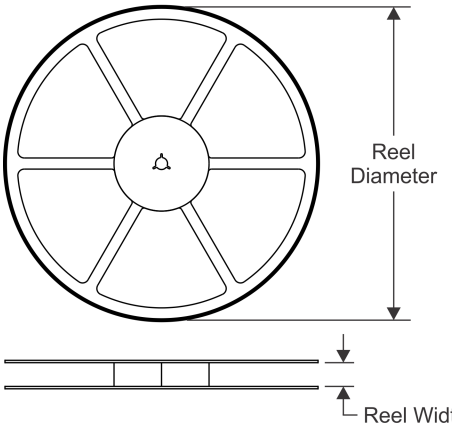
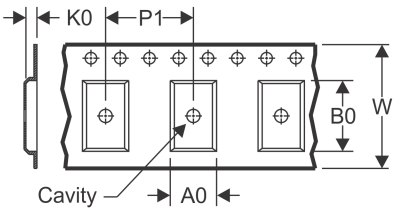
TAPE AND REEL INFORMATION

REEL DIMENSIONS

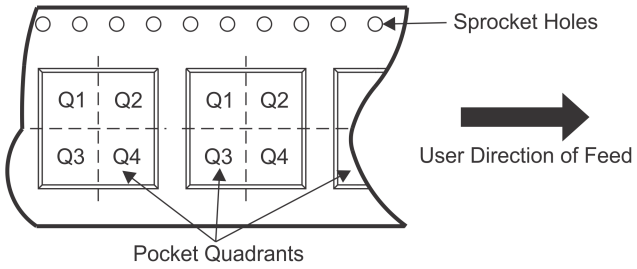


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

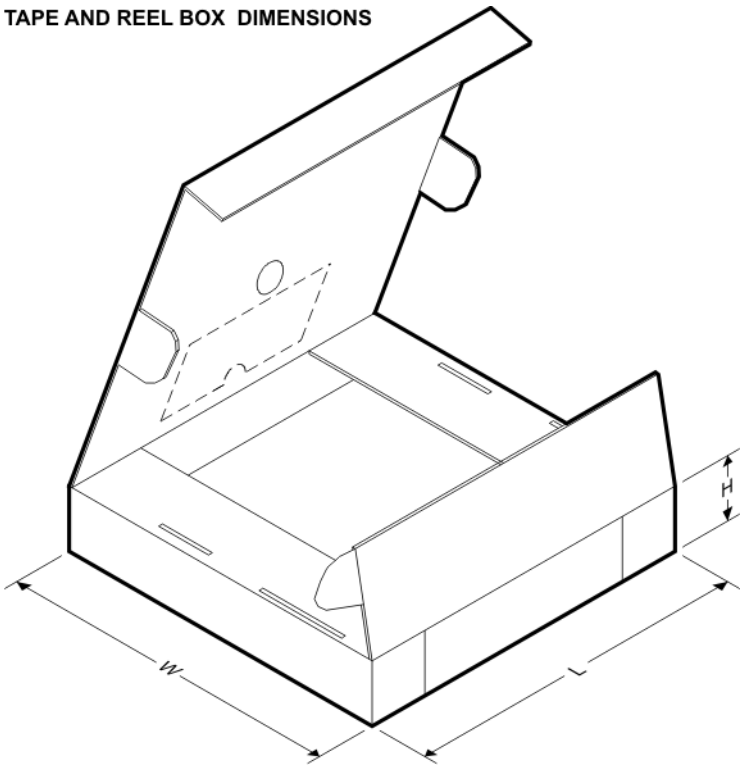
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG1205YFXR	DSBGA	YFX	12	3000	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1
LMG1205YFXT	DSBGA	YFX	12	250	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1

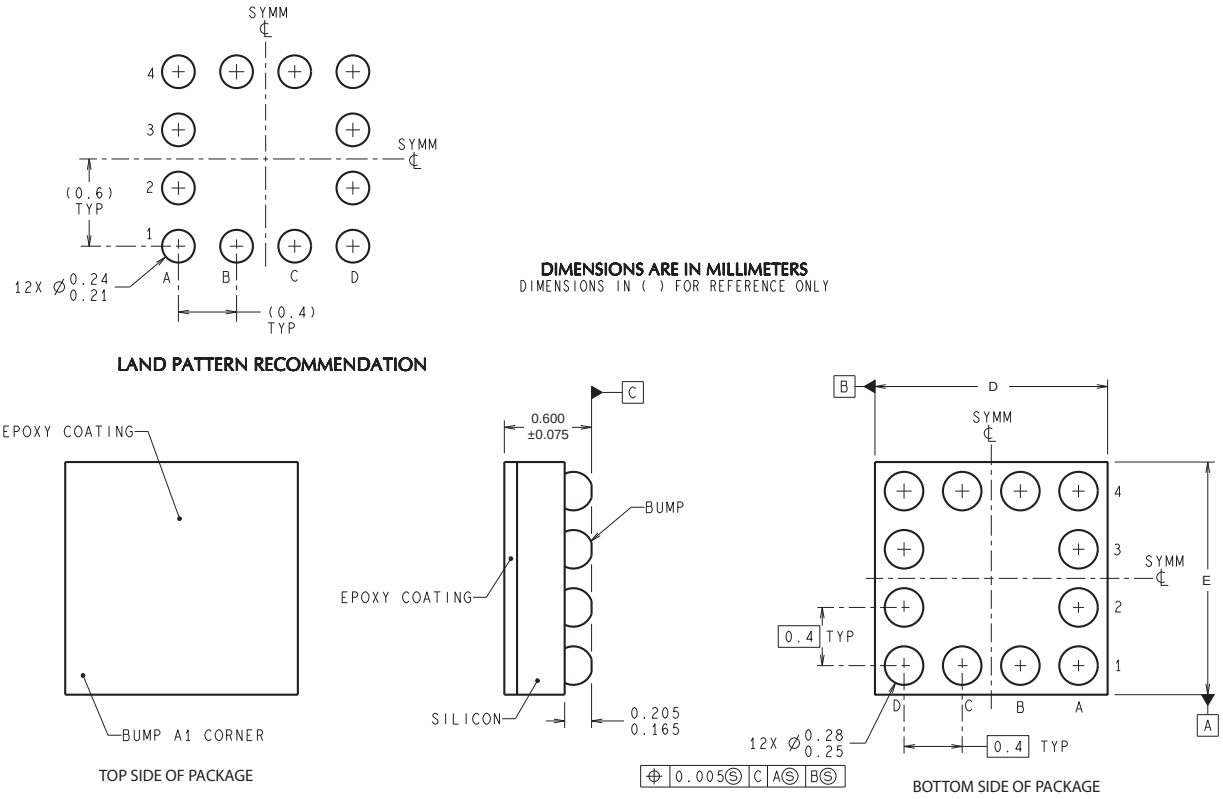
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG1205YFXR	DSBGA	YFX	12	3000	210.0	185.0	35.0
LMG1205YFXT	DSBGA	YFX	12	250	210.0	185.0	35.0

YFX0012



D: Max = 1.905 mm, Min =1.845 mm

E: Max = 1.756 mm, Min =1.695 mm

4215094/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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