LM4871 Boomer® Audio Power Amplifier Series 3W Audio Power Amplifier with Shutdown Mode

Check for Samples: LM4871

FEATURES

- **No Output Coupling Capacitors, Bootstrap Capacitors, or Snubber Circuits Required**
- **Unity-gain Stable**
- **WSON, VSSOP, SOIC, or PDIP Packaging**
- **External Gain Configuration Capability**
- **Pin Compatible with the LM4861**

APPLICATIONS

- **Portable Computers**
- **Desktop Computers**
- **Low Voltage Audio Systems**

KEY SPECIFICATIONS

- **PO at 10% THD+N, 1kHz**
  - **LM4871LD: 3Ω , 4Ω Loads; 3W (typ), 2.5 W (typ)**
  - **All other LM4871 Packages: 8Ω load 1.5 W (typ)**
- **Shutdown Current 0.6µA (typ)**
- **Supply Voltage Range 2.0V to 5.5 V**
- **THD at 1kHz at 1W Continuous Average Output Power into 8Ω 0.5% (max)**

DESCRIPTION

The LM4871 is a mono bridged audio power amplifier capable of delivering 3W of continuous average power into a 3Ω load with less than 10% THD when powered by a 5V power supply (see Note). To conserve power in portable applications, the LM4871's micropower shutdown mode (I_Q = 0.6µA, typ) is activated when V_{DD} is applied to the SHUTDOWN pin.

Boomer audio power amplifiers are designed specifically to provide high power, high fidelity audio output. They require few external components and operate on low supply voltages from 2.0V to 5.5V. Since the LM4871 does not require output coupling capacitors, bootstrap capacitors, or snubber networks, it is ideally suited for low-power portable systems that require minimum volume and weight.

Additional LM4871 features include thermal shutdown protection, unity-gain stability, and external gain set.

Note: An LM4871LD that has been properly mounted to a circuit board will deliver 3W into 3Ω (at 10% THD). The other package options for the LM4871 will deliver 1.5W into 8Ω (at 10% THD). See the Application Information section for further information concerning the LM4871LD, LM4871MM, LM4871M, and the LM4871N.

Connection Diagrams

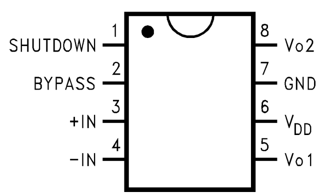


Figure 1. VSSOP, Small Outline, and PDIP Package Top View See Package Number DGK0008A, D0008A, or D0008E

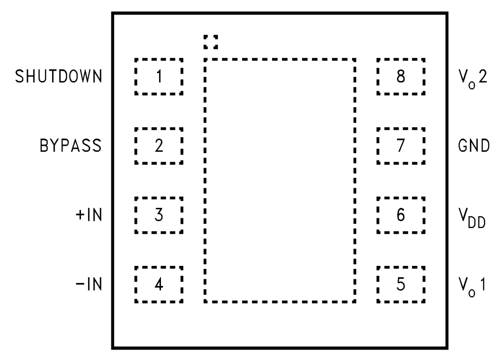


Figure 2. WSON Package (Top View) See Package Number NGN0008A

Typical Application

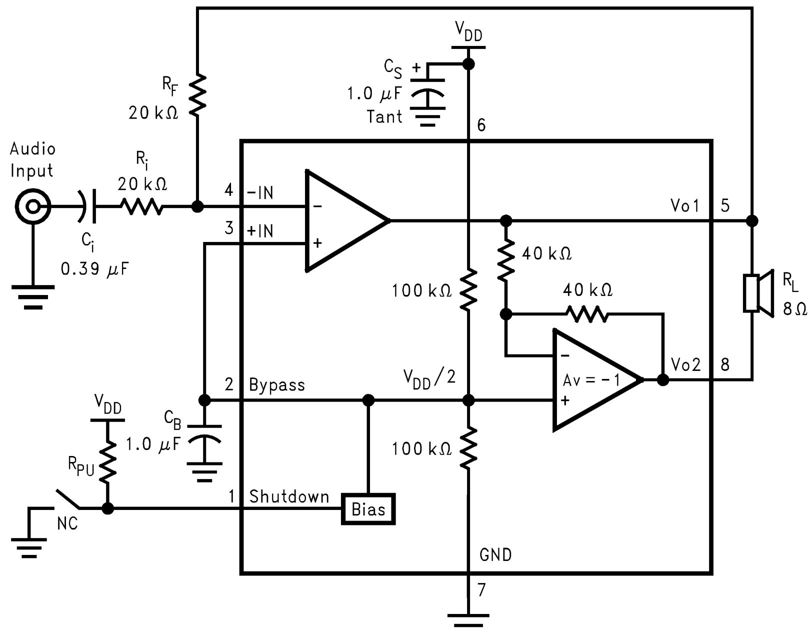


Figure 3. Typical Audio Amplifier Application Circuit

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage			6.0V
Supply Temperature			−65°C to +150°C
Input Voltage			−0.3V to V_{DD} to +0.3V
Power Dissipation[3]			Internally Limited
ESD Susceptibility[4]			5000V
ESD Susceptibility[5]			250V
Junction Temperature			150°C
Soldering Information	Small Outline Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C
$θ_{JC}$ (typ)—D0008A			35°C/W
$θ_{JA}$ (typ)—D0008A			140°C/W
$θ_{JC}$ (typ)—D0008E			37°C/W
$θ_{JA}$ (typ)—D0008E			107°C/W
$θ_{JC}$ (typ)—DGK0008A			56°C/W
$θ_{JA}$ (typ)—DGK0008A			210°C/W
$θ_{JC}$ (typ)—NGN0008A			4.3°C/W
$θ_{JA}$ (typ)—NGN0008A			56°C/W[6]

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, $θ_{JA}$, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/θ_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4871, T_{JMAX} = 150°C. For the $θ_{JA}$'s for different packages, please see the Application Information section or the absolute maximum ratings section.
(4) Human body model, 100pF discharged through a 1.5kΩ resistor.
(5) Machine Model, 220pF–240pF discharged through all pins.
(6) The given $θ_{JA}$ is for an LM4871 packaged in an NGN0008A with the Exposed–DAP soldered to an exposed 1in^2 area of 1oz printed circuit board copper.

Operating Ratings

Temperature Range $T_{MIN} ≤ T_A ≤ T_{MAX}$	$−40°C ≤ T_A ≤ 85°C$
Supply Voltage	$2.0V ≤ V_{DD} ≤ 5.5V$

Electrical Characteristics[1][2]

The following specifications apply for V_{DD} = 5V and R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4871			Units (Limits)
			Min[3]	Typical[4]	Limit[3]	
V_{DD}	Supply Voltage		2.0		5.5	V
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A		6.5	10.0	mA
I_{SD}	Shutdown Current	$V_{PIN1} = V_{DD}$		0.6	2	µA
V_{OS}	Output Offset Voltage	V_{IN} = 0V		5.0	50	mV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typicals are specified at 25°C and represent the parametric norm.
(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).

Electrical Characteristics[1][2] (continued)

The following specifications apply for V_{DD} = 5V and R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4871			Units (Limits)
			Min[3]	Typical[4]	Limit[3]	
P_o	Output Power	THD = 1%, f = 1kHz LM4871LD, R_L = 3Ω[5] LM4871LD, R_L = 4Ω[5] LM4871, R_L = 8Ω[5]		2.38 2 1.2		W
		THD+N = 10%, f = 1kHz LM4871LD, R_L = 3Ω[5] LM4871LD, R_L = 4Ω[5] LM4871, R_L = 8Ω[5]		3 2.5 1.5		W
THD+N	Total Harmonic Distortion+Noise	20Hz ≤ f ≤ 20kHz, A_{VD} = 2 LM4871LD, R_L = 4Ω, P_O = 1.6W LM4871, R_L = 8Ω, P_O = 1W		0.13 0.25		%
PSRR	Power Supply Rejection Ratio	V_{DD} = 4.9V to 5.1V		60		dB

(5) When driving 3Ω or 4Ω loads from a 5V supply, the LM4871LD must be mounted to a circuit board.

External Components Description

(Figure 3)

Components		Functional Description
1.	R_i	Inverting input resistance that sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_i at f_C= 1/(2π R_iC_i).
2.	C_i	Input coupling capacitor that blocks the DC voltage at the amplifiers input terminals. Also creates a highpass filter with R_i at f_c = 1/(2π R_iC_i). Refer to the section, Proper Selection of External Components, for an explanation of how to determine the value of C_i.
3.	R_f	Feedback resistance that sets the closed-loop gain in conjunction with R_i.
4.	C_S	Supply bypass capacitor that provides power supply filtering. Refer to the Power Supply Bypassing section for information concerning proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor that provides half-supply filtering. Refer to the section, Proper Selection of External Components, for information concerning proper placement and selection of C_B.

Typical Performance Characteristics
NGN Specific Characteristics

LM4871LD THD+N vs Output Power

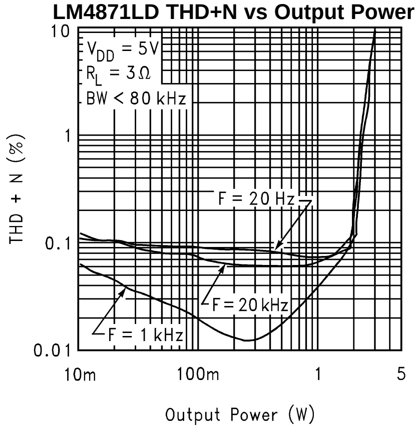


Figure 4.

LM4871LD THD+N vs Frequency

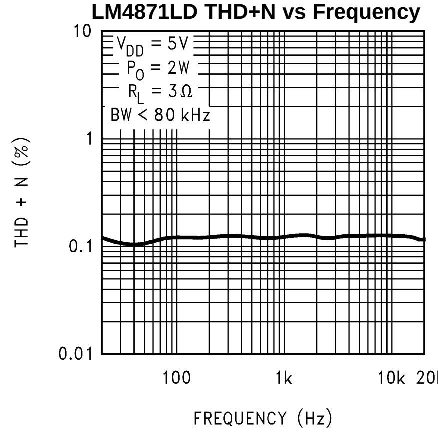


Figure 5.

LM4871LD THD+N vs Frequency

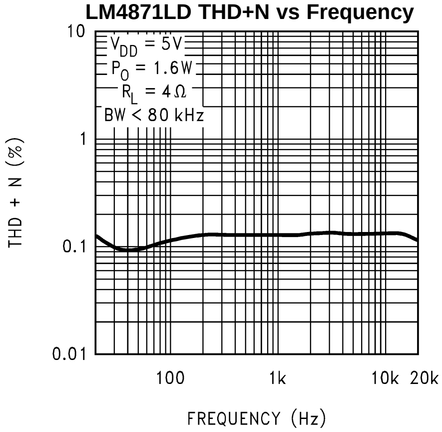


Figure 6.

LM4871LD THD+N vs Output Power

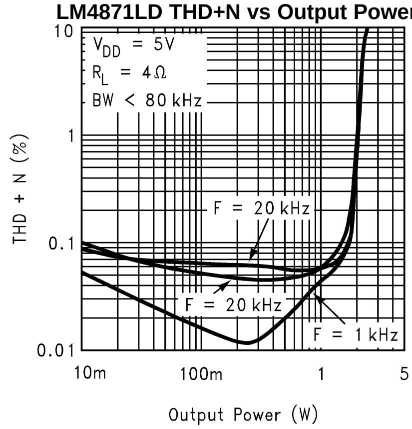


Figure 7.

LM4871LD Power Dissipation vs Output Power

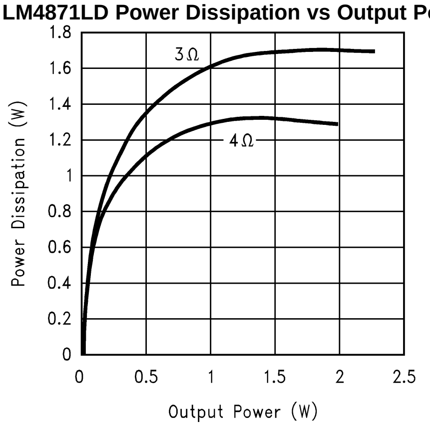
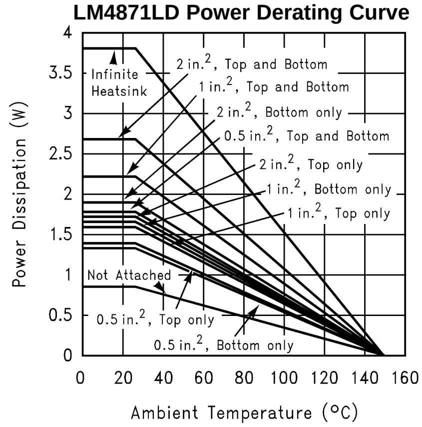


Figure 8.

LM4871LD Power Derating Curve



This curve shows the LM4871LD's thermal dissipation ability at different ambient temperatures given the exposed-DAP of the part is soldered to a plane of 1oz. Cu with an area given in the label of each curve. This label also designates whether the plane exists on the same (top) layer as the chip, on the bottom layer, or on both layers. Infinite heatsink and unattached (no heatsink) conditions are also shown.

Figure 9.

Typical Performance Characteristics
Non-NGN Specific Characteristics

THD+N vs Frequency

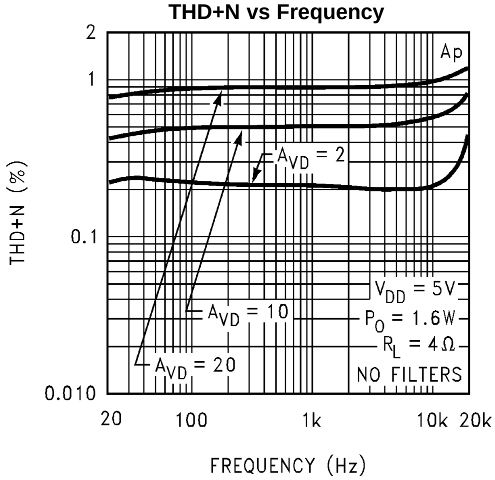


Figure 10.

THD+N vs Frequency

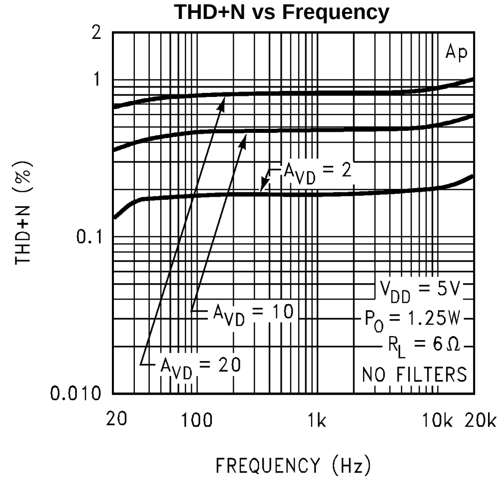


Figure 11.

THD+N vs Frequency

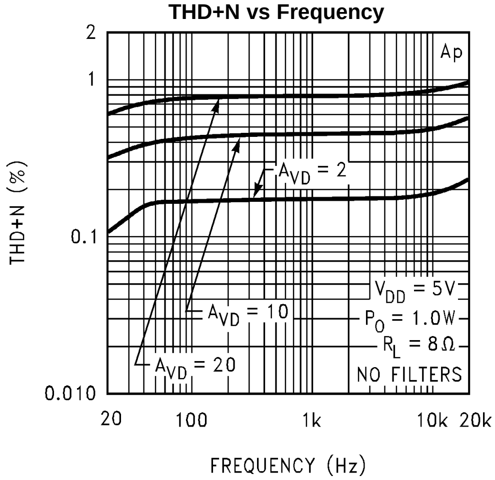


Figure 12.

THD+N vs Output Power

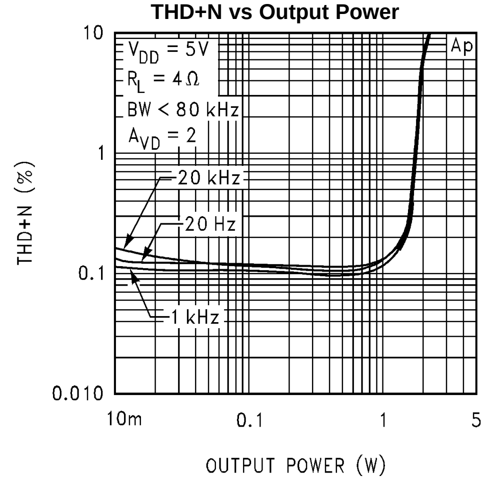


Figure 13.

THD+N vs Output Power

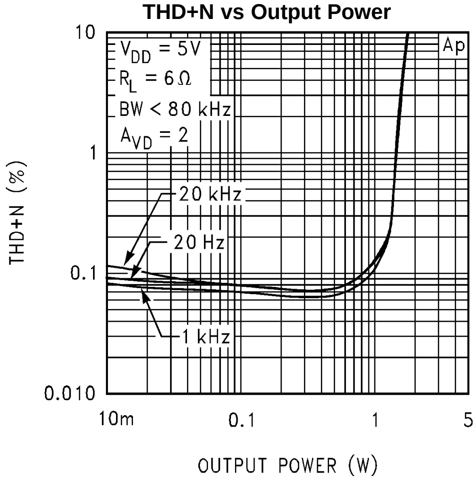


Figure 14.

THD+N vs Output Power

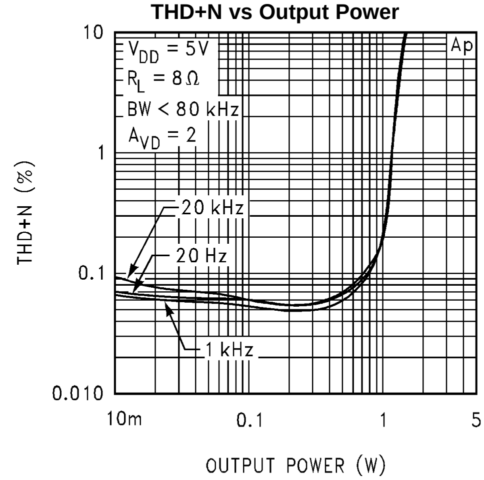


Figure 15.

Typical Performance Characteristics
Non-NGN Specific Characteristics (continued)

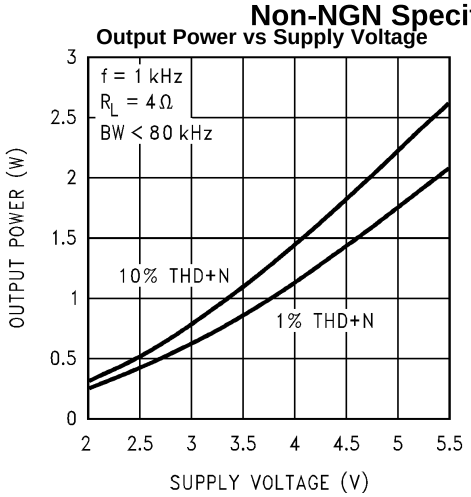


Figure 16.

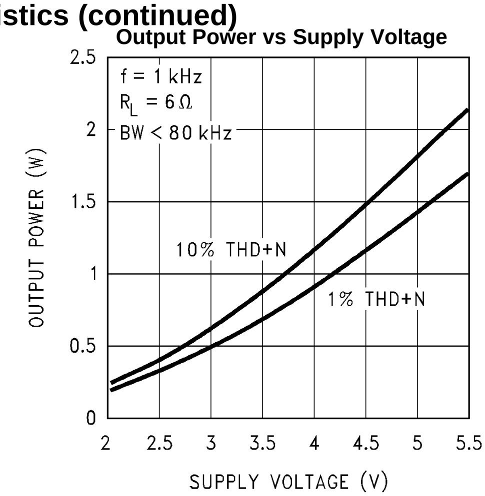


Figure 17.

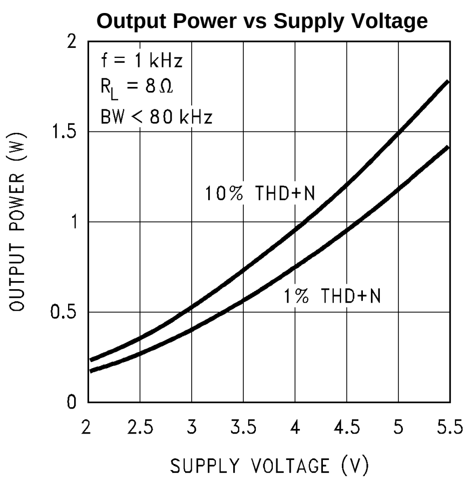


Figure 18.

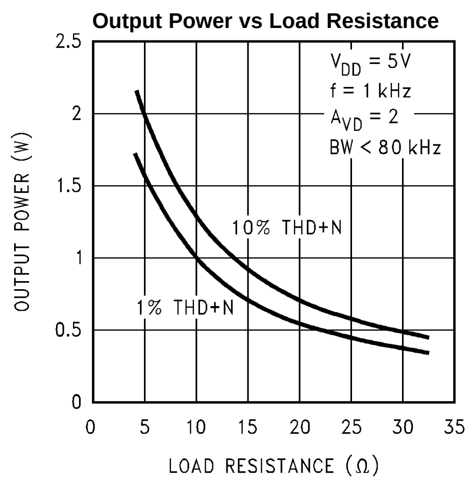


Figure 19.

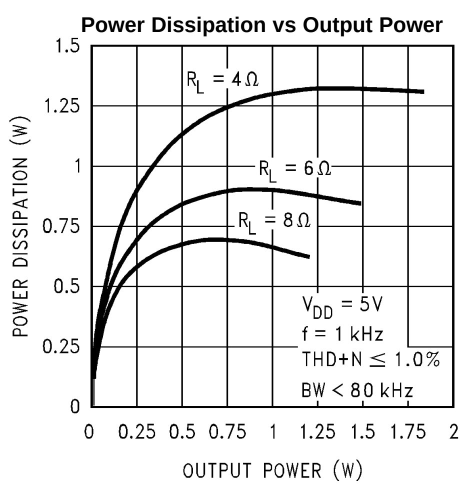


Figure 20.

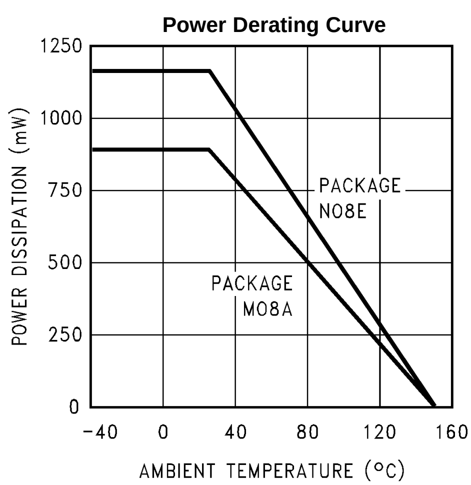


Figure 21.

Typical Performance Characteristics
Non-NGN Specific Characteristics (continued)

Clipping Voltage vs Supply Voltage

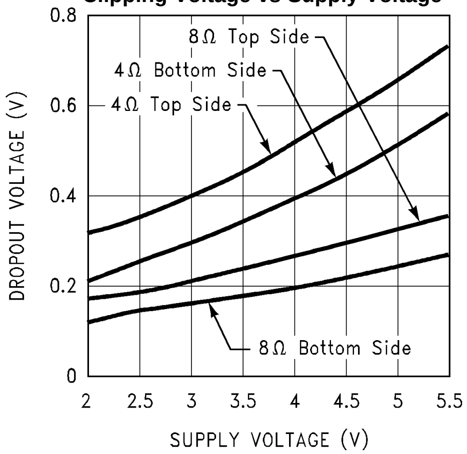


Figure 22.

Noise Floor

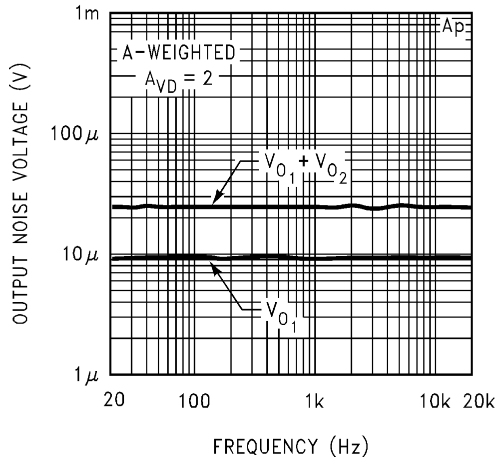


Figure 23.

Frequency Response vs Input Capacitor Size

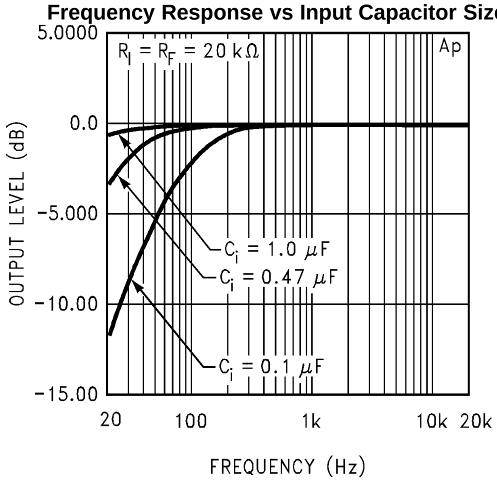


Figure 24.

Power Supply Rejection Ratio

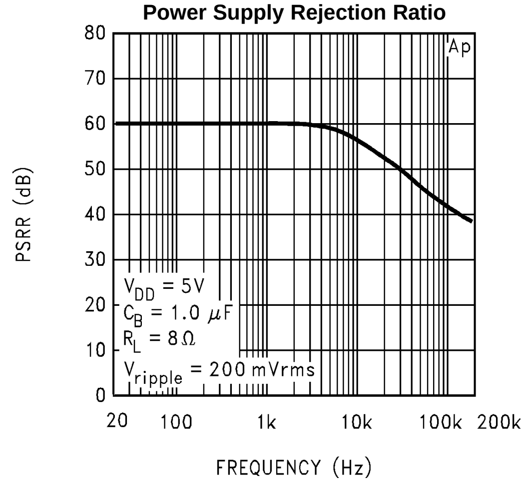


Figure 25.

Open Loop Frequency Response

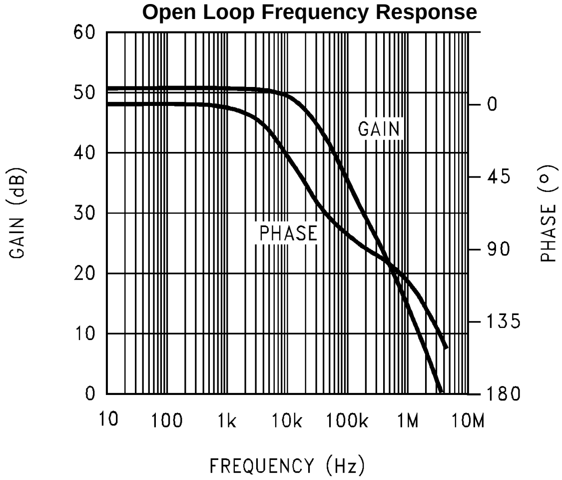


Figure 26.

Supply Current vs Supply Voltage

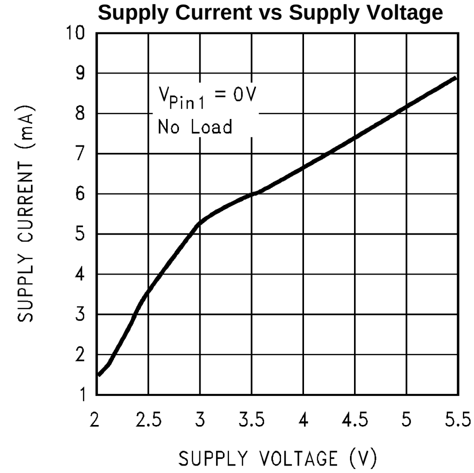


Figure 27.

APPLICATION INFORMATION

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATION

The LM4871's exposed-DAP (die attach paddle) package (NGN) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane, and surrounding air. The result is a low voltage audio power amplifier that produces 2W at ≤ 1% THD with a 4Ω load. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4871's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The NGN package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with 4(2x2) vias. The via diameter should be 0.012in-0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plating through the vias.

Best thermal performance is achieved with the largest practical heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in^2 area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4871 should be 5in^2 (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. Increase the area to compensate for ambient temperatures above 25°C. The LM4871's power de-rating curve in the Typical Performance Characteristics shows the maximum power dissipation versus temperature. An example PCB layout for the NGN package is shown in the Demonstration Board Layout section. Further detailed and specific information concerning PCB layout, fabrication, and mounting an NGN (WSON) package is available from TI's Package Engineering Group under application note AN-1187 (Literature Number SNOA401).

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependant on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.0W to 1.95W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 3, the LM4871 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable; the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 40kΩ resistors. Figure 3 shows that the output of amplifier one serves as the input to amplifier two, which results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Consequently, the differential gain for the IC is

$$A_{VD} = 2 *(R_f/R_i) \quad (1)$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as “bridged mode” is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of its load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the Audio Power Amplifier Design section.

Another advantage of the differential bridge output is no net DC voltage across load. This results from biasing V_O1 and V_O2 at the same DC voltage, in this case $V_{DD}/2$. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single supply amplifier's half-supply bias voltage across the load. The current flow created by the half-supply bias voltage increases internal IC power dissipation and my permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Equation 2 states the maximum power dissipation point for a bridge amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad (2)$$

Since the LM4871 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended ampifier. Even with this substantial increase in power dissipation, the LM4871 does not require heatsinking under most operating conditions and output loading. From Equation 2, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 625 mW. The maximum power dissipation point obtained from Equation 2 must not be greater than the power dissipation that results from Equation 3:

$$P_{DMAX} = (T_{JMAX} – T_A)/\theta_{JA} \quad (3)$$

For the SOIC package, θ_{JA} = 140°C/W, for the PDIP package, θ_{JA} = 107°C/W, and for the VSSOP package, θ_{JA} = 210°C/W assuming free air operation. For the NGN package soldered to a DAP pad that expands to a copper area of 1.0in^2 on a PCB, the LM4871's θ_{JA} is 56°C/W. T_{JMAX} = 150°C for the LM4871. The θ_{JA} can be decreased by using some form of heat sinking. The resultant θ_{JA} will be the summation of the θ_{JC}, θ_{CS}, and θ_{SA}. θ_{JC} is the junction to case of the package (or to the exposed DAP, as is the case with the NGN package), θ_{CS} is the case to heat sink thermal resistance and θ_{SA} is the heat sink to ambient thermal resistance. By adding additional copper area around the LM4871, the θ_{JA} can be reduced from its free air value for the SOIC and VSSOP packages. Increasing the copper area around the NGN package from 1.0in^2 to 2.0in^2 area results in a θ_{JA} decrease to 46°C/W. Depending on the ambient temperature, T_A, and the θ_{JA}, Equation 3 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 2 is greater than that of Equation 3, then either the supply voltage must be decreased, the load impedance increased, the θ_{JA} decreased, or the ambient temperature reduced. For the typical application of a 5V power supply, with an 8Ω load, and no additional heatsinking, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 61°C provided that device operation is around the maximum power dissipation point and assuming surface mount packaging. For the NGN package in a typical application of a 5V power supply, with a 4Ω load, and 1.0in^2 copper area soldered to the exposed DAP pad, the maximum ambient temperature is approximately 77°C providing device operation is around the maximum power dissipation point. Internal power dissipation is a function of output power. If typical operation is not around the maximum power dissipation point, the ambient temperature can be increased. Refer to the Typical Performance Characteristics curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the LM4871 as possible. The capacitor connected between the bypass pin and ground improves the internal bias voltage's stability, producing improved PSRR. The improvements to PSRR increase as the bypass pin capacitor increases. Typical applications employ a 5V regulator with 10µF and a 0.1µF bypass capacitors which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4871 with a 1µF tantalum capacitor. The selection of bypass capacitors, especially C_B, is dependent upon PSRR requirements, click and pop performance as explained in the section, Proper Selection of External Components, system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4871 contains a shutdown pin to externally turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when a logic high is placed on the shutdown pin. The trigger point between a logic low and logic high level is typically half- supply. It is best to switch between ground and supply to provide maximum device performance. By switching the shutdown pin to V_{DD}, the LM4871 supply current draw will be minimized in idle mode. While the device will be disabled with shutdown pin voltages less then V_{DD}, the idle current may be greater than the typical value of 0.6µA. In either case, the shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry which provides a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor. When the switch is closed, the shutdown pin is connected to ground and enables the amplifier. If the switch is open, then the external pull-up resistor will disable the LM4871. This scheme ensures that the shutdown pin will not float thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4871 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4871 is unity-gain stable which gives a designer maximum system flexibility. The LM4871 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 Vrms are available from sources such as audio codecs. Please refer to the section, Audio Power Amplifier Design, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Audio Power Amplifier Design. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Selection Of Input Capacitor Size

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, $C_{i.}$ A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the LM4871 turns on. The slower the LM4871's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0µF is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

Design a 1W/8Ω Audio Amplifier

Given:	
Power Output	1 Wrms
Load Impedance	8Ω
Input Level	1 Vrms
Input Impedance	20 kΩ
Bandwidth	100 Hz–20 kHz ± 0.25 dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the Typical Performance Characteristics section, the supply rail can be easily found. A second way to determine the minimum supply rail is to calculate the required V_{opeak} using Equation 4 and add the output voltage. Using this method, the minimum supply voltage would be (V_{opeak} + (V_{ODTOP} + V_{ODBOT})), where V_{ODBOT} and V_{ODTOP} are extrapolated from the Dropout Voltage vs Supply Voltage curve in the Typical Performance Characteristics section.

$$V_{opeak} = \sqrt{(2R_LP_O)} \quad (4)$$

Using the Output Power vs Supply Voltage graph for an 8Ω load, the minimum supply rail is 4.6V. But since 5V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4871 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the POWER DISSIPATION section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 5.

$$A_{VD} \geq \sqrt{(P_OR_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (5)$$

$$R_f/R_i = A_{VD}/2 \quad (6)$$

From Equation 5, the minimum A_{VD} is 2.83; use A_{VD} = 3.

Since the desired input impedance was 20kΩ, and with a A_{VD} impedance of 2, a ratio of 1.5:1 of R_f to R_i results in an allocation of R_i = 20kΩ and R_f = 30kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of −3dB frequency points. Five times away from a −3dB point is 0.17dB down from passband response which is better than the required ±0.25dB specified.

f_L = 100Hz/5 = 20Hz

f_H = 20kHz * 5 = 100kHz

As stated in the External Components Description section, R_i in conjunction with C_i create a highpass filter.

C_i ≥ 1/(2π*20kΩ*20Hz) = 0.397µF; use 0.39µF

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With a A_{VD} = 3 and f_H = 100kHz, the resulting GBWP = 150kHz which is much smaller than the LM4871 GBWP of 4MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LM4871 can still be used without running into bandwidth limitations.

Demonstration Board Layout

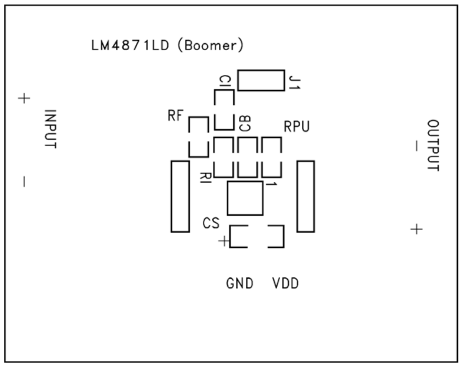


Figure 28. Recommended NGN PC Board Layout: Component-Side Silkscreen

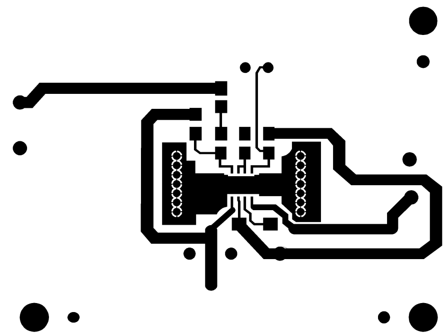


Figure 29. Recommended NGN PC Board Layout: Component-Side Layout

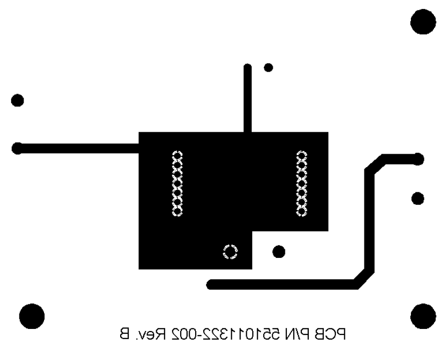


Figure 30. Recommended NGN PC Board Layout: Bottom-Side Layout

LM4871 MDA MWA 3W Audio Power Amplifier With Shutdown Mode

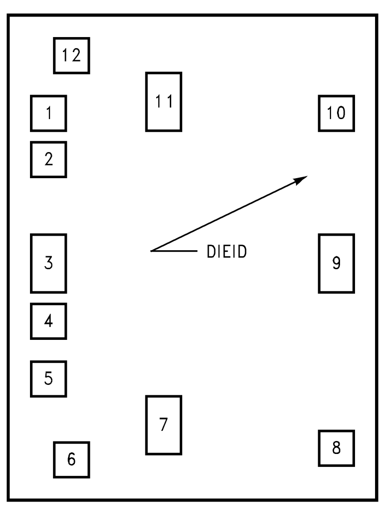


Figure 31. Die Layout (C - Step)

Die/Wafer Characteristics

Fabrication Attributes		**General Die Information**	
Physical Die Identification	LM4871C	Bond Pad Opening Size (min)	102µm x 102µm
Die Step	C	Bond Pad Metalization	0.5% COPPER_BAL. ALUMINUM
Physical Attributes		Passivation	NITRIDE
Wafer Diameter	150mm	Back Side Metal	BARE BACK
Dise Size (Drawn)	1372µm x 1758µm 54mils x 69mils	Back Side Connection	GND
Thickness	406µm Nominal		
Min Pitch	164µm Nominal		

Special Assembly Requirements:
Note: Actual die size is rounded to the nearest micron.

Die Bond Pad Coordinate Locations (C - Step)						
(Referenced to die center, coordinates in µm) NC = No Connection						
SIGNAL NAME	PAD# NUMBER	X/Y COORDINATES		PAD SIZE		
		X	Y	X		Y
SHUTDOWN	1	-559	541	102	x	102
BYPASS	2	-559	376	102	x	102
NC	3	-559	-45	102	x	210
INPUT +	4	-559	-248	102	x	102
INPUT -	5	-559	-486	102	x	102
GND	6	-476	-725	102	x	102
VOUT 1	7	-135	-598	102	x	210
GND	8	554	-686	102	x	102
VDD	9	554	-4	102	x	210
GND	10	554	568	102	x	102
VOUT 2	11	-135	598	102	x	210
GND	12	-473	752	102	x	102

REVISION HISTORY

Changes from Revision E (May 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4871LD	ACTIVE	WSON	NGN	8	1000	TBD	Call TI	Call TI	-40 to 85	L4871	Samples
LM4871LD/NOPB	ACTIVE	WSON	NGN	8	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	L4871	Samples
LM4871LDX/NOPB	ACTIVE	WSON	NGN	8	4500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	L4871	Samples
LM4871M	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	4871	Samples
LM4871M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	4871	Samples
LM4871MM	ACTIVE	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	G71	Samples
LM4871MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	G71	Samples
LM4871MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	G71	Samples
LM4871MX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	4871	Samples
LM4871MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	4871	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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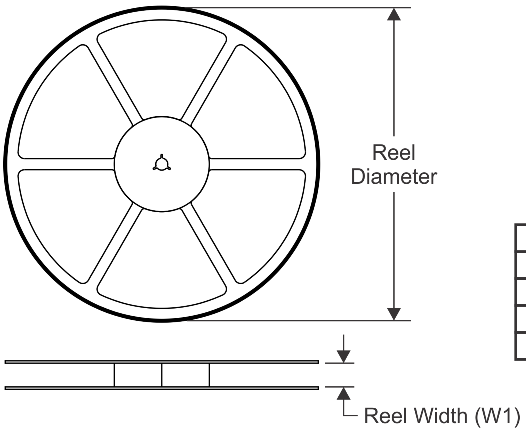
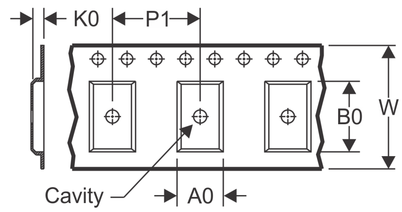
TAPE AND REEL INFORMATION

REEL DIMENSIONS

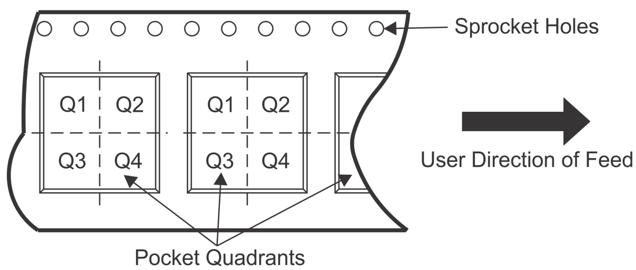


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

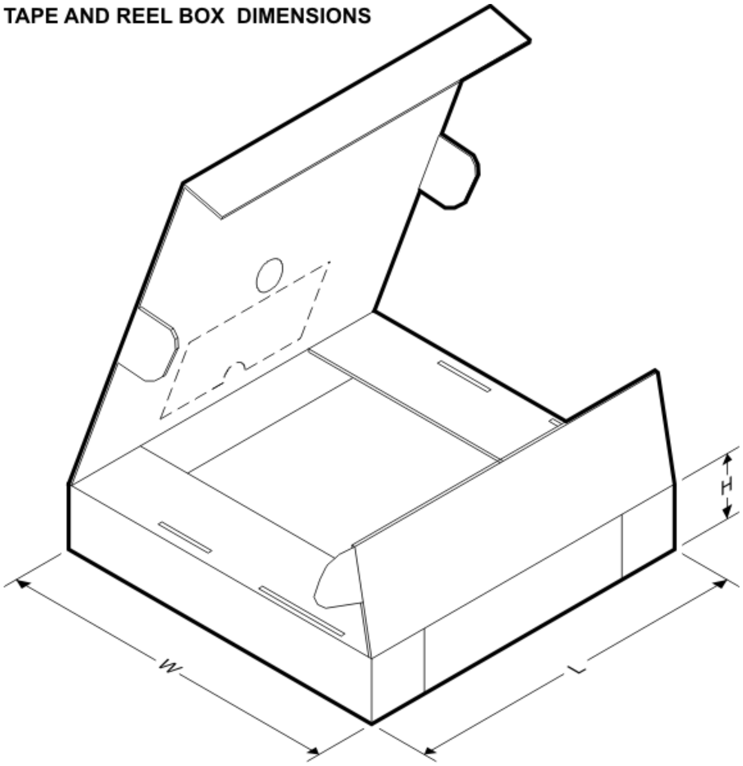
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4871LD	WSON	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM4871LD/NOPB	WSON	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM4871LDX/NOPB	WSON	NGN	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM4871MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4871MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4871MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4871MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4871MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

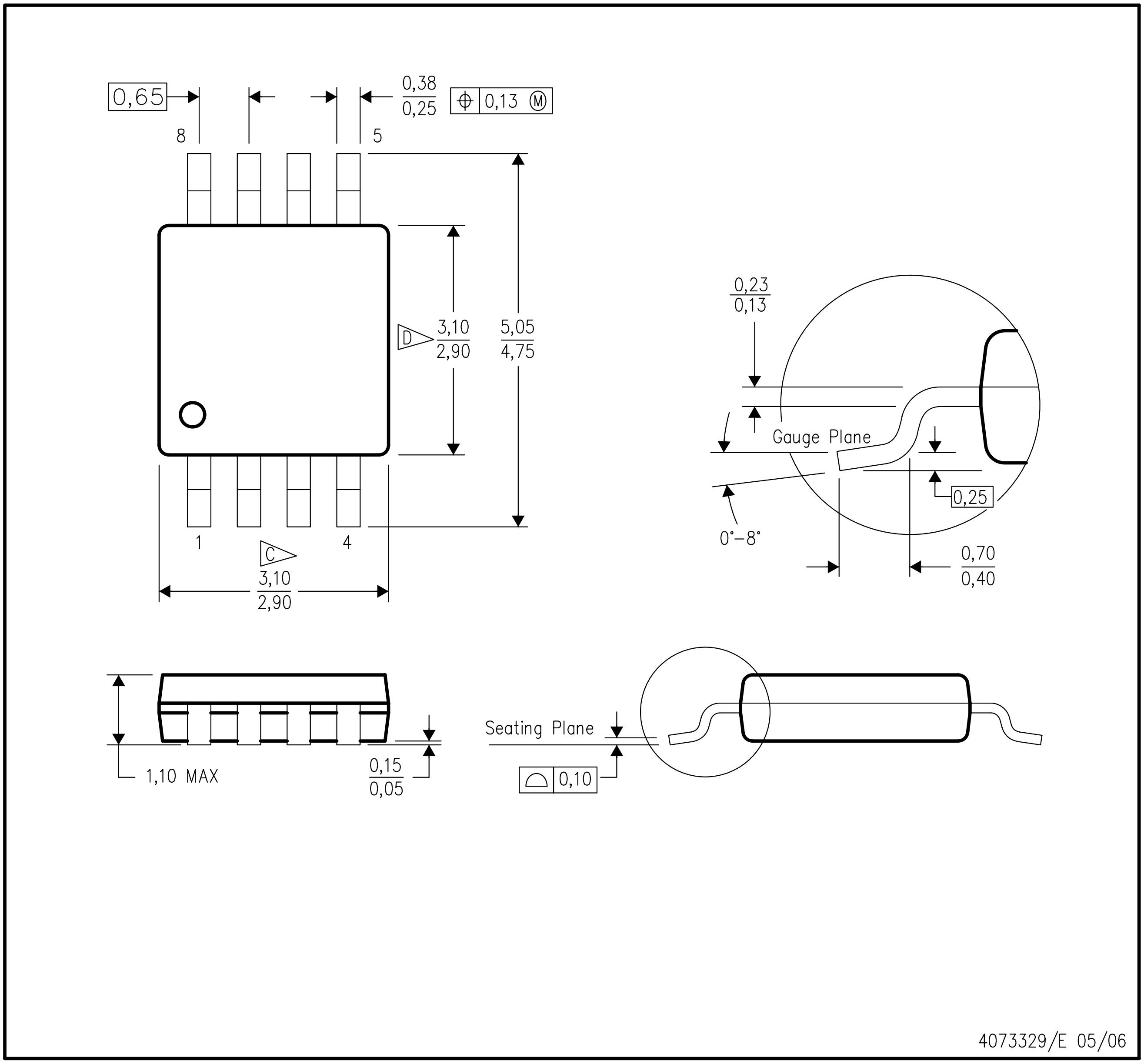
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

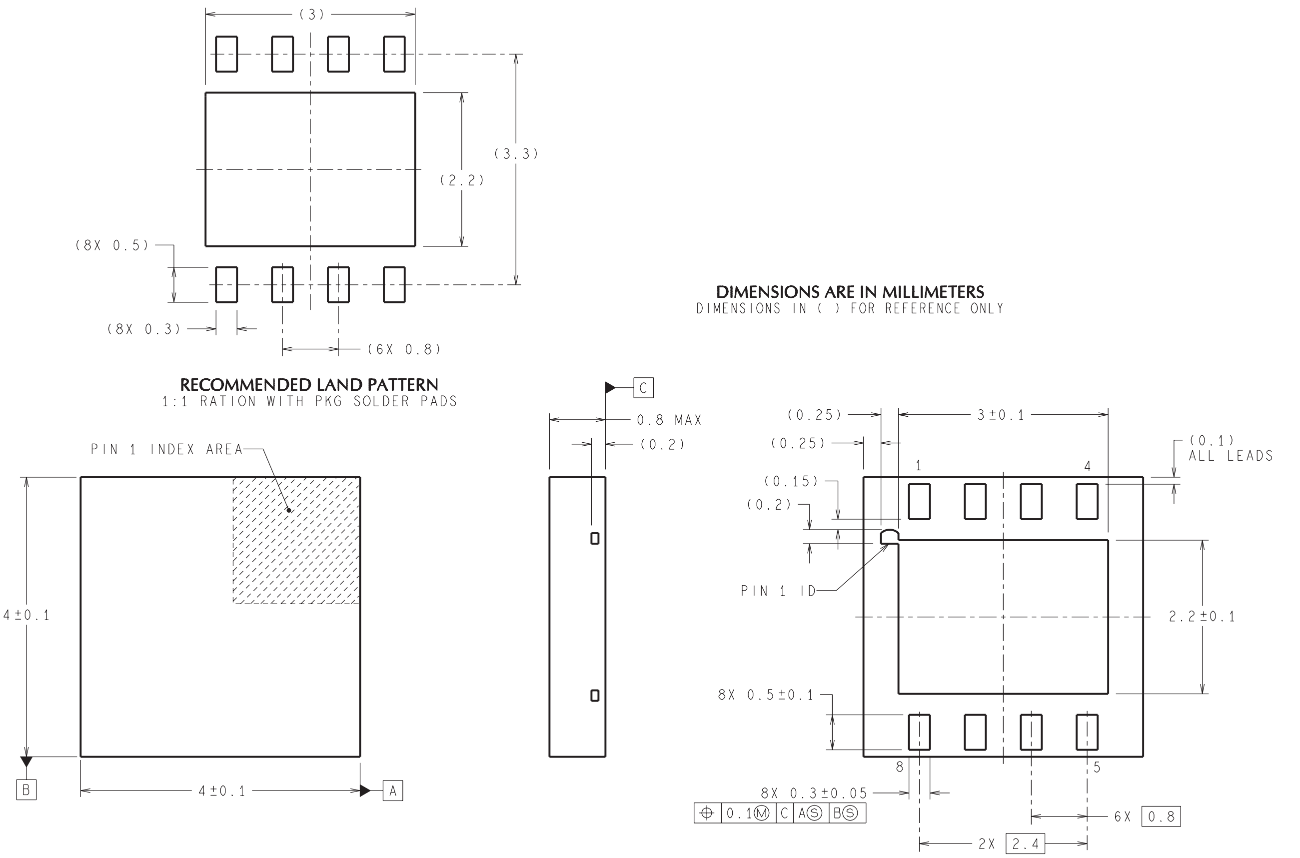
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4871LD	WSON	NGN	8	1000	210.0	185.0	35.0
LM4871LD/NOPB	WSON	NGN	8	1000	213.0	191.0	55.0
LM4871LDX/NOPB	WSON	NGN	8	4500	367.0	367.0	35.0
LM4871MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM4871MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM4871MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM4871MX	SOIC	D	8	2500	367.0	367.0	35.0
LM4871MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



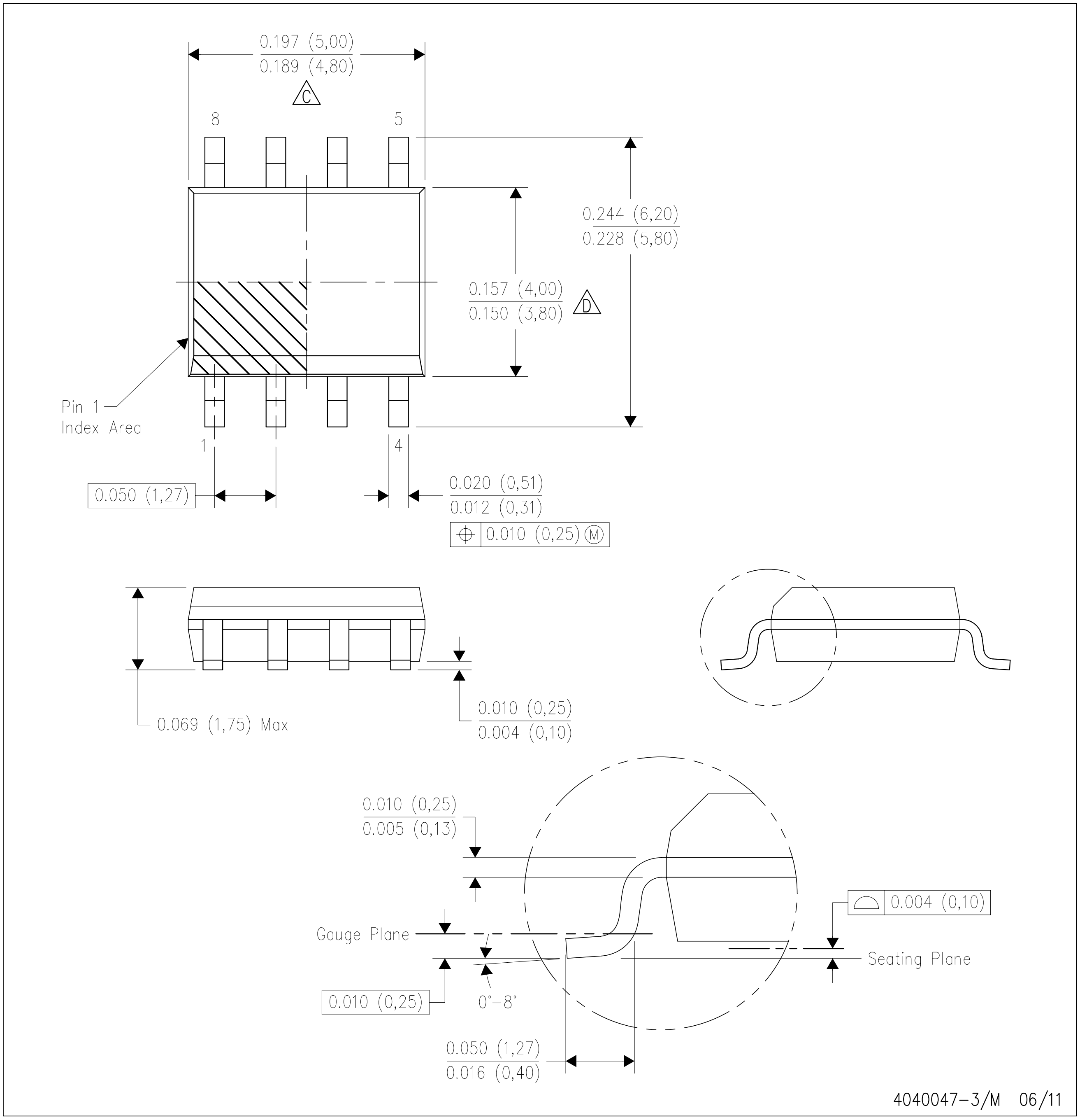
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

NGN0008A



LDC08A (Rev B)

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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