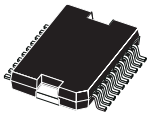
L9822E

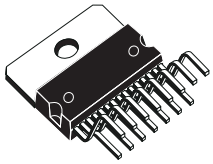
Octal serial solenoid driver

Features

- Eight low R_{DSon} DMOS outputs (0.5 Ω @ I_O = 1 A @ 25 °C V_{CC} = 5 V ± 5 %)
- 8 bit serial input data (SPI)
- 8 bit serial diagnostic output for overload and open circuit conditions
- Output short circuit protection
- Chip enable select function (active low)
- Internal 36 V clamping for each output
- Cascadable with another octal driver
- Low quiescent current (10 mA Max.)
- Multipower BCD technology
- Package Multiwatt 15 and PowerSO-20



PowerSO-20



Multiwatt 15

Description

The L9822E is an octal low-side solenoid driver realized in Multipower BCD technology particularly suited for driving lamps, relays and solenoids in automotive environment. The DMOS outputs L9822E has a very low power consumption.

Data is transmitted serially to the device using the Serial Peripheral Interface (SPI) protocol.

Status monitor function is available on all output lines.

Table 1. Device summary

Order code	Package	Packing
L9822E	Multiwatt 15	Tube
L9822EPD	PowerSO-20	Tube

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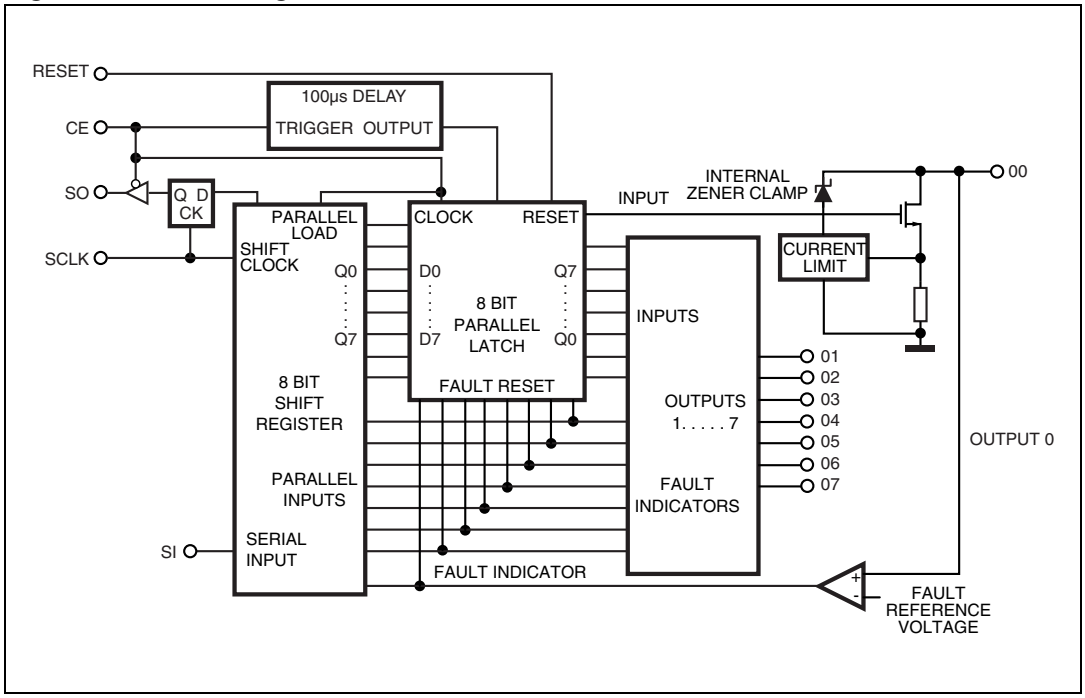
1 Block diagram

Figure 1. Block diagram



2 Pin description

Figure 2. PowerSO-20 pin connection (top view)

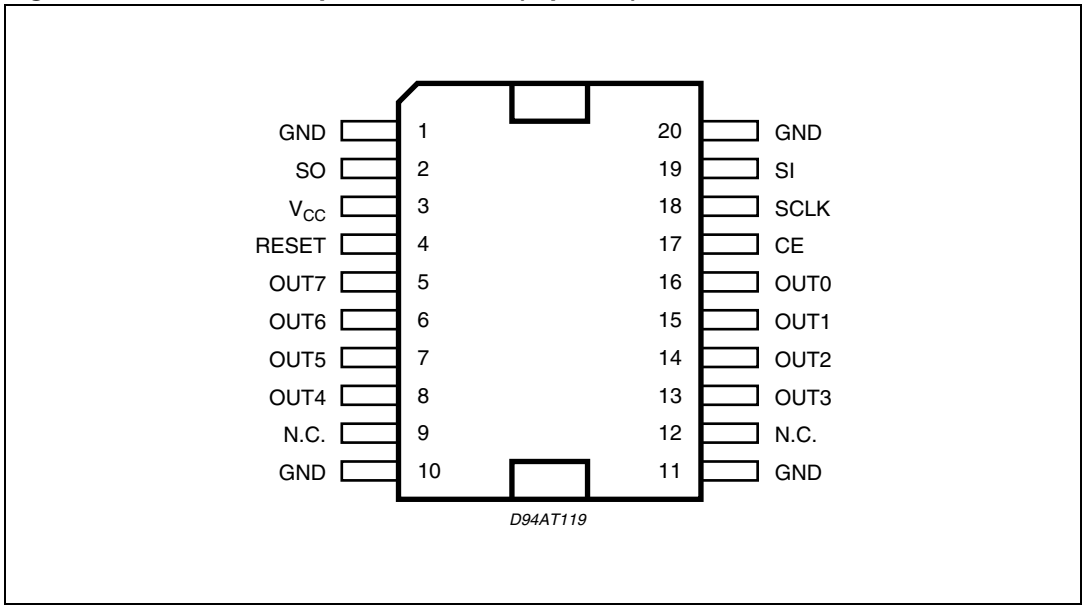
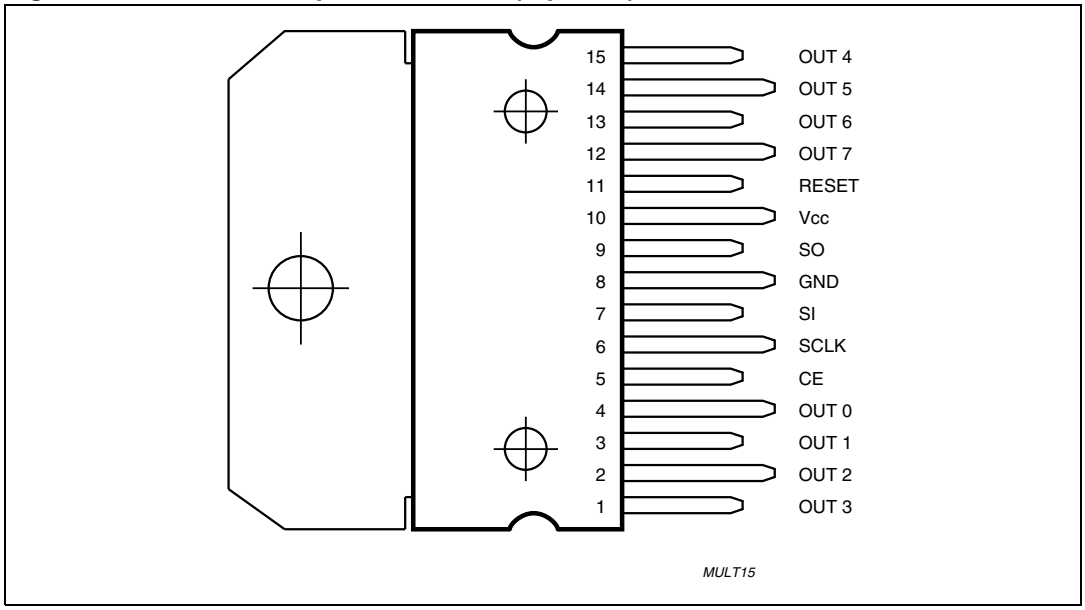


Figure 3. Multiwatt 15 pin connection (top view)



2.1 Pin description

Table 2. Pin function

PowerSO20 pin #	Multiwatt15 pin #	Name	Function
1, 10, 11, 20	8	GND	Device ground. This ground applies for the logic circuits as well as the power output stages.
2	9	SO	Serial output. This pin is the serial output from the shift register and it is tri-stated when CE is high. A high for a data bit on this pin indicates that the particular output is high. A low on this pin for a data bit indicates that the output is low. Comparing the serial output bits with the previous serial input bits the external microcontroller implements the diagnostic data supplied by the L9822E.
3	10	V_{CC}	Logic supply voltage - nominally 5V.
4	11	RESET	Asynchronous reset for the output stages, the parallel latch and the shift register inside the L9822E. This pin is active low and it must not be left floating. A power on clear function may be implemented connecting this pin to VCC with an external resistor and to ground with an external capacitor.
5-8, 13-16	1-4, 12-15	OUTPUT 1-7	Power output pins. The input and output bits corresponding to 07 are sent and received first via the SPI bus and 00 is the last. The outputs are provided with current limiting and voltage sense functions for fault indication and protection. The nominal load current for these outputs is 500mA, but the current limiting is set to a minimum of 1.05A. The outputs also have on board clamps set at about 36V for recirculation of inductive load current.
9,12	-	N.C.	Pins not connected.
17	5	CE	Chip enable. Data is transferred from the shift registers to the outputs on the rising edge of this signal. The falling edge of this signal sets the shift register with the output voltage sense bits coming from the output stages. The output driver for the SO pin is enabled when this pin is low.
18	6	SCLK	Serial clock. This pin clocks the shift register. New SO data will appear on every rising edge of this pin and new SI data will be latched on every SCLK's falling edge into the shift register.
19	7	SI	Serial input. This pin is the serial data input. A high on this pin will program a particular output to be OFF, while a low will turn it ON.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
V_{CC}	DC logic supply voltage	– 0.7	7	V
V_O	Output voltage	– 0.7	40	V
I_I	Input transient current (CE, SI, SCLK, RESET, SO): Duration time t = 1 s, $V_I < 0$ $V_I > V_{CC}$	 – 25	 + 25	mA
I_{Odc}	Continuos output current (for each output)	Internally limited		A
T_j, T_{stg}	Junction and storage temperature range	– 40	150	°C

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter		Multiwatt15	PowerSO20	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction to case	Max.	2	1.5	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	Max.	35	60	°C/W

3.3 Electrical characteristics

Table 5. Electrical characteristics

(V_{CC} = 5 V ± 5 %. T_j = – 40 to 125 °C ; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OC}	Output clamping volt.	I_O = 0.5 A, Output programmed OFF	30		40	V
E_{OC}	Output clamping energy	I_O = 0.5 A, when ON	20			mJ
$I_{O\ leak}$	Output leakage current	V_O = 24 V, Output programmed OFF			1	mA
R_{DSon}	ON resistance	Output programmed ON I_O = 0.5 A I_O = 0.8 A I_O = 1 A With fault reset disabled		 0.55 0.55 0.55	 1 1 1	Ω
I_{OL}	Output self limiting current	Output programmed ON	1.05			A
t_{PHL}	Turn-on delay	I_O = 500 mA no reactive load			10	µs
t_P	Turn-off Delay	I_O = 500 mA no reactive load			10	µs

Table 5. Electrical characteristics (continued)

(V_{CC} = 5 V ± 5 %. T_j = – 40 to 125 °C ; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OREF}	Fault refer. voltage	Output progr. OFF Fault detected if $V_O > V_{OREF}$	1.6		2	V
t_{UD}	Fault reset delay (after CE L to H transition)	See *Figure 6*.	75		250	µs
V_{OFF}	Output OFF voltage	Output pin floating. Output progr. OFF			1	V
Input buffer (SI, CE, SCLK and RESET pins)						
V_{T-}	Threshold voltage at falling edge SCLK only	V_{CC} = 5 V ± 10 %	0.2V_{CC} 0.6			V
V_{T+}	Threshold voltage at rising edge SCLK only	V_{CC} = 5 V ± 10 %			0.7V_{CC} 4.15	V
V_H	Hysteresis voltage	$V_{T+} - V_{T-}$	0.85		2.5	V
I_I	Input current	V_{CC} = 5.50 V, 0 < V_I < V_{CC}	– 10		+ 10	µA
C_I	Input capacitance	0 < V_I < V_{CC}			20	pF
Output buffer (SO pin)						
V_{SOL}	Output low voltage	I_O = 1.6 mA			0.4	V
V_{SOH}	Output high voltage	I_O = 0.8 mA	V_{CC} – 1.3V			V
I_{SOtl}	Output tristate leakage current	0 < V_O < V_{CC}, CE pin held high, V_{CC} = 5.25 V	– 20		20	µA
C_{SO}	Output capacitance	0 < V_O < V_{CC}, CE pin held high			20	pF
I_{CC}	Quiescent supply current at V_{CC} pin	All outputs progr. ON. I_O = 0.5 A per output simultaneously			10	mA
Serial peripheral interface (see *Figure 5*, timing diagram)						
f_{op}	Operating frequency		D.C.		2	MHz
t_{lead}	Enable lead time		250			ns
t_{lag}	Enable lag time		250			ns
t_{wSCKH}	Clock high time		200			ns
t_{wSCKL}	Clock low time		200			ns
t_{su}	Data setup time		75			ns
t_H	Data hold time		75			ns
t_{EN}	Enable time		250			ns
t_{DIS}	Disable time		250			ns
t_V	Data valid time		100			ns
t_{rSO}	Rise time (SO output)	V_{CC} = 20 to 70 % C_L = 200 pF			50	ns
t_{fSO}	Fall time (SO output)	V_{CC} = 70 to 20 % C_L = 200 pF			50	ns
t_{rSI}	Rise time SPI inputs (SCK, SI, CE)	V_{CC} = 20 to 70 % C_L = 200 pF	200			ns
t_{fSI}	Fall time SPI inputs (SCLK, SI, CE)	V_{CC} = 70 to 20 % C_L = 200 pF	200			ns
t_{ho}	Output data hold time		0			µs

4 Functional description

The L9822E DMOS output is a low operating power device featuring, eight 1Ω R_{DSON} DMOS drivers with transient protection circuits in output stages.

Each channel is independently controlled by an output latch and a common RESET line which disables all eight outputs. The driver has low saturation and short circuit protection and can drive inductive and resistive loads such as solenoids, lamps and relays.

Data is transmitted to the device serially using the Serial Peripheral Interface (SPI) protocol.

The circuit receives 8 bit serial data by means of the serial input (SI) which is stored in an internal register to control the output drivers. The serial output (SO) provides 8 bit of diagnostic data representing the voltage level at the driver output. This allows the microprocessor to diagnose the condition of the output drivers.

The output saturation voltage is monitored by a comparator for an out of saturation condition and is able to unlatch the particular driver through the fault reset line. This circuit is also cascadable with another octal driver in order to jam 8 bit multiple data.

The device is selected when the chip enable (CE) line is low.

Additionally the (SO) is placed in a tri-state mode when the device is deselected. The negative edge of the (CE) transfers the voltage level of the drivers to the shift register and the positive edge of the (CE) latches the new data from the shift register to the drivers. When CE is Low, data bit contained into the shift register is transferred to SO output at every SCLK positive transition while data bit present at SI input is latched into the shift register on every SCLK negative transition.

4.1 Internal blocks description

The internal architecture of the device is based on the three internal major blocks:

1. the octal shift register for talking to the SPI bus,
2. the octal latch for holding control bits written into the device
3. the octal load driver array.

4.2 Shift register

The shift register has both serial and parallel inputs and serial and parallel outputs. The serial input accepts data from the SPI bus and the serial output simultaneously sends data into the SPI bus. The parallel outputs are latched into the parallel latch inside the L9822E at the end of a data transfer. The parallel inputs jam diagnostic data into the shift register at the beginning of a data transfer cycle.

4.3 Parallel latch

The parallel latch holds the input data from the shift register. This data then actuates the output stages. Individual registers in the latch may be cleared by fault conditions in order to protect the overloaded output stages. The entire latch may also be cleared by the RESET signal.

4.4 Output stages

The output stages provide an active low drive signal suitable for 0.75 A continuous loads. Each output has a current limit circuit which limits the maximum output current to at least 1.05A to allow for high inrush currents. Additionally, the outputs have internal zeners set to 36 volts to clamp inductive transients at turn-off. Each output also has a voltage comparator observing the output node. If the voltage exceeds 1.8 V on an ON output pin, a fault condition is assumed and the latch driving this particular stage is reset, turning the output OFF to protect it. The timing of this action is described below. These comparators also provide diagnostic feedback data to the shift register. Additionally, the comparators contain an internal pulldown current which will cause the cell to indicate a low output voltage if the output is programmed OFF and the output pin is open circuited.

4.5 Timing data transfer

Figure 5 shows the overall timing diagram from a byte transfer to and from the L9822E using the SPI bus.

4.5.1 CE high to low transition

The action begins when the Chip Enable (CE) pin is pulled low. The tri-state Serial Output (SO) pin driver will be enabled entire time that CE is low. At the falling edge of the CE pin, the diagnostic data from the voltage comparators in the output stages will be latched into the shift register. If a particular output is high, a logic one will be jammed into that bit in the shift register. If the output is low, a logic zero will be loaded there. The most significant bit (07) should be presented at the Serial Input (SI) pin. A zero at this pin will program an output ON, while a one will program the output OFF.

4.5.2 SCLK transitions

The Serial Clock (SCLK) pin should then be pulled high. At this point the diagnostic bit from the most significant output (07) will appear at the SO pin. A high here indicates that the 07 pin is higher than 1.8 V. The SCLK pin should then be toggled low then high. New SO data will appear following every rising edge of SCLK and new SI data will be latched into the L9822E shift register on the falling edges. An unlimited amount of data may be shifted through the device shift register (into the SI pin and out the SO pin), allowing the other SPI devices to be cascaded in a daisy chain with the L9822E.

4.5.3 CE low to high transition

Once the last data bit has been shifted into the L9822E, the CE pin should be pulled high. At the rising edge of CE the shift register data is latched into the parallel latch and the output stages will be actuated by the new data. An internal 160 µs delay timer will also be started at this rising edge (see t_{UD}). During the 160ms period, the outputs will be protected only by the analog current limiting circuits since the resetting of the parallel latches by faults conditions will be inhibited during this period.
This allows the part to overcome any high inrush currents that may flow immediately after turn on. Once the delay period has elapsed, the output voltages are sensed by the comparators and any output with voltages higher than 1.8 V are latched OFF. It should be noted that the SCLK pin should be low at both transitions of the CE pin to avoid any false clocking of the shift register. The SCLK input is gated by the CE pin, so that the SCLK pin is ignored whenever the CE pin is high.

4.6 Fault conditions check

Checking for fault conditions may be done in the following way. Clock in a new control byte. Wait 160 µs or so to allow the outputs to settle.

Clock in the same control byte and observe the diagnostic data that comes out of the device. The diagnostic bits should be identical to the bits that were first clocked in. Any differences would point to a fault on that output. If the output was programmed ON by clocking in a zero, and a one came back as the diagnostic bit for that output, the output pin was still high and a short circuit or overload condition exists.

If the output was programmed OFF by clocking in a one, and a zero came back as the diagnostic bit for that output, nothing had pulled the output pin high and it must be floating, so an open circuit condition exists for that output.

Figure 4. Byte timing with asynchronous reset.

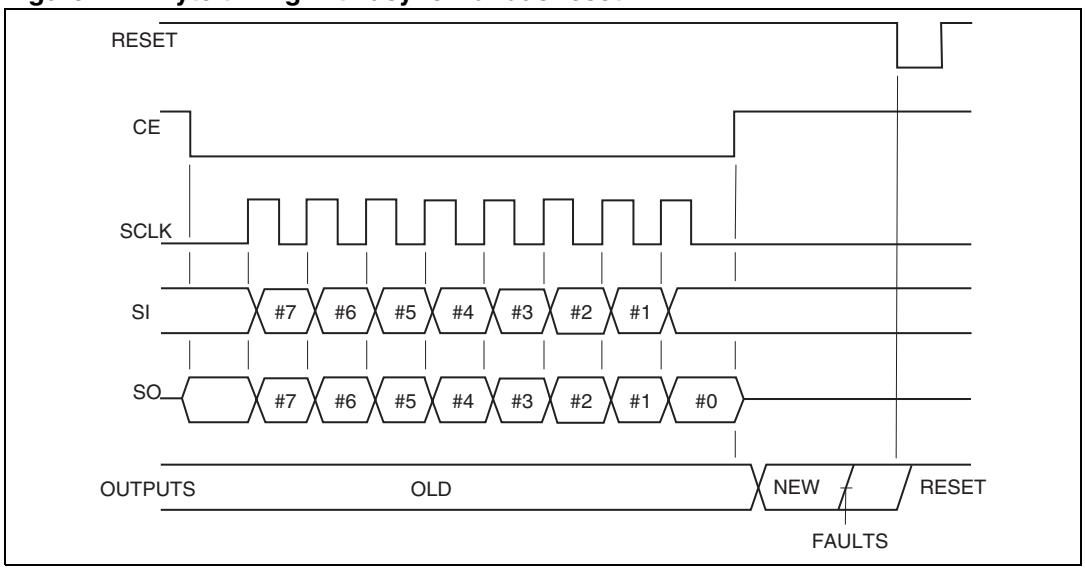


Figure 5. Timing diagram.

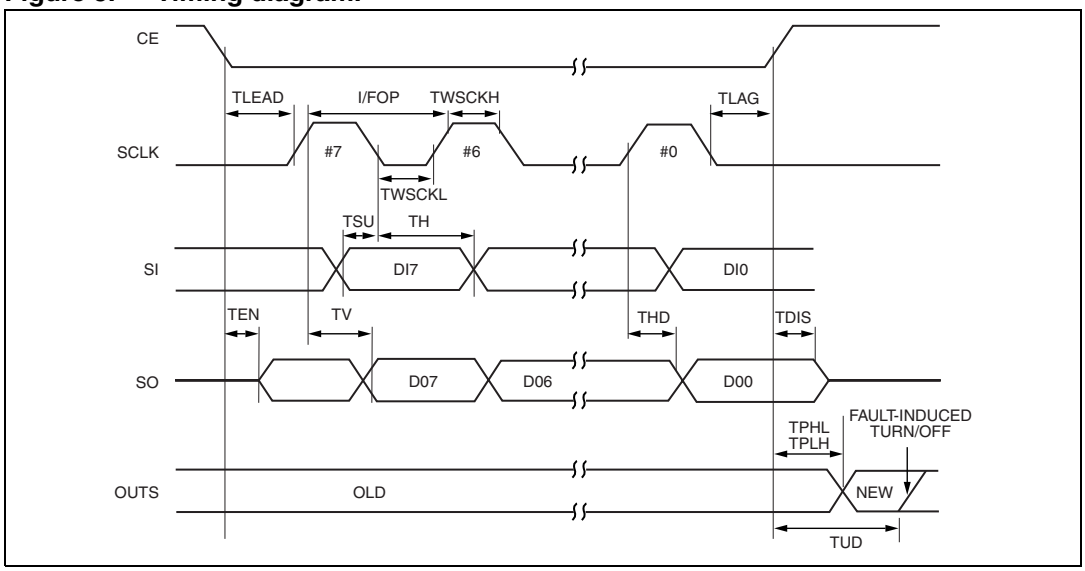
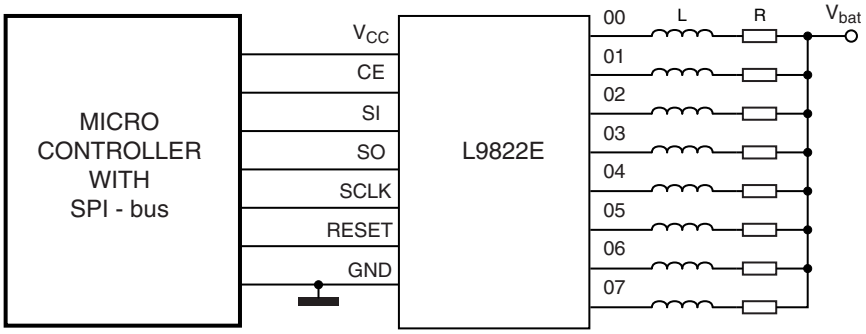


Figure 6. Typical application diagram



V_{CC} = 5.0 V +/- 5 %
Vbat = 14.0 V +/- 0.5 V
R = 30 Ω +/- 5 %
L = 10mH +/- 10 %
8 loads up to 0.75 A each

5 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 7. PowerSO-20 mechanical data and package dimensions

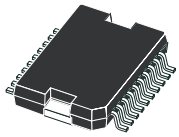
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1 (2)	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8˚(typ.)					
S	8˚(max.)					
T		10			0.394	

(1) "D and E1" do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006")
- Critical dimensions: "E", "G" and "a3".

(2) For subcontractors, the limit is the one quoted in jedec MO-166

OUTLINE AND MECHANICAL DATA

Weight: 1.9gr



JEDEC MO-166

PowerSO-20

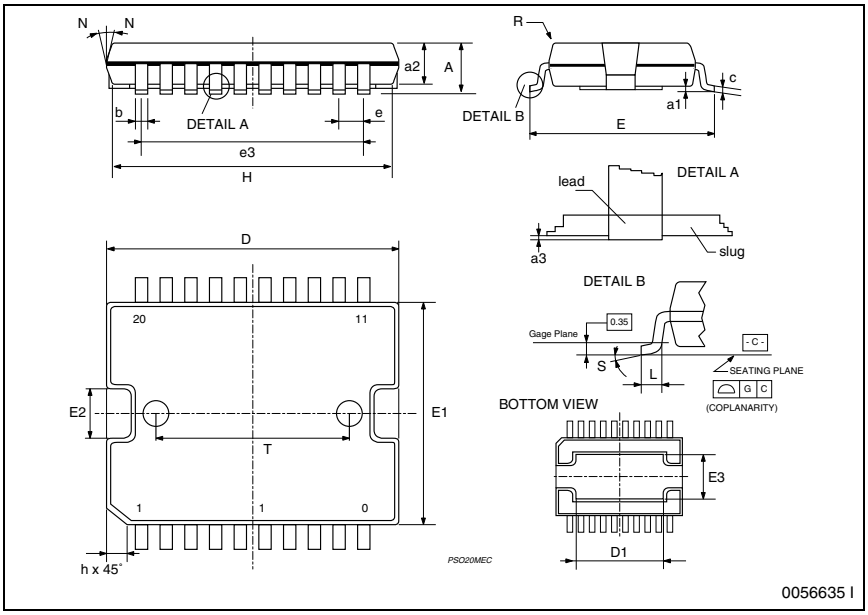
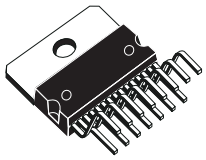


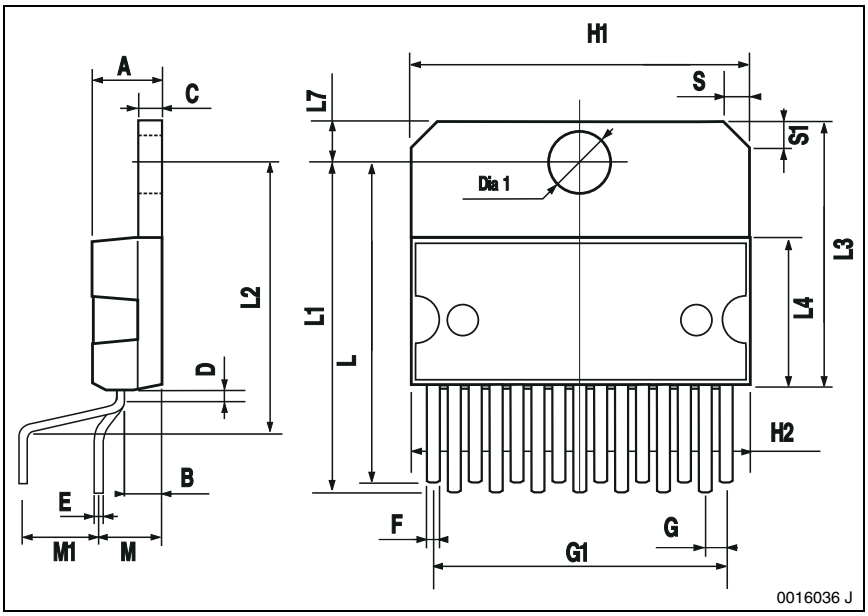
Figure 8. Multiwatt 15 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A5						0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.87	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.73	5.08	5.43	0.186	0.200	0.214
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA



Multiwatt15 (Vertical)



6 Revision history

Table 6. Document revision history

Date	Revision	Changes
12-Jan-2002	1	Initial release.
27-Oct-2008	2	Document reformatted. Corrected in *Table 5: Electrical characteristics*, the max. value of the parameter "C_I Input capacitance".
20-Sep-2013	3	Updated Disclaimer.

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