L6728D

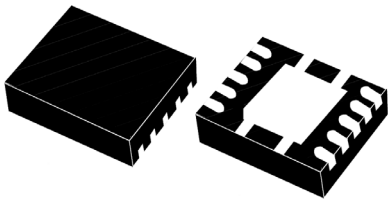
Single-phase PWM controller with Power Good

Features

- Flexible power supply from 5 V to 12 V
- Power conversion input as low as 1.5 V
- 0.8 V internal reference
- 0.8% output voltage accuracy
- High-current integrated drivers
- Power Good output
- Sensorless and programmable OCP across low-side $R_{DS(on)}$
- OV / UV protection
- VSEN disconnection protection
- Oscillator internally fixed at 300 kHz
- LSLess to manage pre-bias startup
- Adjustable output voltage
- Disable function
- Internal soft-start
- DFN10 package

Applications

- Memory and termination supply
- Subsystem power supply (MCH, IOCH, PCI, etc.)
- CPU and DSP power supply
- Distributed power supply
- General DC-DC converters



DFN10

Description

L6728D is a single-phase step-down controller with integrated high-current drivers that provides complete control logic and protection to simplify the design of general DC-DC converters by using a compact DFN10 package.

Device flexibility allows the management of conversions with power input (V_{IN}) as low as 1.5 V, and device supply voltage ranging from 5 V to 12 V.

The L6728D provides a simple control loop with voltage mode EA. The integrated 0.8 V reference allows output voltages regulation with ±0.8% accuracy over line and temperature variations. The oscillator is internally fixed to 300 kHz.

The L6728D provides programmable dual level overcurrent protection, as well as overvoltage and undervoltage protection. Current information is monitored across the low-side MOSFET $R_{DS(on)}$, eliminating the need for expensive and space-consuming sense resistors.

A PGOOD output easily provides real-time information on output voltage status, through the VSEN dedicated output monitor.

Table 1. Device summary

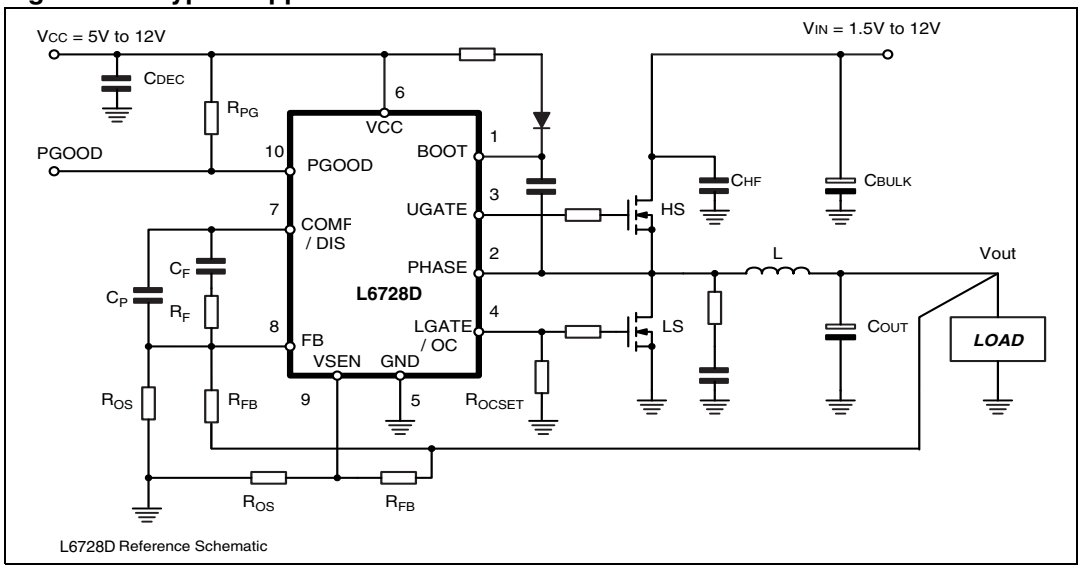
Order codes	Package	Packaging
L6728D	DFN10	Tube
L6728DTR		Tape and reel

Contents

1 Typical application circuit and block diagram

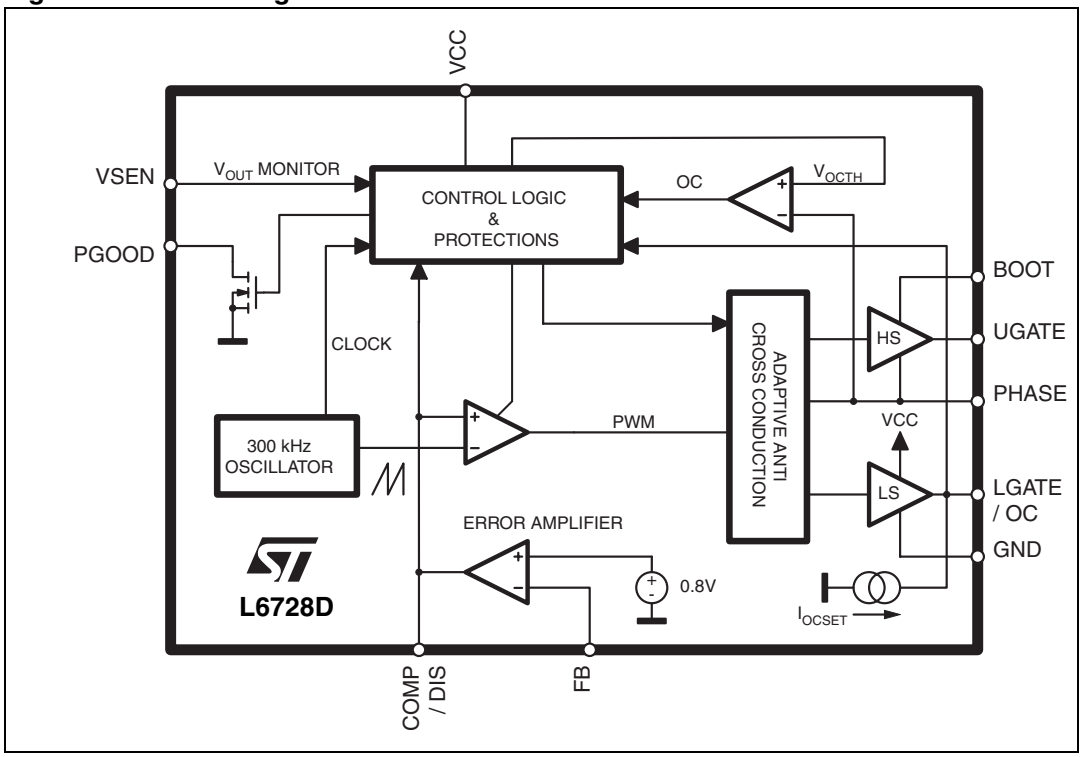
1.1 Application circuit

Figure 1. Typical application circuit of the L6728D



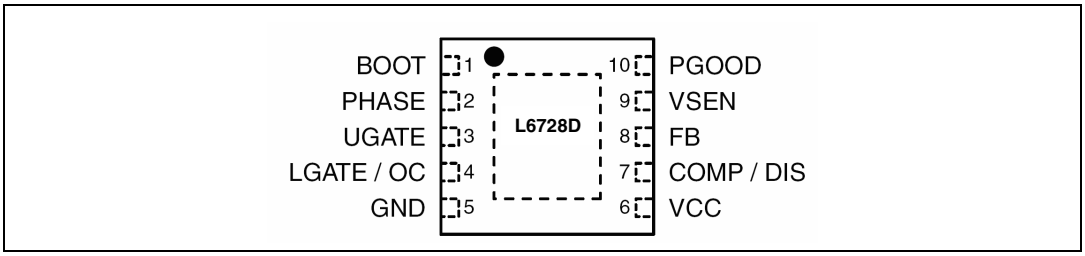
1.2 Block diagram

Figure 2. Block diagram of the L6728D



2 Pin description and connection diagram

Figure 3. Pin connection (top view)



2.1 Pin descriptions

Table 2. Pins description

Pin n°	Name	Function
1	BOOT	HS driver supply. Connect through a capacitor (100 nF) to the floating node (LS-Drain) pin and provide necessary bootstrap diode from VCC.
2	PHASE	HS driver return path, current-reading and adaptive-dead-time monitor. Connect to the LS drain to sense $R_{DS(on)}$ drop to measure the output current. This pin is also used by the adaptive-dead-time control circuitry to monitor when HS MOSFET is OFF.
3	UGATE	HS driver output. Connect directly to HS MOSFET gate.
4	LGATE / OC	*LGATE*: LS driver output. Connect directly to LS MOSFET gate. *OC*: Overcurrent threshold set. During a short period of time following VCC rising over the UVLO threshold, a 10 µA current is sourced from this pin. Connect to GND with an R_{OCSET} resistor greater than 5 kΩ to program the OC threshold. The resulting voltage at this pin is sampled and held internally as the OC set point. The maximum programmable OC threshold is 0.55 V. A voltage greater than 0.6 V activates an internal clamp and causes the OC threshold to be set at the maximum value.
5	GND	All internal references, logic and drivers are connected to this pin. Connect to the PCB ground plane.
6	VCC	Device and driver power supply. Operating range from 5 V to 12 V. Filter with at least 1 µF MLCC to GND.
7	COMP / DIS	*COMP:* Error amplifier output. Connect with an R_F - C_F // C_P to FB to compensate the device control loop. *DIS:* The device can be disabled by pushing this pin lower than 0.75 V (typ). By setting the pin free, the device is enabled again.
8	FB	Error amplifier inverting input. Connect with a resistor R_{FB} to the output regulated voltage. An output resistor divider may be used to regulate voltages higher than the reference.
9	VSEN	Regulated voltage sense pin for OVP and UVP protection and PGOOD. Connect to the output regulated voltage, or to the output resistor divider if the regulated voltage is higher than the reference.
10	PGOOD	Open drain output set free after SS has finished and pulled low when VSEN is outside the relative window. Pull up to a voltage equal or lower than VCC. If not used it can be left floating.

3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JA)}$	Thermal resistance junction-to-ambient (device soldered on 2s2p, 67 mm x 69 mm board)	45	°C/W
$R_{th(JC)}$	Thermal resistance junction-to-case	5	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	-40 to 125	°C
P_{TOT}	Maximum power dissipation at T_A = 25 °C	2.25	W

4 Electrical specifications

4.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	to GND	-0.3 to 15	V
V_{BOOT}, V_{UGATE}	to PHASE to GND to GND; t < 200 ns	15 33 45	V
V_{PHASE}	to GND to GND; t < 200 ns	-5 to 18 -8 to 30	V
V_{LGATE}	to GND	-0.3 to VCC+0.3	V
	FB, COMP, VSEN to GND	-0.3 to 3.6	V
	PGOOD to GND	-0.3 to VCC+0.3	V

4.2 Electrical characteristics

V_{CC} = 5 V to 12 V; T_J = 0 to 70 °C unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-ON						
I_{CC}	VCC supply current	UGATE and LGATE = OPEN		6		mA
I_{BOOT}	BOOT supply current	UGATE = OPEN; PHASE to GND		0.7		mA
UVLO	VCC Turn-ON	VCC rising			4.1	V
	Hysteresis			0.2		V
Oscillator						
F_{SW}	Main oscillator accuracy		270	300	330	kHz
ΔV_{OSC}	PWM ramp amplitude			1.4		V
d_{MAX}	Maximum duty cycle		80			%
Reference and error amplifier						
	Output voltage accuracy		-0.8	-	0.8	%
A_0	DC gain (1)			120		dB
GBWP	Gain-bandwidth product (1)			15		MHz
SR	Slew-rate (1)			8		V/µs
DIS	Disable threshold	COMP falling	0.70		0.85	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Gate drivers						
I_{UGATE}	HS source current	BOOT - PHASE = 5 V		1.5		A
R_{UGATE}	HS sink resistance	BOOT - PHASE = 5 V		1.1		Ω
I_{LGATE}	LS source current	VCC = 5 V		1.5		A
R_{LGATE}	LS sink resistance	VCC = 5 V		0.65		Ω
Overcurrent protection						
I_{OCSET}	OCSET current source	Sourced from LGATE pin, during OC setting phase.	9	10	11	µA
V_{OC_SW}	OC switch-over threshold	$V_{LGATE/OC}$ rising		600		mV
Over and undervoltage protections						
OVP	OVP threshold	VSEN rising	0.970	1.000	1.030	V
		un-latch, VSEN falling	0.35	0.40	0.45	V
UVP	UVP threshold	VSEN falling	0.570	0.600	0.630	V
VSEN	VSEN bias current	Sourced from VSEN		100		nA
PGOOD						
PGOOD	Upper threshold	VSEN rising	0.860	0.890	0.920	V
	Lower threshold	VSEN falling	0.680	0.710	0.740	V
V_{PGOODL}	PGOOD voltage low	I_{PGOOD} = -4 mA			0.4	V

1. Guaranteed by design, not subject to test.

5 Device description

The L6728D is a single-phase PWM controller with embedded high-current drivers which provides complete control logic and protection features for easy implementation of a general DC-DC step-down converter. Designed to drive N-channel MOSFETs in a synchronous buck topology, this 10-pin device provides a high level of integration to allow a reduction in cost and size of power supply solutions, while also providing real-time PGOOD in a compact DFN10 3x3 mm package.

The L6728D is designed to operate from a 5 V or 12 V supply. The output voltage can be precisely regulated to as low as 0.8 V with ±0.8% accuracy over line and temperature variations. The switching frequency is internally set to 300 kHz.

This device provides a simple control loop with a voltage-mode error amplifier. The error amplifier features a 15 MHz gain-bandwidth product and 8 V/µs slew rate, allowing high regulator bandwidth for fast transient response.

To prevent load damage, the L6728D provides protection against overcurrent, overvoltage, undervoltage and feedback disconnection. The overcurrent trip threshold is programmable using a resistor connected from Lgate to GND. Output current is monitored across the low-side MOSFET $R_{DS(on)}$, eliminating the need for expensive and space-consuming sense resistors. Output voltage is monitored through the dedicated VSEN pin.

The L6728D implements soft-start by increasing the internal reference in closed-loop regulation. The low side-less feature allows the device to perform soft-start over a pre-biased output, avoiding high current return through the output inductor and dangerous negative spike at the load side.

The L6728D is available in a compact DFN10 3x3 mm package with exposed pad.

6 Driver section

The integrated high-current drivers permit the use of different types of power MOSFETs (also multiple MOSFETs to reduce the equivalent $R_{DS(on)}$), maintaining fast switching transition.

The driver for the high-side MOSFET uses the BOOT pin for supply and the PHASE pin for return. The driver for low-side MOSFET uses the VCC pin for supply and the GND pin for return.

The controller embodies an anti-shoot-through and adaptive dead-time control to minimize low side body diode conduction time, maintaining good efficiency while eliminating the need for a Schottky diode:

- to check the high-side MOSFET turn-off, the PHASE pin is sensed. When the voltage at the PHASE pin drops, the low-side MOSFET gate drive is suddenly applied
- to check the low-side MOSFET turn-off, the LGATE pin is sensed. When the voltage at LGATE has fallen, the high-side MOSFET gate drive is suddenly applied

If the current flowing in the inductor is negative, voltage on the PHASE pin will never drop. To allow the low-side MOSFET to turn on even in this case, a watchdog controller is enabled. If the source of the high-side MOSFET does not drop, the low side MOSFET is switched on, thereby allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

Power conversion input is flexible: 5 V, 12 V bus or any bus that allows the conversion (see maximum duty cycle limitations) to be chosen freely.

6.1 Power dissipation

The L6728D embeds high current MOSFET drivers for both high side and low side MOSFETs. It is therefore important to consider the power that the device is going to dissipate in driving them, in order to avoid overcoming the maximum junction operating temperature.

Two main factors contribute to device power dissipation: bias power and driver power.

- Device bias power (P_{DC}) depends on the static consumption of the device through the supply pins, and is quantifiable as follows (assuming HS and LS drivers with the same VCC of the device):

$$P_{DC} = V_{CC} \cdot (I_{CC} + I_{BOOT})$$

- Driver power is the power needed by the driver to continuously switch on and off the external MOSFETs. It is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW} dissipated to switch the MOSFETs (easily calculable) is dissipated by three main factors: external gate resistance (when present), intrinsic MOSFET resistance and intrinsic driver resistance. This last factor is the most important one to be determined to calculate the device power dissipation. The total power dissipated to switch the MOSFETs is:

$$P_{SW} = F_{SW} \cdot (Q_{gHS} \cdot V_{BOOT} + Q_{gLS} \cdot V_{CC})$$

External gate resistors help the device to dissipate the switching power since the same power P_{SW} is shared between the internal driver impedance and the external resistor, resulting in a general cooling of the device.

7 Soft-start

The L6728D implements a soft-start to smoothly charge the output filter, avoiding the high in-rush currents to be required from the input power supply. The device gradually increases the internal reference from 0 V to 0.8 V in 4.5 ms (typ.), in closed-loop regulation, linearly charging the output capacitors to the final regulation voltage.

In the event of overcurrent triggering during soft-start, the overcurrent logic overrides the soft-start sequence and shuts down the PWM logic and both the high side and low side gates. This condition is latched. Cycle the VCC to recover.

The device begins the soft-start phase only when the VCC power supply is above the UVLO threshold and the overcurrent threshold setting phase has been completed.

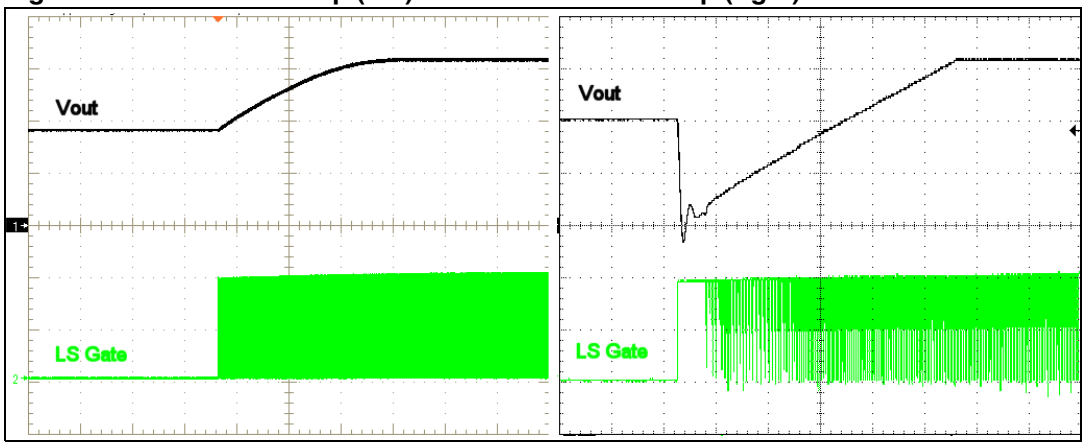
7.1 Low-side-less startup (LSLess)

In order to avoid any kind of negative undershoot and dangerous return from the load during startup, the L6728D performs a special sequence in enabling the LS driver to switch: during the soft-start phase, the LS driver is disabled (LS = OFF) until the HS starts to switch. This prevents the dangerous negative spike on the output voltage which can happen if starting over a pre-biased output.

If the output voltage is pre-biased to a voltage higher than the final one, the HS would never start to switch. In this case, at the end of soft-start time, LS is enabled and discharges the output to the final regulation value.

This particular feature of the device masks the LS turn-on only from the control loop point of view: protection features bypass this turning on of the LS MOSFET if needed.

Figure 4. LSLess startup (left) vs. non-LSLess startup (right)



8 Overcurrent protection

The overcurrent function protects the converter from a shorted output or overload, by sensing the output current information across the low side MOSFET drain-source on-resistance, $R_{DS(on)}$. This method reduces cost and enhances converter efficiency by avoiding the use of expensive and space-consuming sense resistors.

The low side $R_{DS(on)}$ current sense is implemented by comparing the voltage at the PHASE node when the LS MOSFET is turned on with the programmed OCP threshold voltages, internally held. If the monitored voltage is higher than these thresholds, an overcurrent event is detected.

For maximum safety and load protection, the L6728D implements a dual-level overcurrent protection system:

- **1st level threshold**: This is the user externally-set threshold. If the monitored voltage on PHASE exceeds this threshold, a 1st level overcurrent is detected. If four 1st level OC events are detected in four consecutive switching cycles, overcurrent protection is triggered.
- **2nd level threshold**: This is an internal threshold whose value is equal to the 1st level threshold multiplied by a factor 1.5. If the monitored voltage on PHASE exceeds this threshold, overcurrent protection is triggered immediately.

When overcurrent protection is triggered, the device turns off both the LS and HS MOSFETs in a latched condition.

To recover from an overcurrent protection-triggered condition, the VCC power supply must be cycled.

8.1 Overcurrent threshold setting

The L6728D allows easy programming of a 1st level overcurrent threshold ranging from 50 mV to 550 mV, simply by adding a resistor (R_{OCSET}) between LGATE and GND. The 2nd level threshold is automatically set accordingly.

During a short period of time (about 5 ms) following VCC rising over UVLO threshold, an internal 10 µA current (I_{OCSET}) is sourced from the LGATE pin, determining a voltage drop across R_{OCSET}. This voltage drop is sampled and internally held by the device as a 1st level overcurrent threshold. The OC setting procedure's overall time period is about 5 ms.

Connecting an R_{OCSET} resistor between LGATE and GND, the programmed 1st level threshold is:

$$I_{OCth1} = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{dsON}}$$

the programmed 2nd level threshold is:

$$I_{OCth2} = 1.5 \cdot \frac{I_{OCSET} \cdot R_{OCSET}}{R_{dsON}}$$

R_{OCSET} values range from 5 kΩ to 55 kΩ.

In case R_{OCSET} is not connected, the device sets the OCP thresholds to the maximum values: an internal safety clamp on LGATE is triggered as soon as the LGATE voltage reaches 600 mV, setting the maximum threshold and suddenly ending the OC setting phase.

9 Output voltage setting and protections

The L6728D is capable of precisely regulating an output voltage as low as 0.8 V. In fact, the device is equipped with a fixed 0.8 V internal reference that guarantees the output regulated voltage remains within a ±0.8% tolerance over line and temperature variations (excluding output resistor divider tolerance, when present).

Output voltages higher than 0.8 V can be easily achieved by adding a resistor R_{OS} between the FB pin and ground. Referring to *Figure 1*, the steady-state DC output voltage is:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{FB}}{R_{OS}}\right)$$

where V_{REF} is 0.8 V.

The L6728D monitors the voltage at the VSEN pin and compares it to the internal reference voltage in order to provide undervoltage and overvoltage protection as well as a PGOOD signal. Depending on the level of VSEN, different actions are performed by the controller:

- **PGOOD:** If the voltage monitored through VSEN goes outside the PGOOD window limits, the device de-asserts the PGOOD signal while still continuing to switch and regulate. PGOOD is asserted at the end of the soft-start phase.
- **Undervoltage protection:** If the voltage at VSEN pin drops below the UV threshold, the device turns off both the HS and LS MOSFETs, latching the condition. Cycle the VCC to recover.
- **Overvoltage protection:** If the voltage at VSEN pin rises over OV threshold (1 V typ), overvoltage protection turns off the HS MOSFET and turns on the LS MOSFET. The LS MOSFET is turned off as soon as VSEN goes below Vref/2 (0.4 V). The condition is latched. Cycle the VCC to recover. Note that even if the device is latched, the device still controls the LS MOSFET and can switch it on whenever VSEN rises above the OV threshold.
- **Feedback disconnection protection:** In order to provide load protection even if the VSEN pin is not connected, a 100 nA bias current is always sourced from this pin. If VSEN pin is not connected, this current permanently pulls it up, causing the device to detect an OV. Thus, LS is latched on, preventing the output voltage from rising out of control.

10 Application details

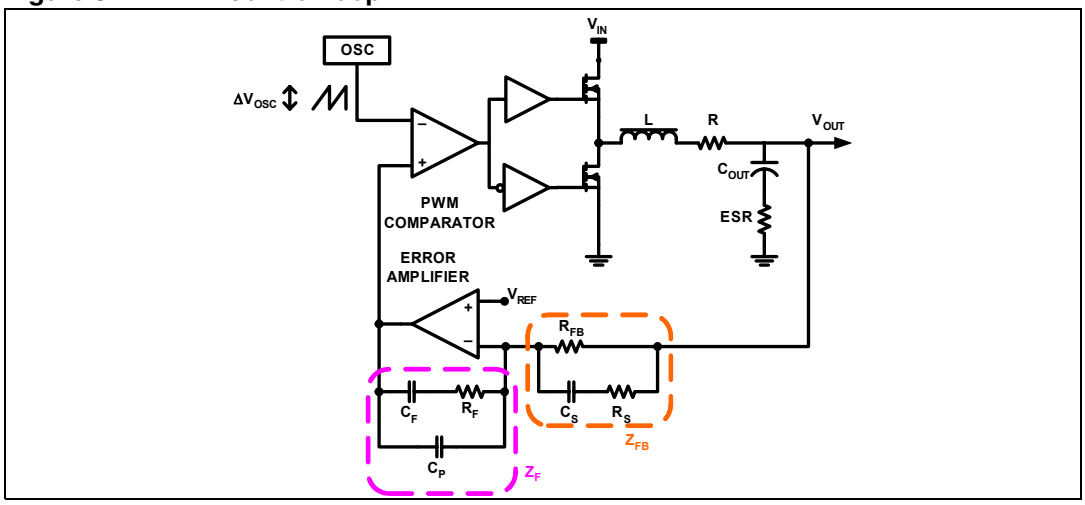
10.1 Compensation network

The control loop shown in *Figure 5* is a voltage mode control loop. The output voltage is regulated to the internal reference (when present, the offset resistor between the FB node and GND can be neglected in control loop calculation).

The error amplifier output is compared to the oscillator sawtooth waveform to provide the PWM signal to the driver section. The PWM signal is then transferred to the switching node with V_{IN} amplitude. This waveform is filtered by the output filter.

The converter transfer function is the small signal transfer function between the output of the EA and V_{OUT}. This function has a double pole at frequency F_{LC} depending on the L-C_{OUT} resonance and a zero at F_{ESR} depending on the output capacitor ESR. The DC gain of the modulator is simply the input voltage V_{IN} divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Figure 5. PWM control loop



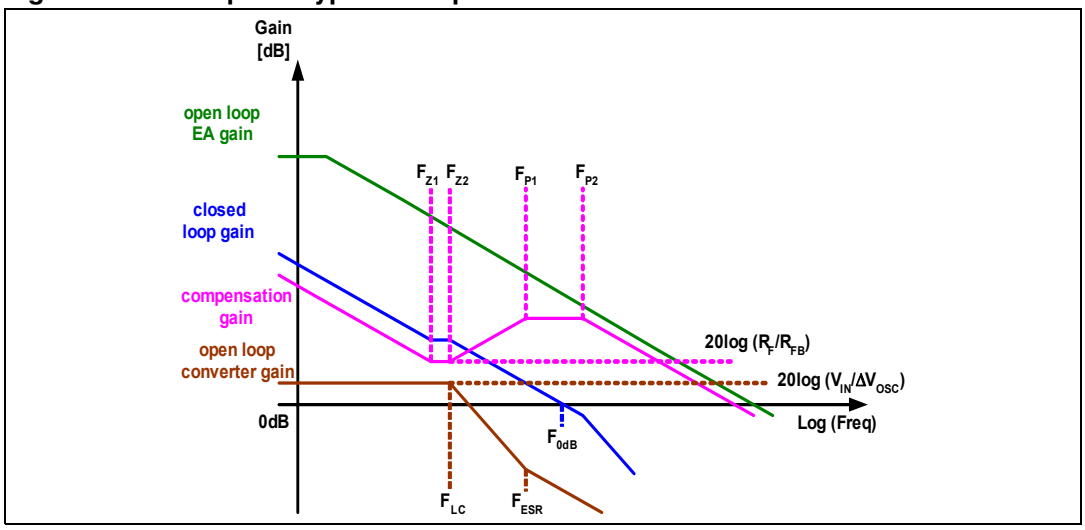
The compensation network closes the loop, joining the V_{OUT} and EA output with transfer function ideally equal to $-Z_F/Z_{FB}$.

The compensation goal is to close the control loop while assuring high DC regulation accuracy, good dynamic performance and stability. To achieve this, the overall loop needs high DC gain, high bandwidth and good phase margin.

High DC gain is achieved by giving an integrator shape to the compensation network transfer function. The loop bandwidth (F_{0dB}) can be fixed by choosing the correct R_F/R_{FB} ratio. However, for stability, it should not exceed $F_{SW}/2\pi$. To achieve a good phase margin, the control loop gain must cross the 0 dB axis with -20 dB/decade slope.

As an example, *Figure 6* shows an asymptotic bode plot of a type III compensation.

Figure 6. Example of type III compensation



- Open loop converter singularities:

a) $F_{LC} = \frac{1}{2\pi\sqrt{L \cdot C_{OUT}}}$

b) $F_{ESR} = \frac{1}{2\pi \cdot C_{OUT} \cdot ESR}$

- Compensation network singularities frequencies:

a) $F_{Z1} = \frac{1}{2\pi \cdot R_F \cdot C_F}$

b) $F_{Z2} = \frac{1}{2\pi \cdot (R_{FB} + R_S) \cdot C_S}$

c) $F_{P1} = \frac{1}{2\pi \cdot R_F \cdot \left(\frac{C_F \cdot C_P}{C_F + C_P}\right)}$

d) $F_{P2} = \frac{1}{2\pi \cdot R_S \cdot C_S}$

To place the poles and zeroes of the compensation network, the following suggestions can be followed:

a) Set the gain R_F/R_{FB} in order to obtain the desired closed loop regulator bandwidth according to the approximated formula (suggested values for R_{FB} are in the range of a few kΩ):

$$\frac{R_F}{R_{FB}} = \frac{F_{0dB}}{F_{LC}} \cdot \frac{\Delta V_{OSC}}{V_{IN}}$$

b) Place F_{Z1} below F_{LC} (typically 0.5*F_{LC}):

$$C_F = \frac{1}{\pi \cdot R_F \cdot F_{LC}}$$

c) Place F_{P1} at F_{ESR}:

$$C_P = \frac{C_F}{2\pi \cdot R_F \cdot C_F \cdot F_{ESR} - 1}$$

d) Place F_{Z2} at F_{LC} and F_{P2} at half of the switching frequency:

$$R_S = \frac{R_{FB}}{\frac{F_{SW}}{2 \cdot F_{LC}} - 1}$$

$$C_S = \frac{1}{\pi \cdot R_S \cdot F_{SW}}$$

e) Check that the compensation network gain is lower than open loop EA gain before F_{0dB}

f) Check the phase margin obtained (it should be greater than 45°) and repeat if necessary.

10.2 Layout guidelines

The L6728D provides control functions and high current integrated drivers to implement high-current step-down DC-DC converters. In this type of application, a good layout is very important.

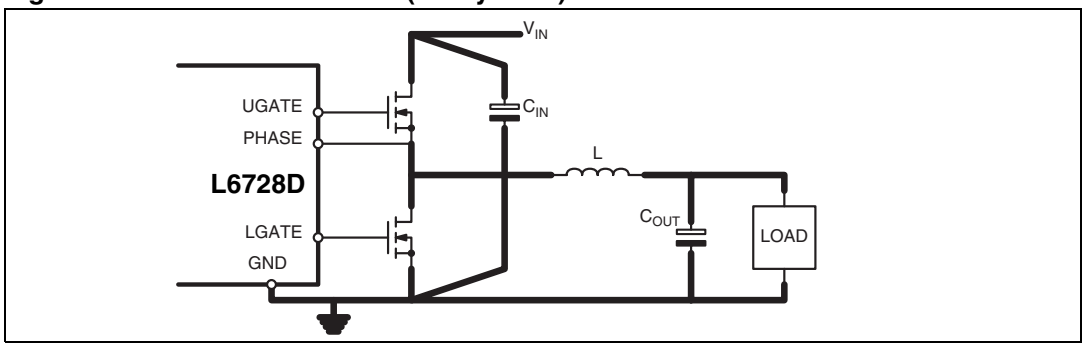
The first priority when placing components for these applications must be reserved for the power section, minimizing the length of each connection and loop as much as possible. To minimize noise and voltage spikes (EMI and losses) power connections (highlighted in *Figure 7*) must be a part of a power plane and in any case constructed with wide and thick copper traces. The loop must be minimized. The critical components, i.e. the power MOSFETs, must be close to each other. The use of multi-layer printed circuit boards is recommended.

The input capacitance (C_{IN}), or at least a portion of the total capacitance needed, must be placed close to the power section in order to eliminate the stray inductance generated by the copper traces. Low ESR and ESL capacitors are preferred. MLCC are suggested to be connected near the HS drain.

Use the appropriate number of VIAs when power traces have to move between different planes on the PCB in order to reduce both parasitic resistance and inductance. Moreover, reproducing the same high-current trace on more than one PCB layer reduces the parasitic resistance associated with that connection.

Connect output bulk capacitors (C_{OUT}) as near as possible to the load, minimizing parasitic inductance and resistance associated with the copper trace, and also adding extra decoupling capacitors along the way to the load when this results in being far from the bulk capacitor bank.

Figure 7. Power connections (heavy lines)

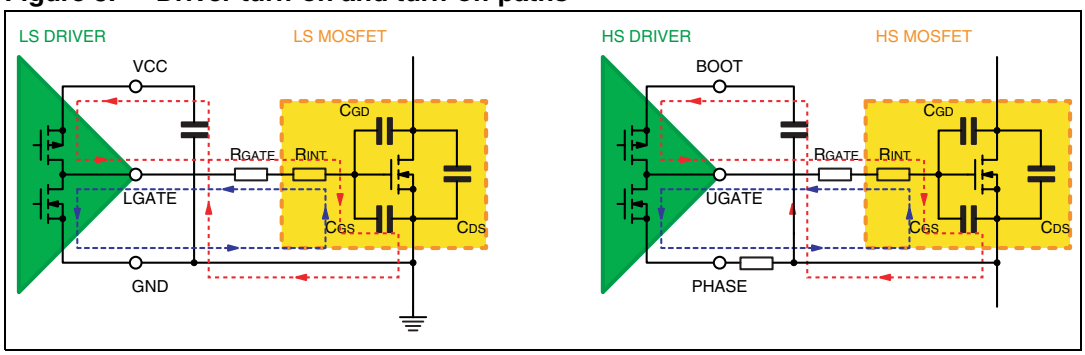


Gate traces and phase traces must be sized according to the driver RMS current delivered to the power MOSFET. The device robustness allows the management of applications with the power section far from the controller without compromising performance. In any case, when possible it is recommended to minimize the distance between the controller and power section.

Small signal components and connections to critical nodes of the application, as well as bypass capacitors for the device supply, are also important. Locate bypass capacitor (VCC and bootstrap capacitor) and feedback compensation components as close to the device as practical. For overcurrent programmability, place R_{OCSET} close to the device and avoid leakage current paths on the LGATE / OC pin, since internal current source is only 10 µA.

Systems that do not use a Schottky diode in parallel to the low-side MOSFET might show big negative spikes on the phase pin. This spike must be limited within the absolute maximum ratings (for example, adding a gate resistor in series to the HS MOSFET gate), as well as the positive spike, but has an additional consequence: it causes the bootstrap capacitor to be over-charged. This extra charge can cause, in the worst-case condition of maximum input voltage and during particular transients, that boot-to-phase voltage overcomes the absolute maximum ratings, also causing device failures. It is then suggested in this cases to limit this extra charge by adding a small resistor in series to the bootstrap diode.

Figure 8. Driver turn-on and turn-off paths



11 Application information

11.1 Inductor design

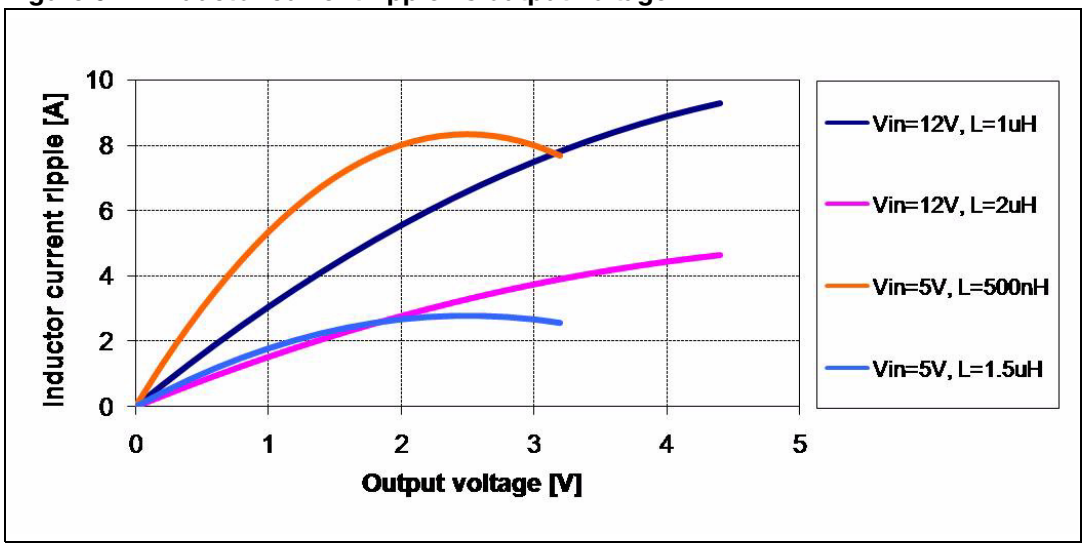
The inductance value is defined by a compromise between the dynamic response time, the efficiency, the cost and the size. The inductor has to be calculated to maintain the ripple current (ΔI_L) between 20% and 30% of the maximum output current (typ). The inductance value can be calculated with the following equation:

$$L = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency, V_{IN} is the input voltage and V_{OUT} is the output voltage. *Figure 9* shows the ripple current vs. the output voltage for different values of the inductor, with V_{IN} = 5 V and V_{IN} = 12 V.

Increasing the value of the inductance reduces the current ripple but, at the same time, increases the converter response time to a dynamic load change. The response time is the time required by the inductor to change its current from initial to final value. Until the inductor has finished its charging time, the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitance required. If the compensation network is well-designed, during a load variation the device is able to set a duty cycle value very different (0% or 80%) from a steady-state one. When this condition is reached, the response time is limited by the time required to change the inductor current.

Figure 9. Inductor current ripple vs output voltage



11.2 Output capacitor(s)

The output capacitors are basic components to define the ripple voltage across the output and for the fast transient response of the power supply. They depend on the output voltage ripple requirements, as well as any output voltage deviation requirement during a load transient.

During steady-state conditions, the output voltage ripple is influenced by both the ESR and capacitive value of the output capacitors as follow:

$$\Delta V_{OUT\_ESR} = \Delta I_L \cdot ESR$$

$$\Delta V_{OUT\_C} = \Delta I_L \cdot \frac{1}{8 \cdot C_{OUT} \cdot F_{SW}}$$

Where ΔI_L is the inductor current ripple. In particular, the expression that defines ΔV_{OUT_C} takes into consideration the output capacitor charge and discharge as a consequence of the inductor current ripple.

During a load variation, the output capacitor supplies the current to the load or absorbs the current stored into the inductor until the converter reacts. In fact, even if the controller immediately recognizes the load transient and sets the duty cycle at 80% or 0%, the current slope is limited by the inductor value. The output voltage has a drop that, in this case also, depends on the ESR and capacitive charge/discharge as follows:

$$\Delta V_{OUT\_ESR} = \Delta I_{OUT} \cdot ESR$$

$$\Delta V_{OUT\_C} = \Delta I_{OUT} \cdot \frac{L \cdot \Delta I_{OUT}}{2 \cdot C_{OUT} \cdot \Delta V_L}$$

Where ΔV_L is the voltage applied to the inductor during the transient response ($D_{MAX} \cdot V_{IN} - V_{OUT}$ for the load appliance or V_{OUT} for the load removal).

MLCC capacitors have typically low ESR to minimize the ripple but also have low capacitances that do not minimize the voltage deviation during dynamic load variations. On the contrary, electrolytic capacitors have big capacitances to minimize voltage deviation during load transients, while they do not show the same ESR values of the MLCC resulting then in higher ripple voltages. For these reasons, a mix between electrolytic and MLCC capacitor is suggested to minimize ripple and reduce voltage deviation in dynamic mode.

11.3 Input capacitors

The input capacitor bank is designed considering mainly the input RMS current, which depends on the output deliverable current (I_{OUT}) and the duty cycle (D) for regulation as follows:

$$I_{rms} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

The equation reaches its maximum value, $I_{OUT}/2$, with D = 0.5. The losses depend on the input capacitor's ESR and, in the worst case, are:

$$P = ESR \cdot (I_{OUT}/2)^2$$

12 20 A demonstration board

The L6728D demonstration board is constructed using a four-layer PCB, and is designed as a step-down DC-DC converter. The board demonstrates the operation of the device in a general-purpose application. The input voltage can range from 5 V to 12 V buses and the output voltage is fixed at 1.25 V. The application can deliver an output current up to 30 A. The switching frequency is 300 kHz.

Figure 10. 20 A demonstration board (left) and component placement (right)

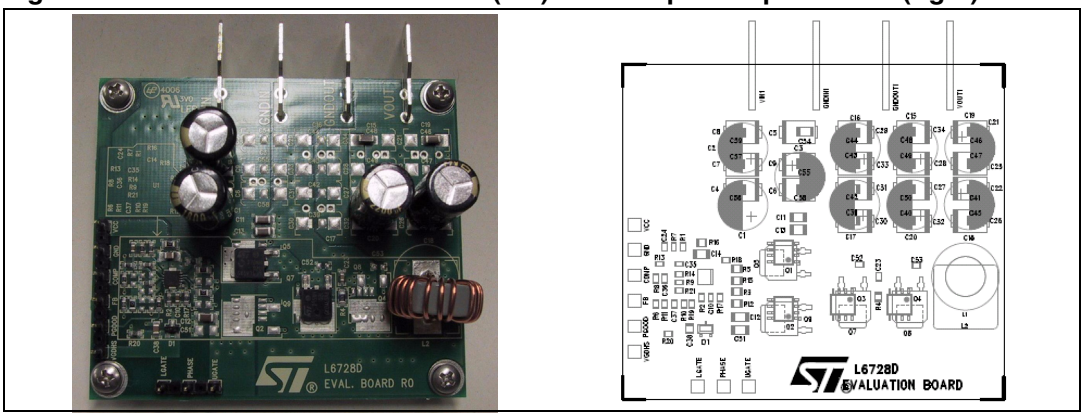


Figure 11. 20 A demonstration board top (left) and bottom (right) layers

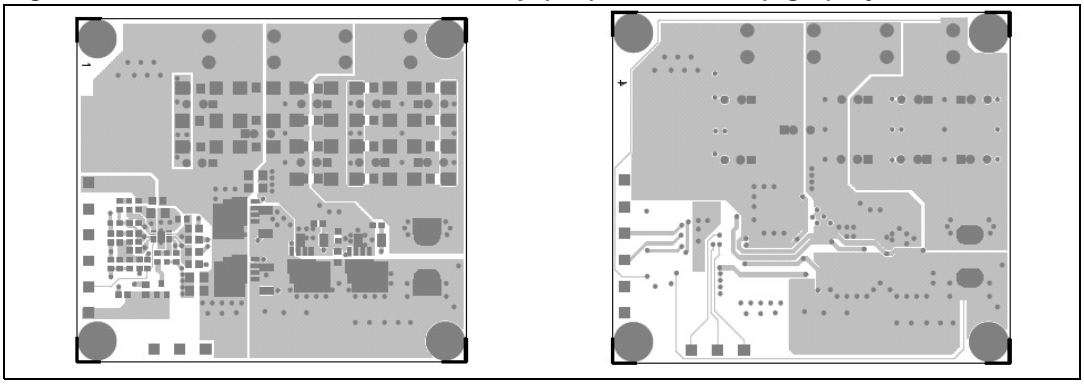


Figure 12. 20 A demonstration board inner layers

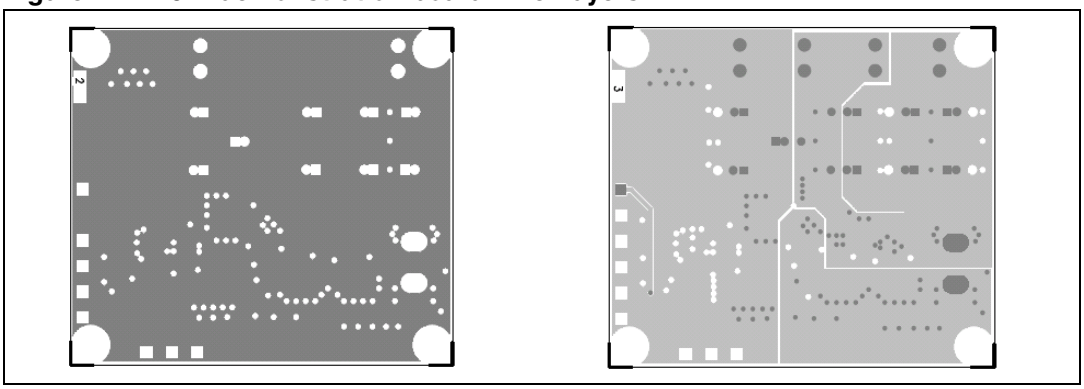


Figure 13. 20 A demonstration board schematic

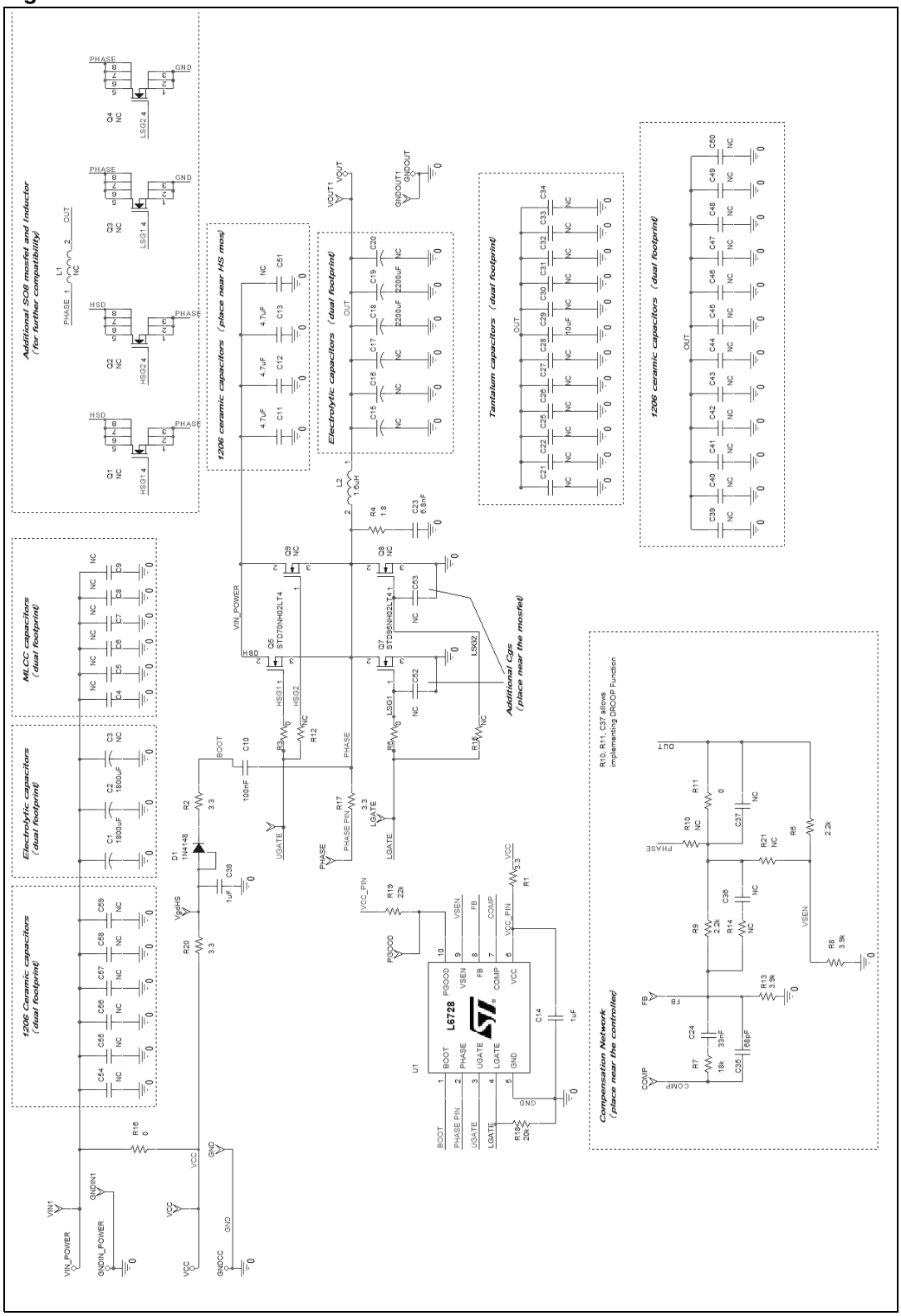


Table 6. 20 A demonstration board - bill of material

Qty	Reference	Description	Package
Capacitors			
2	C1, C2	Electrolytic capacitor 1800 µF 16 V Nippon chemi-con KZJ or KZG	Radial 10 x 25 mm
1	C10	MLCC, 100 nF, 16V, X7R	SMD0603
3	C11 to C13	MLCC, 4.7 µF, 16V, X5R Murata GRM31CR61C475MA01	SMD1206
2	C14, C38	MLCC, 1 µF, 16V, X7R	SMD0805
2	C15, C19	MLCC, 10 µF, 6.3 V, X7R Murata GRM31CR70J106KA01L	SMD1206
2	C18, C20	Electrolytic capacitor 2200 µF 6.3 V Nippon chemi-con KZJ or KZG	Radial 10 x 20 mm
1	C23	MLCC, 6.8 nF, X7R	SMD0603
1	C24	MLCC, 33 nF, X7R	
1	C35	MLCC, 68 pF, X7R	
Resistors			
4	R1, R2, R20, R17	Resistor, 3R3, 1/16W, 1%	SMD0603
4	R3, R5, R11, R16	Resistor, 0R, 1/8W, 1%	SMD0805
1	R4	Resistor, 1R8, 1/8W, 1%	
2	R6, R9	Resistor, 2K2, 1/16W, 1%	SMD0603
2	R8, R13	Resistor, 3K9, 1/16W, 1%	
1	R7	Resistor, 18K, 1/16W, 1%	
1	R19	Resistor, 22K, 1/16W, 1%	
1	R18	Resistor, 20K, 1/16W, 1%	
Inductor			
1	L1	Inductor, 1.25 µH, T60-18, 6 turns Easymagnet AP106019006P-1R1M	na
Active components			
1	D1	Diode, 1N4148 or BAT54	SOT23
1	Q5	STD70N02L	DPACK
1	Q7	STD95NH02LT4	
1	U1	Controller, L6728D	DFN10, 3x3 mm

12.1 Board description

12.1.1 Power input (Vin)

This is the input voltage for the power conversion. The high-side drain is connected to this input. This voltage can range from 1.5 V to 12 V bus.

If the voltage is between 4.5 V and 12 V it can also supply the device (through the Vcc pin) and in this case the R16 (0 Ω) resistor must be present.

12.1.2 Output (Vout)

The output voltage is fixed at 1.25 V but can be changed by replacing the resistors R8 (sense partition lower resistor) and R13 (feedback partition lower resistor). R18 allows adjustment of the OCP threshold.

12.1.3 Signal input (Vcc)

When using the input voltage Vin to supply the controller, no power is required at this input. However the controller can be supplied separately from the power stage through the Vcc input (4.5-12 V) and, in this case, the R16 (0 Ω) resistor must be unsoldered.

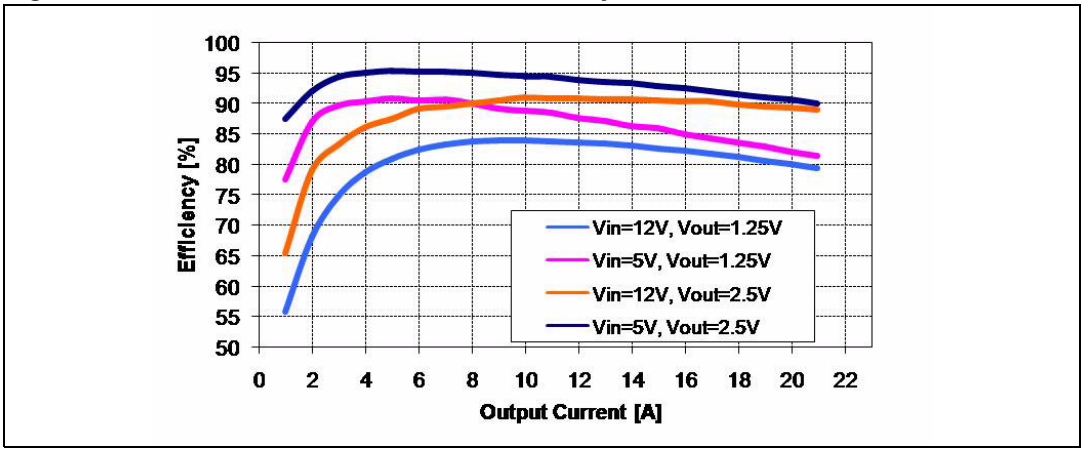
12.1.4 Test points

Several test points are provided for easy access to all the important signals that characterize the device:

- COMP: The output of the error amplifier
- FB: The inverting input of the error amplifier
- PGOOD: Signaling regular functioning (active high)
- VGDHS: The bootstrap diode anode
- PHASE: Phase node
- LGATE: Low-side gate pin of the device
- HGATE: High-side gate pin of the device

12.1.5 Board characterization

Figure 14. 20 A demonstration board efficiency



13 5 A demonstration board

The L6728D demonstration board is constructed using a two-layer PCB, and is designed as a step-down DC-DC converter. The board demonstrates the operation of the device in a general-purpose, low-current application. The input voltage can range from 5 V to 12 V buses and the output voltage is fixed at 1.25 V. The application can deliver an output current in excess of 5 A. The switching frequency is 300 kHz.

Figure 15. 5 A demonstration board (left) and component placement (right)

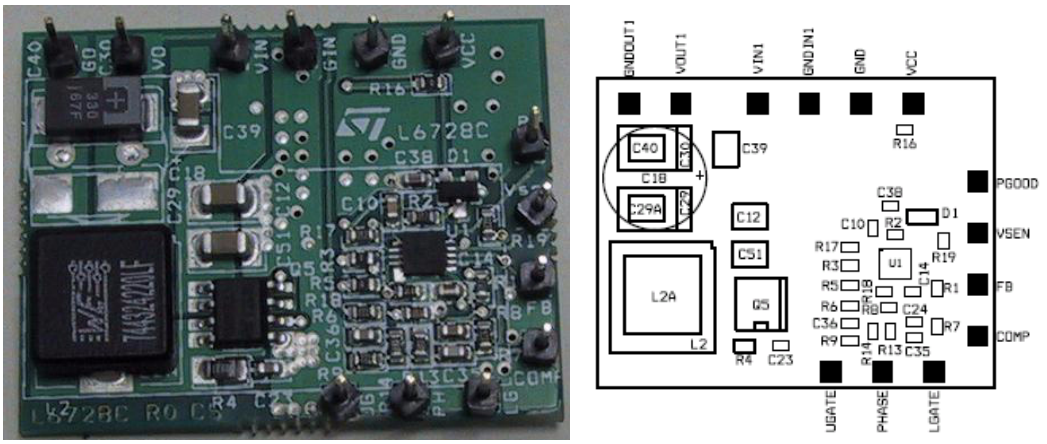


Figure 16. 5 A demonstration board top (left) and bottom (right) layers

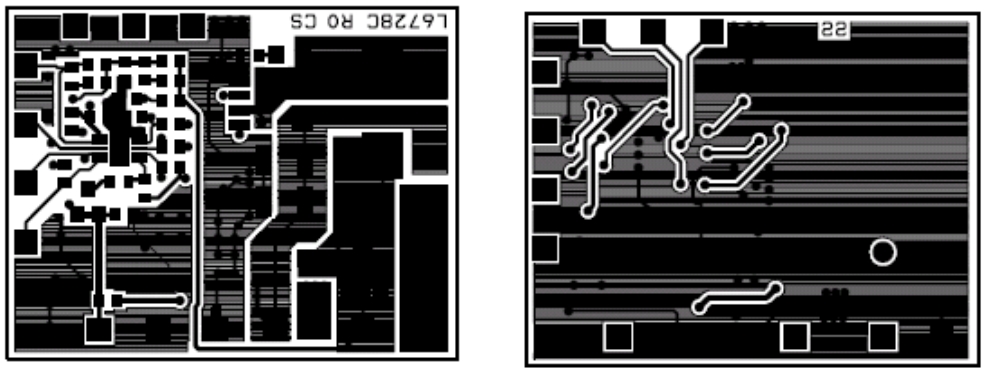
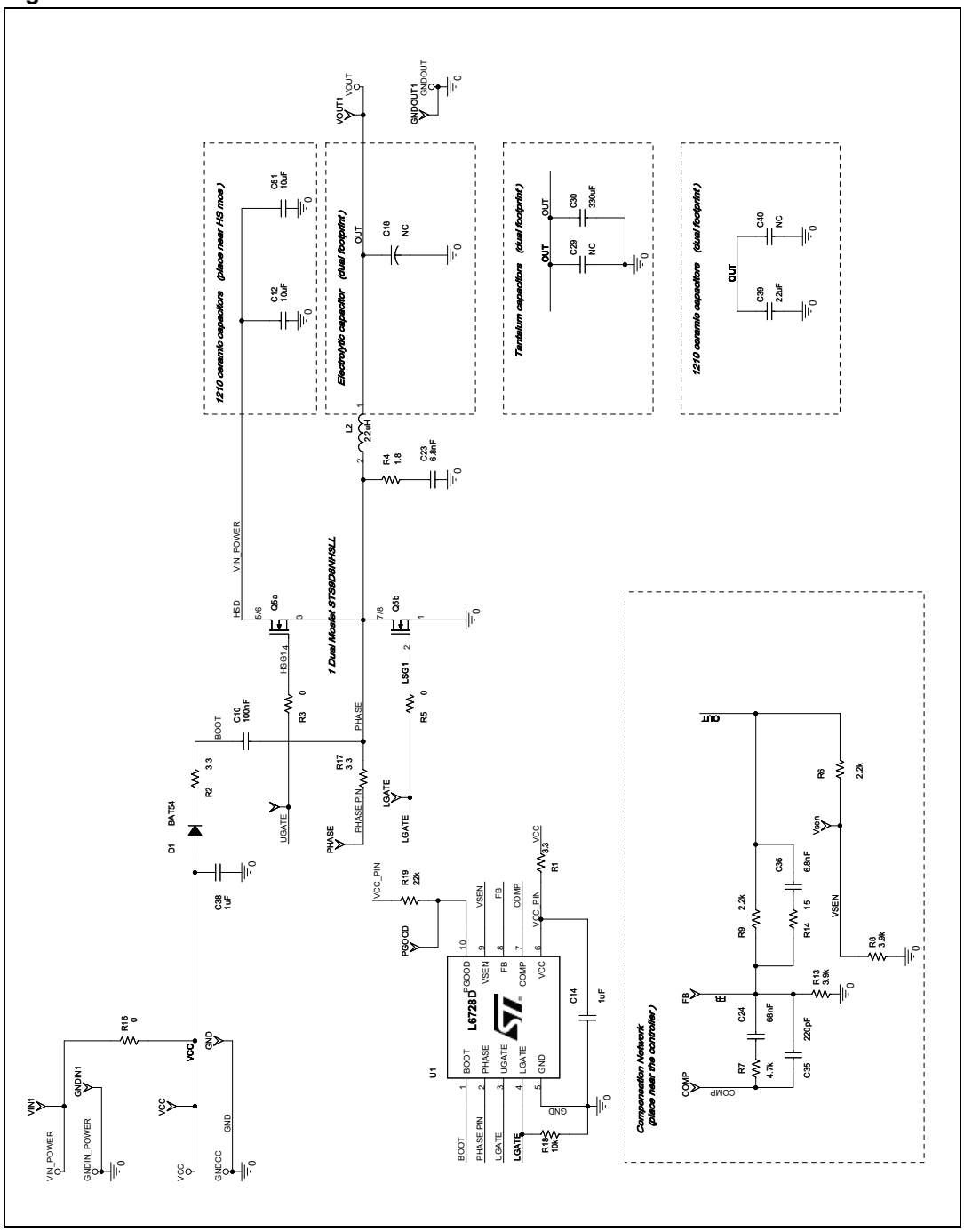


Figure 17. 5 A demonstration board schematic



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Qty	Reference	Description	Package
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1	C10	MLCC, 100 nF, 16 V, X7R	SMD0603
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1	C39	MLCC, 22 µF, 6.3 V, X5R Murata GRM31CR60J226ME19L	SMD1206
1	C30	330 µF, 6.3 V, 9 mΩ Sanyo 6TPF330M9L	SMD7343
2	C23, C36	MLCC, 6.8 nF, X7R	SMD0603
1	C24	MLCC, 68 nF, X7R	
1	C35	MLCC, 220 pF, X7R	
Resistors			
3	R1, R2, R17	Resistor, 3R3, 1/16 W, 1%	SMD0603
3	R3, R5, R16	Resistor, 0R, 1/16 W, 1%	SMD0603
1	R4	Resistor, 1R8, 1/8 W, 1%	SMD0805
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1	R7	Resistor, 4K7, 1/16 W, 1%	
1	R19	Resistor, 22K, 1/16 W, 1%	
1	R18	Resistor, 10K, 1/16 W, 1%	
Inductor			
1	L1	Inductor, 2.2 µH, WURTH 744324220LF	na
Active components			
1	D1	Diode, BAT54	SOT23
1	Q5	STS9D8NH3LL	SO8
1	U1	Controller, L6728D	DFN10, 3x3 mm

13.1 Board description

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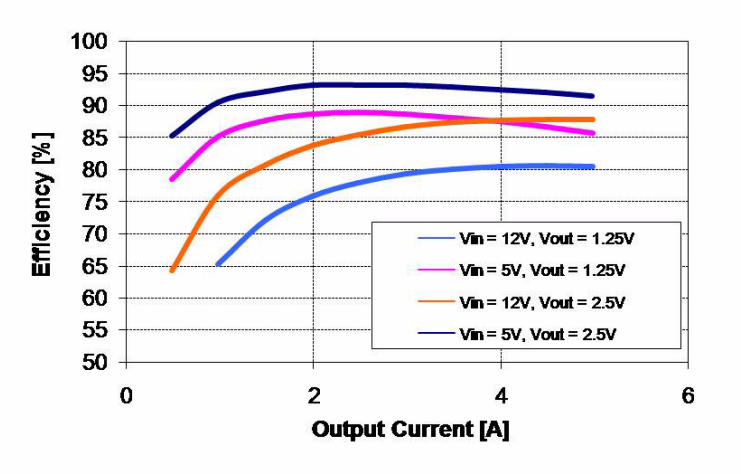
13.1.5 Board characterization

Figure 18. 5 A demonstration board efficiency



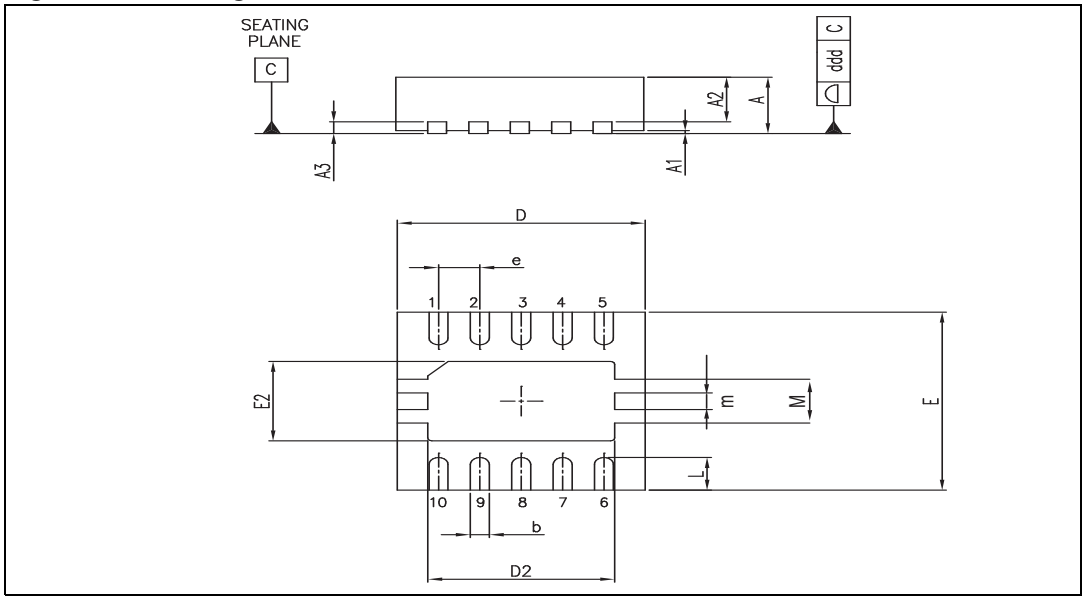
14 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 8. DFN10 mechanical data

Dim.	mm			mils		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	31.5	35.4	39.4
A1		0.02	0.05		0.8	2.0
A2		0.70			27.6	
A3		0.20			7.9	
b	0.18	0.23	0.30	7.1	9.1	11.8
D		3.00			118.1	
D2	2.21	2.26	2.31	87.0	89.0	90.9
E		3.00			118.1	
E2	1.49	1.64	1.74	58.7	64.6	68.5
e		0.50			19.7	
L	0.3	0.4	0.5	11.8	15.7	19.7
M		0.75			29.5	
m		0.25			9.8	

Figure 19. Package dimensions



15 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Feb-2010	1	Initial release.

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