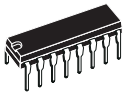
L6598

HIGH VOLTAGE RESONANT CONTROLLER

1 FEATURES

- HIGH VOLTAGE RAIL UP TO 600V
- dV/dt IMMUNITY ±50V/ns IN FULL TEMPERATURE RANGE
- DRIVER CURRENT CAPABILITY: 250mA SOURCE 450mA SINK
- SWITCHING TIMES 80/40ns RISE/FALL WITH 1nF LOAD
- CMOS SHUT DOWN INPUT
- UNDER VOLTAGE LOCK OUT
- SOFT START FREQUENCY SHIFTING TIMING
- SENSE OP AMP FOR CLOSED LOOP CONTROL OR PROTECTION FEATURES
- HIGH ACCURACY CURRENT CONTROLLED OSCILLATOR
- INTEGRATED BOOTSTRAP DIODE
- CLAMPING ON Vs
- SO16, DIP16 PACKAGES

Figure 1. Packages



DIP-16

SO-16N

Table 1. Order Codes

Part Number	Package
L6598	DIP-16
L6598D	SO-16N
L6598D013TR	Tape & Reel

2 DESCRIPTION

The device is manufactured with the BCD OFF LINE technology, able to ensure voltage ratings up to 600V, making it perfectly suited for AC/DC Adapters and wherever a Resonant Topology can be beneficial. The device is intended to drive two Power MOS, in the classical Half Bridge Topology. A dedicated Timing Section allows the designer to set Soft Start Time, Soft Start and Minimum Frequency. An Error Amplifier, together with the two Enable inputs, are made available. In addition, the integrated Bootstrap Diode and the Zener Clamping on low voltage supply, reduces to a minimum the external parts needed in the applications.

Figure 2. Block Diagram

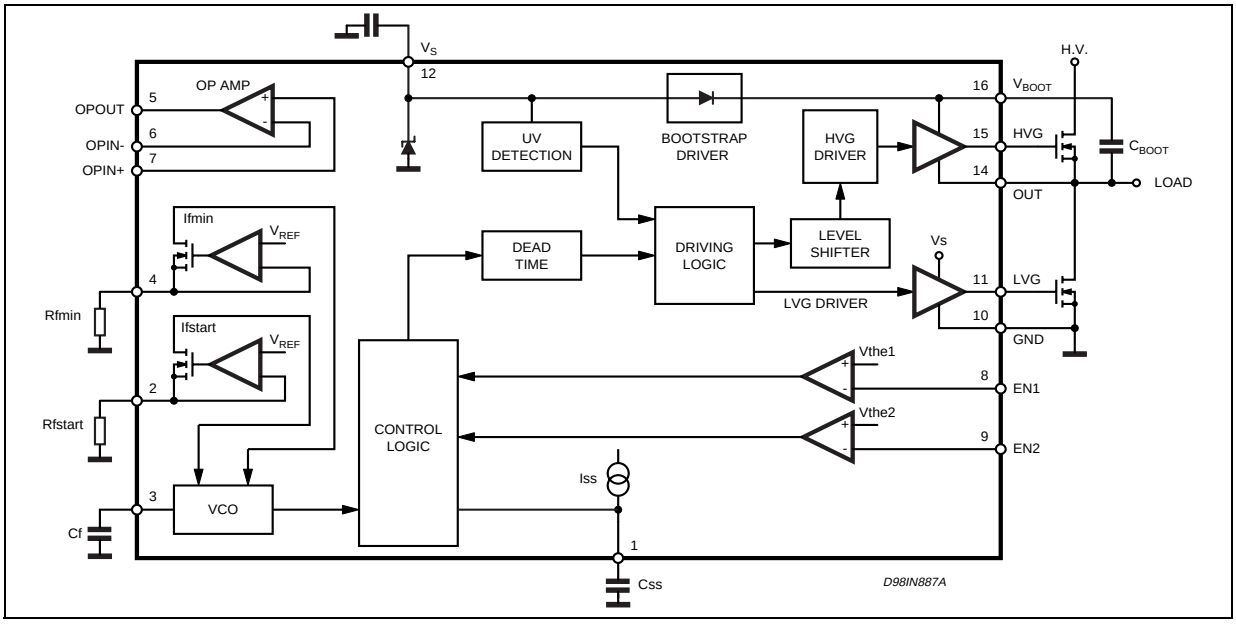


Figure 3. Pin Connection

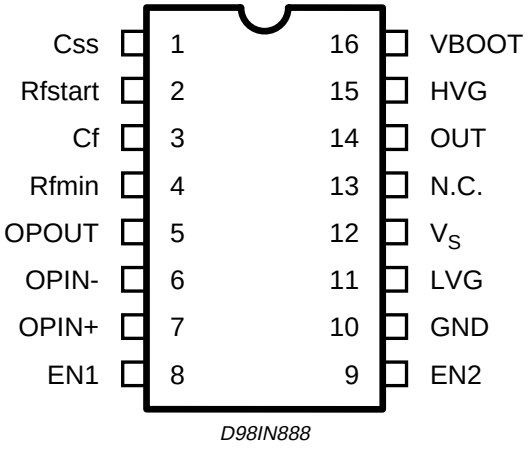


Table 2. Thermal Data

Symbol	Parameter	SO16N	DIP16	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	120	80	°C/W

Table 3. Pin Function

N.	Name	Function
1	C_{SS}	Soft Start Timing Capacitor
2	R_{fstart}	Soft Start Frequency Setting - Low Impedance Voltage Source - See also C_f
3	C_f	Oscillator Frequency Setting - see also R_{fmin}, R_{fstart}
4	R_{fmin}	Minimum Oscillation Frequency Setting - Low Impedance Voltage Source - See also C_f
5	OP_{out}	Sense OP AMP Output - Low Impedance
6	OP_{on-}	Sense Op Amp Inverting Input - High Impedance
7	OP_{on+}	Sense Op Amp Non Inverting Input - High Impedance
8	EN1	Half Bridge Latched Enable
9	EN2	Half Bridge Unlatched Enable
10	GND	Ground
11	LVG	Low Side Driver Output
12	V_S	Supply Volatge with Internal Zener Clamp
13	N.C.	Not Connected
14	OUT	High Side Driver Reference
15	HVG	High Side Driver Output
16	V_{boot}	Bootstrapped Supply Voltage

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
I_S	Supply Current at V_{cl} (*)	25	mA
V_{LVG}	Low Side Output	14.6	V
V_{OUT}	High Side Reference	-1 to V_{BOOT} -18	V
V_{HVG}	High Side Output	-1 to V_{BOOT}	V
V_{BOOT}	Floating Supply Voltage	618	V
$dV_{BOOT/dt}$	VBOOT pin Slew Rate (repetitive)	±50	V/ns
$dV_{OUT/dt}$	OUT pin Slew Rate (repetitive)	±50	V/ns
V_{ir}	Forced Input Voltage (pins Rfmin, Rfstart)	-0.3 to 5	V
V_{ic}	Forced Input Volatge (pins Css, Cf)	-0.3 to 5	V
V_{EN1}, V_{EN2}	Enable Input Voltage	-0.3 to 5	V
I_{EN1}, I_{EN2}	Enable Input Current	±3	mA
V_{opc}	Sense Op Amp Common Mode Range	-0.3 to 5	V
V_{opd}	Sense Op Amp Differential Mode Range	-5 to 5	V
V_{opo}	Sense Op Amp Output Voltage (forced)	4.6	V
T_{stg}	Storage Temperature	-40 to +150	°C
T_j	Junction Temperature	-40 to +150	°C
T_{amb}	Ambient Temperature	-40 to +125	°C

(*) The device is provided of an internal Clamping Zener between GND and the Vs pin, It must not be supplied by a low impedance voltage source.
Note : ESD immunity for pins 14, 15 and 16 is guaranteed up to 900 (Human Body Model).

Table 5. Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	10 to V_{cl}	V
V_{out} (*)	High Side Reference	-1 to Vboot-V_{cl}	V
V_{boot} (*)	Floating Supply Rail	500	V
f_{max}	Maximum Switching Frequency	400	kHz

(*) If the condition Vboot - Vout < 18 is guaranteed, Vout can range from -3 to 580V.

Table 6. Electrical Characteristcs

(V_S = 12V; V_{BOOT} - V_{OUT} = 12V; T_{amb} = 25°C)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE							
V_{suvp}	12	V_S Turn On Threshold		10	10.7	11.4	V
V_{suvn}		V_S Turn Off Threshold		7.3	8	8.7	V
V_{suvh}		Supply Voltage Under Voltage hysteresis			2.7		V
V_{cl}		Supply Voltage Clamping		14.6	15.6	16.6	V
I_{su}		Start Up Current	$V_s < V_{suvn}$			250	µA
I_q		Quiescent Current, fout = 60kHz, no load	$V_s > V_{suvp}$		2	3	mA
HIGH VOLTAGE SECTION							
$I_{bootleak}$	16	BOOT pin Leakage Current	V_{BOOT} = 580V			5	µA
$I_{outleak}$	14	OUT pin Leakage Current	V_{OUT} = 562V			5	µA
R_{don}	16	Bootstrap Driver On Resistance		100	150	300	Ω
HIGH/LOW SIDE DRIVERS							
I_{hvgso}	15	High Side Driver Source Current	V_{HVG}-V_{OUT} = 0	170	250		mA
I_{hvgsi}		High Side Driver Sink Current	V_{HVG}-V_{BOOT} = 0	300	450		mA
I_{lvgso}	11	Low Side Driver Source Current	$V_{LVG-GND}$ = 0	170	250		mA
I_{lvgsi}		Low Side Driver Sink Current	$V_{LVG - VS}$ = 0	300	450		mA
t_{rise}	15,11	Low/High Side Output Rise Time	C_{load} = 1nF		80	120	ns
t_{fall}			C_{load} = 1nF		40	80	ns
OSCILLATOR							
DC	14	Output Duty Cycle		48	50	52	%
f_{min}		Minimum Output Oscillation Frequency	C_f = 470pF; R_{fmin} = 50k	58.2	60	61.8	kHz
f_{start}		Soft Start Output Oscillation Frequency	C_f = 470pF; R_{fmin} = 50k; R_{fstart} = 47k	114	120	126	kHz
V_{ref}	2, 4	Voltage to Current Converters Threshold		1.9	2	2.1	V
t_d	14	Dead Time between Low and High Side Conduction		0.2	0.27	0.35	µs
TIMING SECTION							
k_{ss}	1	Soft Start Timing constant	C_{ss} = 330nF	0.115	0.15	0.185	s/µF
SENSE OP AMP							
I_{IB}	6, 7	Input Bias Current				0.1	µA
V_{io}		Input Offset Voltage		-10		10	mV
R_{out}	5	Output Resistance		200		300	Ω
I_{out-}		Source Output Current	V_{out} = 4.5V	1			mA
I_{out+}		Sink Output Current	V_{out} = 0.2V	1			mA
V_{ic}	6,7	OP AMP input common mode range		-0.2		3	V

Table 6. Electrical Characteristcs (continued)
(V_S = 12V; V_{BOOT} - V_{OUT} = 12V; T_{amb} = 25°C)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
GBW		Sense Op Amp Gain Band Width Product (*)		0.5	1		MHz
G_{dc}		DC Open Loop Gain		60	80		dB
COMPARATORS							
V_{the1}	8	Enabling Comparator Threshold		0.56	0.6	0.64	V
V_{the2}	9	Enabling Comparator Threshold		1.05	1.2	1.35	V
t_{pulse}	8,9	Minimum Pulse lenght				200	ns

(*) Guaranted by design

Figure 4. EN2 Timing Diagrams

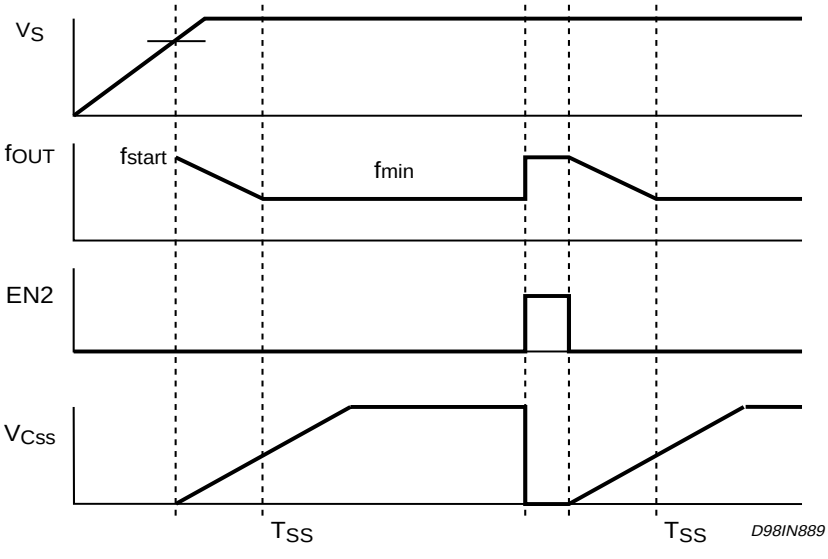


Figure 5. EN1 Timing Diagrams

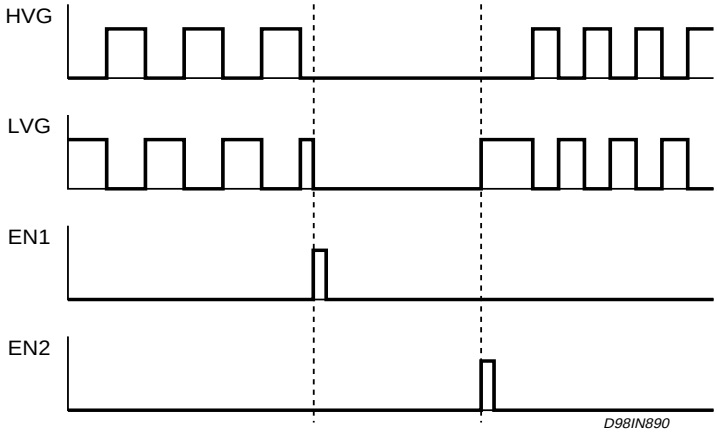
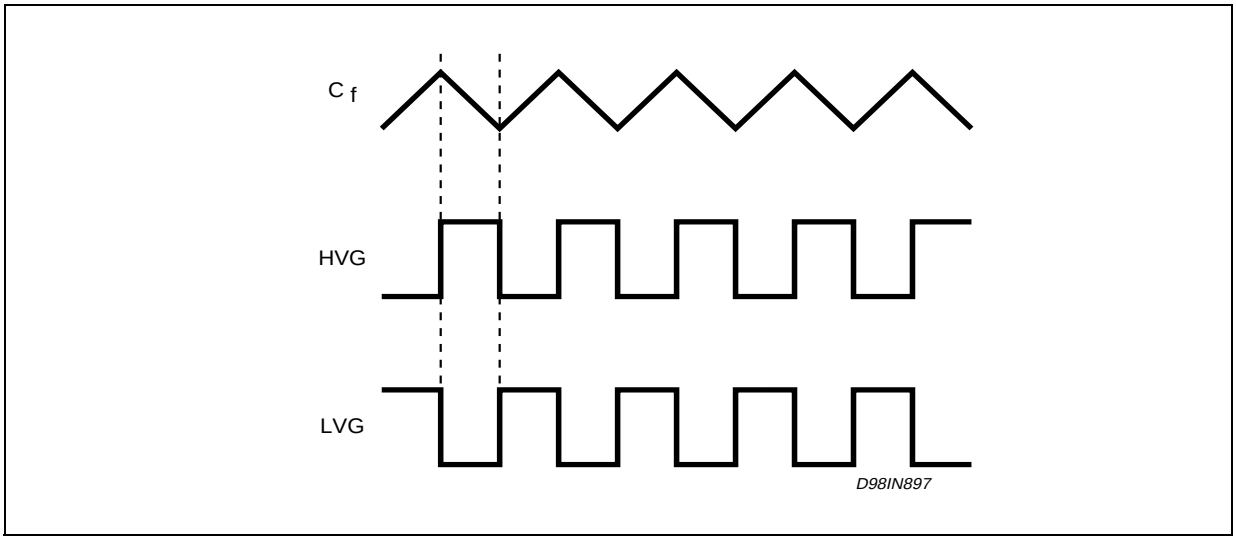


Figure 6. Oscillator/Output Timing Diagram



3 BLOCK'S DIAGRAM DESCRIPTION

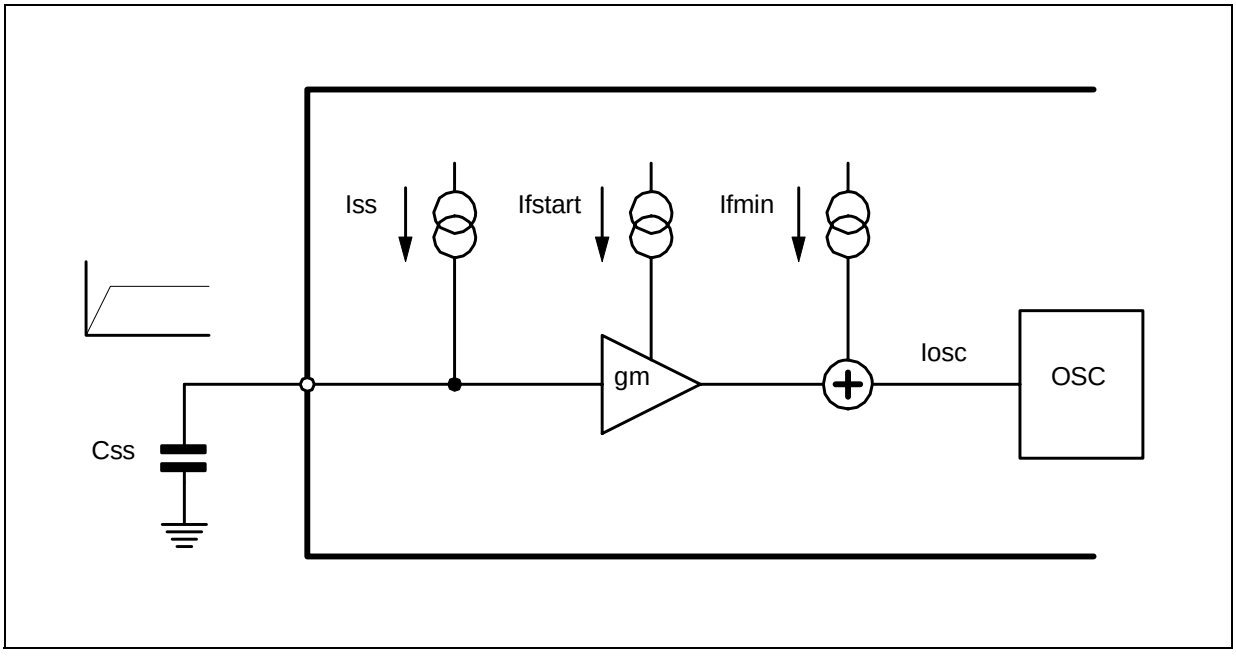
3.1 High/Low Side driving section

An High and Low Side driving Section provide the proper driving to the external Power MOS or IGBT. An high sink/source driving current (450/250 mA typ) ensure fast switching times also when size4 Power MOS are used. The internal logic ensures a minimum dead time to avoid cross-conduction of the power devices.

3.2 Timing and Oscillator Section

The device is provided of a soft start function. It consists in a period of time, T_{SS}, in which the switching frequency shifts from f_{start} to f_{min}. This feature is explained in the following description (ref. fig.7 and fig.8).

Figure 7. Soft Start and frequency shifting block



During the soft start time the current I_{SS} charges the capacitor C_{SS}, generating a voltage ramp which is delivered to a transconductance amplifier, as shown in fig. 7. Thus this voltage signal is converted in a growing current which is subtracted to I_{fstart}. Therefore the current which drives the oscillator to set the frequency during the soft start is equal to:

$$I_{osc} = I_{fmin} + (I_{fstart} - g_m V_{Css}(t)) = I_{fmin} + \left(I_{fstart} - \frac{g_m I_{ss}}{C_{ss}} t\right) \quad [1]$$

$$\text{where } I_{fmin} = \frac{V_{REF}}{R_{fmin}}, I_{fsart} = \frac{V_{REF}}{R_{fstart}}, V_{REF} = 2V \quad [2]$$

At the start-up (t=0) the oscillator frequency is set by:

$$I_{osc}(0) = I_{fmin} + I_{fstart} = V_{REF}\left(\frac{1}{R_{fmin}} + \frac{1}{R_{fstart}}\right) \quad [3]$$

At the end of soft start ($t = T_{SS}$) the second term of eq.1 decreases to zero and the switching frequency is set only by I_{min} (i.e. R_{fmin}):

$$I_{osc}(T_{ss}) = I_{fmin} = \frac{V_{REF}}{R_{fmin}} \quad [4]$$

Since the second term of eq.1 is equal to zero, we have:

$$I_{fstart} - \frac{g_m I_{ss}}{C_{ss}} T_{SS} = 0 \rightarrow T_{SS} = \frac{C_{ss} I_{fstart}}{g_m I_{ss}} \quad [5]$$

Note that there is not a fixed threshold of the voltage across C_{SS} in which the soft start finishes (i.e. the end of the frequency shifting), and T_{SS} depends on C_{SS}, I_{fstart}, g_m, and I_{SS} (eq. 5). Making T_{SS} independent of I_{fstart}, the I_{SS} current has been designed to be a fraction of I_{fstart}, so:

$$I_{SS} = \frac{I_{fstart}}{K} \rightarrow T_{SS} = \frac{C_{ss} I_{fstart}}{g_m I_{fstart} K} \rightarrow T_{SS} = \frac{C_{ss}}{g_m K} \rightarrow T_{SS} - k_{SS} C_{SS} \quad [6]$$

In this way the soft start time depends only on the capacitor C_{SS}. The typical value of the k_{SS} constant (Soft Start Timing Constant) is 0.15 s/µF.

The current I_{osc} is fed to the oscillator as shown in fig. 7. It is twice mirrored (x4 and x8) generating the triangular wave on the oscillator capacitor C_f. Referring to the internal structure of the oscillator (fig.7), a good relationship to compute an approximate value of the oscillator frequency in normal operation is:

$$f_{min} = \frac{1.41}{R_{fmin} C_f} \quad [7]$$

The degree of approximation depends on the frequency value, but it remains very good in the range from 30kHz to 100kHz (figg.9-13)

Figure 8. Oscillator Block

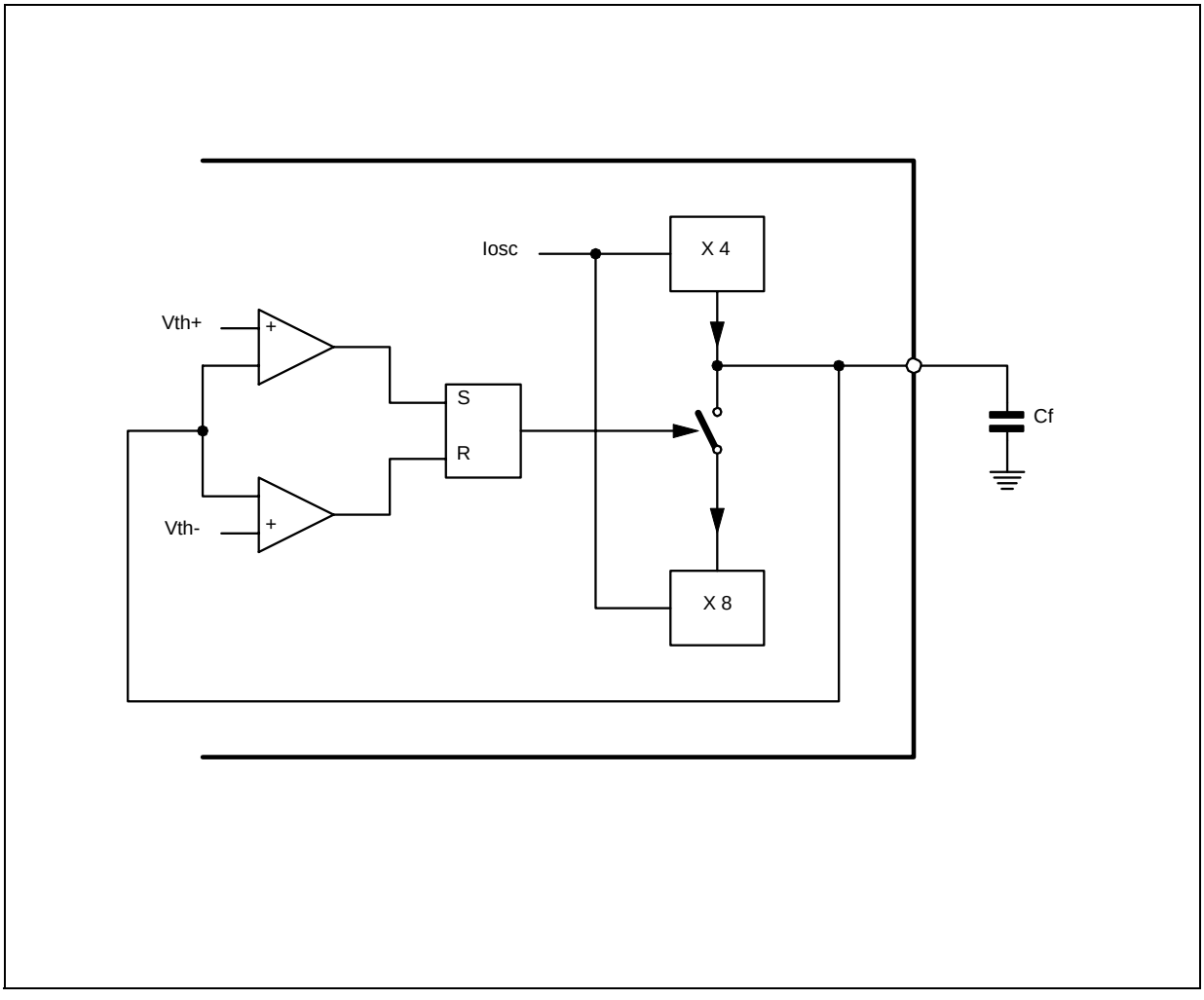


Figure 9. Typ. fmin vs. Rfmin @ Cf = 470pF

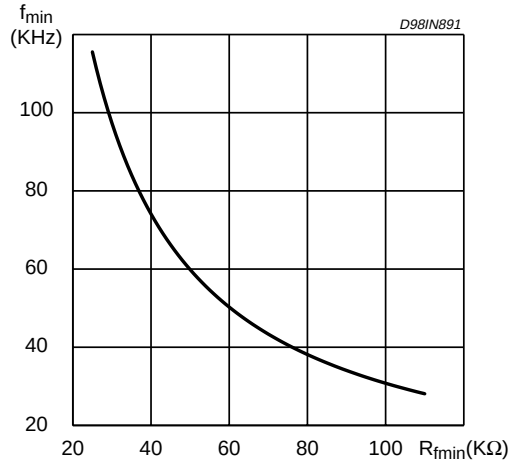


Figure 10. Typ. (fstart-fmin) vs. Rfstar @ Cf = 470pF

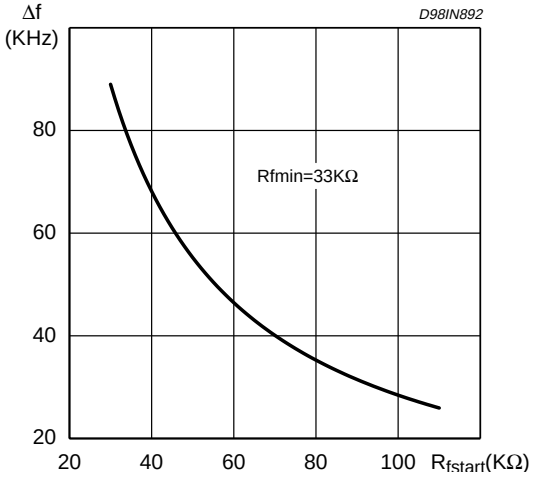


Figure 11. Typ. (fstart-fmin) vs. Rfstar @ Cf = 470pF

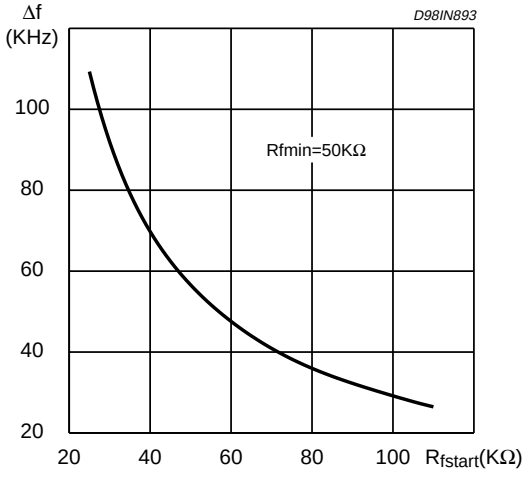


Figure 12. Typ. (fstart-fmin) vs. Rfstar @ Cf = 470pF

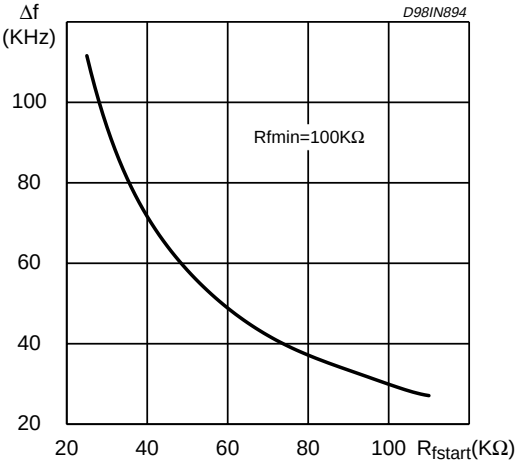
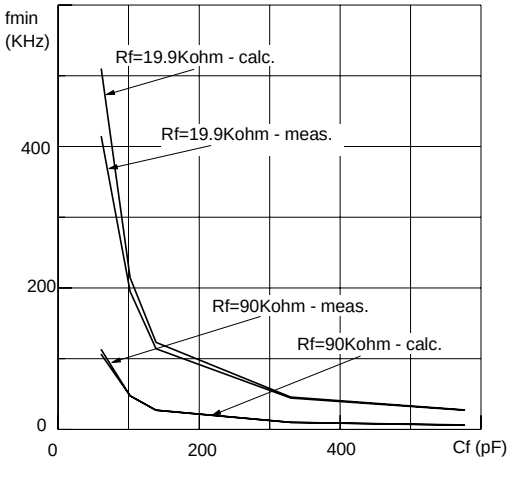


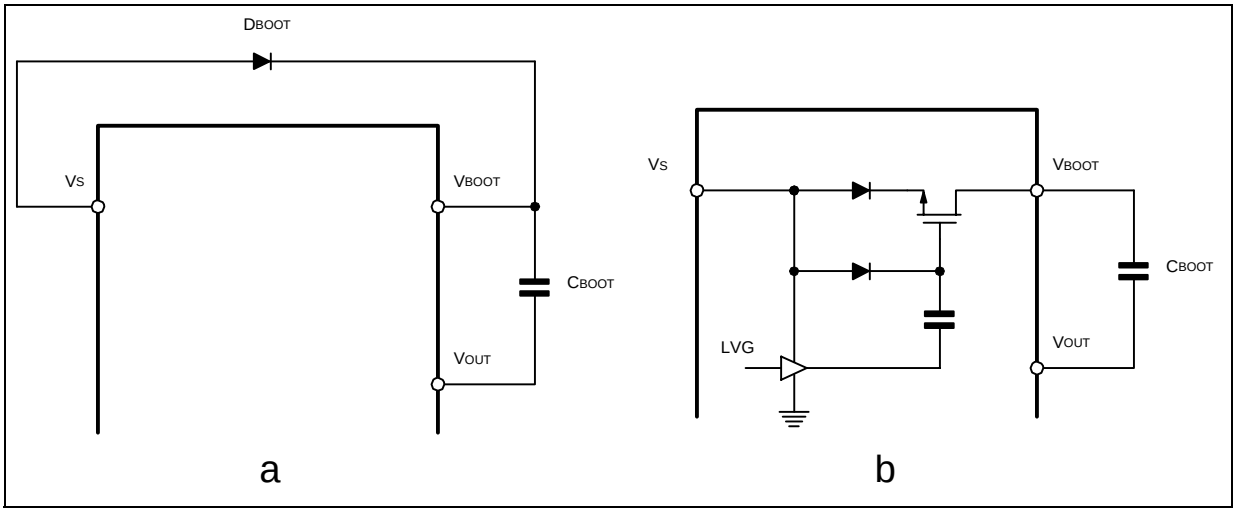
Figure 13. fmin @ different Rf vs Cf



3.3 Bootstrap Section

The supply of the high voltage section is obtained by means of a bootstrap circuitry. This solution normally requires an high voltage fast recovery diode for charging the bootstrap capacitor (fig. 14a). In the device a patented integrated structure, replaces this external diode. It is realised by means of a high voltage DMOS, driven synchronously with the low side driver (LVG), with in series a diode, as shown in fig. 14b.

Figure 14. Bootstrap driver



To drive the synchronised DMOS it is necessary a voltage higher than the supply voltage Vs. This voltage is obtained by means of an internal charge pump (fig. 14b).
The diode connected in series to the DMOS has been added to avoid undesirable turn on of it. The introduction of the diode prevents any current can flow from the V_{boot} pin to the V_S one in case that the supply is quickly turned off when the internal capacitor of the pump is not fully discharged.

The bootstrap driver introduces a voltage drop during the recharging of the capacitor C_{boot} (i.e. when the low side driver is on), which increases with the frequency and with the size of the external power MOS. It is the sum of the drop across the R_{DSON} and of the diode threshold voltage. At low frequency this drop is very small and can be neglected. Anyway increasing the frequency it must be taken in to account. In fact the drop, reducing the amplitude of the driving signal, can significantly increase the R_{DSON} of the external power MOS (and so the dissipation).
To be considered that in resonant power supplies the current which flows in the power MOS decreases increasing the switching frequency and generally the increases of R_{DSON} is not a problem because power dissipation is negligible. The following equation is useful to compute the drop on the bootstrap driver:

$$V_{drop} = I_{charge} R_{dson} + V_{diode} \rightarrow V_{drop} = \frac{Q_g}{T_{charge}} R_{dson} + V_{diode} \quad [8]$$

where Q_g is the gate charge of the external power MOS, R_{dson} is the on resistance of the bootstrap DMOS, and T_{charge} is the time in which the bootstrap driver remains on (about the semiperiod of the switching frequency minus the dead time). The typical resistance value of the bootstrap DMOS is 150 Ohm. For example using a power MOS with a total gate charge of 30nC the drop on the bootstrap driver is about 3V, at a switching frequency of 200kHz. In fact:

$$V_{drop} = \frac{30nC}{2.23\mu s} 150\Omega + 0.6V \sim 2.6V$$

To summarise, if a significant drop on the bootstrap driver (at high switching frequency when large power MOS are used) represents a problem, an external diode can be used, avoiding the drop on the R_{DSON} of the DMOS.

3.4 OP AMP Section

The integrated OP AMP is designed to offer Low Output Impedance, wide band, High input Impedance and wide Common Mode Range. It can be readily used to implement protection features or a closed loop control. For this purpose the OP AMP Output can be properly connected to R_{fmin} pin to adjust the oscillation frequency.

3.5 Comparators

Two CMOS comparators are available to perform protection schemes. Short pulses (>= 200ns) on Comparators Input are recognised. The EN1 input (active High), has a threshold of 0.6V (typical value) forces the device in a latched shut down state (e.g. LVG Low, HVG low, Oscillator stopped), as in the Under Voltage Conditions. Normal Operating conditions are resumed after a power-off power-on sequence. The EN2 input (active high), with a threshold of 1.2V (typical value) restarts a Soft Start sequence (see Timing Diagrams). In addition the EN2 Comparator, when activated, removes a latched shutdown caused by EN1.

Figure 15. Switching Time Waveform Definitions

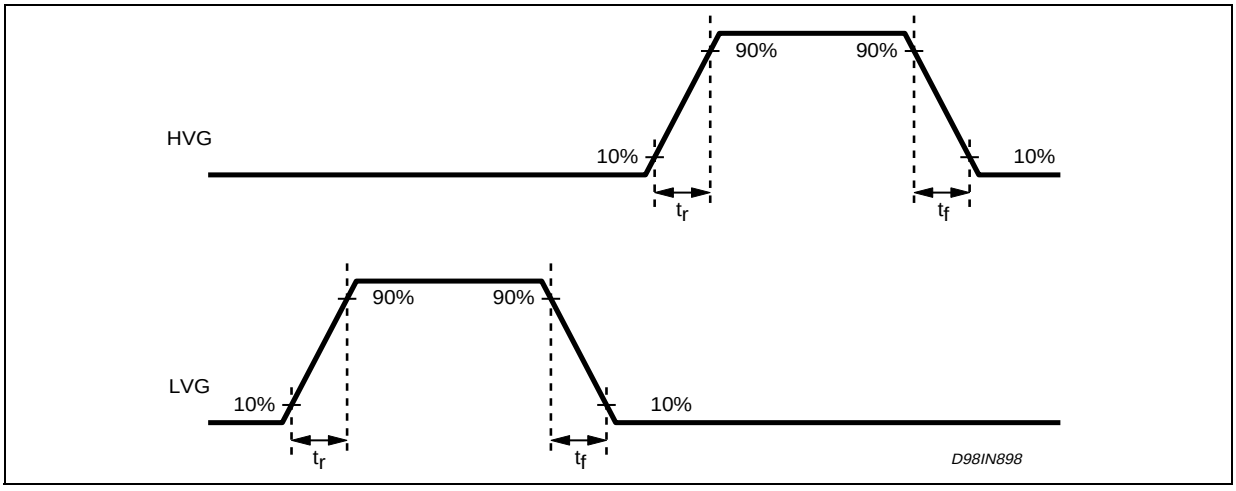


Figure 16. Dead Time and Duty Cycle Waveform Definition

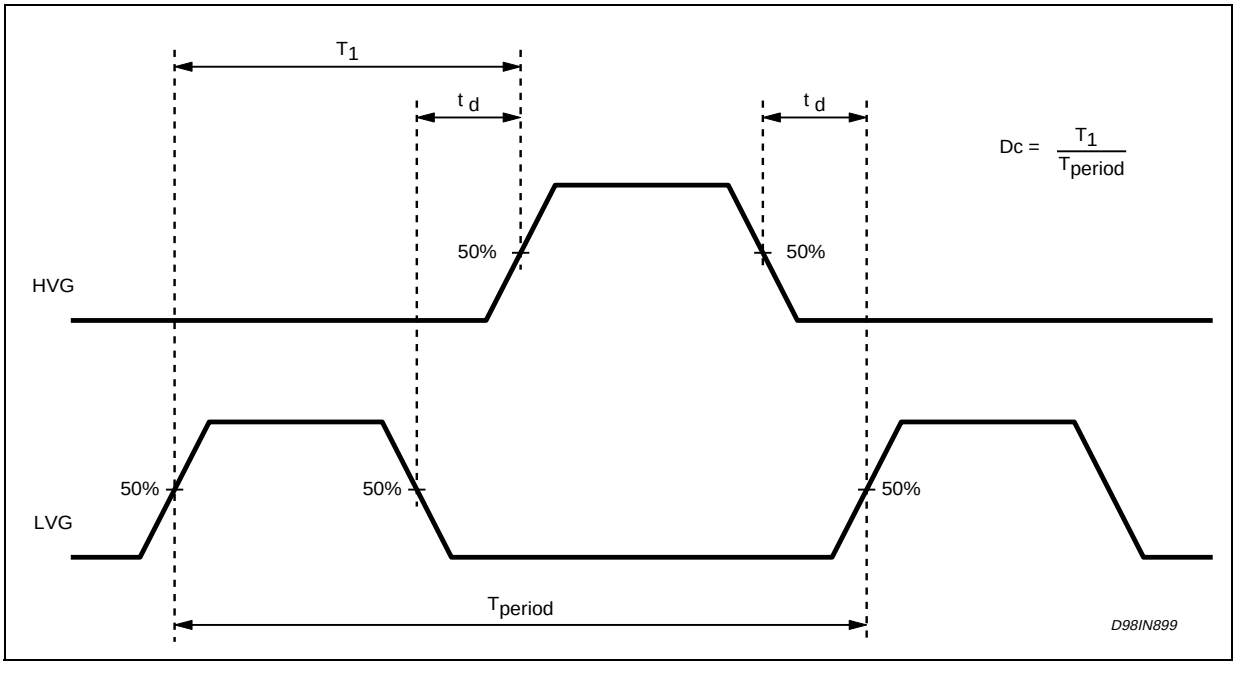


Figure 17. Typ. fmin vs. Temperature

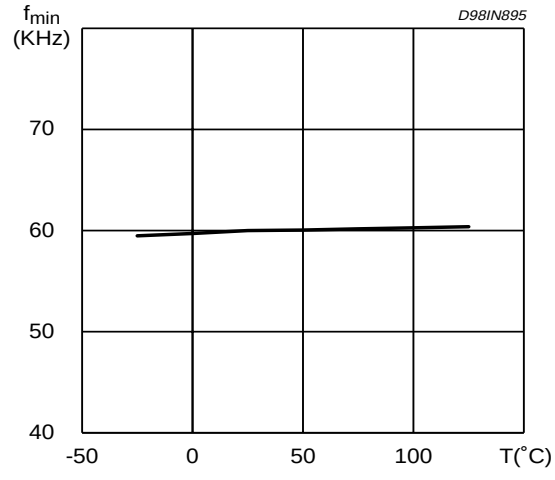


Figure 18. Typ. fstart vs. Temperature

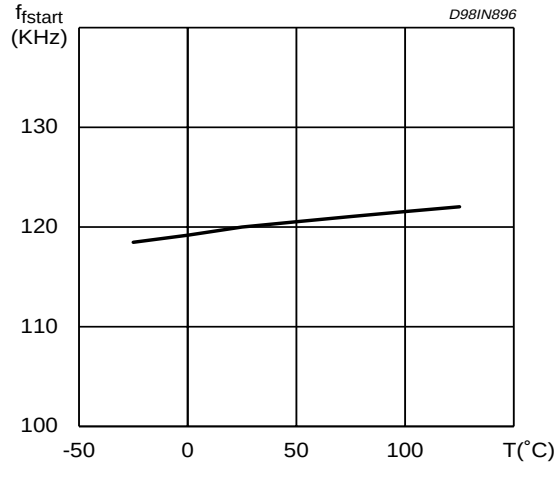


Figure 19. Vs thresholds and clamp vs temp.

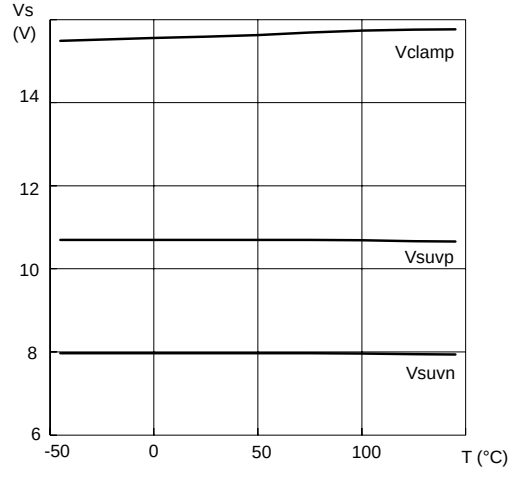


Figure 20. Start Up Current vs Temperature

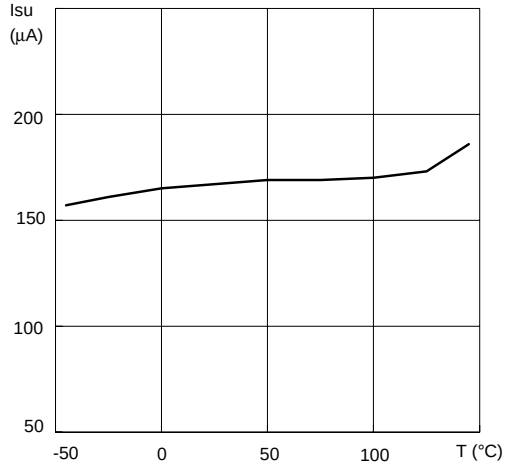


Figure 21. Quiescent Current vs Temperature

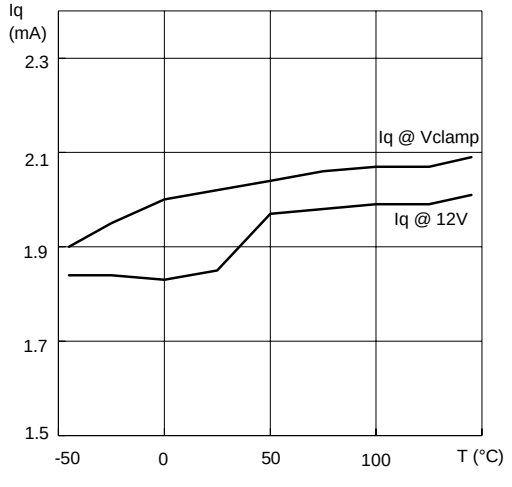


Figure 22. HVG Source and Sink Current vs. Temperature

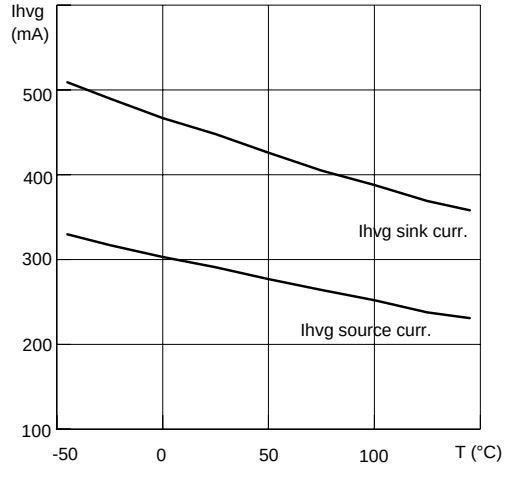


Figure 23. LVG Source and Sink Current vs. Temperature

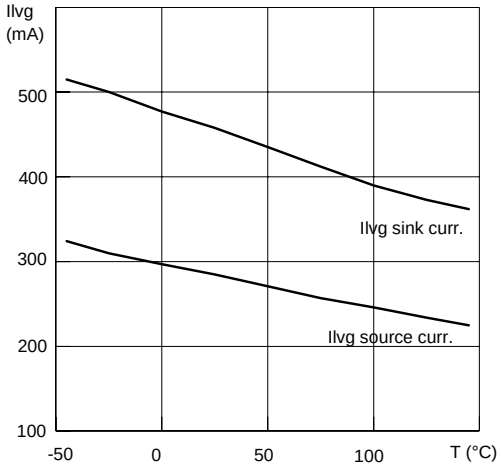


Figure 24. Soft Start Timing Constant vs. Temperature

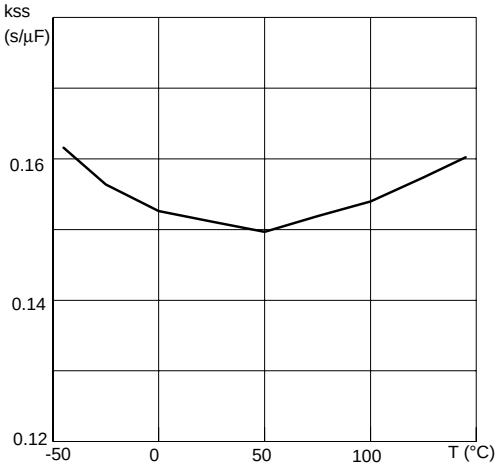


Figure 25. Wide Range AC/DC Adapter Application

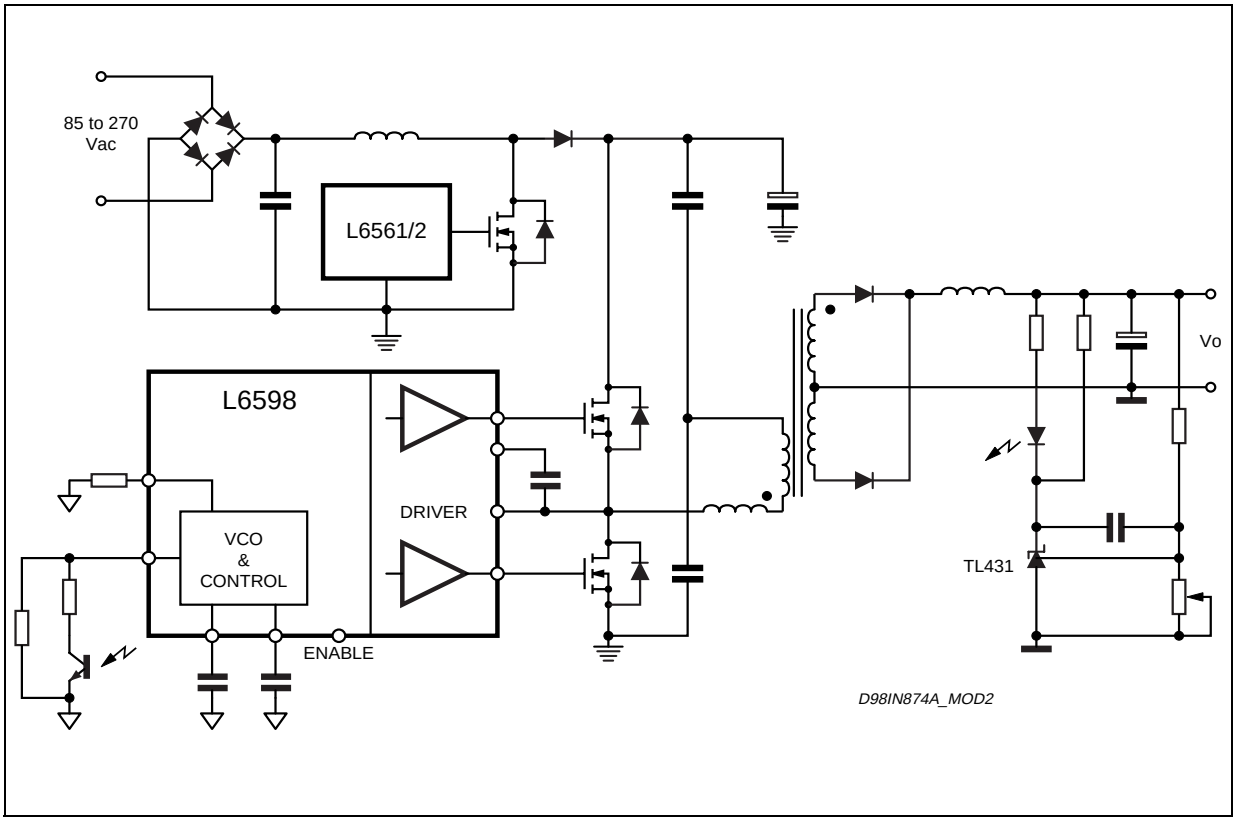
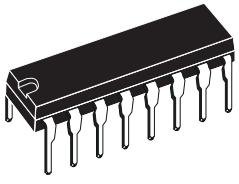


Figure 26. DIP-16 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA



DIP16

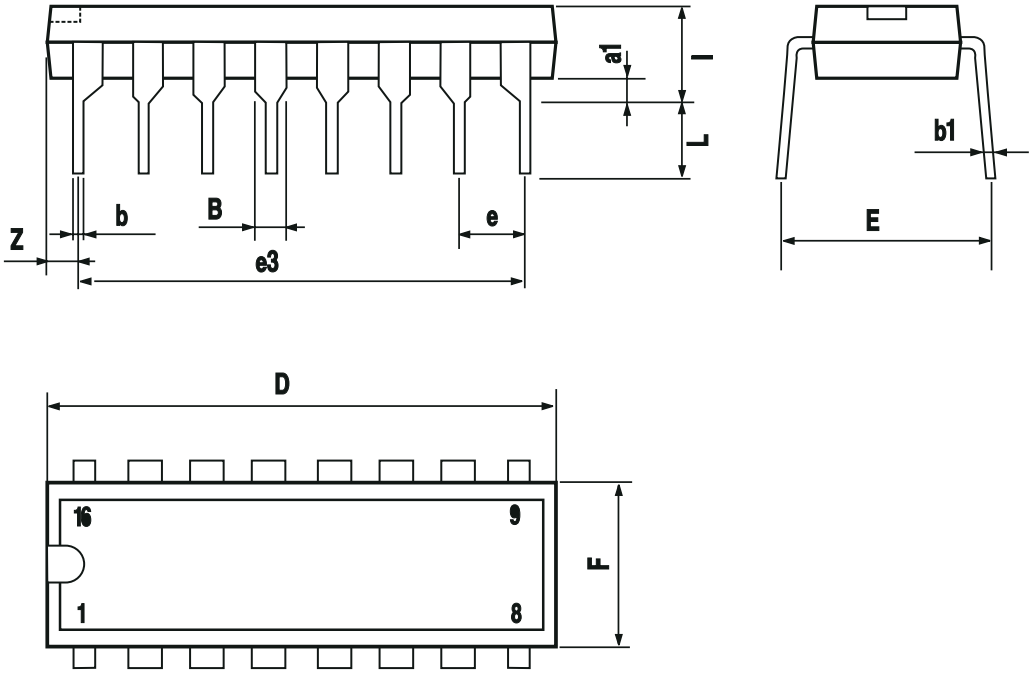
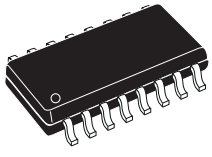


Figure 27. SO-16N Mechanical Data & Package Dimensions

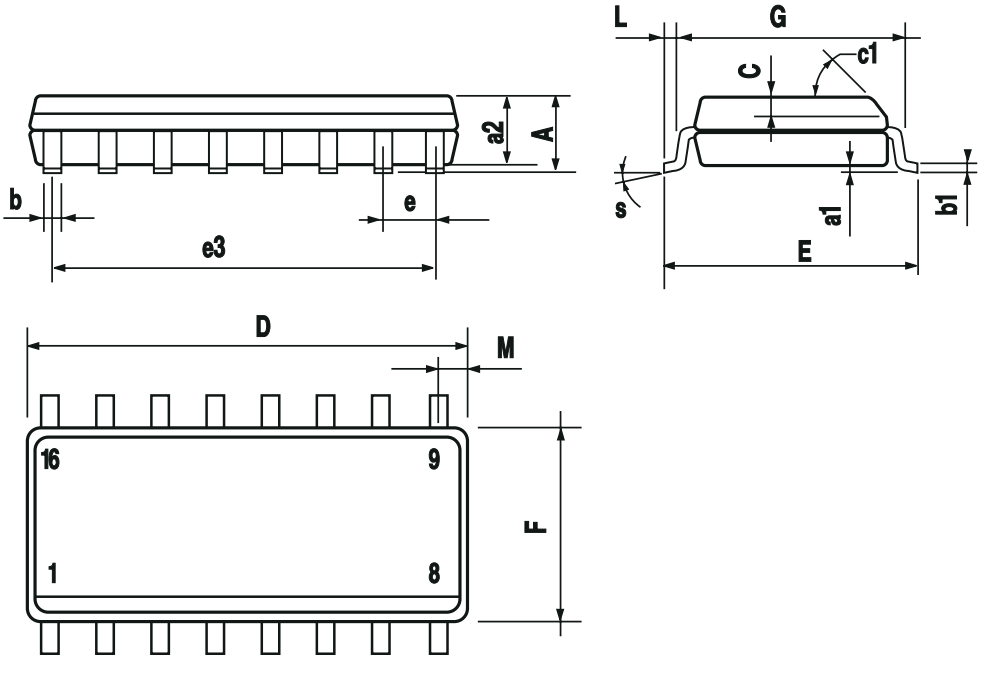
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1			45°	(typ.)		
D(1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F(1)	3.8		4.0	0.150		0.157
G	4.60		5.30	0.181		0.208
L	0.4		1.27	0.150		0.050
M			0.62			0.024
S	8 ° (max.)					

(1) "D" and "F" do not include mold flash or protrusions - Mold flash or protrusions shall not exceed 0.15mm (.006inc.)

OUTLINE AND MECHANICAL DATA



SO16 (Narrow)



0016020 D

Figure 28. Revision History

Date	Revision	Description of Changes
June 2004	5	Changed the impagination following the new release of “Corporate Technical Pubblication Design Guide”. Done a few of corrections in the text.