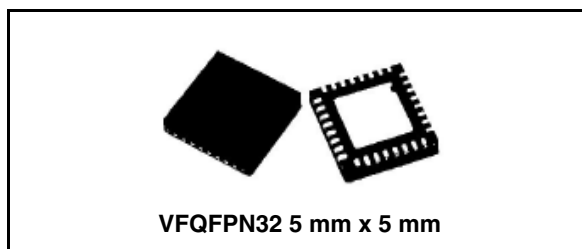


Features

- Operating supply voltage from 8 to 52 V
- 2.8 A output peak current (1.4 A DC)
- $R_{DS(on)}$ 0.73 Ω typ. value @ $T_J = 25^\circ\text{C}$
- Operating frequency up to 100 kHz
- Non dissipative overcurrent protection
- Dual independent constant t_{OFF} PWM current controllers
- Slow decay synchronous rectification
- Cross conduction protection
- Thermal shutdown
- Under voltage lockout
- Integrated fast free wheeling diodes

Applications

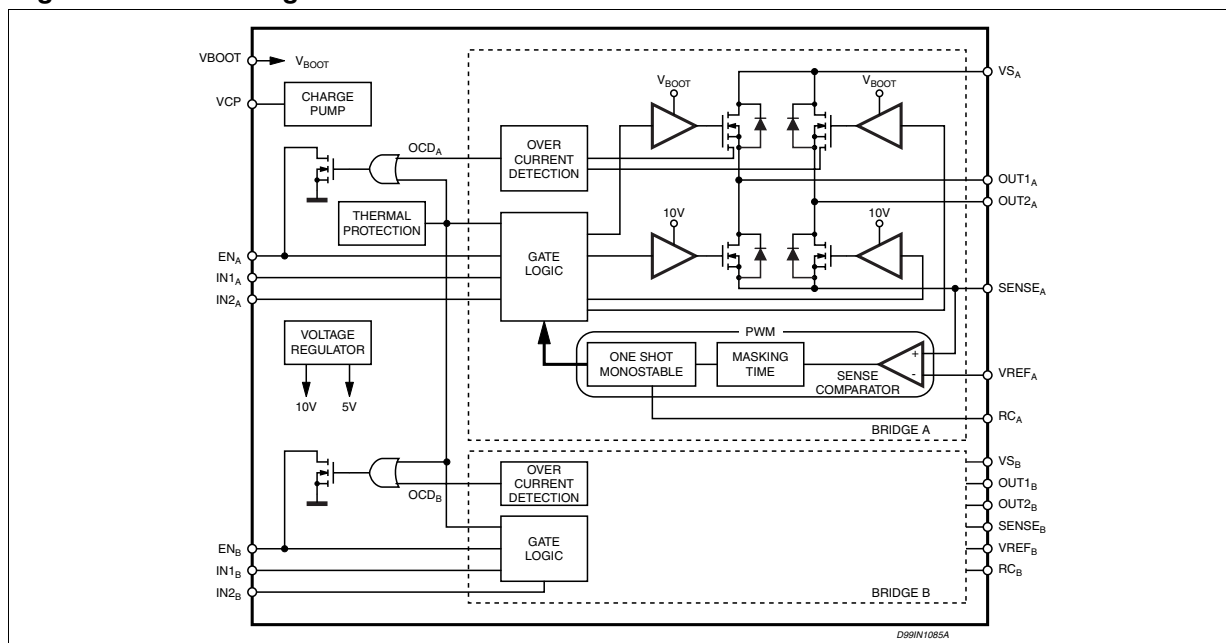
- Bipolar stepper motor
- Dual or quad DC motor



Description

The L6227Q is a DMOS dual full bridge designed for motor control applications, realized in BCDmultipower technology, which combines isolated DMOS power transistors with CMOS and bipolar circuits on the same chip. The device also includes two independent constant off time PWM current controllers that performs the chopping regulation. Available in VQFPN32 5 mm x 5 mm package, the L6227Q features a non-dissipative overcurrent protection on the high side power MOSFETs and thermal shutdown.

Figure 1. Block diagram



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1 Electrical data

1.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Parameter | Value | Unit |
|---------------------------------|--|---|------------|------|
| V_S | Supply voltage | $V_{SA} = V_{SB} = V_S$ | 60 | V |
| V_{OD} | Differential voltage between V_{SA} , OUT1 _A , OUT2 _A , SENSE _A and V_{SB} , OUT1 _B , OUT2 _B , SENSE _B | $V_{SA} = V_{SB} = V_S = 60\text{ V}$; $V_{SENSEA} = V_{SENSEB} = \text{GND}$ | 60 | V |
| V_{BOOT} | Bootstrap peak voltage | $V_{SA} = V_{SB} = V_S$ | $V_S + 10$ | V |
| V_{IN}, V_{EN} | Input and enable voltage range | | -0.3 to +7 | V |
| V_{REFA}, V_{REFB} | Voltage range at pins V_{REFA} and V_{REFB} | | -0.3 to +7 | V |
| V_{RCA}, V_{RCB} | Voltage range at pins RC_A and RC_B | | -0.3 to +7 | V |
| V_{SENSEA}, V_{SENSEB} | Voltage range at pins SENSE _A and SENSE _B | | -1 to +4 | V |
| $I_{S(\text{peak})}$ | Pulsed supply current (for each V_S pin), internally limited by the overcurrent protection | $V_{SA} = V_{SB} = V_S$; $t_{\text{PULSE}} < 1\text{ ms}$ | 3.55 | A |
| I_S | RMS supply current (for each V_S pin) | $V_{SA} = V_{SB} = V_S$ | 1.4 | A |
| $T_{\text{stg}}, T_{\text{OP}}$ | Storage and operating temperature range | | -40 to 150 | °C |

1.2 Recommended operating conditions

Table 2. Recommended operating conditions

| Symbol | Parameter | Parameter | Min | Max | Unit |
|--------------------------|--|--|----------|--------|--------|
| V_S | Supply voltage | $V_{SA} = V_{SB} = V_S$ | 8 | 52 | V |
| V_{OD} | Differential voltage between V_{SA} , OUT1 _A , OUT2 _A , SENSE _A and V_{SB} , OUT1 _B , OUT2 _B , SENSE _B | $V_{SA} = V_{SB} = V_S$; $V_{SENSEA} = V_{SENSEB}$ | | 52 | V |
| V_{REFA}, V_{REFB} | Voltage range at pins V_{REFA} and V_{REFB} | | -0.1 | 5 | V |
| V_{SENSEA}, V_{SENSEB} | Voltage range at pins SENSE _A and SENSE _B | (pulsed $t_W < t_{rr}$) (DC) | -6 -1 | 6 1 | V V |
| I_{OUT} | RMS output current | | | 1.4 | A |
| T_J | Operating junction temperature | | -25 | +125 | °C |
| f_{sw} | Switching frequency | | | 100 | kHz |

1.3 Thermal data

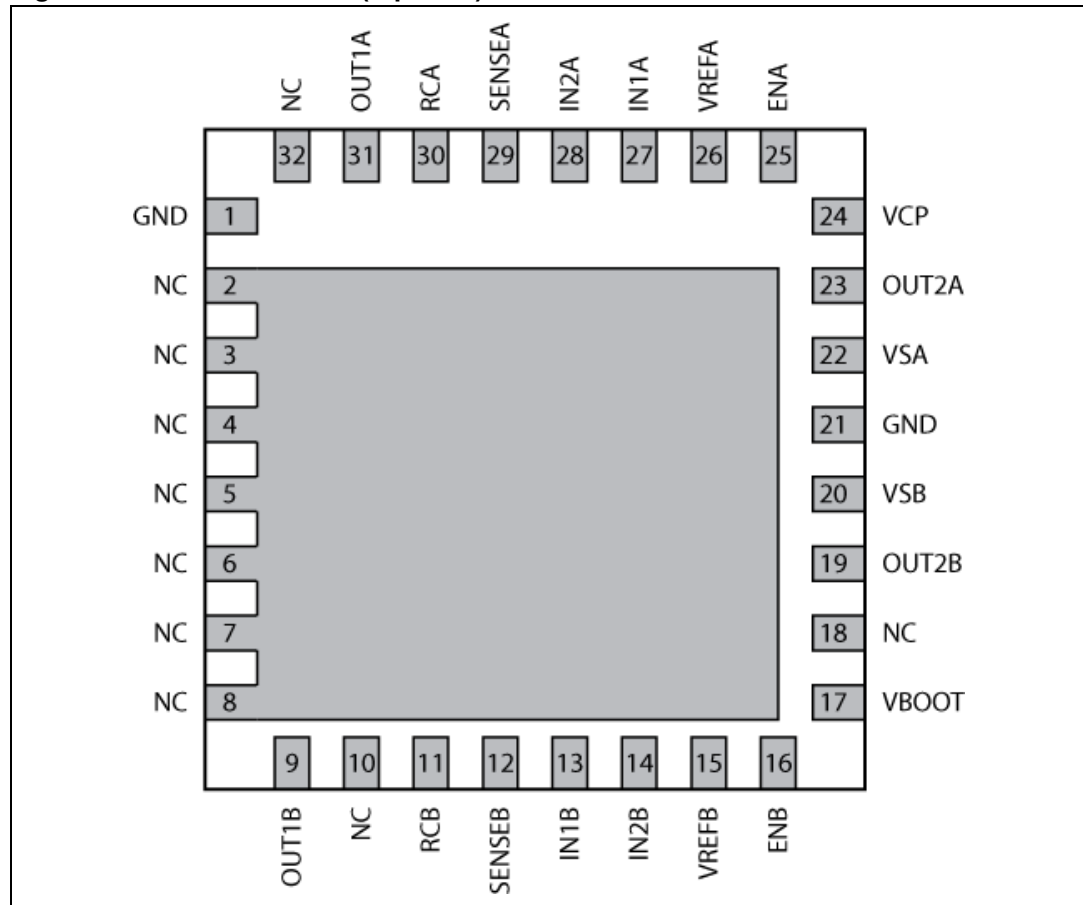
Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|--------------|--|-------|------|
| $R_{th(JA)}$ | Thermal resistance junction-ambient max ⁽¹⁾ . | 42 | °C/W |

1. Mounted on a double-layer FR4 PCB with a dissipating copper surface of 0.5 cm² on the top side plus 6 cm² ground layer connected through 18 via holes (9 below the IC).

2 Pin connection

Figure 2. Pin connection (top view)



- Note:
- 1 The pins 2 to 8 are connected to die PAD
 - 2 The die PAD must be connected to GND pin

Table 4. Pin description

| N° | Pin | Type | Function |
|-------|--------------------|----------------------------|---|
| 1, 21 | GND | GND | Signal ground terminals. |
| 9 | OUT1 _B | Power output | Bridge B output 1. |
| 11 | RC _B | RC pin | RC network pin. A parallel RC network connected between this pin and ground sets the current controller OFF-time of the bridge B. |
| 12 | SENSE _B | Power supply | Bridge B source pin. This pin must be connected to power ground through a sensing power resistor. |
| 13 | IN1 _B | Logic input | Bridge B input 1 |
| 14 | IN2 _B | Logic input | Bridge B input 2 |
| 15 | VREF _B | Analog input | Bridge B current controller reference voltage. Do not leave this pin open or connect to GND. |
| 16 | EN _B | Logic input ⁽¹⁾ | Bridge B enable. LOW logic level switches OFF all power MOSFETs of bridge B. This pin is also connected to the collector of the overcurrent and thermal protection transistor to implement over current protection. If not used, it has to be connected to +5 V through a resistor. |
| 17 | VBOOT | Supply voltage | Bootstrap voltage needed for driving the upper power MOSFETs of both bridge A and Bridge B. |
| 19 | OUT2 _B | Power output | Bridge B output 2. |
| 20 | VS _B | Power supply | Bridge B power supply voltage. It must be connected to the supply voltage together with pin VS _A . |
| 22 | VS _A | Power supply | Bridge A power supply voltage. It must be connected to the supply voltage together with pin VS _B . |
| 23 | OUT2 _A | Power output | Bridge A output 2. |
| 24 | VCP | Output | Charge pump oscillator output. |
| 25 | EN _A | Logic input ⁽¹⁾ | Bridge A enable. LOW logic level switches OFF all power MOSFETs of bridge A. This pin is also connected to the collector of the overcurrent and thermal protection transistor to implement over current protection. If not used, it has to be connected to +5 V through a resistor. |
| 26 | VREF _A | Analog input | Bridge A current controller reference voltage. Do not leave this pin open or connect to GND. |
| 27 | IN1 _A | Logic input | Bridge A logic input 1. |
| 28 | IN2 _A | Logic input | Bridge A logic input 2. |
| 29 | SENSE _A | Power supply | Bridge A source pin. This pin must be connected to power ground through a sensing power resistor. |
| 30 | RC _A | RC pin | RC network pin. A parallel RC network connected between this pin and ground sets the current controller OFF-time of the bridge A. |
| 31 | OUT1 _A | Power output | Bridge A output 1. |

1. Also connected at the output drain of the over current and thermal protection MOSFET. Therefore, it has to be driven putting in series a resistor with a value in the range of 2.2 kΩ - 180 kΩ, recommended 100 kΩ.

3 Electrical characteristics

Table 5. Electrical characteristics ($T_A = 25\text{ }^{\circ}\text{C}$, $V_S = 48\text{ V}$, unless otherwise specified)

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---------------------------|--|--|------|------|------|------|
| V _{Sth(ON)} | Turn-on threshold | | 5.8 | 6.3 | 6.8 | V |
| V _{Sth(OFF)} | Turn-off threshold | | 5 | 5.5 | 6 | V |
| I _S | Quiescent supply current | All Bridges OFF; T _J = -25 °C to 125 °C ⁽¹⁾ | | 5 | 10 | mA |
| T _{J(OFF)} | Thermal shutdown temperature | | | 165 | | °C |
| Output DMOS transistors | | | | | | |
| R _{DS(on)} | High-side + low-side switch ON resistance | T _J = 25 °C | | 1.47 | 1.69 | Ω |
| | | T _J =125 °C ⁽¹⁾ | | 2.35 | 2.7 | Ω |
| I _{DSS} | Leakage current | EN = Low; OUT = V _S | | | 2 | mA |
| | | EN = Low; OUT = GND | -0.3 | | | mA |
| Source drain diodes | | | | | | |
| V _{SD} | Forward ON voltage | I _{SD} = 1.4 A, EN = LOW | | 1.15 | 1.3 | V |
| t _{rr} | Reverse recovery time | I _f = 1.4 A | | 300 | | ns |
| t _{fr} | Forward recovery time | | | 200 | | ns |
| Logic input | | | | | | |
| V _{IL} | Low level logic input voltage | | -0.3 | | 0.8 | V |
| V _{IH} | High level logic input voltage | | 2 | | 7 | V |
| I _{IL} | Low level logic input current | GND logic input voltage | -10 | | | μA |
| I _{IH} | High level logic input current | 7 V logic input voltage | | | 10 | μA |
| V _{th(ON)} | Turn-on input threshold | | | 1.8 | 2.0 | V |
| V _{th(OFF)} | Turn-off input threshold | | 0.8 | 1.3 | | V |
| V _{th(HYS)} | Input threshold hysteresis | | 0.25 | 0.5 | | V |
| Switching characteristics | | | | | | |
| t _{D(on)EN} | Enable to out turn ON delay time ⁽²⁾ | I _{LOAD} =1.4 A, resistive load | 500 | | 800 | ns |
| t _{D(on)IN} | Input to out turn ON delay time | I _{LOAD} =1.4 A, resistive load (dead time included) | | 1.9 | | μs |
| t _{RISE} | Output rise time ⁽²⁾ | I _{LOAD} =1.4 A, resistive load | 40 | | 250 | ns |
| t _{D(off)EN} | Enable to out turn OFF delay time ⁽²⁾ | I _{LOAD} =1.4 A, resistive load | 500 | 800 | 1000 | ns |
| t _{D(off)IN} | Input to out turn OFF delay time | I _{LOAD} =1.4 A, resistive load | 500 | 800 | 1000 | ns |
| t _{FALL} | Output fall time ⁽²⁾ | I _{LOAD} =1.4 A, resistive load | 40 | | 250 | ns |
| t _{dt} | Dead time protection | | 0.5 | 1 | | μs |
| f _{CP} | Charge pump frequency | -25 °C < T _J < 125 °C | | 0.6 | 1 | MHz |

Table 5. Electrical characteristics (continued) ($T_A = 25\text{ }^{\circ}\text{C}$, $V_S = 48\text{ V}$, unless otherwise specified)

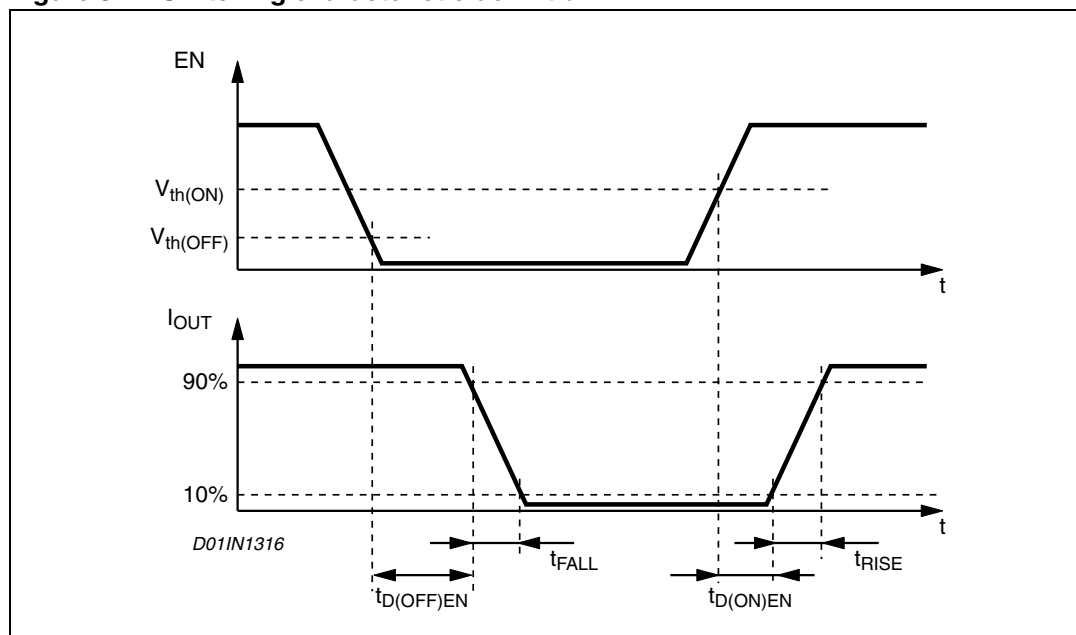
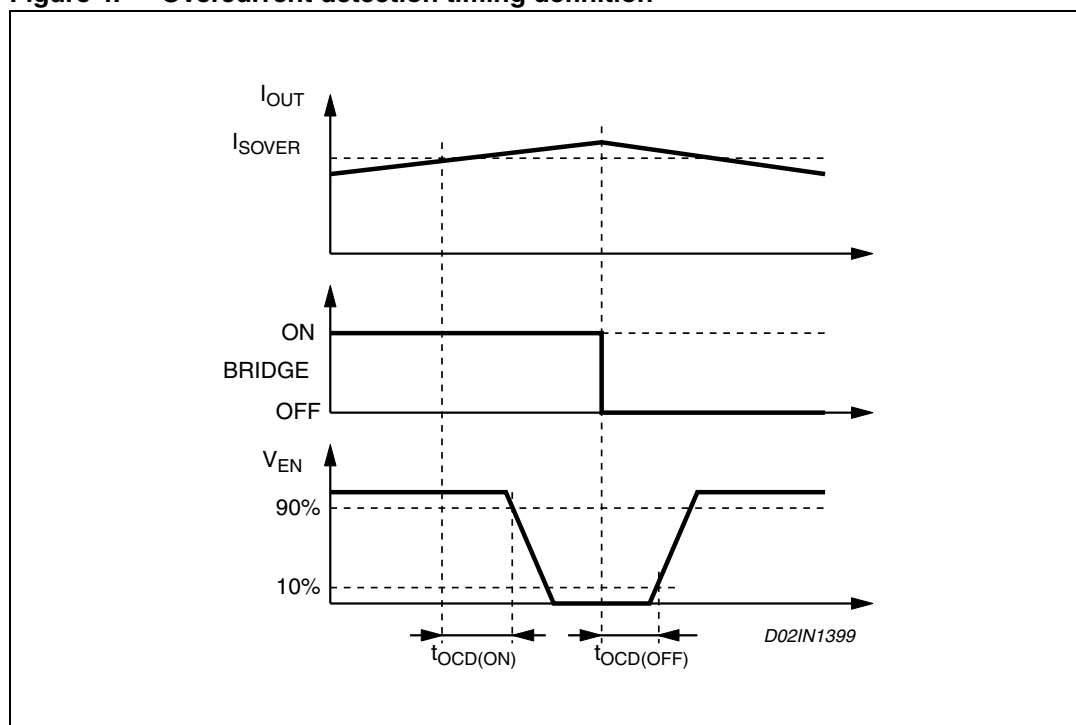
| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|--------------------------------------|--|---|-----|---------|-----|---------------|
| PWM comparator and monostable | | | | | | |
| I_{RCA}, I_{RCB} | Source current at pins RC_A and RC_B | $V_{RCA} = V_{RCB} = 2.5\text{ V}$ | 3.5 | 5.5 | | mA |
| V_{offset} | Offset voltage on sense comparator | $V_{REFA}, V_{REFB} = 0.5\text{ V}$ | | ± 5 | | mV |
| t_{PROP} | Turn OFF propagation delay ⁽³⁾ | | | 500 | | ns |
| t_{BLANK} | Internal blanking time on SENSE pins | | | 1 | | μs |
| $t_{ON(MIN)}$ | Minimum on time | | | 2.5 | 3 | μs |
| t_{OFF} | PWM recirculation time | $R_{OFF} = 20\text{ k}\Omega$; $C_{OFF} = 1\text{ nF}$ | | 13 | | μs |
| | | $R_{OFF} = 100\text{ k}\Omega$; $C_{OFF} = 1\text{ nF}$ | | 61 | | μs |
| I_{BIAS} | Input bias current at pins $VREF_A$ and $VREF_B$ | | | | 10 | μA |
| Over current protection | | | | | | |
| I_{SOVER} | Input supply overcurrent protection threshold | $T_J = -25\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ ⁽¹⁾ | | 2.8 | | A |
| R_{OPDR} | Open drain ON resistance | $I = 4\text{ mA}$ | | 40 | 60 | Ω |
| $t_{OCD(ON)}$ | OCD turn-on delay time ⁽⁴⁾ | $I = 4\text{ mA}$; $C_{EN} < 100\text{ pF}$ | | 200 | | ns |
| $t_{OCD(OFF)}$ | OCD turn-off delay time ⁽⁴⁾ | $I = 4\text{ mA}$; $C_{EN} < 100\text{ pF}$ | | 100 | | ns |

1. Tested at $25\text{ }^{\circ}\text{C}$ in a restricted range and guaranteed by characterization.

2. See [Figure 3 on page 9](#)

3. Measured applying a voltage of 1 V to pin SENSE and a voltage drop from 2 V to 0 V to pin VREF.

4. See [Figure 4 on page 9](#)

Figure 3. Switching characteristic definition**Figure 4. Overcurrent detection timing definition**

4 Circuit description

4.1 Power stages and charge pump

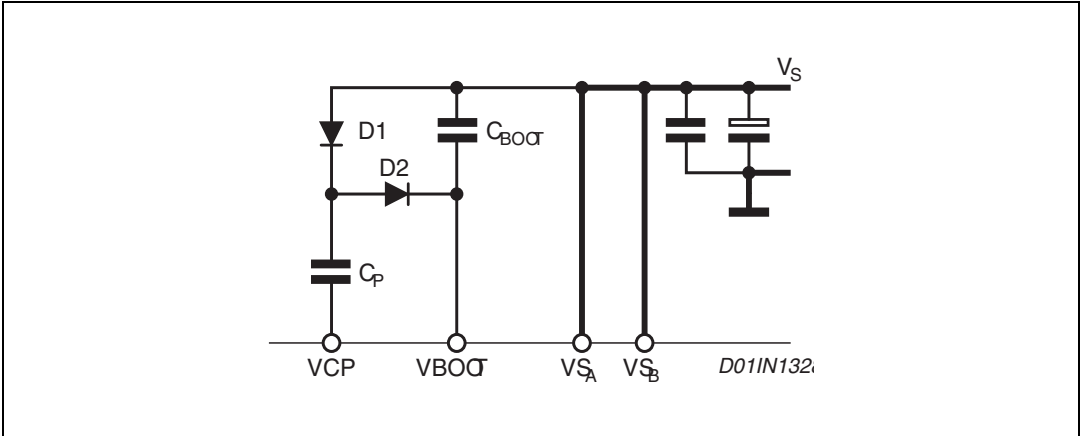
The L6227Q integrates two independent power MOS Full Bridges. Each power MOS has an $R_{DS(on)} = 0.73 \Omega$ (typical value @ 25 °C), with intrinsic fast freewheeling diode. Cross conduction protection is achieved using a dead time ($t_d = 1 \mu s$ typical) between the switch off and switch on of two power MOS in one leg of a bridge.

Using N-channel power MOS for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage. The bootstrapped (VBOOT) supply is obtained through an internal oscillator and few external components to realize a charge pump circuit as shown in [Figure 5](#). The oscillator output (VCP) is a square wave at 600 kHz (typical) with 10 V amplitude. Recommended values/part numbers for the charge pump circuit are shown in [Table 6](#).

Table 6. Charge pump external components values

| Component | Value |
|------------|--------|
| C_{BOOT} | 220 nF |
| C_P | 10 nF |
| D1 | 1N4148 |
| D2 | 1N4148 |

Figure 5. Charge pump circuit



4.2 Logic inputs

Pins $IN1_A$, $IN2_B$, $IN1_B$ and $IN2_B$ are TTL/CMOS and microcontroller compatible logic inputs. The internal structure is shown in [Figure 6](#). Typical value for turn-on and turn-off thresholds are respectively $V_{thon} = 1.8\text{ V}$ and $V_{thoff} = 1.3\text{ V}$.

Pins EN_A and EN_B have identical input structure with the exception that the drains of the Overcurrent and thermal protection MOSFETs (one for the bridge A and one for the bridge B) are also connected to these pins. Due to these connections some care needs to be taken in driving these pins. The EN_A and EN_B inputs may be driven in one of two configurations as shown in [Figure 7](#) or [Figure 8](#). If driven by an open drain (collector) structure, a pull-up resistor R_{EN} and a capacitor C_{EN} are connected as shown in [Figure 7](#). If the driver is a standard push-pull structure the resistor R_{EN} and the capacitor C_{EN} are connected as shown in [Figure 8](#). The resistor R_{EN} should be chosen in the range from $2.2\text{ k}\Omega$ to $180\text{ k}\Omega$. Recommended values for R_{EN} and C_{EN} are respectively $100\text{ k}\Omega$ and 5.6 nF . More information on selecting the values is found in the overcurrent protection section.

Figure 6. Logic inputs internal structure

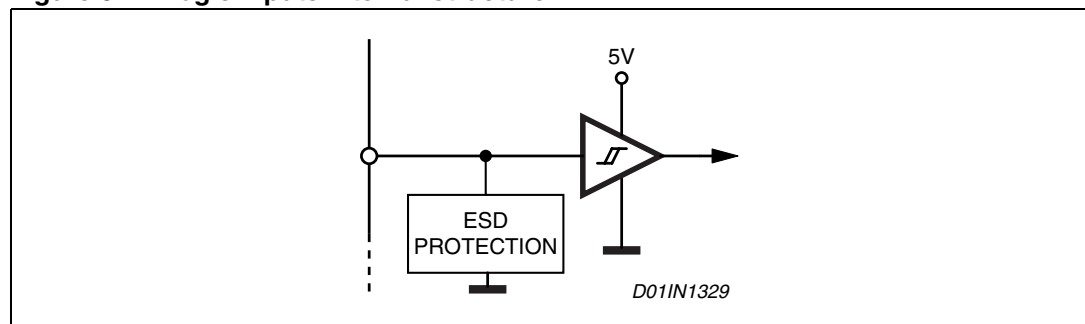


Figure 7. EN_A and EN_B pins open collector driving

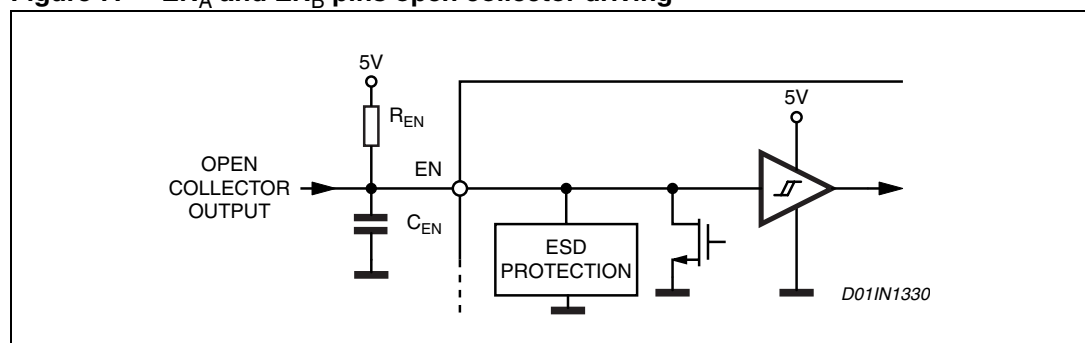
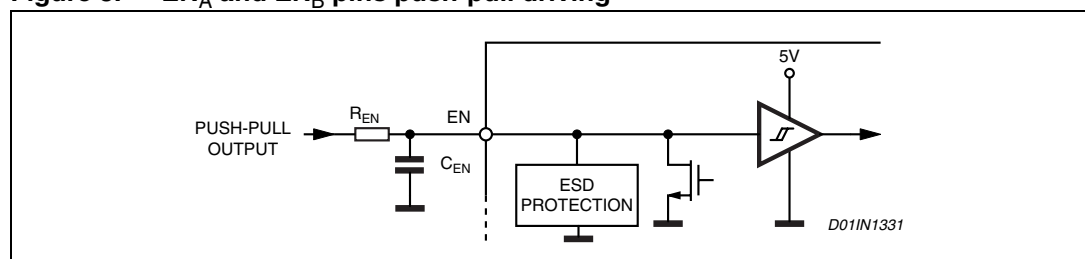


Figure 8. EN_A and EN_B pins push-pull driving



4.3 Truth table

Table 7. Truth table

| Inputs | | | Outputs | | Description ⁽¹⁾ |
|--------|------------------|-----|-------------------------|----------|----------------------------|
| EN | IN1 | IN2 | OUT1 | OUT2 | |
| L | X ⁽²⁾ | X | High Z ⁽³⁾ | High Z | Disable |
| H | L | L | GND | GND | Brake mode (lower path) |
| H | H | L | Vs | GND (Vs) | Forward |
| H | L | H | GND (Vs) ⁽⁴⁾ | Vs | Reverse |
| H | H | H | Vs | Vs | Brake mode (upper path) |

1. Valid only in case of load connected between OUT1 and OUT2
2. X = don't care
3. High Z = high impedance output
4. GND (Vs) = GND during Ton, Vs during Toff

4.4 PWM current control

The L6227Q includes a constant off time PWM current controller for each of the two bridges. The current control circuit senses the bridge current by sensing the voltage drop across an external sense resistor connected between the source of the two lower power MOS transistors and ground, as shown in [Figure 9](#). As the current in the load builds up the voltage across the sense resistor increases proportionally. When the voltage drop across the sense resistor becomes greater than the voltage at the reference input ($VREF_A$ or $VREF_B$) the sense comparator triggers the monostable switching the low-side MOS off. The low-side MOS remain off for the time set by the monostable and the motor current recirculates in the upper path. When the monostable times out the bridge will again turn on. Since the internal dead time, used to prevent cross conduction in the bridge, delays the turn on of the power MOS, the effective off time is the sum of the monostable time plus the dead time.

Figure 9. PWM current controller simplified schematic

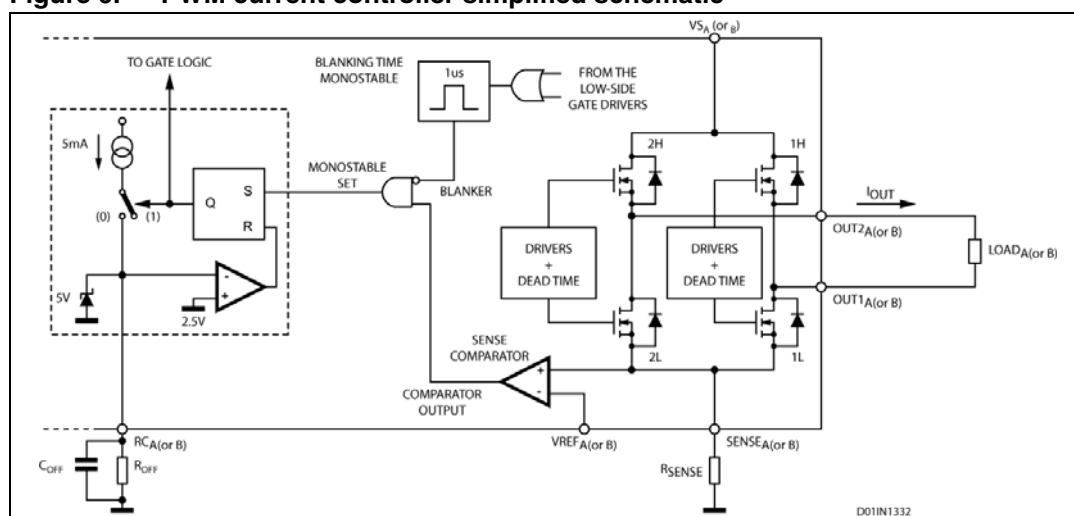


Figure 10 shows the typical operating waveforms of the output current, the voltage drop across the sensing resistor, the RC pin voltage and the status of the bridge. Immediately after the low-side power MOS turns on, a high peak current flows through the sensing resistor due to the reverse recovery of the freewheeling diodes. The L6227Q provides a $1\text{ }\mu\text{s}$ blanking time t_{BLANK} that inhibits the comparator output so that this current spike cannot prematurely re-trigger the monostable.

Figure 10. Output current regulation waveforms

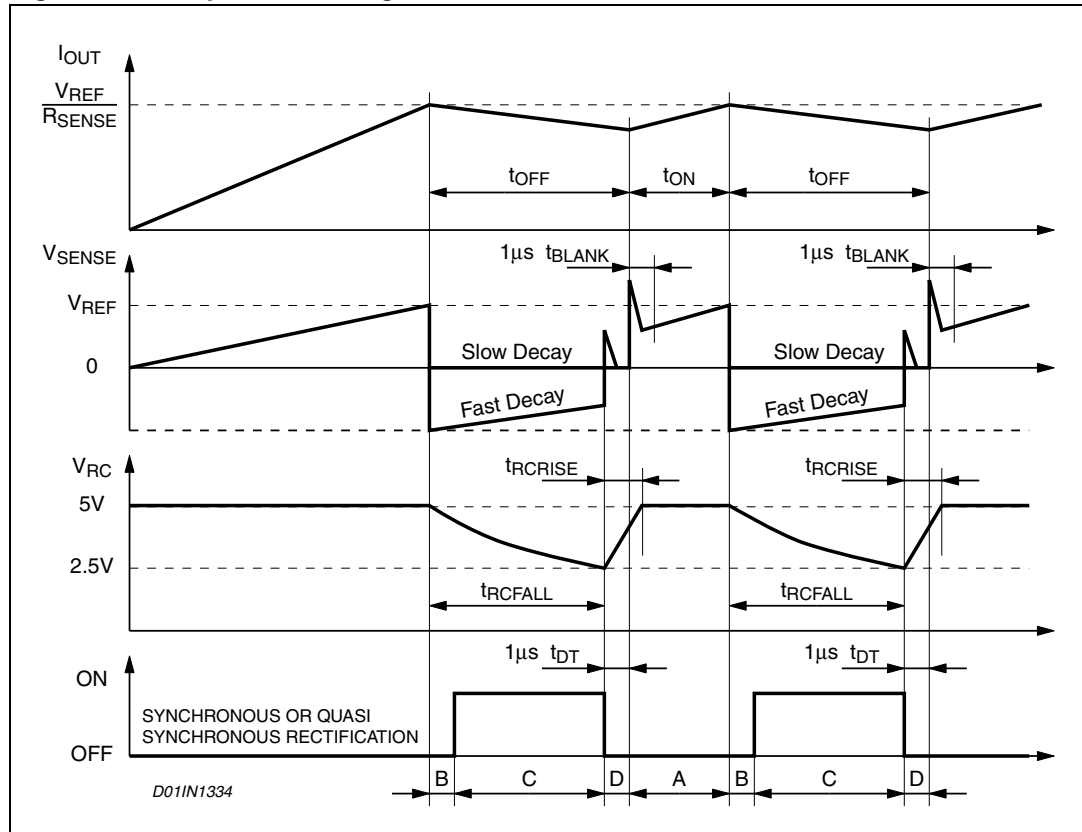


Figure 11 shows the magnitude of the off time t_{OFF} versus C_{OFF} and R_{OFF} values. It can be approximately calculated from the equations:

$$t_{\text{RCFALL}} = 0.6 \cdot R_{\text{OFF}} \cdot C_{\text{OFF}}$$

$$t_{\text{OFF}} = t_{\text{RCFALL}} + t_{\text{DT}} = 0.6 \cdot R_{\text{OFF}} \cdot C_{\text{OFF}} + t_{\text{DT}}$$

where R_{OFF} and C_{OFF} are the external component values and t_{DT} is the internally generated Dead Time with:

$$20\text{ k}\Omega \leq R_{\text{OFF}} \leq 100\text{ k}\Omega$$

$$0.47\text{ nF} \leq C_{\text{OFF}} \leq 100\text{ nF}$$

$$t_{\text{DT}} = 1\text{ }\mu\text{s (typical value)}$$

Therefore:

$$t_{\text{OFF(MIN)}} = 6.6\text{ }\mu\text{s}$$

$$t_{\text{OFF(MAX)}} = 6\text{ ms}$$

These values allow a sufficient range of t_{OFF} to implement the drive circuit for most motors.

The capacitor value chosen for C_{OFF} also affects the rise time t_{RCRISE} of the voltage at the pin R_{COFF} . The rise time t_{RCRISE} will only be an issue if the capacitor is not completely charged before the next time the monostable is triggered. Therefore, the on time t_{ON} , which depends by motors and supply parameters, has to be bigger than t_{RCRISE} for allowing a good current regulation by the PWM stage. Furthermore, the on time t_{ON} can not be smaller than the minimum on time $t_{ON(MIN)}$.

$$\begin{cases} t_{ON} > t_{ON(MIN)} = 2.5\mu s \\ t_{ON} > t_{RCRISE} - t_{DT} \end{cases}$$

$$t_{RCRISE} = 600 \cdot C_{OFF}$$

[Figure 12 on page 15](#) shows the lower limit for the on time t_{ON} for having a good PWM current regulation capacity. It has to be said that t_{ON} is always bigger than $t_{ON(MIN)}$ because the device imposes this condition, but it can be smaller than $t_{RCRISE} - t_{DT}$. In this last case the device continues to work but the off time t_{OFF} is not more constant.

So, small C_{OFF} value gives more flexibility for the applications (allows smaller on time and, therefore, higher switching frequency), but, the smaller is the value for C_{OFF} the more influential will be the noises on the circuit performance.

Figure 11. t_{OFF} versus C_{OFF} and R_{OFF}

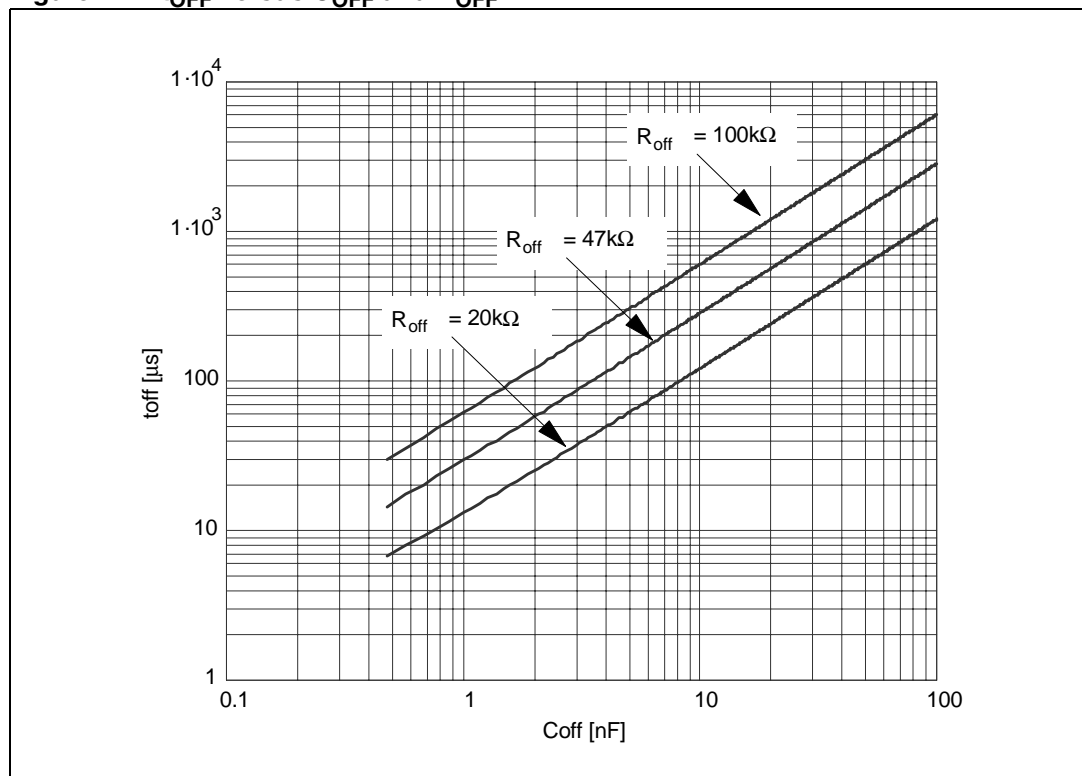
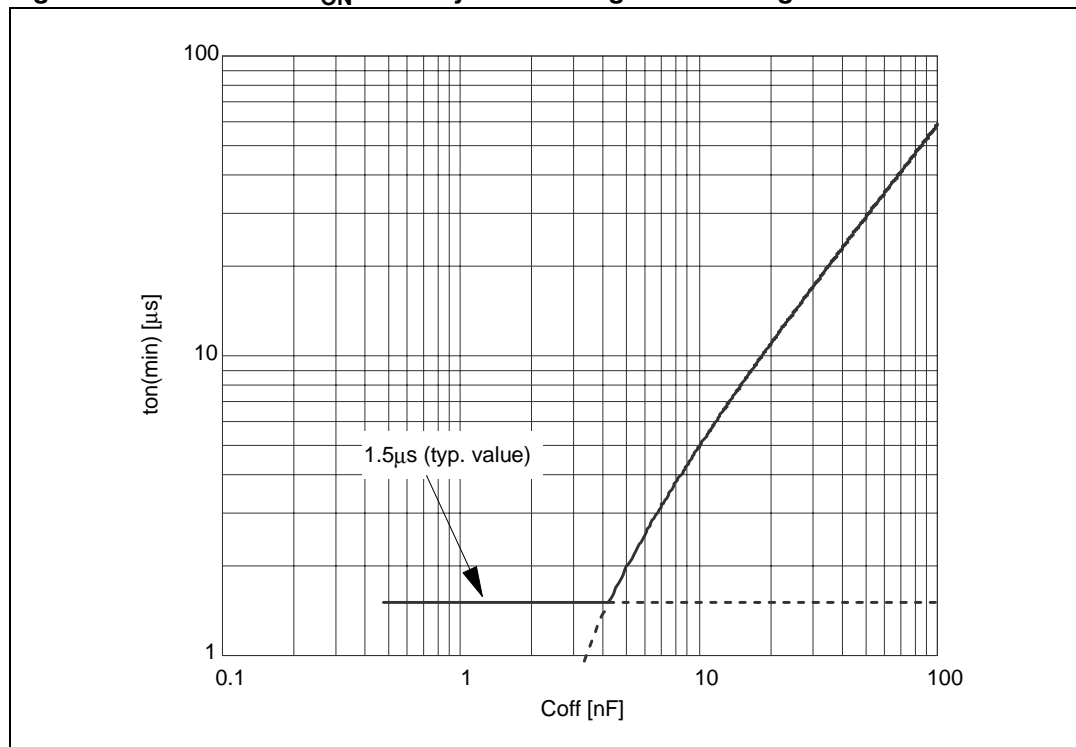
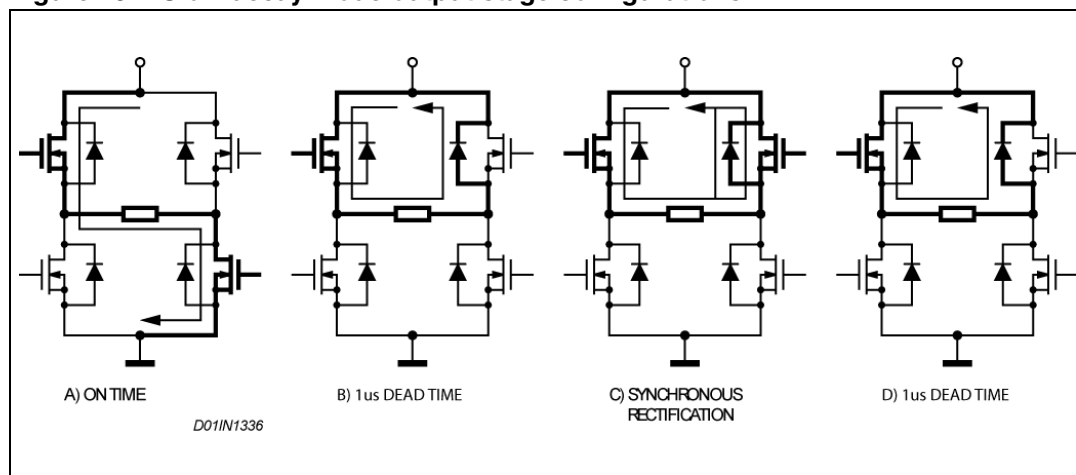


Figure 12. Area where t_{ON} can vary maintaining the PWM regulation

4.5 Slow decay mode

Figure 13 shows the operation of the bridge in the slow decay mode. At the start of the off time, the lower power MOS is switched off and the current recirculates around the upper half of the bridge. Since the voltage across the coil is low, the current decays slowly. After the dead time the upper power MOS is operated in the synchronous rectification mode. When the monostable times out, the lower power MOS is turned on again after some delay set by the dead time to prevent cross conduction.

Figure 13. Slow decay mode output stage configurations

4.6 Non-dissipative overcurrent protection

The L6227Q integrates an overcurrent detection circuit (OCD). This circuit provides protection against a short circuit to ground or between two phases of the bridge. With this internal over current detection, the external current sense resistor normally used and its associated power dissipation are eliminated. *Figure 14* shows a simplified schematic of the overcurrent detection circuit.

To implement the over current detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high side power MOS. Since this current is a small fraction of the output current there is very little additional power dissipation. This current is compared with an internal reference current I_{REF} . When the output current in one bridge reaches the detection threshold (typically 2.8 A) the relative OCD comparator signals a fault condition. When a fault condition is detected, the EN pin is pulled below the turn off threshold (1.3 V typical) by an internal open drain MOS with a pull down capability of 4 mA. By using an external R-C on the EN pin, the off time before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs.

Figure 14. Overcurrent protection simplified schematic

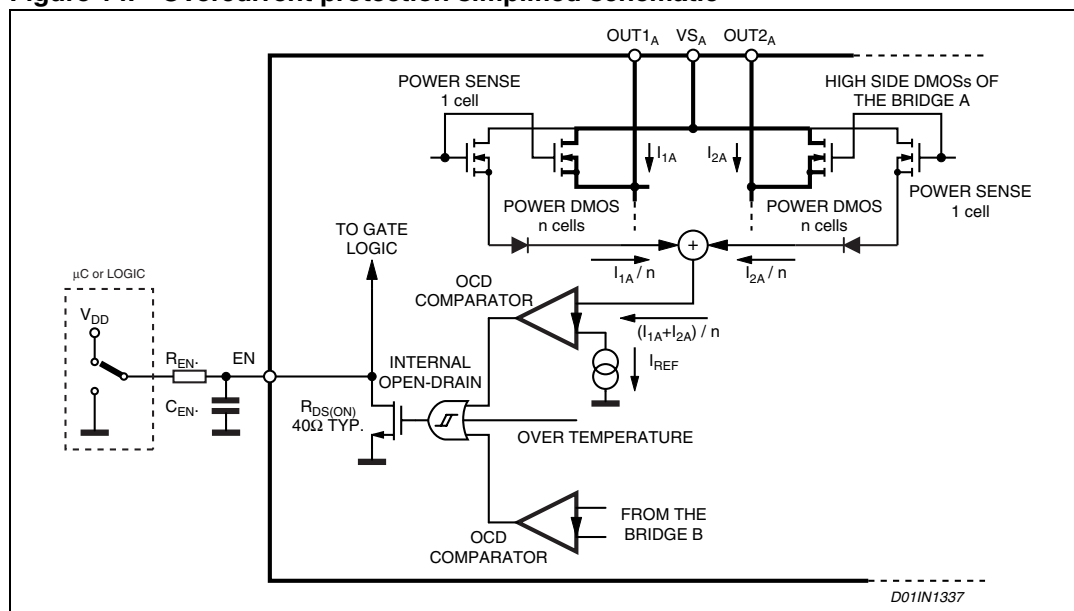


Figure 15 shows the overcurrent detection operation. The disable time t_{DISABLE} before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs. It is affected whether by C_{EN} and R_{EN} values and its magnitude is reported in *Figure 16*. The delay time t_{DELAY} before turning off the bridge when an overcurrent has been detected depends only by C_{EN} value. Its magnitude is reported in *Figure 17*.

C_{EN} is also used for providing immunity to pin EN against fast transient noises. Therefore the value of C_{EN} should be chosen as big as possible according to the maximum tolerable delay time and the R_{EN} value should be chosen according to the desired disable time.

The resistor R_{EN} should be chosen in the range from 2.2 k Ω to 180 k Ω . Recommended values for R_{EN} and C_{EN} are respectively 100 k Ω and 5.6 nF that allow obtaining 200 μ s disable time.

Figure 15. Overcurrent protection waveforms

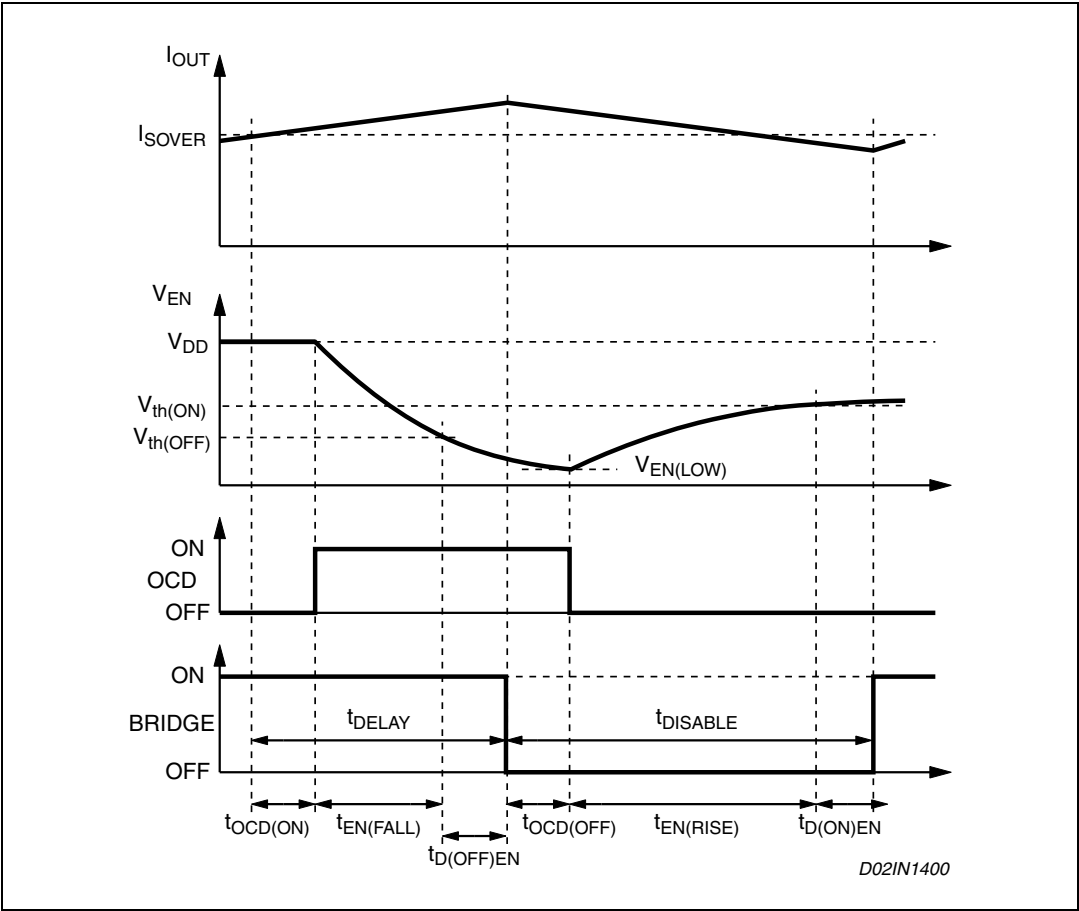


Figure 16. t_{DISABLE} versus C_{EN} and R_{EN} ($V_{\text{DD}} = 5 \text{ V}$)

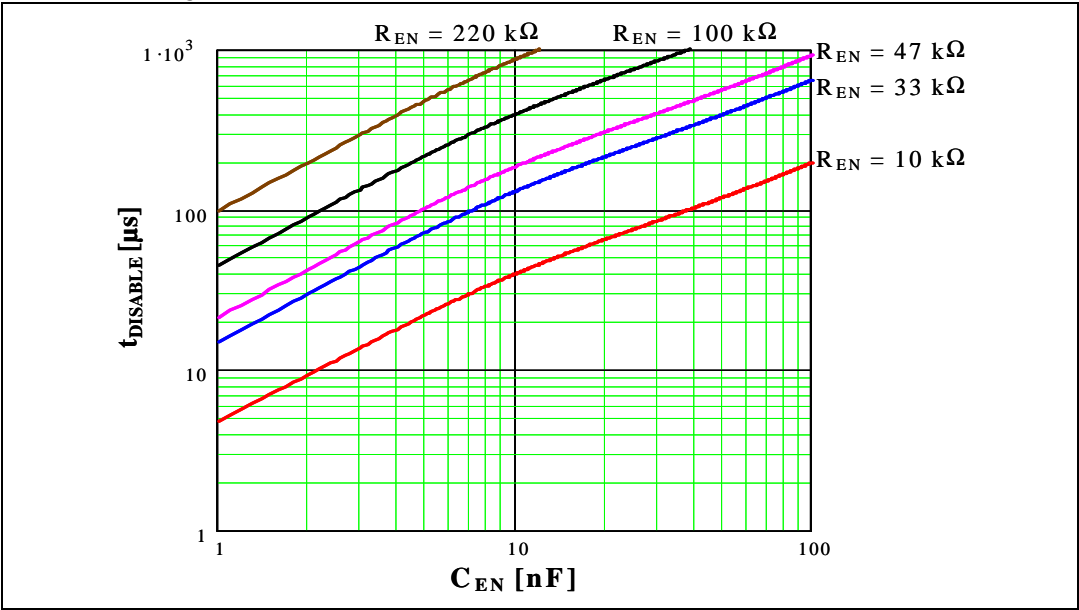
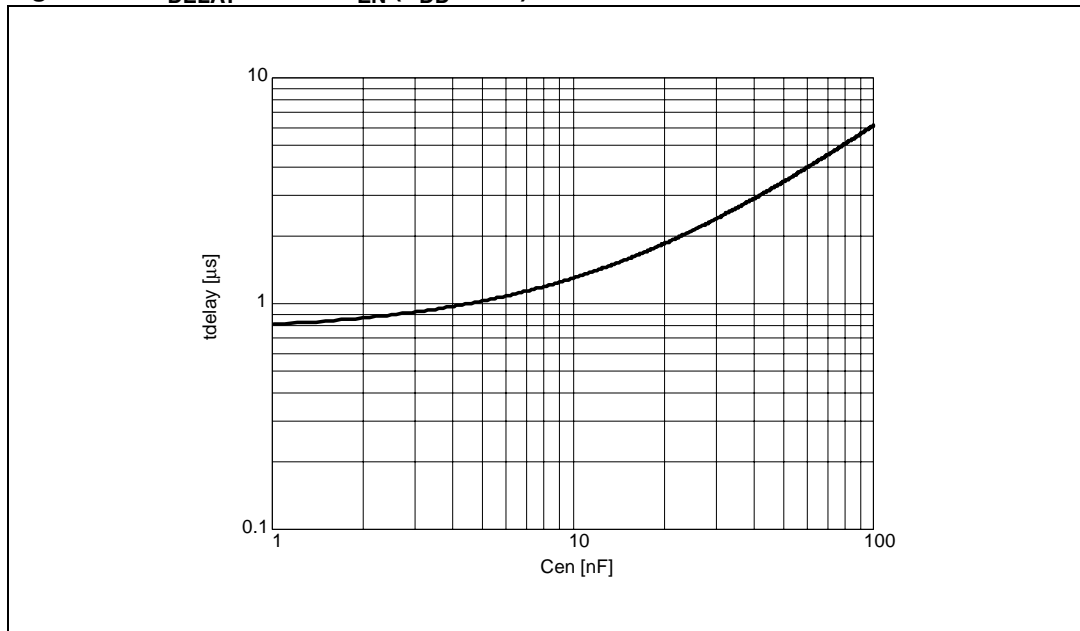


Figure 17. t_{DELAY} versus C_{EN} ($V_{\text{DD}} = 5 \text{ V}$)

4.7 Thermal protection

In addition to the overcurrent protection, the L6227Q integrates a thermal protection for preventing the device destruction in case of junction over temperature. It works sensing the die temperature by means of a sensible element integrated in the die. The device switch-off when the junction temperature reaches 165 °C (typ. value) with 15 °C hysteresis (typ. value).

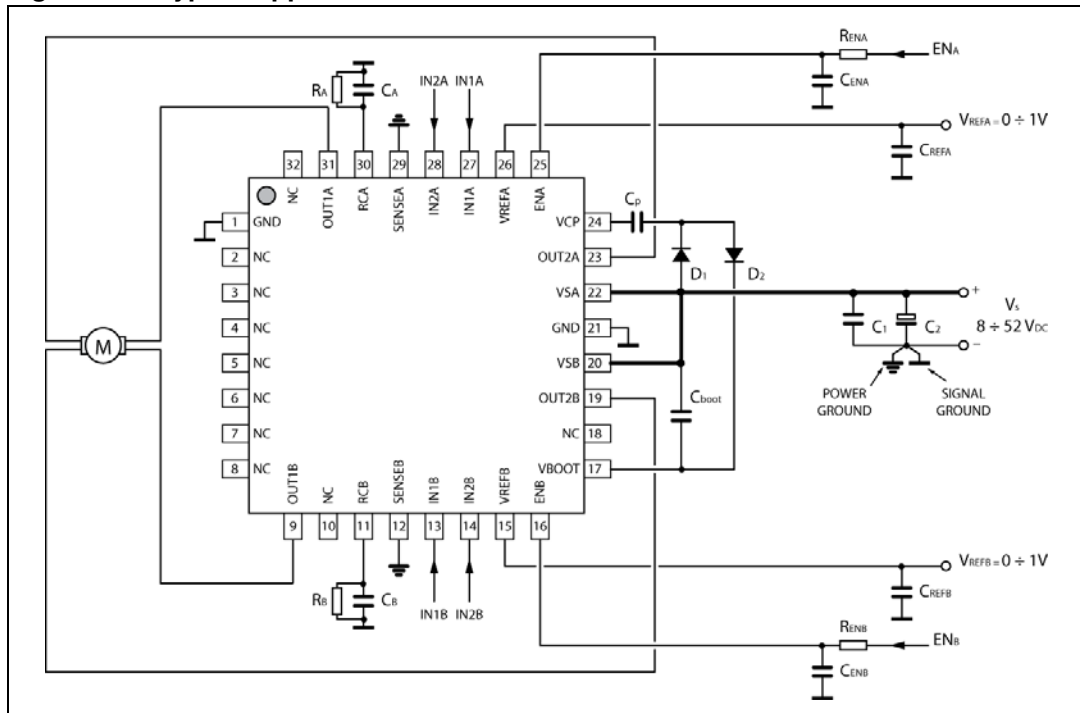
5 Application information

A typical application using L6227Q is shown in [Figure 18](#). Typical component values for the application are shown in [Table 8](#). A high quality ceramic capacitor in the range of 100 to 200 nF should be placed between the power pins (VS_A and VS_B) and ground near the L6227Q to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching. The capacitors connected from the EN_A and EN_B inputs to ground set the shut down time for the bridge A and bridge B respectively when an over current is detected (see overcurrent protection). The two current sensing inputs ($SENSE_A$ and $SENSE_B$) should be connected to the sensing resistors with a trace length as short as possible in the layout. The sense resistors should be non-inductive resistors to minimize the dI/dt transients across the resistor. To increase noise immunity, unused logic pins (except EN_A and EN_B) are best connected to 5 V (high logic level) or GND (low logic level) (see pin description). It is recommended to keep power ground and signal ground separated on PCB.

Table 8. Component values for typical application

| Component | Value |
|--------------|----------------|
| C_1 | 100 μ F |
| C_2 | 100 nF |
| C_A | 1 nF |
| C_B | 1 nF |
| C_{BOOT} | 220 nF |
| C_P | 10 nF |
| C_{ENA} | 5.6 nF |
| C_{ENB} | 5.6 nF |
| C_{REFA} | 68 nF |
| C_{REFB} | 68 nF |
| D_1 | 1N4148 |
| D_2 | 1N4148 |
| R_A | 39 k Ω |
| R_B | 39 k Ω |
| R_{ENA} | 100 k Ω |
| R_{ENB} | 100 k Ω |
| R_{SENSEA} | 0.6 Ω |
| R_{SENSEB} | 0.6 Ω |

Figure 18. Typical application



Note: To reduce the IC thermal resistance, therefore improve the dissipation path, the NC pins can be connected to GND.

6 Output current capability and IC power dissipation

In [Figure 19](#) and [Figure 20](#) are shown the approximate relation between the output current and the IC power dissipation using PWM current control driving two loads, for two different driving types:

- One full bridge ON at a time ([Figure 19](#)) in which only one load at a time is energized.
- Two full bridges ON at the same time ([Figure 20](#)) in which two loads at the same time are energized.

For a given output current and driving type the power dissipated by the IC can be easily evaluated, in order to establish which package should be used and how large must be the on-board copper dissipating area to guarantee a safe operating junction temperature (125 °C maximum).

Figure 19. IC power dissipation vs output current with one full bridge ON at a time

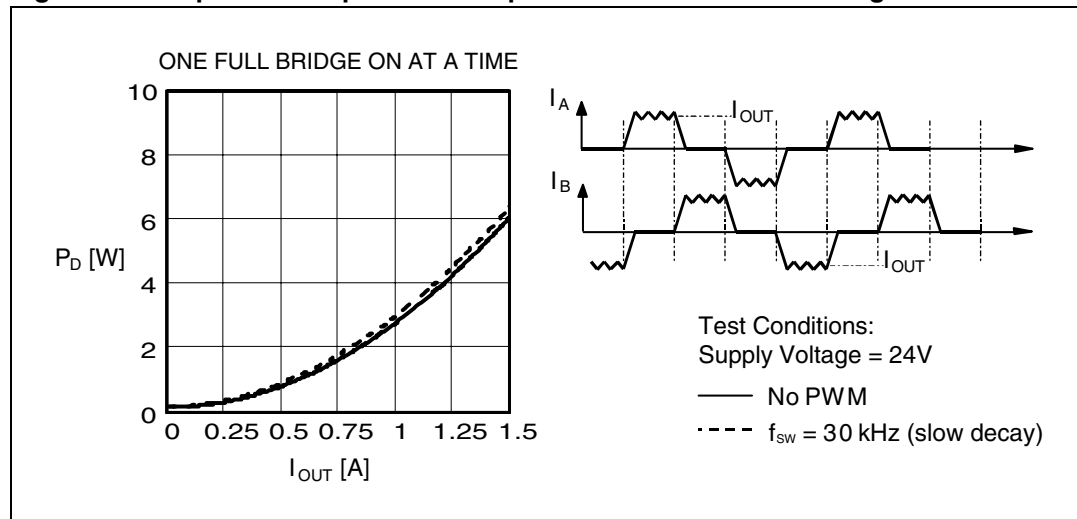
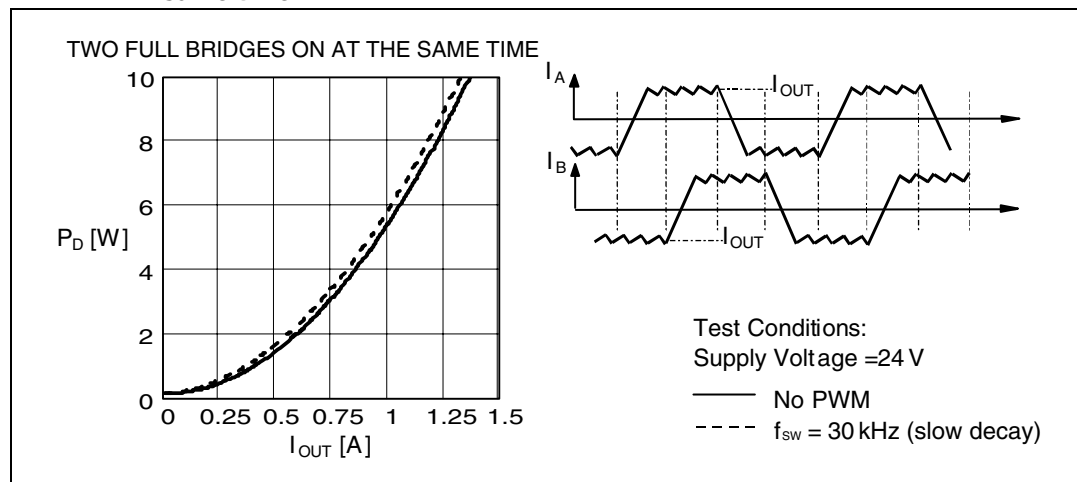


Figure 20. IC power dissipation versus output current with two full bridges ON at the same time



7 Thermal management

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be delivered by the device in a safe operating condition. Therefore, it has to be taken into account very carefully. Besides the available space on the PCB, the right package should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness. For instance, using a VFQFPN32L 5x5 package the typical $R_{th}(JA)$ is about 42 °C/W when mounted on a double-layer FR4 PCB with a dissipating copper surface of 0.5 cm² on the top side plus 6 cm² ground layer connected through 18 via holes (9 below the IC).

8 Package mechanical data

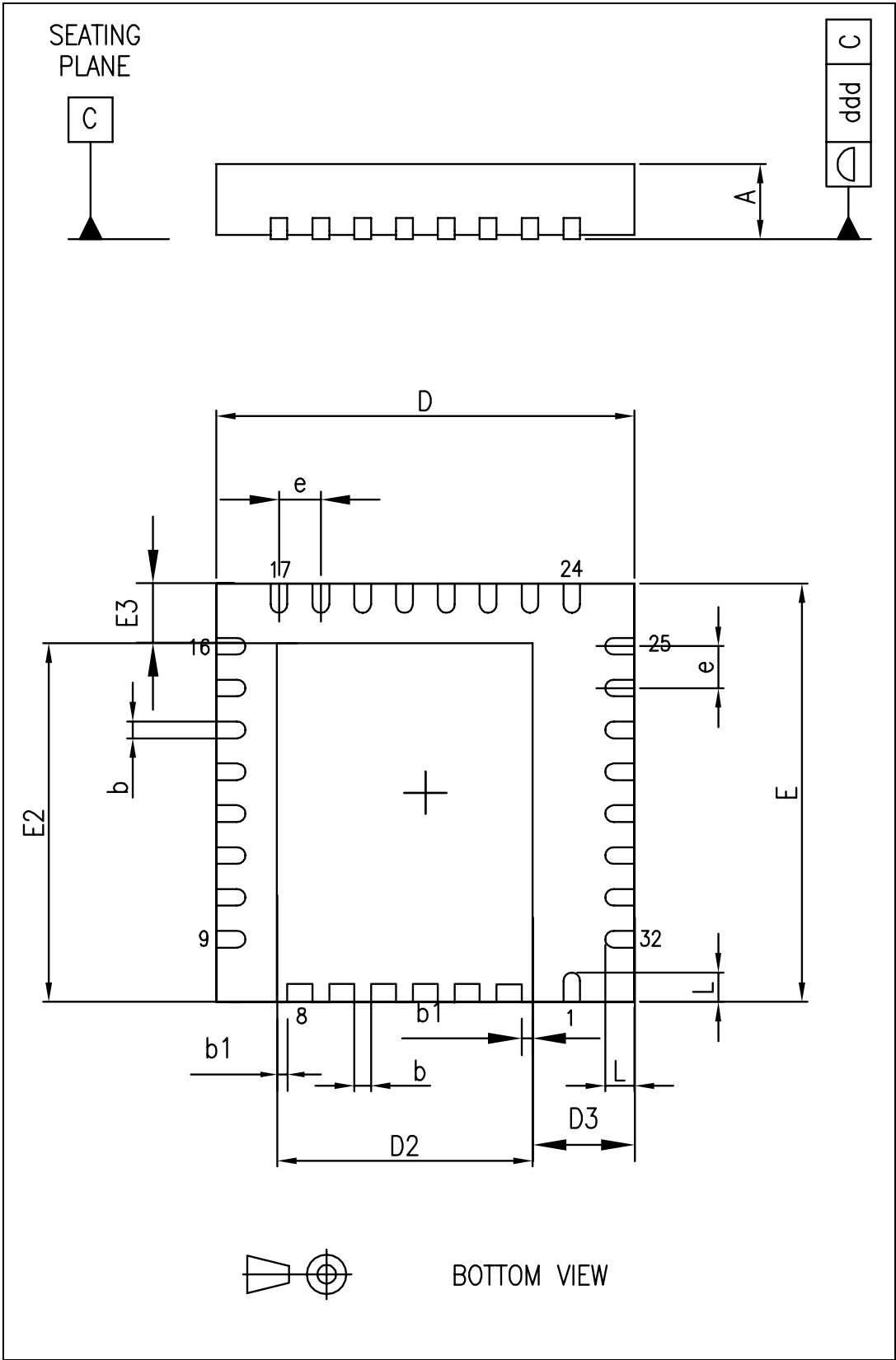
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 9. VFQFPN32 5x5x1.0 pitch 0.50

| Dim. | Databook (mm) | | |
|------|---------------|-------|-------|
| | Min | Typ | Max |
| A | 0.80 | 0.85 | 0.95 |
| b | 0.18 | 0.25 | 0.30 |
| b1 | 0.165 | 0.175 | 0.185 |
| D | 4.85 | 5.00 | 5.15 |
| D2 | 3.00 | 3.10 | 3.20 |
| D3 | 1.10 | 1.20 | 1.30 |
| E | 4.85 | 5.00 | 5.15 |
| E2 | 4.20 | 4.30 | 4.40 |
| E3 | 0.60 | 0.70 | 0.80 |
| e | | 0.50 | |
| L | 0.30 | 0.40 | 0.50 |
| ddd | | | 0.08 |

- Note:**
- 1 VFQFPN stands for thermally enhanced very thin profile fine pitch quad flat package no lead. Very thin profile: $0.80 < A = 1.00$ mm.
 - 2 Details of terminal 1 are optional but must be located on the top surface of the package by using either a mold or marked features.

Figure 21. Package dimensions



9 Order codes

Table 10. Order code

| Order code | Package | Packaging |
|------------|-------------------------|-----------|
| L6227Q | VFQFPN32 5 x 5 x 1.0 mm | Tube |

10 Revision history

Table 11. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 07-Dec-2007 | 1 | First release |
| 10-Jun-2008 | 2 | Updated: Figure 18 on page 20 Added: Note 1 on page 4 |
| 28-Jan-2009 | 3 | Updated value in Table 3: Thermal data on page 4 |

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