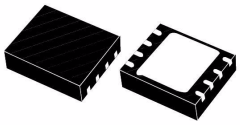
L5987

3 A step-down switching regulator

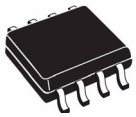
Preliminary Data

Features

- 3 A DC output current
- 2.9 V to 18 V input voltage
- Output voltage adjustable from 0.6 V
- 250 kHz switching frequency, programmable up to 1 MHz
- Internal soft-start and inhibit
- Low dropout operation: 100 % duty cycle
- Voltage feed-forward
- Zero load current operation
- Over current and thermal protection
- VFQFPN3x3-8L and HSOP8 package



VFQFPN8 3x3 mm



HSOP8 exposed pad

Applications

- Consumer:
  STB, DVD, DVD recorder, car audio, LCD TV and monitors
- Industrial:
  PLD, PLA, FPGA, chargers
- Networking: XDSL, modems, DC-DC modules
- Computer:
  Optical storage, hard disk drive, printers, audio/graphic cards
- LED driving

Description

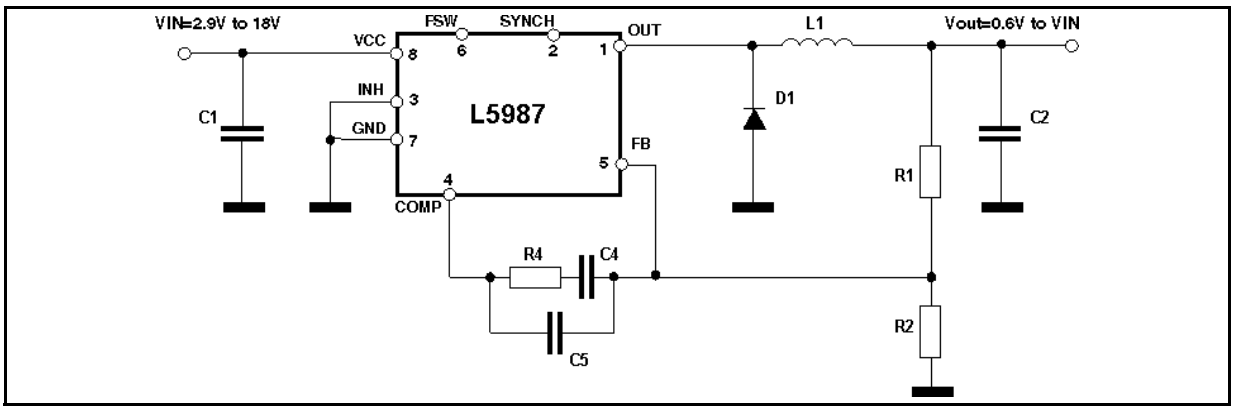
The L5987 is a step down switching regulator with 3.5 A (minimum) current limited embedded power MOSFET, so it is able to deliver up to 3 A current to the load depending on the application conditionals *Section 5.7* and *Section 5.8*).

The input voltage can range from 2.9 V to 18 V, while the output voltage can be set starting from 0.6 V to V_{IN}. Having a minimum input voltage of 2.9 V, the device is suitable also for 3.3 V bus.

Requiring a minimum set of external components, the device includes an internal 250 kHz switching frequency oscillator that can be externally adjusted up to 1 MHz.

The QFN and the HSOP package with exposed pad allow reducing the R_{thJA} down to 60 °C/W and 40 °C/W respectively.

Figure 1. Application circuit

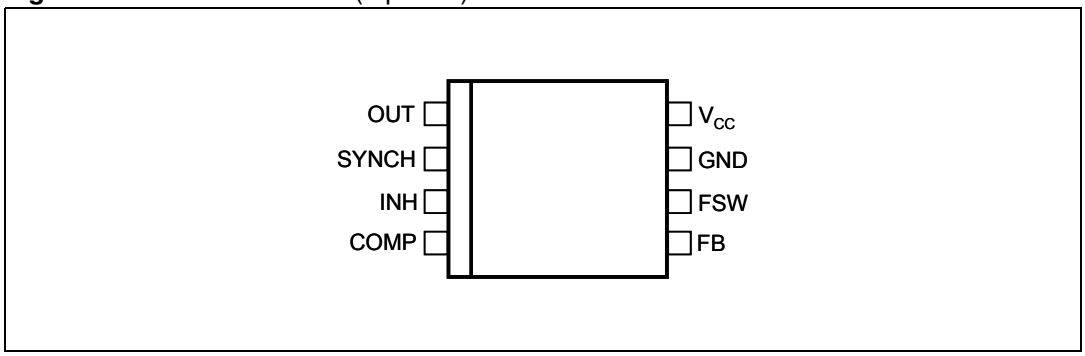


Contents

1 Pin settings

1.1 Pin connection

Figure 1. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

N.	Type	Description
1	OUT	Regulator output
2	SYNCH	Master/slave synchronization. When it is left floating, a signal with a phase shift of half a period respect to the power turn on is present at the pin. When connected to an external signal at a frequency higher than the internal one, then the device is synchronized by the external signal, with zero phase shift. Connecting together the SYNCH pin of two devices, the one with higher frequency works as master and the other one as slave; so the two powers turn on have a phase shift of half a period.
3	INH	A logical signal (active high) disable the device. With INH higher than 1.9 V the device is OFF and with INH lower than 0.6 V the device is ON.
4	COMP	Error amplifier output to be used for loop frequency compensation
5	FB	Feedback input. Connecting the output voltage directly to this pin the output voltage is regulated at 0.6 V. To have higher regulated voltages an external resistor divider is required from Vout to FB pin.
6	F_{SW}	The switching frequency can be increased connecting an external resistor from FSW pin and ground. If this pin is left floating the device works at its free-running frequency of 250 kHz.
7	GND	Ground
8	V_{CC}	Unregulated DC input voltage

2 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter		Value	Unit
Vcc	Input voltage		20	V
OUT	Output DC voltage		-0.3 to V_{CC}	
F_{SW}, COMP, SYNCH	Analog pin		-0.3 to 4	
INH	Inhibit pin		-0.3 to V_{CC}	
FB	Feedback voltage		-0.3 to 1.5	
P_{TOT}	Power dissipation at T_A < 60 °C	VFQFPN	1.5.	W
		HSOP	2	
T_J	Junction temperature range		-40 to 150	°C
T_{stg}	Storage temperature range		-55 to 150	°C

3 Thermal data

Table 3. Thermal data

Symbol	Parameter		Value	Unit
R_{thJA}	Maximum thermal resistance junction-ambient (1)	VFQFPN	60	°C/W
		HSOP	40	

1. Package mounted on demonstration board.

4 Electrical characteristics

T_J = 25 °C, V_{CC} = 12 V, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
V_{CC}	Operating input voltage range	(1)	2.9		18	V
V_{CCON}	Turn on V_{CC} threshold	(1)			2.9	
V_{CCOFF}	Turn off V_{CC} threshold	(1)	2.4			
$R_{DS(on)}$	Mosfet on resistance			140	170	mΩ
		(1)		140	220	
I_{LIM}	Maximum limiting current		3.5	4.0	4.4	A
Oscillator						
F_{SW}	Switching frequency		225	250	275	kHz
		(1)	220		265	
V_{FSW}	FSW pin voltage			1.262		V
D	Duty cycle		0		100	%
F_{ADJ}	Adjustable switching frequency	R_{FSW} = 33 kΩ		1000		kHz
Dynamic characteristics						
V_{FB}	Feedback voltage	2.9 V < V_{CC} < 18 V (1)	0.593	0.6	0.607	V
DC characteristics						
I_Q	Quiescent current	Duty Cycle = 0, V_{FB} = 0.8 V			2.4	mA
I_{QST-BY}	Total stand-by quiescent current			20	30	µA
Inhibit						
	INH threshold voltage	Device ON level			0.6	V
		Device OFF level	1.9			
	INH current	INH = 0		7.5	10	µA
Soft-start						
T_{SS}	Soft-start duration	FSW pin floating	7.4	8.2	9.1	ms
		F_{SW} = 1 MHz, R_{FSW} = 33 kΩ		2		

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Error amplifier						
V_{CH}	High level output voltage	V_{FB} < 0.6 V	3			V
V_{CL}	Low level output voltage	V_{FB} > 0.6 V			0.1	
I_{FB}	Bias source current	V_{FB} = 0 V to 0.8 V		1		µA
$I_{O\ SOURCE}$	Source COMP pin	V_{FB} = 0.5 V, V_{COMP} = 1 V		17		mA
$I_{O\ SINK}$	Sink COMP pin	V_{FB} = 0.7 V, V_{COMP} = 1 V		25		mA
G_V	Open loop voltage gain	(2)		100		dB
Synchronization function						
	High input voltage		2		3.3	V
	Low input voltage				1	
	Slave sink current	V_{SYNCH} = 2.9 V		0.7	0.9	mA
	Master output amplitude	I_{SOURCE} = 200 µA		3.0		V
	Output pulse width	SYNCH floating		110		ns
	Input pulse width		70			
Protection						
I_{FBDISC}	FB disconnection source current			1		µA
T_{SHDN}	Thermal shutdown			150		°C
	Hysteresis			30		

1. Specification referred to T_J from -40 to +125 °C. Specification in the -40 to +125 °C temperature range are assured by design, characterization and statistical correlation.
2. Guaranteed by design.

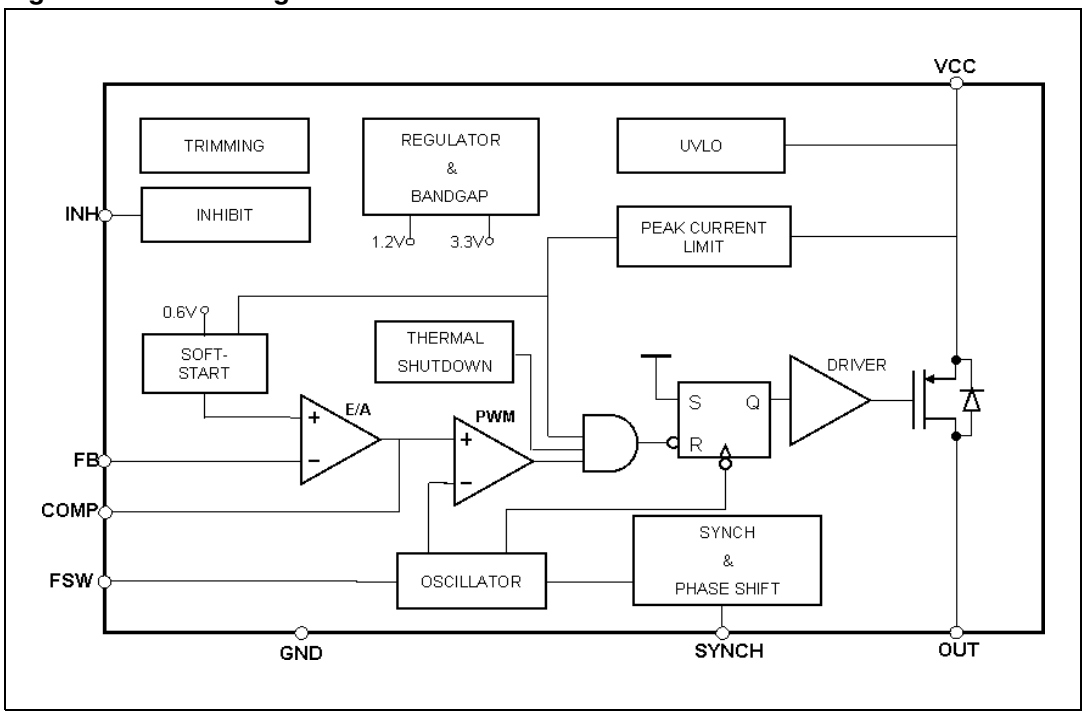
5 Functional description

The L5987 is based on a “voltage mode”, constant frequency control. The output voltage V_{OUT} is sensed by the feedback pin (FB) compared to an internal reference (0.6 V) providing an error signal that, compared to a fixed frequency sawtooth, controls the on and off time of the power switch.

The main internal blocks are shown in the block diagram in *Figure 2*. They are:

- A fully integrated oscillator that provides sawtooth to modulate the duty cycle and the synchronization signal. Its switching frequency can be adjusted by an external resistor. The voltage and frequency feed forward are implemented.
- The soft-start circuitry to limit inrush current during the start up phase.
- The voltage mode error amplifier
- The pulse width modulator and the relative logic circuitry necessary to drive the internal power switch.
- The High-side driver for embedded P-channel power MOSFET switch.
- The peak current limit sensing block, to handle over load and short circuit conditions.
- A voltage regulator and internal reference. It supplies internal circuitry and provides a fixed internal reference.
- A voltage monitor circuitry (UVLO) that checks the input and internal voltages.
- A thermal shutdown block, to prevent thermal run away.

Figure 2. Block diagram



5.1 Oscillator and synchronization

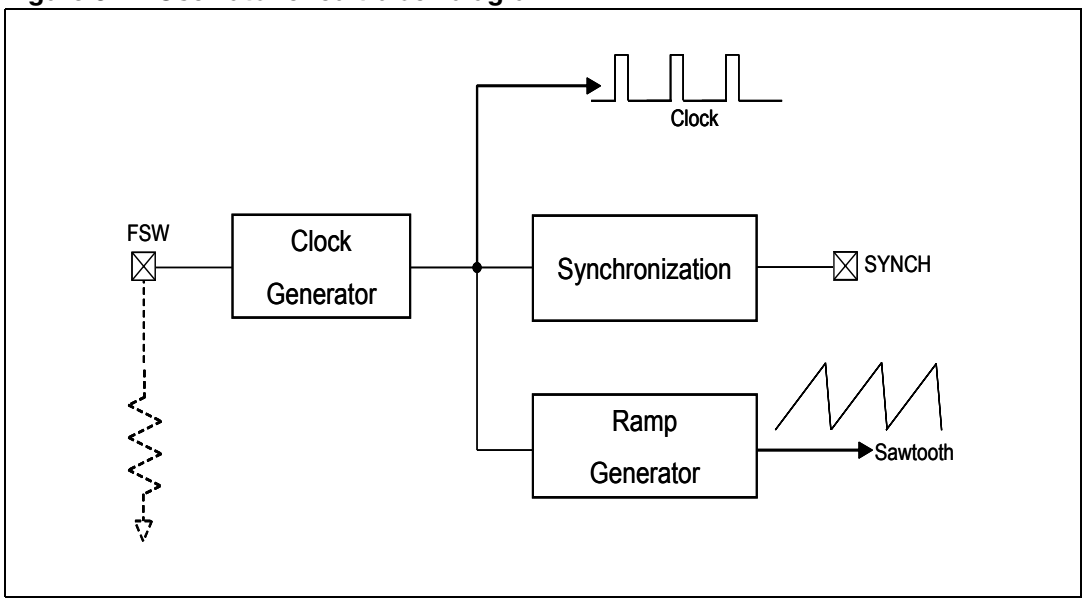
Figure 3 shows the block diagram of the oscillator circuit. The internal oscillator provides a constant frequency clock. Its frequency depends on the resistor externally connect to FSW pin. In case the FSW pin is left floating the frequency is 250 kHz; it can be increased as shown in *Figure 5* by external resistor connected to ground.

To improve the line transient performance, keeping the PWM gain constant versus the input voltage, the voltage feed forward is implemented by changing the slope of the sawtooth according to the input voltage change (see *Figure 4*.a).

The slope of the sawtooth also changes if the oscillator frequency is increased by the external resistor. In this way a frequency feed forward is implemented (*Figure 4*.b) in order to keep the PWM gain constant versus the switching frequency (see *Section 6.4* for PWM gain expression).

On the SYNCH pin the synchronization signal is generated. This signal has a phase shift of 180° with respect to the clock. This delay is useful when two devices are synchronized connecting the SYNCH pin together. When SYNCH pins are connected, the device with higher oscillator frequency works as Master, so the Slave device switches at the frequency of the master but with a delay of half a period. This minimizes the RMS current flowing through the input capacitor [see L5988D data sheet].

Figure 3. Oscillator circuit block diagram



The device can be synchronized to work at higher frequency feeding an external clock signal. The synchronization changes the sawtooth amplitude, changing the PWM gain (*Figure 4*.c). This changing has to be taken into account when the loop stability is studied. To minimize the change of the PWM gain, the free running frequency should be set (with a resistor on FSW pin) only slightly lower than the external clock frequency. This pre-adjusting of the frequency will change the sawtooth slope in order to get negligible the truncation of sawtooth, due to the external synchronization.

Figure 4. Sawtooth: voltage and frequency feed forward; external synchronization

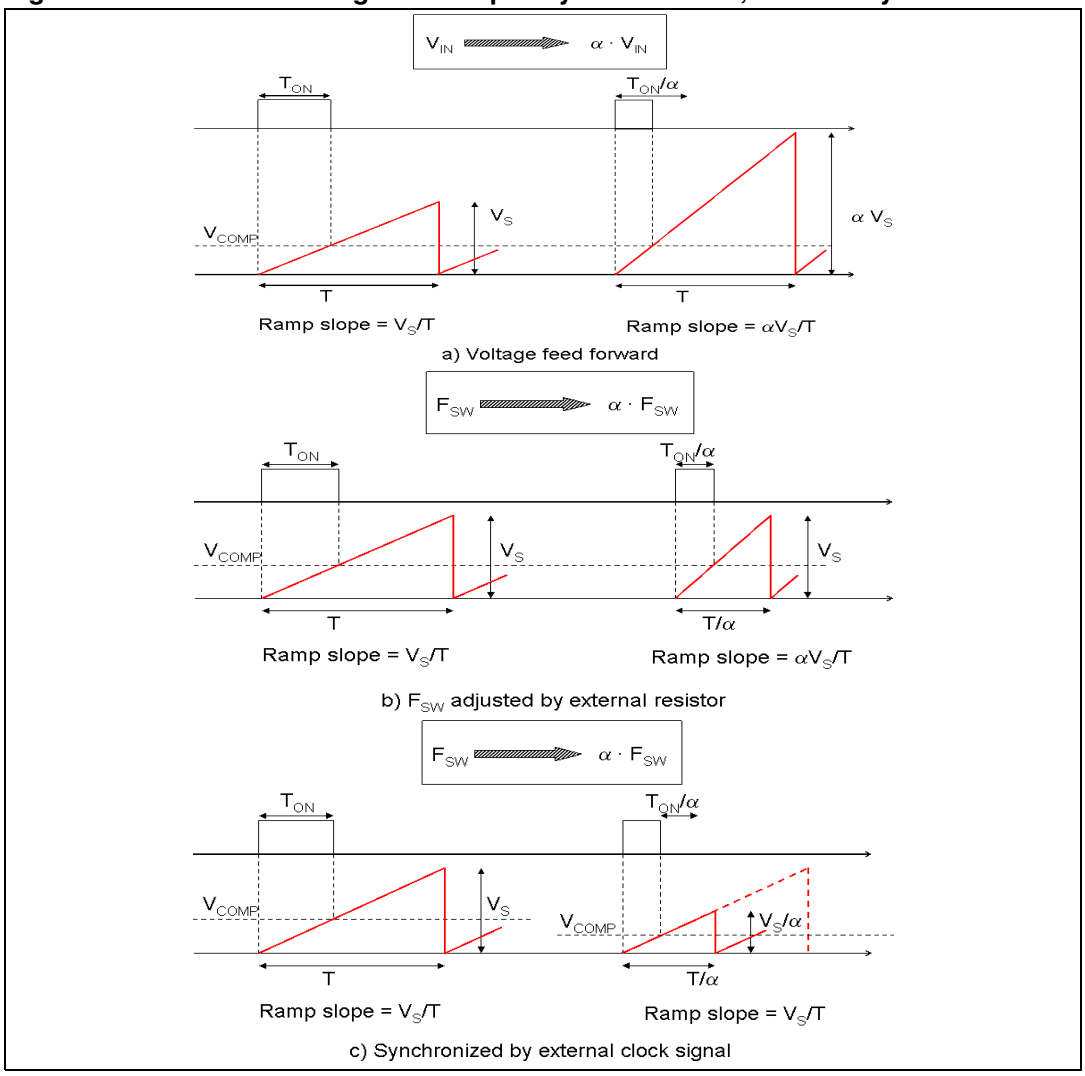
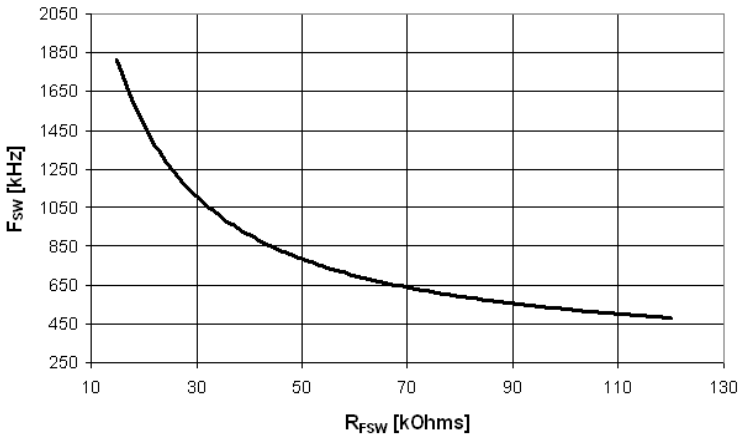


Figure 5. Oscillator frequency versus FSW pin resistor



5.2 Soft-start

The soft-start is essential to assure correct and safe start up of the step-down converter. It avoids inrush current surge and makes the output voltage increases monothonically.

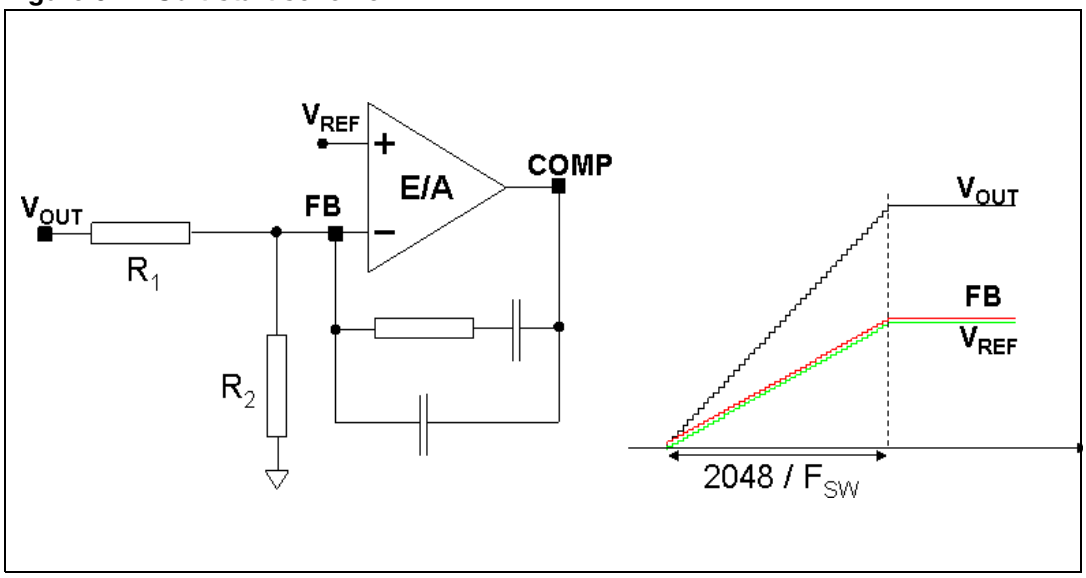
The soft-start is performed by a staircase ramp on the non-inverting input (V_{REF}) of the error amplifier. So the output voltage slew rate is:

Equation 1

$$SR_{OUT} = SR_{VREF} \cdot \left(1 + \frac{R1}{R2}\right)$$

where SR_{VREF} is the slew rate of the non-inverting input, while R1and R2 is the resistor divider to regulate the output voltage (see *Figure 6*). The soft-start stair case consists of 64 steps of 9.5 mV each one, from 0 V to 0.6 V. The time base of one step is of 32 clock cycles. So the soft-start time and then the output voltage slew rate depend on the switching frequency.

Figure 6. Soft-start scheme



Soft-start time results:

Equation 2

$$SS_{TIME} = \frac{32 \cdot 64}{Fsw}$$

For example with a switching frequency of 250 kHz the SS_{TIME} is 8 ms.

5.3 Error amplifier and compensation

The error amplifier (E/A) provides the error signal to be compared with the sawtooth to perform the pulse width modulation. Its non-inverting input is internally connected to a 0.6 V voltage reference, while its inverting input (FB) and output (COMP) are externally available for feedback and frequency compensation. In this device the error amplifier is a voltage mode operational amplifier so with high DC gain and low output impedance.

The uncompensated error amplifier characteristics are the following:

Table 5. Uncompensated error amplifier characteristics

Parameter	Value
Low frequency gain	100 dB
GBWP	4.5 MHz
Slew rate	7 V/µs
Output voltage swing	0 to 3.3 V
Maximum source/sink current	25 mA/40 mA

In continuos conduction mode (CCM), the transfer function of the power section has two poles due to the LC filter and one zero due to the ESR of the output capacitor. Different kinds of compensation networks can be used depending on the ESR value of the output capacitor. In case the zero introduced by the output capacitor helps to compensate the double pole of the LC filter a type II compensation network can be used. Otherwise, a type III compensation network has to be used (see *Chapter 6.4* for details about the compensation network selection).

Anyway the methodology to compensate the loop is to introduce zeros to obtain a safe phase margin.

5.4 Over-current protection

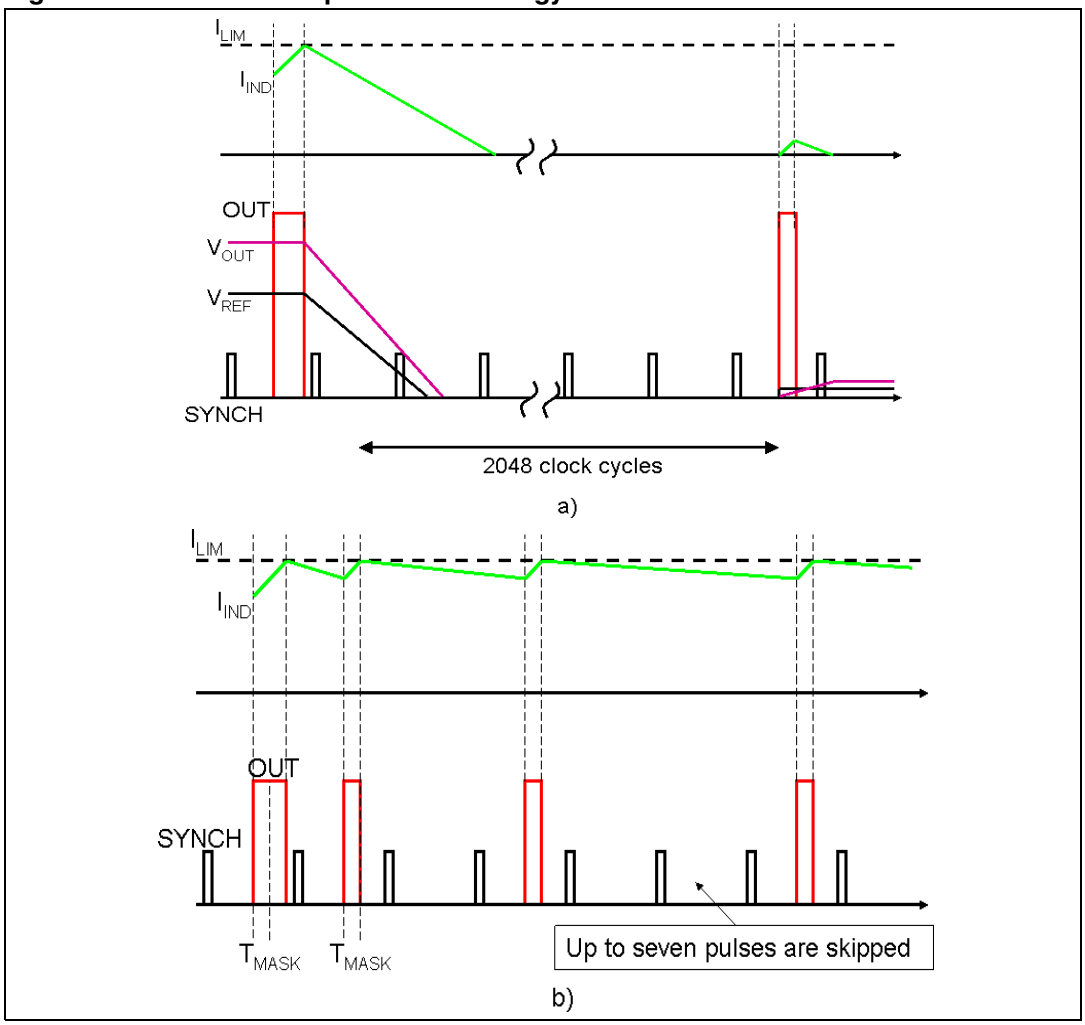
The L5987 implements the over-current protection sensing current flowing through the power MOSFET. Due to the noise created by the switching activity of the power MOSFET, the current sensing is disabled during the initial phase of the conduction time. This avoids an erroneous detection of a fault condition. This interval is generally known as “masking time” or “blanking time”. The masking time is about 200 ns.

When the over-current is detected, two different behaviors are possible depending on the operating condition.

1. **Output voltage in regulation**. When the over current is sensed, the power MOSFET is switched off and the internal reference (V_{REF}), that biases the non-inverting input of the error amplifier, is set to zero and kept in this condition for a soft-start time (T_{SS}, 2048 clock cycles). After this time, a new soft-start phase takes place and the internal reference begins ramping (see *Figure 7*.a).
2. **Soft-start phase**. If the over current limit is reached the power MOSFET is turned off implementing the pulse by pulse over current protection. During the soft-start phase, under over current condition, the device can skip pulses in order to keep the output current constant and equal to the current limit. If at the end of the “masking time” the current is higher than the over current threshold, the power MOSFET is turned off and it will skip one pulse. If, at the next switching on at the end of the “masking time” the current is still higher than the threshold, the device will skip two pulses. This mechanism is repeated and the device can skip up to seven pulses. While, if at the end of the “masking time” the current is lower than the over current threshold, the number of skipped cycles is decreased of one unit. At the end of soft-start phase the output voltage is in regulation and if the over current persists the behavior explained above takes place. (see *Figure 7*.b)

So the over current protection can be summarized as an “hiccup” intervention when the output is in regulation and a constant current during the soft-start phase. If the output is shorted to ground when the output voltage is on regulation, the over current is triggered and the device starts cycling with a period of 2048 clock cycles between “hiccup” (power MOSFET off and no current to the load) and “constant current” with very short on-time and with reduced switching frequency (up to one eighth of normal switching frequency). See for short circuit behavior.

Figure 7. Over-current protection strategy



5.5 Inhibit function

The inhibit feature allows to put in stand-by mode the device.With INH pin higher than 1.9 V the device is disabled and the power consumption is reduced to less than 30 µA. With INH pin lower than 0.6 V, the device is enabled. If the INH pin is left floating, an internal pull up ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also VCC compatible.

5.6 Hysteretic thermal shutdown

The thermal shutdown block generates a signal that turns off the power stage if the junction temperature goes above 150 °C. Once the junction temperature goes back to about 130 °C, the device restarts in normal operation. The sensing element is very close to the PDMOS area, so ensuring an accurate and fast temperature detection.

5.7 Maximum DC output current L5987A (HSOP8)

The L5987A can manage DC output currents up to 3 A and the rated RMS current of its internal power switch is 3 A. So the L5987A can deliver 3 A with 100 % of duty cycle.

5.8 Maximum DC output current L5987 (VFQFPN)

The L5987 can manage DC output currents up to 3 A. However the rated RMS current of its internal power switch is 2.5 A.

Since the current flows through the integrated power element only during the on time, the RMS value is given by:

Equation 3

$$I_{RMS} = I_O \cdot \sqrt{D}$$

Where D is the duty cycle (V_O/V_{IN}).

Considering I_O = 3 A, the maximum duty cycle that can be managed is:

Equation 4

$$D = \frac{I_{RMS}^2}{I_O^2} = 69\%$$

In *Figure 8* the maximum DC output current is reported as a function of the duty cycle. For duty cycles lower than 69 %, the RMS current does not limit the maximum DC output current of 3 A. For duty cycles higher than the 69 % the maximum DC output current is limited by the RMS current to:

Equation 5

$$I_{O,MAX} = \frac{2.5}{\sqrt{D}} \quad [A] \quad \text{if } D \geq 69\%$$

In order to have a more accurate calculation of the maximum DC output current, the complete expression for the duty cycle can be adopted, considering the voltage drop across the power MOSFET, the series resistance of the inductor and the forward voltage of the rectification diode. The duty cycle results:

Equation 6

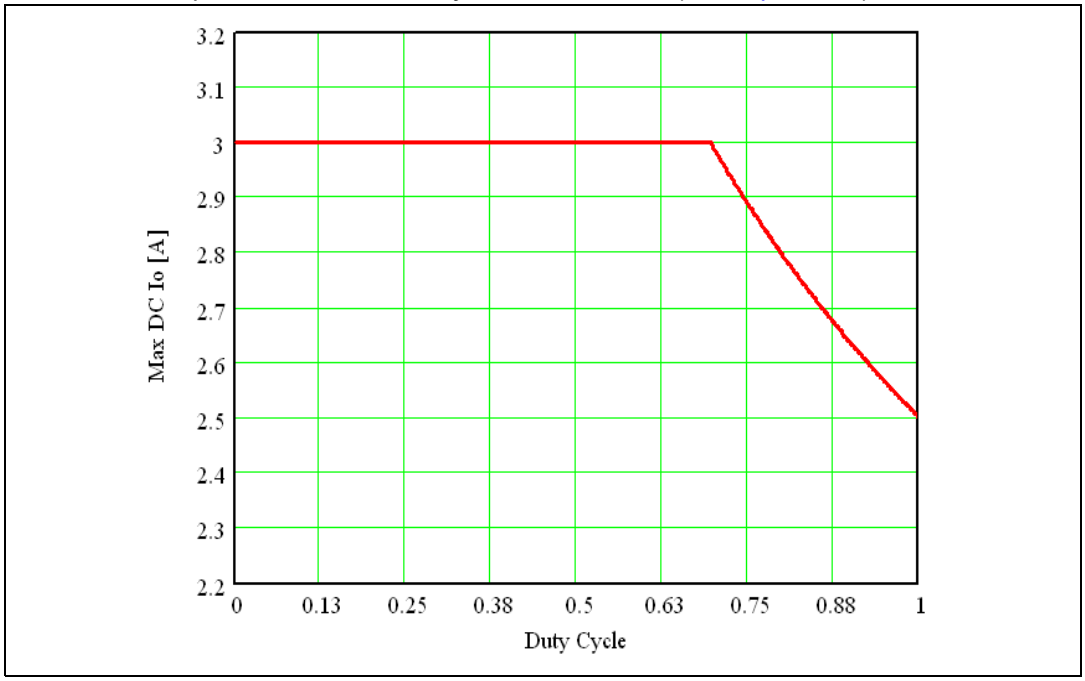
$$D = \frac{V_{OUT} + V_F + DCR \cdot I_O}{V_{IN} + V_F - R_{DSON} \cdot I_O}$$

where I_O is the desired DC output current.

For example with V_{IN} = 5 V, V_{OUT} = 3.3 V, I_O = 2.6 A, $R_{DS(on)}$ = 220 mΩ, V_F = 0.35 V and DCR = 30 mΩ, the duty results D = 78 %, so according to *Equation 5* the maximum DC output current is 2.83 A, which is higher than desired current.

With V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_O = 2.7 A, $R_{DS(on)}$ = 220 mΩ, V_F = 0.35 V and DCR = 30 mΩ, the duty is D = 73 %, so the maximum DC output current results 2.926 A, higher than the desired current.

Figure 8. Maximum DC output current for VQFN package vs duty cycle. For duty cycles lower than 69 %, the RMS current does not limit the maximum DC output current of 3 A. For duty cycles higher than the 69 % the maximum DC output current is limited by the RMS current (see *Equation 5*)



6 Application information

6.1 Input capacitor selection

The capacitor connected to the input has to be capable to support the maximum input operating voltage and the maximum RMS input current required by the device. The input capacitor is subject to a pulsed current, the RMS value of which is dissipated over its ESR, affecting the overall system efficiency.

So the input capacitor must have a RMS current rating higher than the maximum RMS input current and an ESR value compliant with the expected efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

Equation 7

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

Where Io is the maximum DC output current, D is the duty cycle, η is the efficiency. Considering $\eta = 1$, this function has a maximum at D = 0.5 and it is equal to Io/2.

In a specific application the range of possible duty cycles has to be considered in order to find out the maximum RMS input current. The maximum and minimum duty cycles can be calculated as:

Equation 8

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}}$$

and

Equation 9

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

Where V_F is the forward voltage on the freewheeling diode and V_{SW} is voltage drop across the internal PDMOS. In *Table 6.* some multi layer ceramic capacitors suitable for this device are reported:

Table 6. Input MLCC capacitors

Manufacture	Series	Cap value (µF)	Rated voltage (V)
MURATA	GRM31	10	25
	GRM55	10	25
TDK	C3225	10	25

6.2 Inductor selection

The inductance value fixes the current ripple flowing through the output capacitor. So the minimum inductance value in order to have the expected current ripple has to be selected. The rule to fix the current ripple value is to have a ripple at 20 %-40 % of the output current.

In the continuos current mode (CCM), the inductance value can be calculated by the following equation:

Equation 10

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT} + V_F}{L} \cdot T_{OFF}$$

Where T_{ON} is the conduction time of the internal high side switch and T_{OFF} is the conduction time of the external diode (in CCM, $F_{SW} = 1/(T_{ON} + T_{OFF})$). The maximum current ripple, at fixed Vout, is obtained at maximum T_{OFF} that is at minimum duty cycle (see previous section to calculate minimum duty). So fixing ΔI_L = 20 % to 30 % of the maximum output current, the minimum inductance value can be calculated:

Equation 11

$$L_{MIN} = \frac{V_{OUT} + V_F}{\Delta I_{MAX}} \cdot \frac{1 - D_{MIN}}{F_{SW}}$$

where F_{SW} is the switching frequency, $1/(T_{ON} + T_{OFF})$.

For example for V_{OUT} = 3.3 V, V_{IN} = 12 V, I_O = 3 A and F_{SW} = 250 kHz the minimum inductance value to have ΔI_L = 30 % of I_O is about 10 µH.

The peak current through the inductor is given by:

Equation 12

$$I_{L,PK} = I_O + \frac{\Delta I_L}{2}$$

So if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. The higher is the inductor value, the higher is the average output current that can be delivered, without reaching the current limit.

In the table below some inductor part numbers are listed.

Table 7. Inductors

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	MSS1038	3.8 to 10	3.9 to 6.5
	MSS1048	12 to 22	3.84 to 5.34

Table 7. Inductors (continued)

Manufacturer	Series	Inductor value (μH)	Saturation current (A)
Wurth	PD Type L	8.2 to 15	3.75 to 6.25
	PD Type M	2.2 to 4.7	4 to 6
SUMIDA	CDRH6D226/HP	1.5 to 3.3	3.6 to 5.2
	CDR10D48MN	6.6 to 12	4.1 to 5.7

6.3 Output capacitor selection

The current in the capacitor has a triangular waveform which generates a voltage ripple across it. This ripple is due to the capacitive component (charge or discharge of the output capacitor) and the resistive component (due to the voltage drop across its ESR). So the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements.

The amount of the voltage ripple can be calculated starting from the current ripple obtained by the inductor selection.

Equation 13

$$\Delta V_{OUT} = ESR \cdot \Delta I_{MAX} + \frac{\Delta I_{MAX}}{8 \cdot C_{OUT} \cdot f_{SW}}$$

Usually the resistive component of the ripple is much higher than the capacitive one, if the output capacitor adopted is not a multi layer ceramic capacitor (MLCC) with very low ESR value.

The output capacitor is important also for loop stability: it fixes the double LC filter pole and the zero due to its ESR. In *Chapter 6.4*, it will be illustrated how to consider its effect in the system stability.

For example with V_{OUT} = 3.3 V, V_{IN} = 12 V, ΔI_L = 0.9 A (resulting by the inductor value), in order to have a $\Delta V_{OUT} = 0.01 \cdot V_{OUT}$, if the multi layer ceramic capacitor are adopted, 13 μF are needed and the ESR effect on the output voltage ripple can be neglected. In case of not negligible ESR (electrolytic or tantalum capacitors), the capacitor is chosen taking into account its ESR value. So in case of 330 μF with ESR = 30 mΩ, the resistive component of the drop dominates and the voltage ripple is 27 mV.

The output capacitor is also important to sustain the output voltage when a load transient with high slew rate is required by the load. When the load transient slew rate exceeds the system bandwidth the output capacitor provides the current to the load. So if the high slew rate load transient is required by the application the output capacitor and system bandwidth have to be chosen in order to sustain the load transient.

In the table below some capacitor series are listed.

Table 8. Output capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
MURATA	GRM32	22 to 100	6.3 to 25	< 5
	GRM31	10 to 47	6.3 to 25	< 5
PANASONIC	ECJ	10 to 22	6.3	< 5
	EEFCD	10 to 68	6.3	15 to 55
SANYO	TPA/B/C	100 to 470	4 to 16	40 to 80
TDK	C3225	22 to 100	6.3	< 5

6.4 Compensation network

The compensation network has to assure stability and good dynamic performance. The loop of the L5987 is based on the voltage mode control. The error amplifier is a voltage operational amplifier with high bandwidth. So selecting the compensation network the E/A will be considered as ideal, that is, its bandwidth is much larger than the system one.

The transfer functions of PWM modulator and the output LC filter are studied (see *Figure 10.*). The transfer function of the PWM modulator, from the error amplifier output (COMP pin) to the OUT pin, results:

Equation 14

$$G_{PW0} = \frac{V_{IN}}{V_s}$$

where V_S is the sawtooth amplitude. As seen in *Chapter 5.1*, the voltage feed forward generates a sawtooth amplitude directly proportional to the input voltage, that is:

Equation 15

$$V_S = K \cdot V_{IN}$$

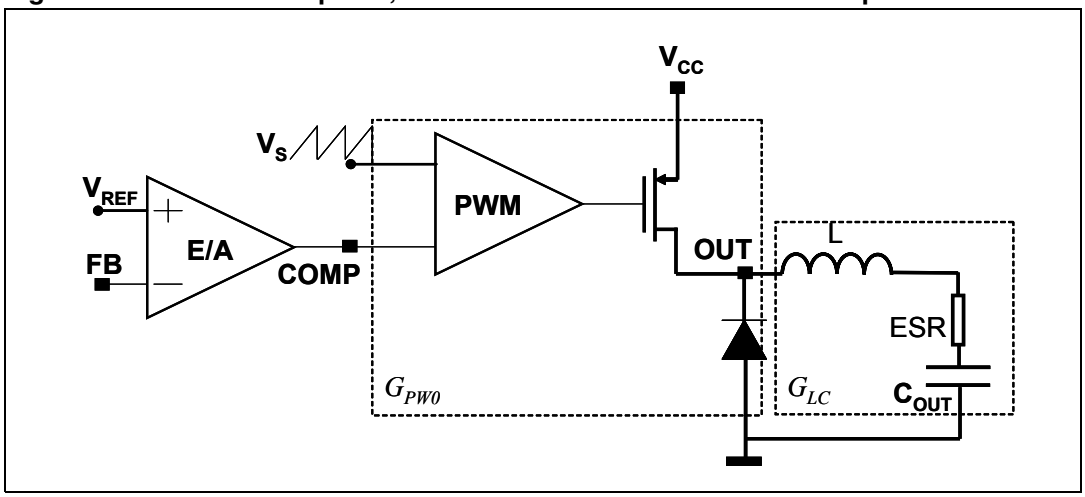
In this way the PWM modulator gain results constant and equals to:

Equation 16

$$G_{PW0} = \frac{V_{IN}}{V_s} = \frac{1}{K} = 9$$

The synchronization of the device with an external clock provided trough SYNCH pin can modifies the PWM modulator gain (see *Chapter 5.1* to understand how this gain changes and how to keep it constant in spite of the external synchronization).

Figure 9. The error amplifier, the PWM modulation and the LC output filter



The transfer function on the LC filter is given by:

Equation 17

$$G_{LC}(s) = \frac{1 + \frac{s}{2\pi \cdot f_{zESR}}}{1 + \frac{s}{2\pi \cdot Q \cdot f_{LC}} + \left(\frac{s}{2\pi \cdot f_{LC}}\right)^2}$$

where:

Equation 18

$$f_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C_{OUT}} \cdot \sqrt{1 + \frac{ESR}{R_{OUT}}}}, \qquad f_{zESR} = \frac{1}{2\pi \cdot ESR \cdot C_{OUT}}$$

Equation 19

$$Q = \frac{\sqrt{R_{OUT} \cdot L \cdot C_{OUT} \cdot (R_{OUT} + ESR)}}{L + C_{OUT} \cdot R_{OUT} \cdot ESR}, \qquad R_{OUT} = \frac{V_{OUT}}{I_{OUT}}$$

As seen in *Chapter 5.3* two different kind of network can compensate the loop. In the two following paragraph the guidelines to select the Type II and Type III compensation network are illustrated.

6.4.1 Type III compensation network

The methodology to stabilize the loop consists of placing two zeros to compensate the effect of the LC double pole, so increasing phase margin; then to place one pole in the origin to minimize the dc error on regulated output voltage; finally to place other poles far away the zero dB frequency.

If the equivalent series resistance (ESR) of the output capacitor introduces a zero with a frequency higher than the desired bandwidth (that is: $2\pi*ESR*COUT<1/BW$), the type III compensation network is needed. Multi layer ceramic capacitors (MLCC) have very low ESR (<1 mΩ), with very high frequency zero, so type III network is adopted to compensate the loop.

In *Figure 10* the type III compensation network is shown. This network introduces two zeros (f_{Z1}, f_{Z2}) and three poles (f_{P0}, f_{P1}, f_{P2}). They expression are:

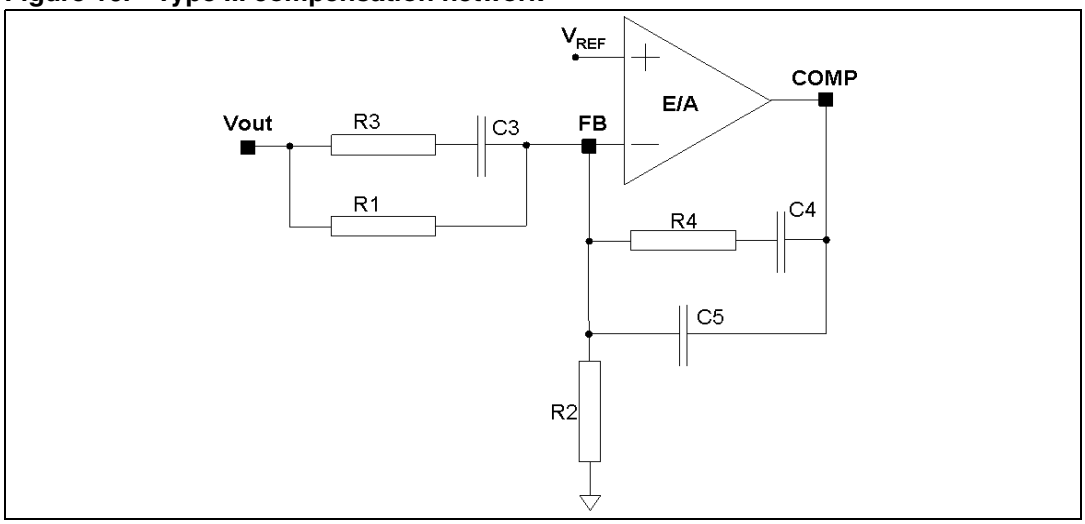
Equation 20

$$f_{Z1} = \frac{1}{2\pi \cdot C_3 \cdot (R_1 + R_3)}, \qquad f_{Z2} = \frac{1}{2\pi \cdot R_4 \cdot C_4}$$

Equation 21

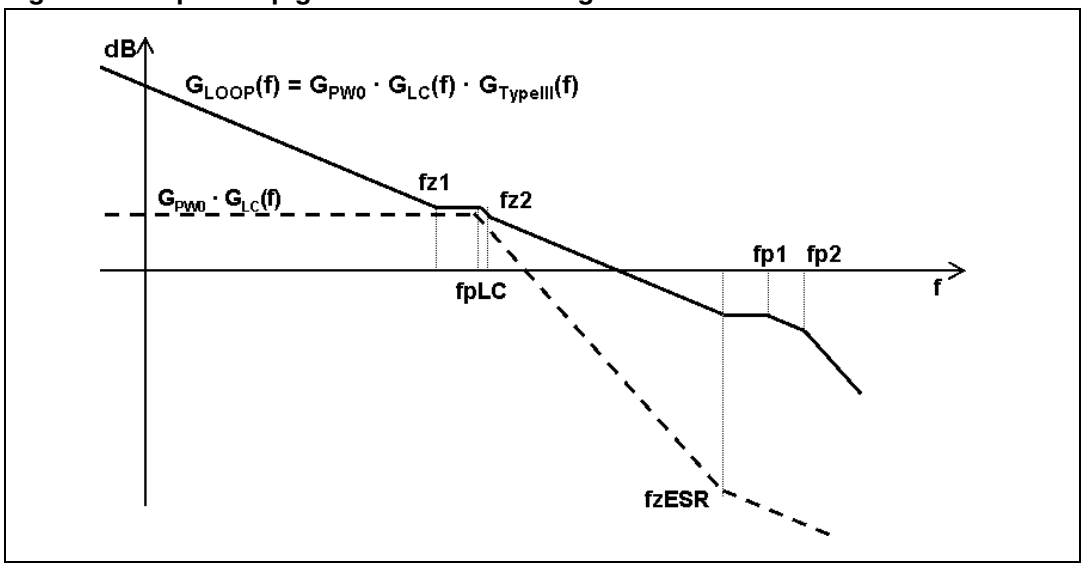
$$f_{P0} = 0, \qquad f_{P1} = \frac{1}{2\pi \cdot R_3 \cdot C_3}, \qquad f_{P2} = \frac{1}{2\pi \cdot R_4 \cdot \frac{C_4 \cdot C_5}{C_4 + C_5}}$$

Figure 10. Type III compensation network



In *Figure 11* the bode diagram of the PWM and LC filter transfer function ($G_{PW0} \cdot G_{LC}(f)$) and the open loop gain ($G_{LOOP}(f) = G_{PW0} \cdot G_{LC}(f) \cdot G_{TYPEIII}(f)$) are drawn.

Figure 11. Open loop gain: module bode diagram



The guidelines for positioning the poles and the zeroes and for calculating the component values can be summarized as follow:

1. Choose a value for R_1, usually between 1 k and 5 k.
2. Choose a gain (R_4/R_1) in order to have the required bandwidth (BW), that means:

Equation 22

$$R_4 = \frac{BW}{f_{LC}} \cdot \frac{1}{K} \cdot R_1$$

where K is the feed forward constant and 1/K is equals to 9.

3. Calculate C_4 by placing the zero at 50 % of the output filter double pole frequency (f_{LC}):

Equation 23

$$C_4 = \frac{1}{\pi \cdot R_4 \cdot f_{LC}}$$

4. Calculate C_5 by placing the second pole at four times the system bandwidth (BW):

Equation 24

$$C_5 = \frac{C_4}{2\pi \cdot R_4 \cdot C_4 \cdot 4 \cdot BW - 1}$$

5. Set also the first pole at four times the system bandwidth and also the second zero at the output filter double pole:

Equation 25

$$R_3 = \frac{R_1}{\frac{4 \cdot BW}{f_{LC}} - 1}, \qquad C_3 = \frac{1}{2\pi \cdot R_3 \cdot 4 \cdot BW}$$

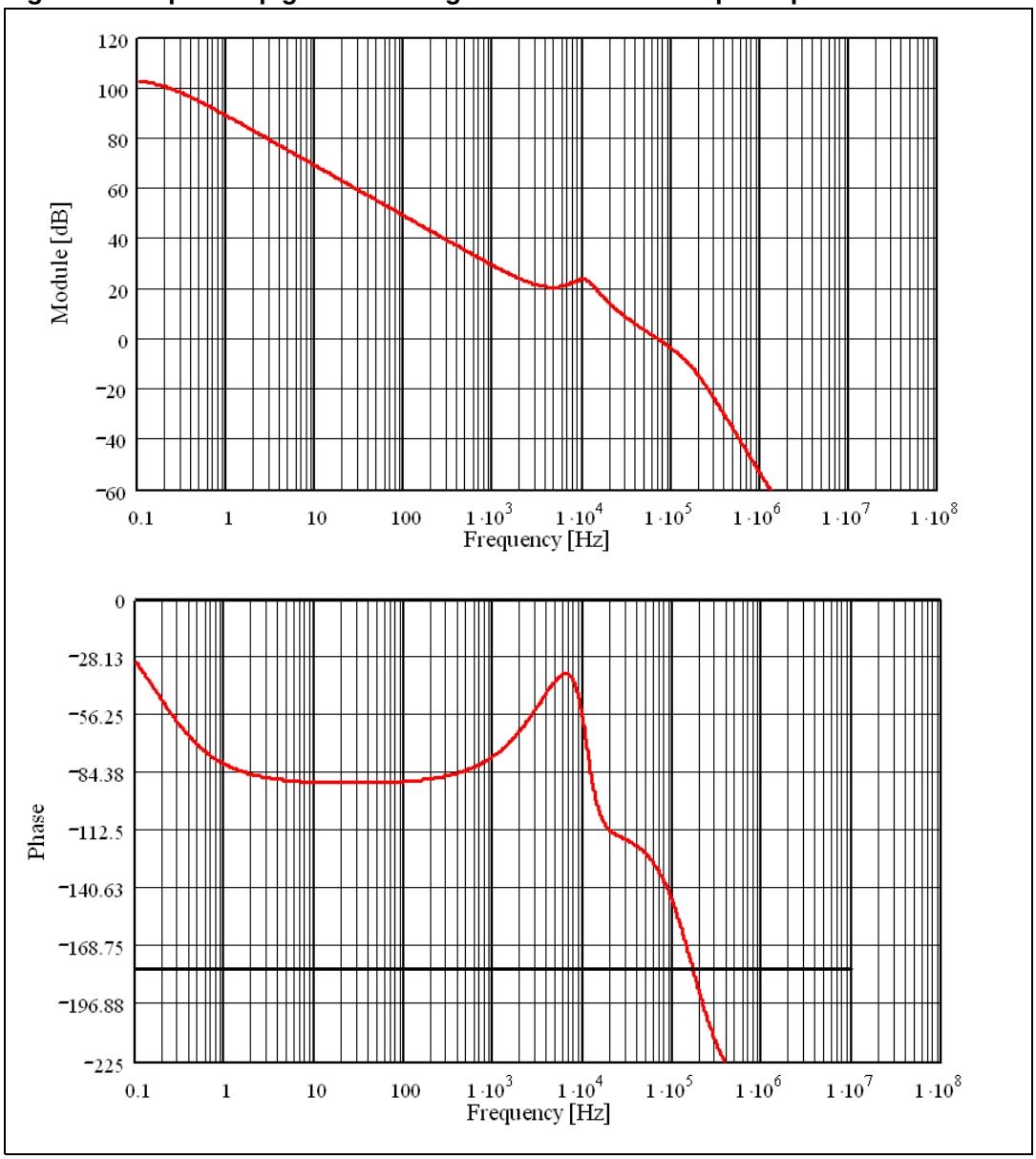
The suggested maximum system bandwidth is equals to the switching frequency divided by 3.5 (F_{SW}/3.5), anyway lower than 100 kHz if the F_{SW} is set higher than 500 kHz.

For example with V_{OUT} = 3.3 V, V_{IN} = 12 V, I_O = 3 A, L = 10 µH, C_{OUT} = 22 µF, ESR < 1 mΩ, the type III compensation network is:

R_1 = 4.99kΩ, R_2 = 1.1kΩ, R_3 = 220Ω, R_4 = 3.3kΩ, C_3 = 3.3nF, C_4 = 10nF, C_5 = 180pF

In *Figure 12* is shown the module and phase of the open loop gain. The bandwidth is about 71 kHz and the phase margin is 46°.

Figure 12. Open loop gain bode diagram with ceramic output capacitor

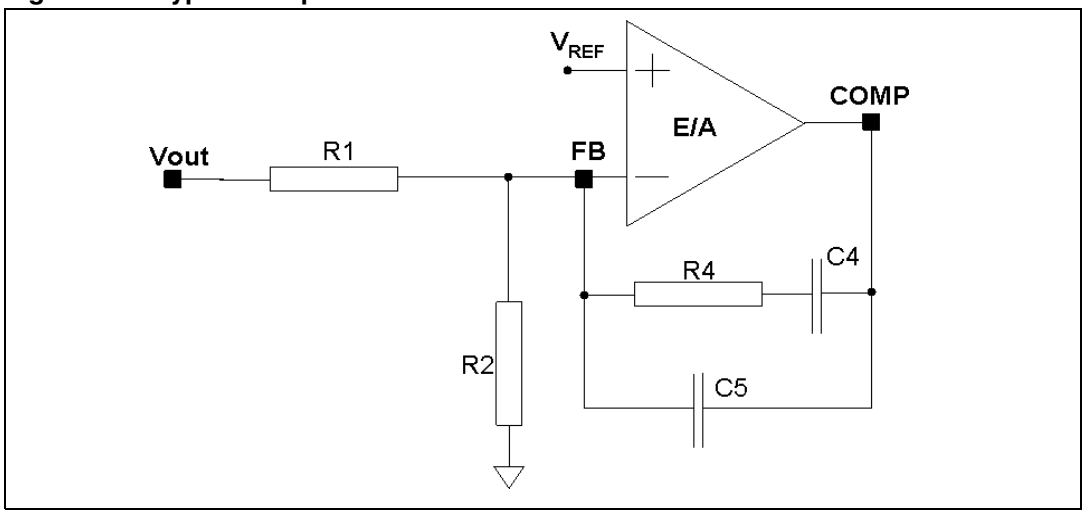


6.4.2 Type II compensation network

If the equivalent series resistance (ESR) of the output capacitor introduces a zero with a frequency lower than the desired bandwidth (that is: 2π∗ESR∗COUT>1/BW), this zero helps stabilize the loop. Electrolytic capacitors show not negligible ESR (>30 mΩ), so with this kind of output capacitor the type II network combined with the zero of the ESR allows stabilizing the loop.

In *Figure 13* the type II network is shown.

Figure 13. Type II compensation network

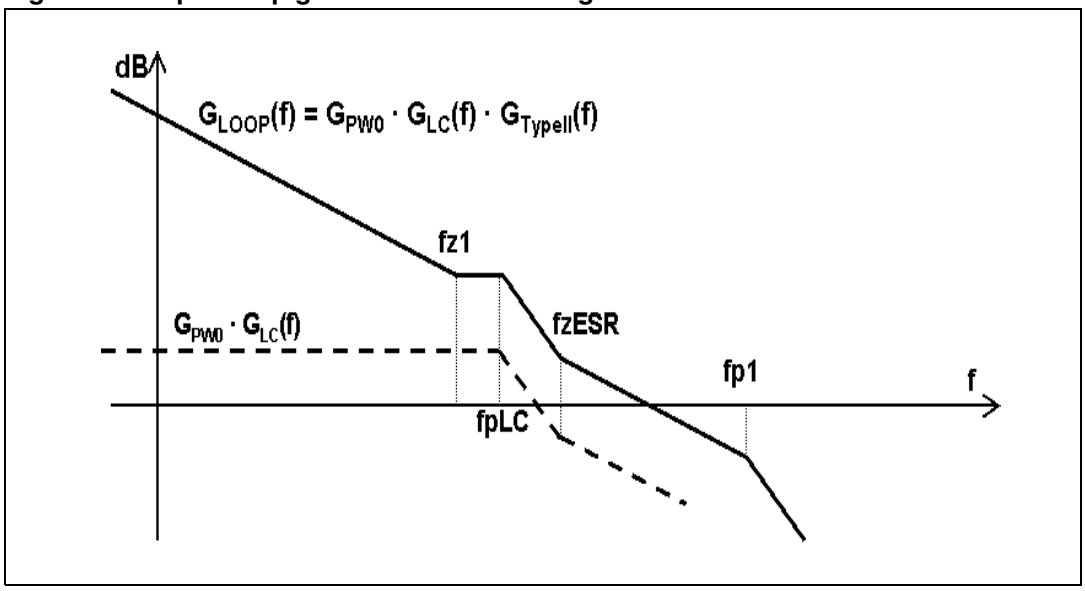


The singularities of the network are:

$$f_{Z1} = \frac{1}{2\pi \cdot R_4 \cdot C_4}, \quad f_{P0} = 0, \quad f_{P1} = \frac{1}{2\pi \cdot R_4 \cdot \frac{C_4 \cdot C_5}{C_4 + C_5}}$$

In *Figure 14* the bode diagram of the PWM and LC filter transfer function ($G_{PW0} \cdot G_{LC}(f)$) and the open loop gain ($G_{LOOP}(f) = G_{PW0} \cdot G_{LC}(f) \cdot G_{TYPEII}(f)$) are drawn.

Figure 14. Open loop gain: module bode diagram



The guidelines for positioning the poles and the zeroes and for calculating the component values can be summarized as follow:

1. Choose a value for R_1, usually between 1k and 5k, in order to have values of C4 and C5 not comparable with parasitic capacitance of the board.
2. Choose a gain (R_4/R_1) in order to have the required bandwidth (BW), that means:

Equation 26

$$R_4 = \left(\frac{f_{ESR}}{f_{LC}}\right)^2 \cdot \frac{BW}{f_{ESR}} \cdot \frac{V_S}{V_{IN}} \cdot R_1$$

Where f_{ESR} is the ESR zero:

Equation 27

$$f_{ESR} = \frac{1}{2\pi \cdot ESR \cdot C_{OUT}}$$

and Vs is the saw-tooth amplitude. The voltage feed forward keeps the ratio Vs/Vin constant.

3. Calculate C_4 by placing the zero one decade below the output filter double pole:

Equation 28

$$C_4 = \frac{10}{2\pi \cdot R_4 \cdot f_{LC}}$$

4. Then calculate C_3 in order to place the second pole at four times the system bandwidth (BW):

Equation 29

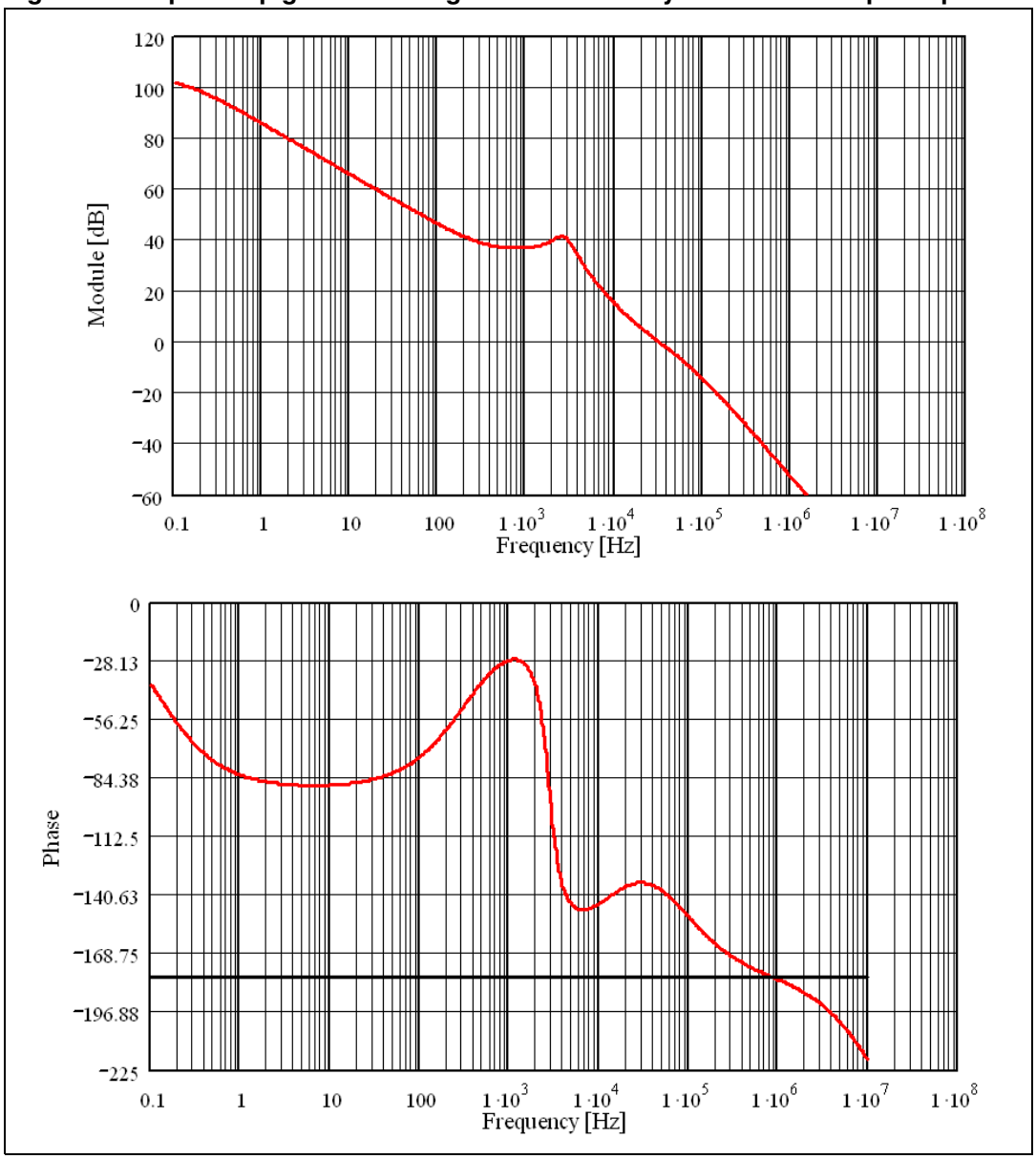
$$C_5 = \frac{C_4}{2\pi \cdot R_4 \cdot C_4 \cdot 4 \cdot BW - 1}$$

For example with V_{OUT} = 3.3 V, V_{IN} = 12 V, I_O = 3 A, L = 10 µH, C_{OUT} = 330 µF, ESR = 35 mΩ, the type II compensation network is:

$$R_1 = 1.5k\Omega, \quad R_2 = 330\Omega, \quad R_4 = 10k\Omega, \quad C_4 = 47nF, \quad C_5 = 82pF$$

In *Figure 15* is shown the module and phase of the open loop gain. The bandwidth is about 32 kHz and the phase margin is 45°.

Figure 15. Open loop gain bode diagram with electrolytic/tantalum output capacitor



6.5 Thermal considerations

The thermal design is important to prevent the thermal shutdown of device if junction temperature goes above 150 °C. The three different sources of losses within the device are:

a) conduction losses due to the not negligible $R_{DS(on)}$ of the power switch; these are equal to:

Equation 30

$$P_{ON} = R_{DSON} \cdot (I_{OUT})^2 \cdot D$$

Where D is the duty cycle of the application and the maximum $R_{DS(on)}$ over temperature is 220 mΩ. Note that the duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN}, but actually it is quite higher to compensate the losses of the regulator. So the conduction losses increases compared with the ideal case.

b) switching losses due to power MOSFET turn ON and OFF; these can be calculated as:

Equation 31

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot Fsw = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW}$$

Where T_{RISE} and T_{FALL} are the overlap times of the voltage across the power switch (V_{DS}) and the current flowing into it during turn ON and turn OFF phases, as shown in *Figure 16*. T_{SW} is the equivalent switching time. For this device the typical value for the equivalent switching time is 50ns.

c) Quiescent current losses, calculated as:

Equation 32

$$P_Q = V_{IN} \cdot I_Q$$

where I_Q is the quiescent current (I_Q = 2.4 mA).

The junction temperature T_J can be calculated as:

Equation 33

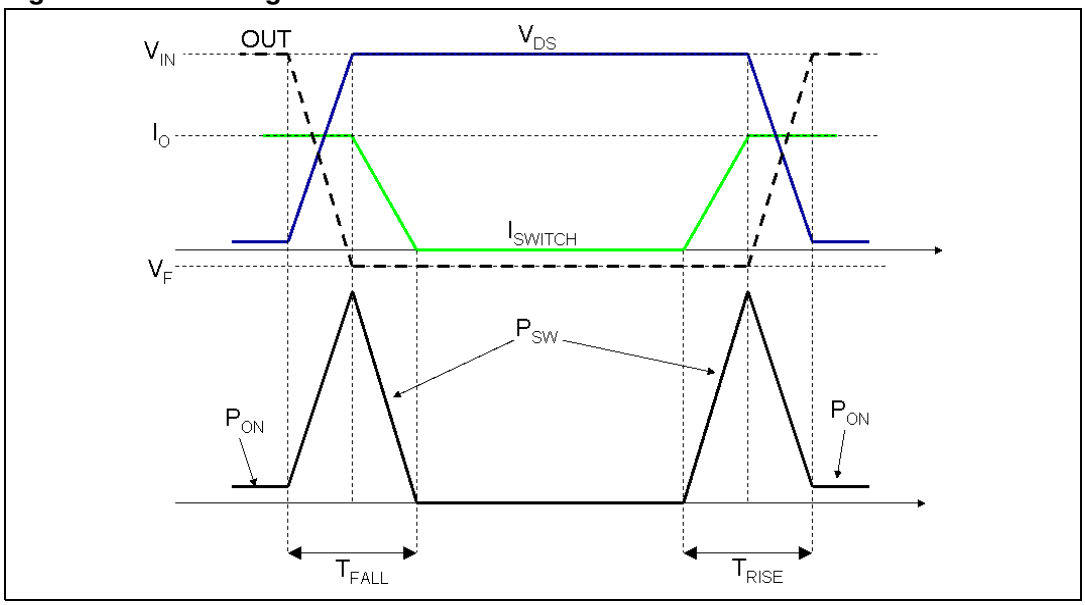
$$T_J = T_A + Rth_{JA} \cdot P_{TOT}$$

Where T_A is the ambient temperature and P_{TOT} is the sum of the power losses just seen.

Rth_{JA} is the equivalent thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junction to the ambient. For this device the path through the exposed pad is the one conducting the largest amount

of heat. The Rth_{JA} measured on the demonstration board described in the following paragraph is about 60 °C/W for the VFQFPN package and about 40 °C/W for the HSOP package.

Figure 16. Switching losses



6.6 Layout considerations

The PC board layout of switching DC/DC regulator is very important to minimize the noise injected in high impedance nodes and interferences generated by the high switching current loops.

In a step down converter the input loop (including the input capacitor, the power MOSFET and the free wheeling diode) is the most critical one. This is due to the fact that the high value pulsed current are flowing through it. In order to minimize the EMI, this loop has to be as short as possible.

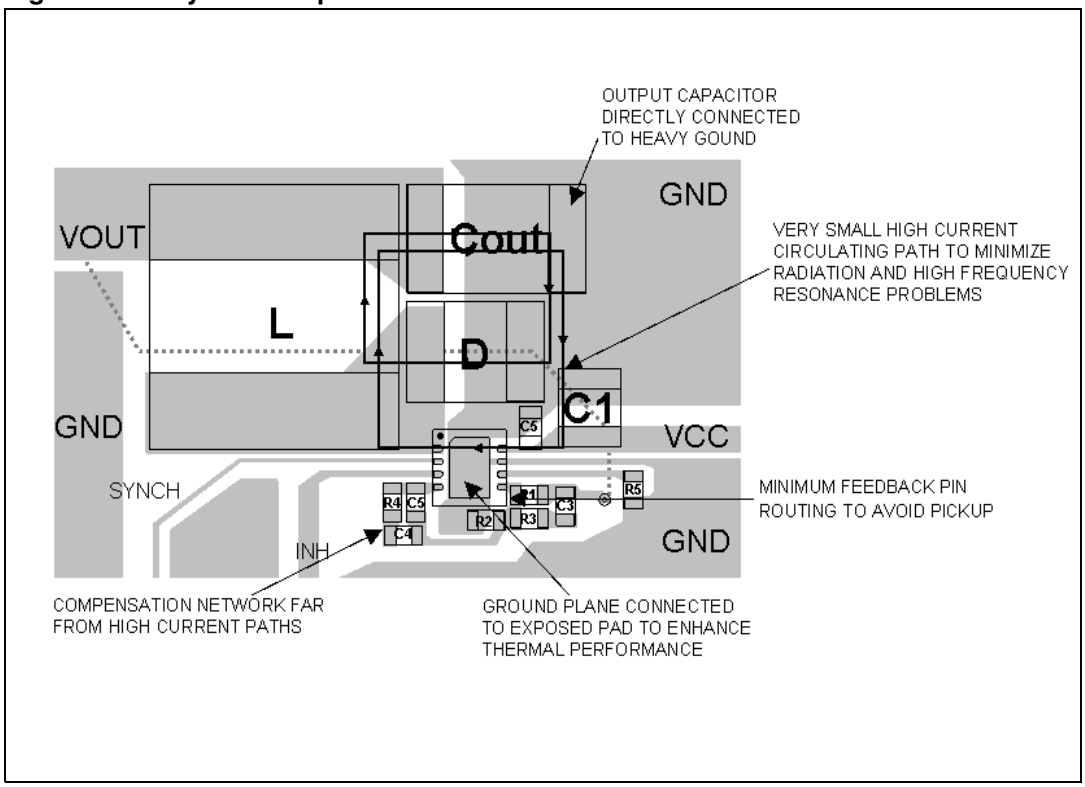
The feedback pin (FB) connection to external resistor divider is a high impedance node, so the interferences can be minimized placing the routing of feedback node as far as possible from the high current paths. To reduce the pick up noise the resistor divider has to be placed very close to the device.

To filter the high frequency noise, a small capacitor (220 nF) can be added as close as possible to the input voltage pin of the device.

Thanks to the exposed pad of the device, the ground plane helps to reduce the thermal resistance junction to ambient; so a large ground plane enhances the thermal performance of the converter allowing high power conversion.

In *Figure 17* a layout example is shown.

Figure 17. Layout example



6.7 Application circuit

In *Figure 18* the demonstration board application circuit is shown.

Figure 18. Demonstration board application circuit

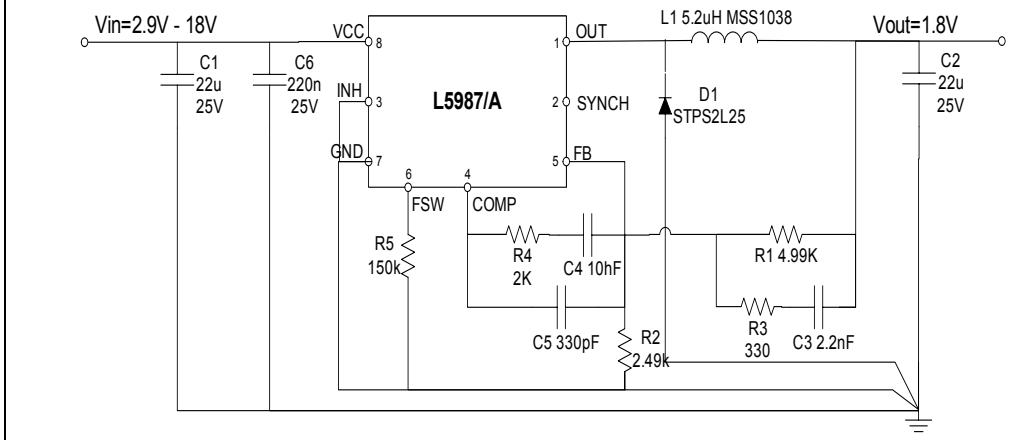


Table 9. Component list

Reference	Part number	Description	Manufacturer
C1	GRM32ER61E226KE15	22µF, 25V	Murata
C2	GRM32ER61E226KE15	22µF, 25V	Murata
C3		2.2nF, 50V	
C4		10nF, 50V	
C5		330pF, 50V	
C6		220nF, 25V	
R1		4.99 kΩ, 1%, 0.1W 0603	
R2		2.49kΩ, 1%, 0.1W 0603	
R3		330 Ω, 1%, 0.1W 0603	
R4		2 kΩ, 1%, 0.1W 0603	
R5		100k.	
D1	STPS2L25V	2A DC, 25V	STMicroelectronics
L1	MSS1038-522NL	5.2µH, 30%, 5.28A, DCR_{MAX}=22mΩ	Coilcraft

Figure 19. PCB layout: L5987 and L5987A (component side)

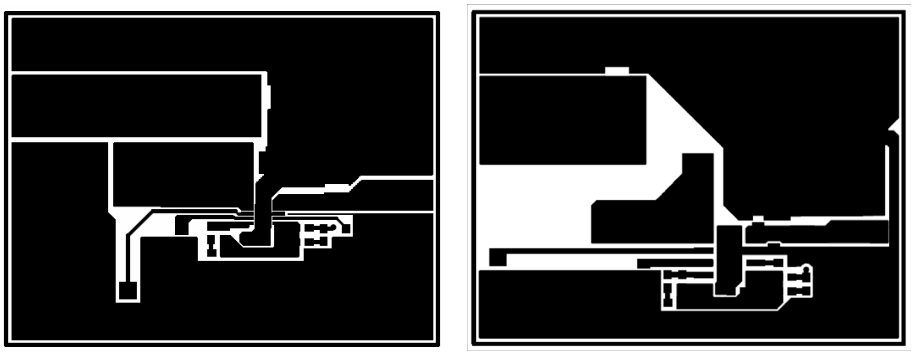


Figure 20. PCB layout: L5987 and L5987A (bottom side)

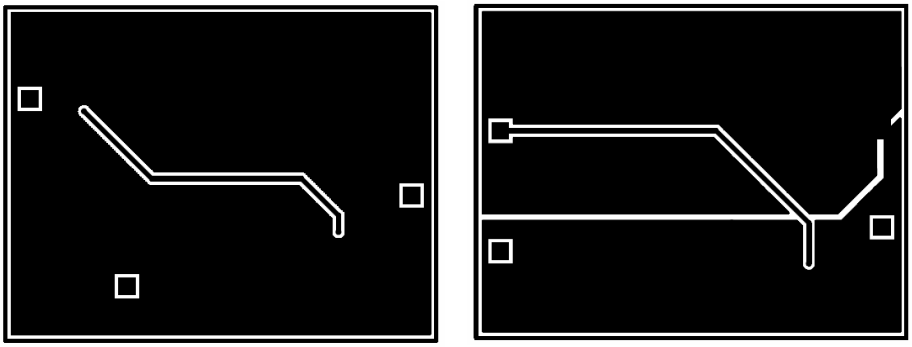


Figure 21. PCB layout: L5987 and L5987A (front side)

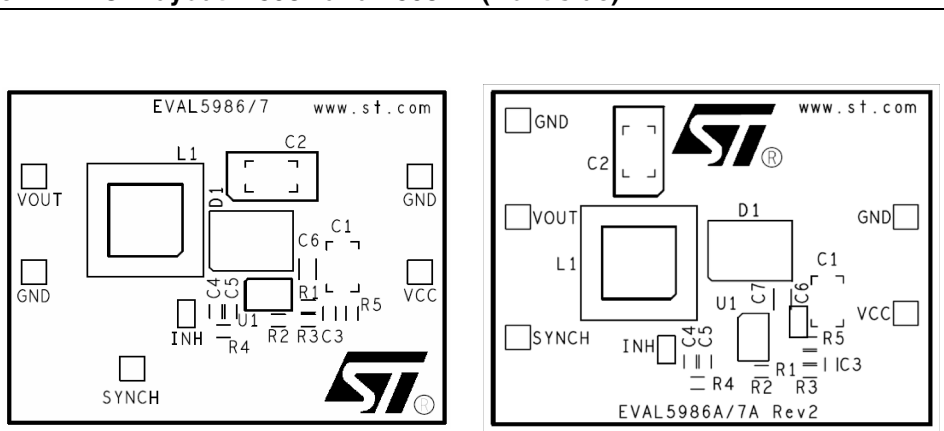


Figure 22. Junction temperature vs output current

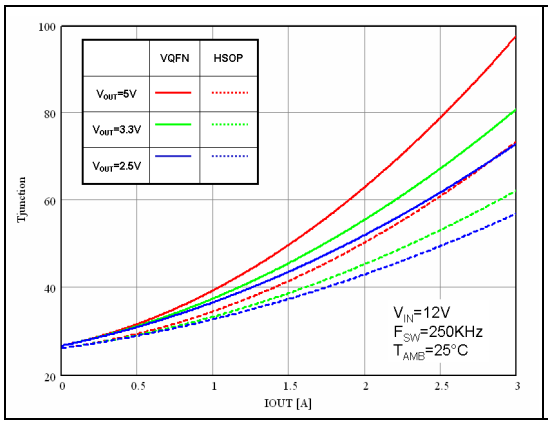


Figure 23. Junction temperature vs output current

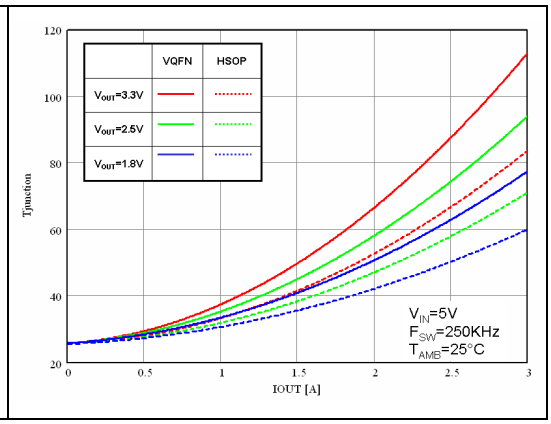


Figure 24. Junction temperature vs output current

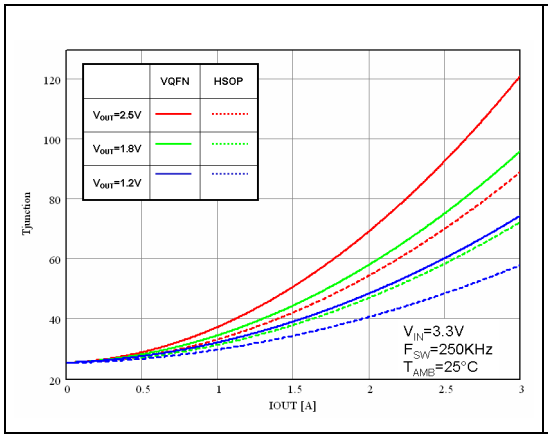


Figure 25. Efficiency vs output current

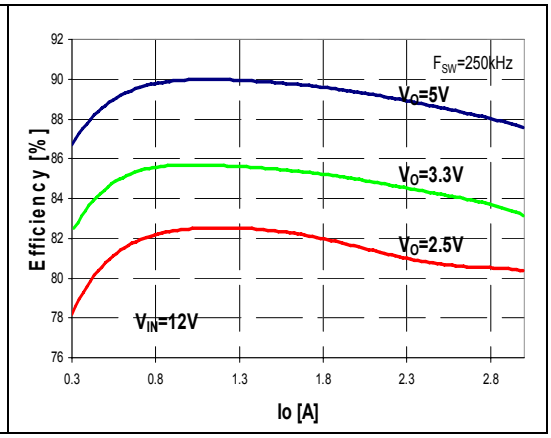


Figure 26. Efficiency vs output current

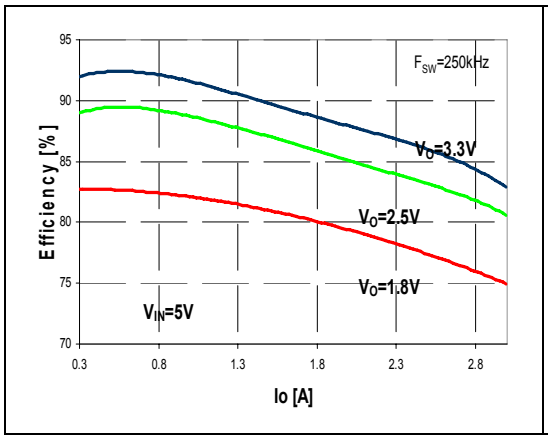


Figure 27. Efficiency vs output current

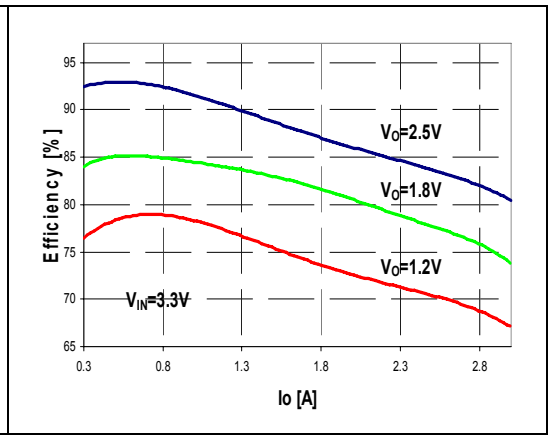


Figure 28. Load regulation

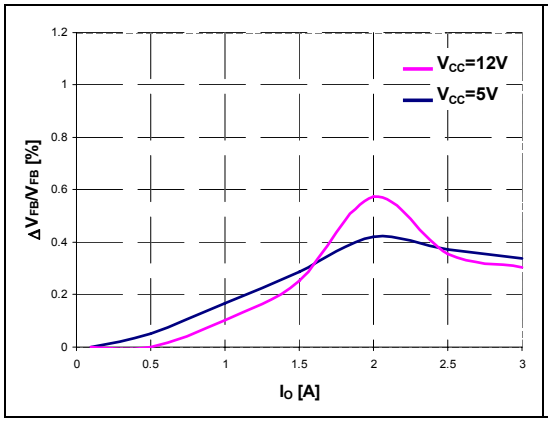


Figure 29. Line regulation

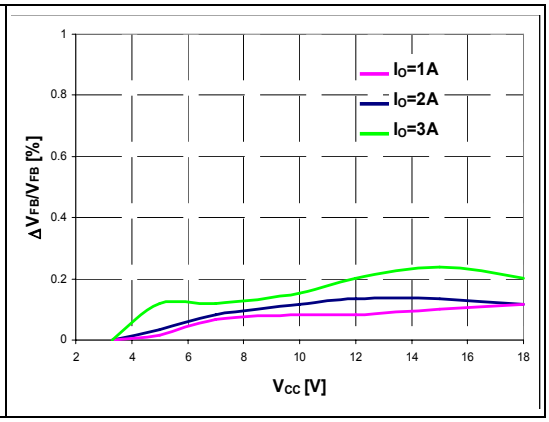


Figure 30. Load transient: from 0.4 A to 3 A

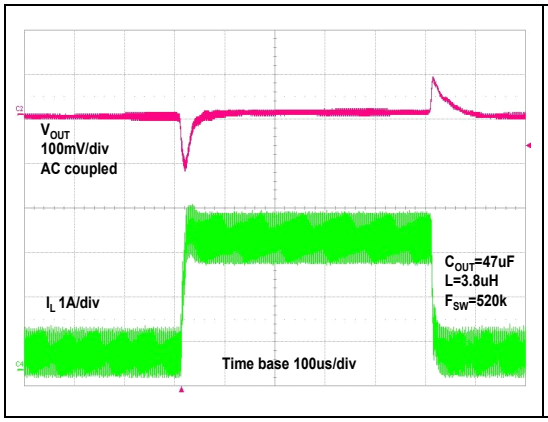


Figure 31. Soft-start

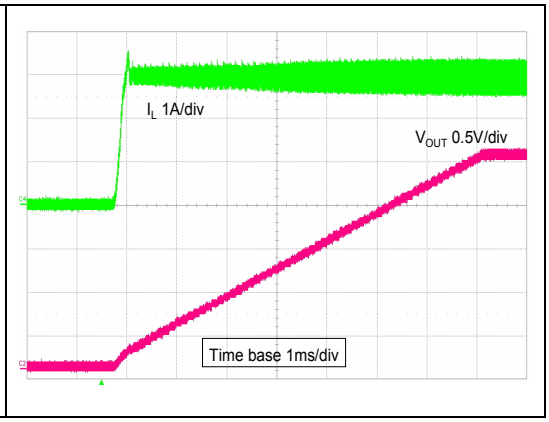
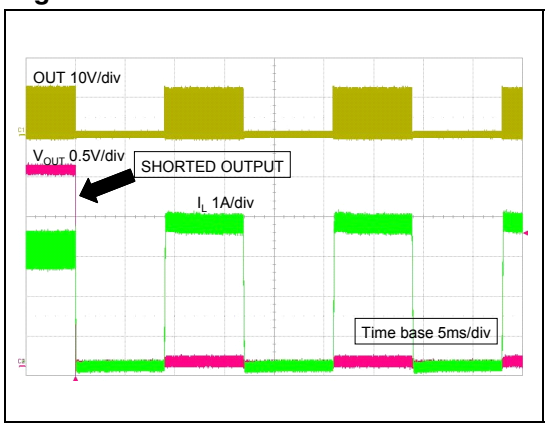


Figure 32. Short-circuit behavior



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of the second level interconnect is marked on the package and on the inner box label, in compliance with the JEDEC Standard JESD97. The maximum ratings related to soldering condition are also marked on the inner box label. ECOPACK® is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 10. VFQFPN8 (3x3x1.08 mm) mechanical data

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1		0.02	0.05		0.0008	0.0020
A2		0.70			0.0276	
A3		0.20			0.0079	
b	0.18	0.23	0.30	0.0071	0.0091	0.0118
D	2.95	3.00	3.05	0.1161	0.1181	0.1200
D2	2.23	2.38	2.48	0.0878	0.0937	0.0976
E	2.95	3.00	3.05	0.1161	0.1181	0.1200
E2	1.65	1.70	1.75	0.0649	0.0669	0.0689
e		0.50			0.0197	
L	0.35	0.40	0.45	0.0137	0.0157	0.0177
ddd			0.08			0.0031

Figure 33. Package dimensions

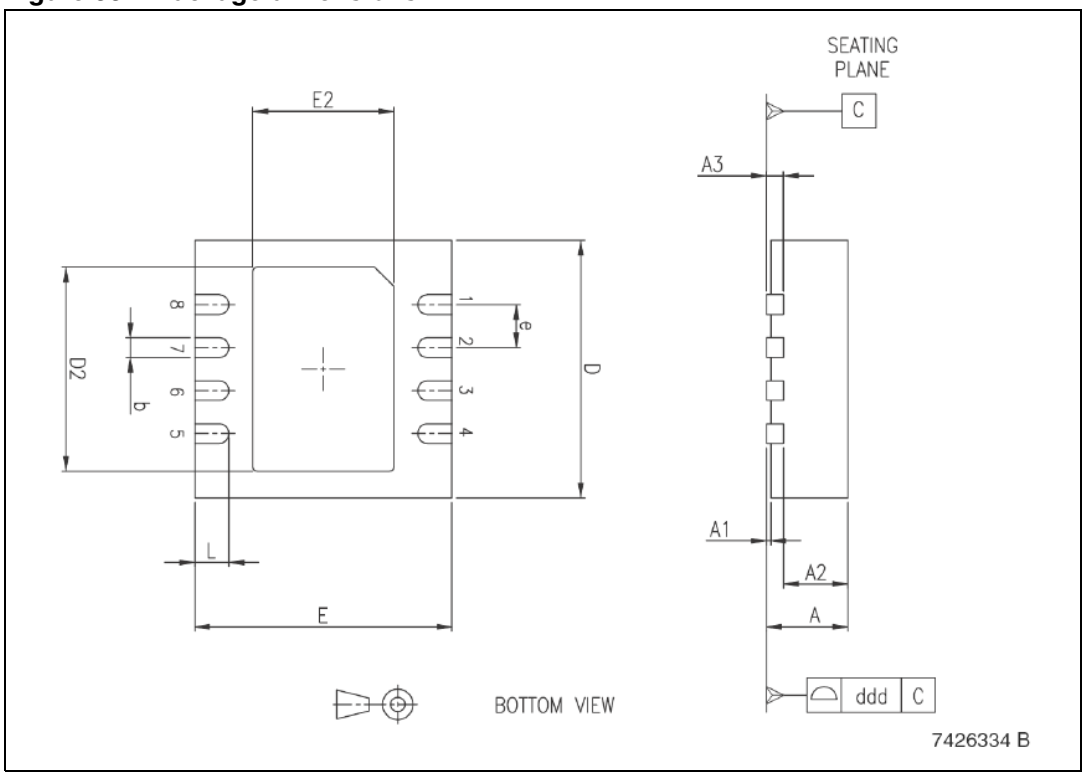
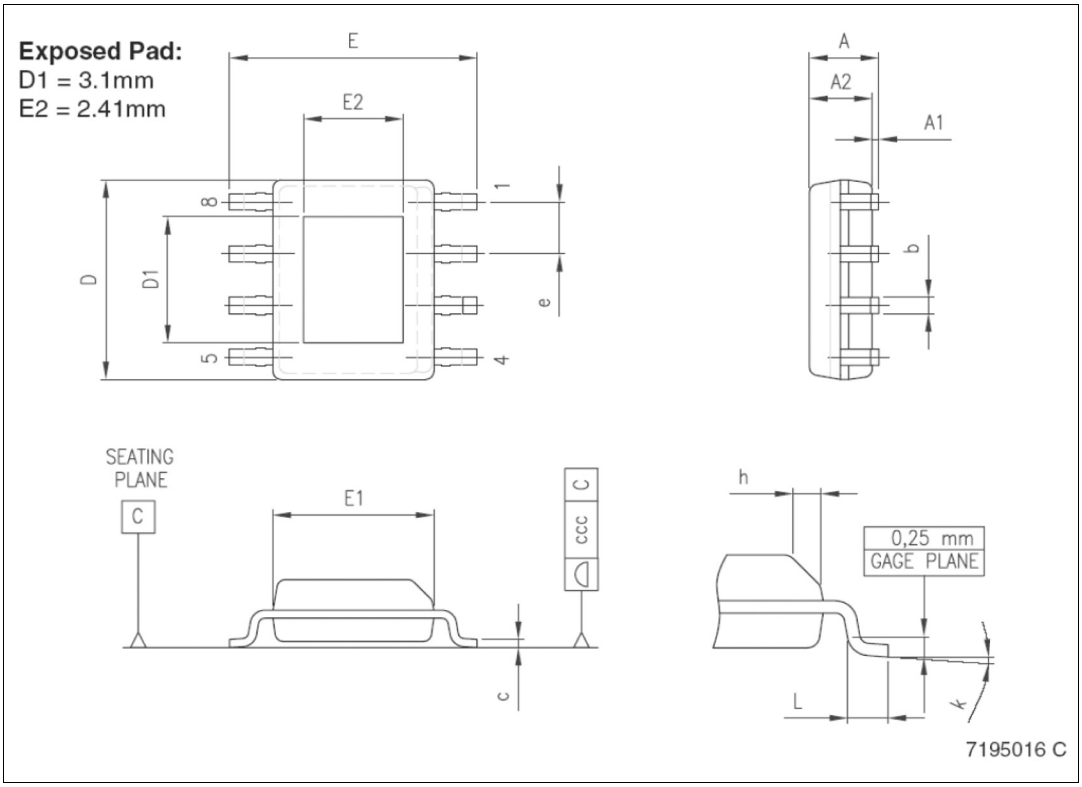


Table 11. HSOP8 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.70			0.0669
A1	0.00		0.15		0.00	0.0059
A2	1.25			0.0492		
b	0.31		0.51	0.0122		0.0201
c	0.17		0.25	0.0067		0.0098
D	4.80	4.90	5.00	0.1890	0.1929	0.1969
E	5.80	6.00	6.20	0.2283		0.2441
E1	3.80	3.90	4.00	0.1496		0.1575
e		1.27				
h	0.25		0.50	0.0098		0.0197
L	0.40		1.27	0.0157		0.0500
k	0		8			0.3150
ccc			0.10			0.0039

Figure 34. Package dimensions



8 Order codes

Table 12. Order codes

Order codes	Package	Packaging
L5987	VFQFPN8	Tube
L5987A	HSOP8	
L5987TR	VFQFPN8	Tape and reel
L5987ATR	HSOP8	

9 Revision history

Table 13. Document revision history

Date	Revision	Changes
29-Aug-2008	1	Initial release

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