



L5150CJ L5150CS

5 V low dropout voltage regulator

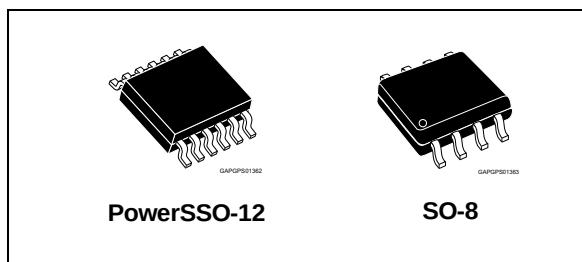
Datasheet — production data

Features

Max DC supply voltage	V_S	40 V
Max output voltage tolerance	ΔV_O	+/-2%
Max dropout voltage	V_{dp}	500 mV
Output current	I_O	150 mA
Quiescent current	I_{qn}	55 $\mu A^{(1)}$

1. Typical value

- Operating DC supply voltage range
5.6 V to 40 V
- Low dropout voltage
- Low quiescent current consumption
- Precision output voltage 5 V +/- 2%
- Reset circuit sensing the output voltage
- Programmable reset pulse delay with external capacitor
- Adjustable reset threshold
- Early warning
- Very wide stability range with low value output capacitor
- Thermal shutdown and short-circuit protection
- Wide temperature range ($T_j = -40\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$)



Description

L5150CJ and L5150CS are low dropout linear regulators with microprocessor control functions such as power on reset, low voltage reset, early warning.

Typical quiescent current is 55 μA at very low output current.

On chip trimming results in high output voltage accuracy (2%). Accuracy is kept over wide temperature range, line and load variation. Early warning circuit monitors the input voltage and compares it with an internal voltage reference.

Output voltage reset threshold can be adjusted down to 3.5 V by means of an external voltage divider.

The maximum input voltage is 40 V. The max output current is internally limited. Internal temperature protection disables the voltage regulator output. In addition, only low-value ceramic capacitor on output is required for stability.

Table 1. Device summary

Package	Order codes	
	Tube	Tape & reel
PowerSSO-12	L5150CJ	L5150CJTR
SO-8	L5150CS	L5150CSTR

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1 Block diagram and pins description

Figure 1. Block diagram

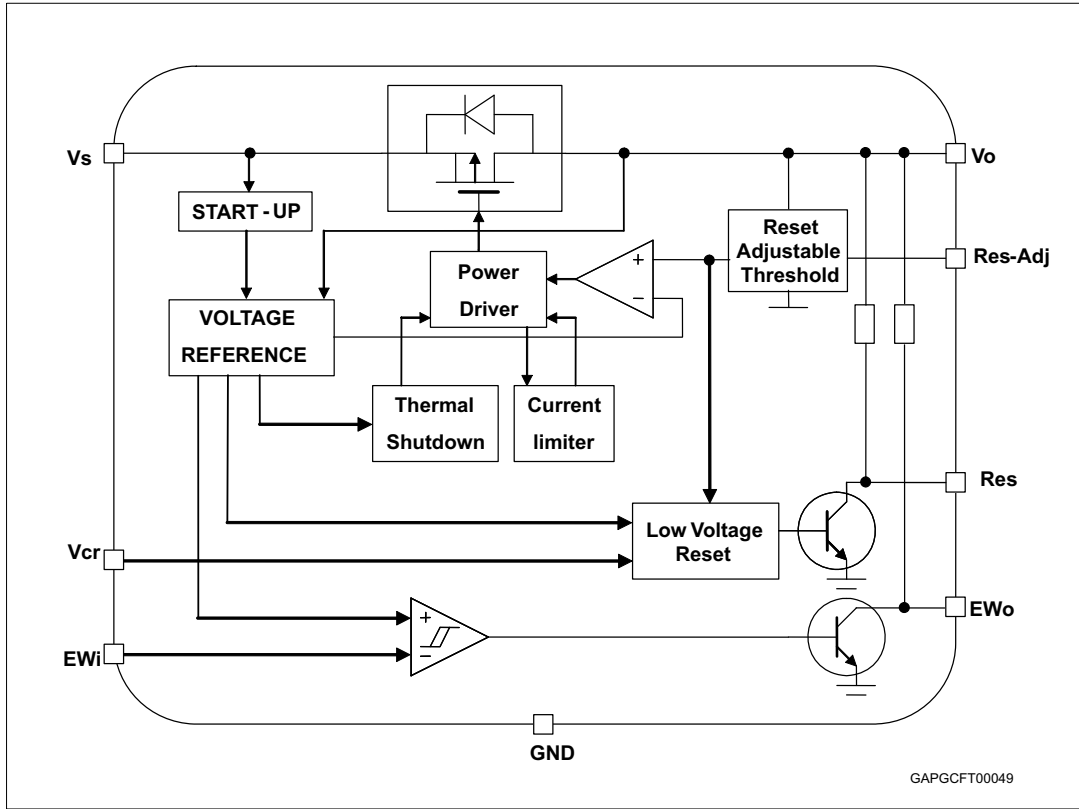


Figure 2. Configuration diagram (top view)

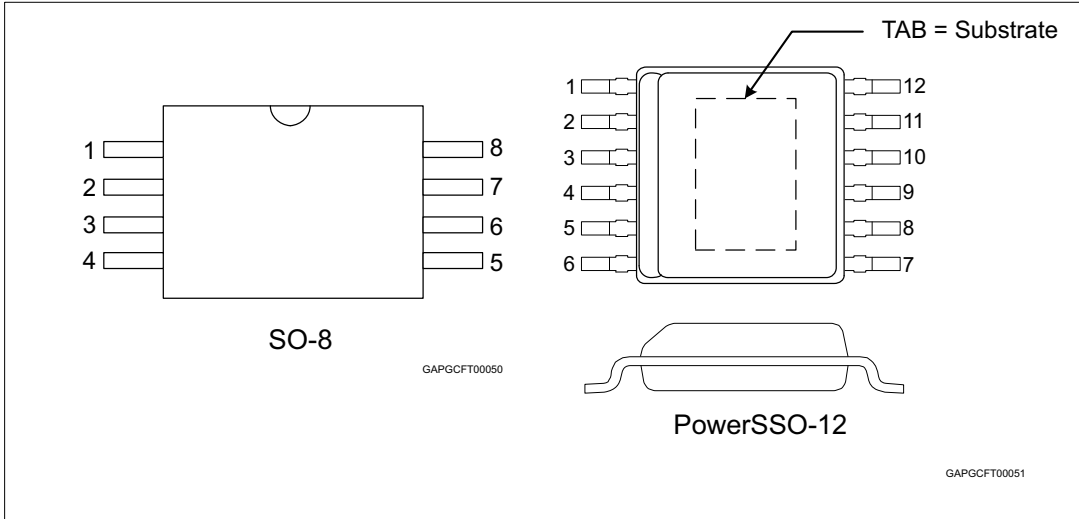


Table 2. Pins description

Pin name	PowerSSO-12 pin #	SO-8 pin #	Function
R_{es_Adj}	1	8	Reset adjustable threshold. Connected to an appropriate external voltage divider, it allows to properly set the reset threshold down to 3.5 V. Connect to GND if not needed.
R_{es}	2	1	Reset output. Internally connected to V_o through a 20 K Ω pull up resistor. This pin is pulled low when $V_o < V_{o_th}$. Keep open if not needed.
V_{cr}	3	2	Reset delay. Connect an external capacitor between V_{cr} pin and ground to adjust the reset delay time. Keep open if not needed.
GND	4	3	Ground reference.
NC	5, 11, 8, 9	-	Not connected.
V_o	6	4	5 V regulated output. Block to GND with a ceramic capacitor ($C_o \geq 220$ nF for regulator stability).
V_S	7	5	Supply voltage, block directly to GND on the IC with a capacitor.
EW_i	10	6	Early warning input. This pin monitors the V_S voltage level through a resistor divider. Connect to V_S if not needed.
EW_o	12	7	Early warning output. Internally connected to V_o through 20 K Ω pull up resistor. This pin is pulled low when EW_i is below bandgap reference voltage. Keep open if not needed.
TAB	-	-	TAB is connected to the substrate of the chip: connect to GND or leave open (see Figure 2 for PowerSSO-12 only).

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the [Table 3: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{sdc}	DC supply voltage	-0.3 to 40	V
I _{sdc}	Input current	internally limited	
V _{odc}	DC output voltage	-0.3 to 6	V
I _{odc}	DC output current	internally limited	
V _{od Res}	Open drain output voltage R _{es}	-0.3 to V _{odc} + 0.3	V
I _{od Res}	Open drain output current R _{es}	internally limited	
V _{Res_adj}	V _{Res_adj} voltage	-0.3 to V _{odc} + 0.3	V
V _{od EW₀}	Open drain output voltage EW ₀	-0.3 to V _{odc} + 0.3	V
I _{od EW₀}	Open drain output current EW ₀	internally limited	
V _{cr}	V _{cr} voltage	-0.3 to V _o + 0.3	V
V _{EWi}	Early warning input voltage	-0.3 to 40	V
T _j	Junction temperature	-40 to 150	°C
V _{ESD HBM}	ESD HBM voltage level (HBM-MIL STD 883C)	+/- 2	kV
V _{ESD CDM}	ESD CDM voltage level (CDM-)	+/- 750	V

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value		Unit
		PowerSSO-12	SO-8	
$R_{thj-case}$	Thermal resistance junction to case:	8		°K/W
$R_{thj-lead}$	Thermal resistance junction to lead:		40	°K/W
$R_{thj-amb}^{(1)}$	Thermal resistance junction to ambient:	52	112	°K/W

1. **PowerSSO-12:** The values quoted are for PCB 77 mm x 86 mm x 1.6 mm, FR4, double copper layer with single heatsink layer, copper thickness 70 µm, thermal vias, copper area 2 cm².
SO-8: The values quoted are for PCB 48 mm x 48 mm x 2 mm, FR4, double copper layer with single heatsink layer, copper thickness 35 µm, copper area 2 cm².

2.3 Electrical characteristics

Values specified in this section are for $V_S = 5.6\text{ V}$ to 31 V , $T_j = -40\text{ °C}$ to $+150\text{ °C}$ unless otherwise stated.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_O	V_{O_ref}	Output voltage	$V_S = 8\text{ V}$ to 18 V $I_O = 8\text{ mA}$ to 150 mA	4.9	5.0	5.1	V
V_O	V_{O_ref}	Output voltage	$V_S = 5.6\text{ V}$ to 31 V $I_O = 8\text{ mA}$ to 150 mA	4.85	5.0	5.15	V
V_O	V_{O_ref}	Output voltage	$V_S = 5.6\text{ V}$ to 31 V $I_O = 0.1\text{ mA}$ to 8 mA	4.75	5.0	5.25	V
V_O	I_{short}	Short-circuit current	$V_S = 13.5\text{ V}$	0.65	0.95	1.25	A
V_O	I_{lim}	Output current capability ⁽¹⁾	$V_S = 13.5\text{ V}$	280	470	660	mA
V_S, V_O	V_{line}	Line regulation voltage	$V_S = 6\text{ V}$ to 28 V $I_O = 30\text{ mA}$			40	mV
V_O	V_{load}	Load regulation voltage	$V_S = 8\text{ V}$ to 18 V , $I_O = 8\text{ mA}$ to 150 mA			55	mV
			$V_S = 13.5\text{ V}$, $T_j = 25\text{ °C}$ $I_O = 8\text{ mA}$ to 150 mA			40	
V_S, V_O	V_{dp}	Drop voltage ⁽²⁾	$I_O = 150\text{ mA}$			500	mV
V_S, V_O	SVR	Ripple rejection	$f_r = 100\text{ Hz}^{(3)}$		60		dB
V_O	I_{Oth_H}	Normal consumption mode output current	$V_S = 8\text{ V}$ to 18 V	8			mA
V_O	I_{Oth_L}	Very low consumption mode output current	$V_S = 8\text{ V}$ to 18 V			1.1	mA
V_O	I_{Oth_Hyst}	Output current switching threshold hysteresis	$V_S = 13.5\text{ V}$ $T_j = 25\text{ °C}$		0.8		mA

Table 5. General (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S, V_O	I_{qn_1}	Current consumption $I_{qn_1} = I_{VS} - I_O$	$V_S = 13.5\text{ V}$, $I_O = 0.1\text{ mA to }1\text{ mA}$, $T_j = 25\text{ °C}$		55	80	μA
			$V_S = 13.5\text{ V}$, $I_O = 0.1\text{ mA to }1\text{ mA}$,			95	
V_S, V_O	I_{qn_150}	Current consumption $I_{qn_150} = I_{VS} - I_O$	$V_S = 13.5\text{ V}$ $I_O = 150\text{ mA}$		3	4.2	mA
	T_w	Thermal protection temperature		150		190	$^{\circ}\text{C}$
	T_{w_hy}	Thermal protection temperature hysteresis			10		$^{\circ}\text{C}$

1. Measured Output Current when the output voltage has dropped 100 mV from its nominal Value obtained at 13.5 V and $I_O = 75\text{ mA}$.
2. $V_S - V_O$ Measured Dropout when the output voltage has dropped 100 mV from its nominal Value obtained at 13.5 V and $I_O = 75\text{ mA}$.
3. Guaranteed by design.

Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{es}	V_{res_l}	Reset output low voltage	$R_{ext} = 5\text{ k}\Omega$ $V_O > 1\text{ V}$			0.4	V
R_{es}	I_{Res_lkg}	Reset output high leakage current	$V_{Res} = 5\text{ V}$			1	μA
R_{es}	R_{Res}	Pull up internal resistance	Versus V_O	10	20	40	$\text{k}\Omega$
R_{es}	V_{O_th}	V_O out of regulation threshold	$V_{res_adj} < 0.2\text{ V}$, V_O decreasing	6	8	10	% Below V_{O_ref}
R_{es_adj}	V_{res_adj}	Reset adjustable switching threshold		2.35	2.5	2.65	V
R_{es_adj}	V_{Res_adjl}	Reset adjustable low voltage		0.4	0.9	1.3	V
R_{es_adj}	$I_{Res_adj_lkg}$	Reset adjustable leakage current	$V_{res_adj} = 2.5\text{ V}$	-1		1	μA
V_{cr}	V_{Rlth}	Reset timing low threshold	$V_S = 13.5\text{ V}$	15	18	22	% V_{O_ref}
V_{cr}	V_{Rhth}	Reset timing high threshold	$V_S = 13.5\text{ V}$	47	50	53	% V_{O_ref}
V_{cr}	I_{cr}	Charge current	$V_S = 13.5\text{ V}$	10	20	30	μA
V_{cr}	I_{dr}	Discharge current	$V_S = 13.5\text{ V}$	10	20	30	μA

Table 6. Reset (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R _{es}	T _{rr}	Reset reaction time				2	μs
R _{es}	T _{rd}	Reset delay time	V _S = 13.5 V; C _{tr} = 1000 pF	2	4	11	ms

Table 7. Early warning

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
EW _i	V _{EWi_thl}	EW input low threshold voltage		2.35	2.50	2.65	V
EW _i	V _{EWi_thh}	EW input high threshold voltage		2.42	2.57	2.72	V
EW _i	V _{EWi_thhyst}	EW input threshold hysteresis			70		mV
EW _i	I _{EWi_lkg}	EW input leakage current	V _{EWi} = 2.5 V, V _S > 4 V	-1		1	μA
EW _o	R _{EWo}	Pull up internal resistance	Versus V _o	10	20	40	kΩ
EW _o	V _{EWo_lv}	EW output low voltage (with external pull up)	V _{EWi} < 2.35 V; V _S > 4 V; R _{ext} = 5 kΩ			0.4	V
EW _o	I _{EWo_lkg}	EW output leakage current	V _{EWo} = 5 V			1	μA

2.4 Electrical characteristics curves

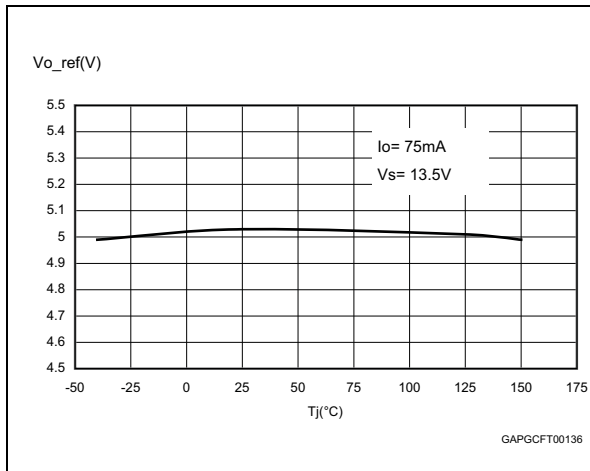
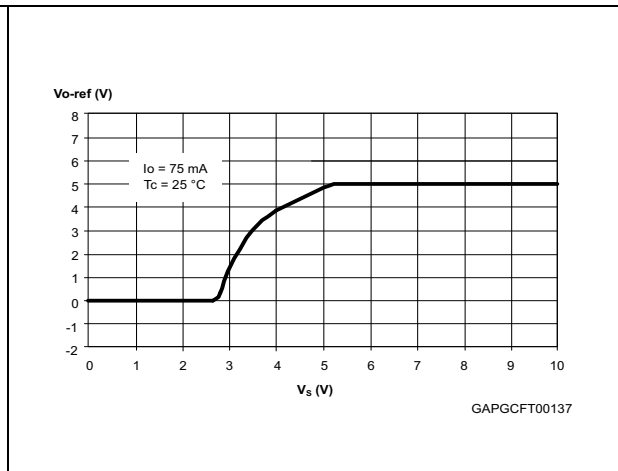
Figure 3. Output voltage vs. T_j Figure 4. Output voltage vs. V_S 

Figure 5. Drop voltage vs. output current

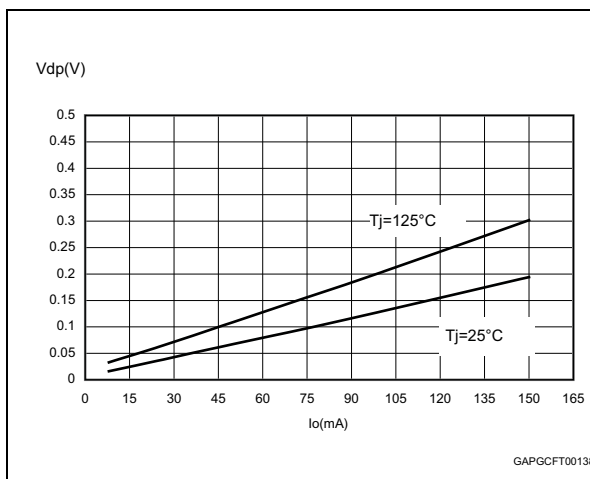


Figure 6. Current consumption vs. output current

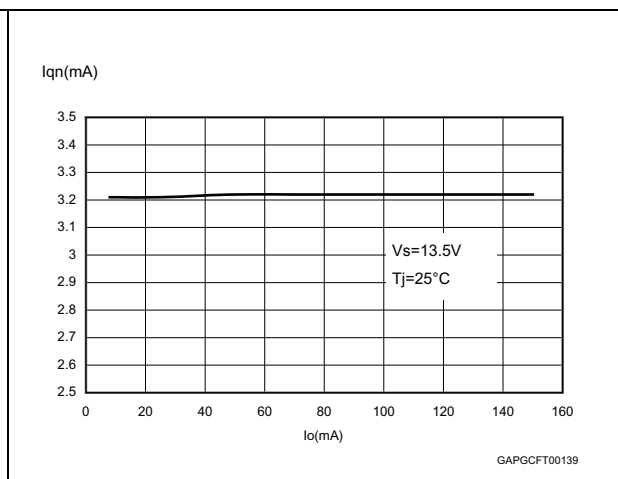


Figure 7. Current consumption vs. output current (at light load condition)

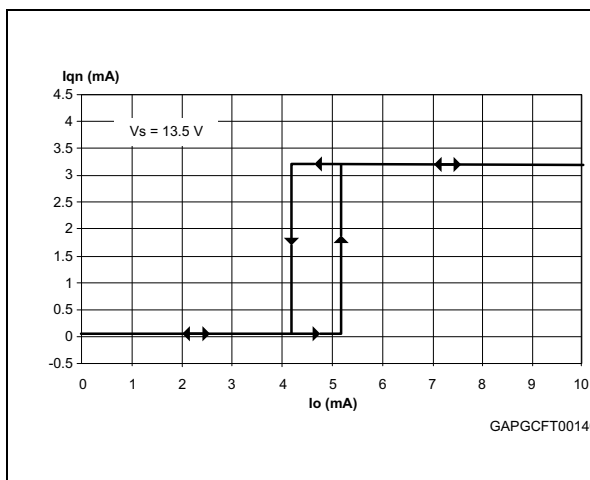
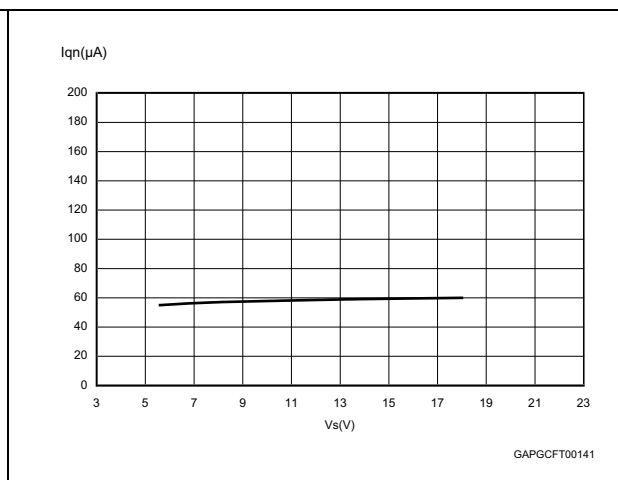
Figure 8. Current consumption vs. input voltage ($I_o = 0.1$ mA)

Figure 9. Current consumption vs. input voltage ($I_o = 75\text{ mA}$)

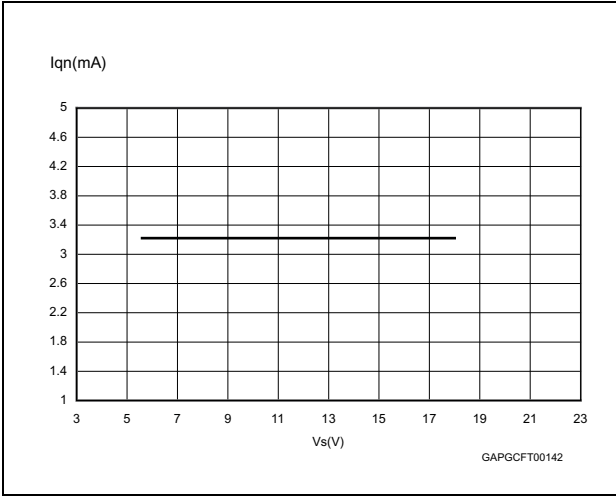


Figure 10. Current limitation vs. T_j

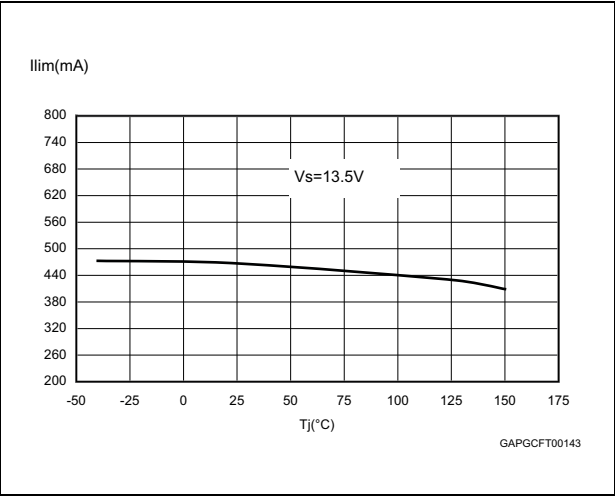


Figure 11. Current limitation vs. input voltage

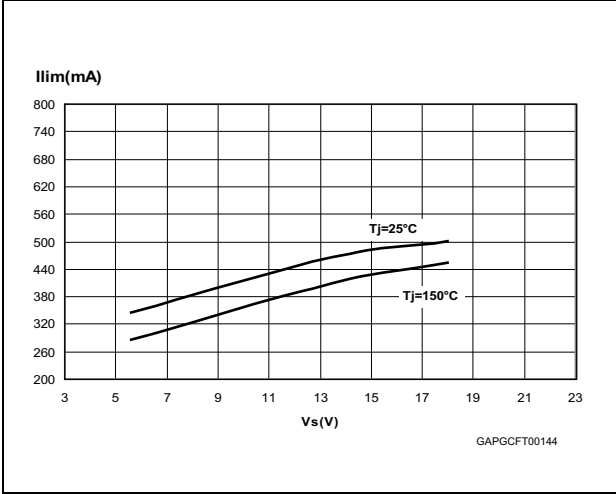


Figure 12. Short-circuit current vs. T_j

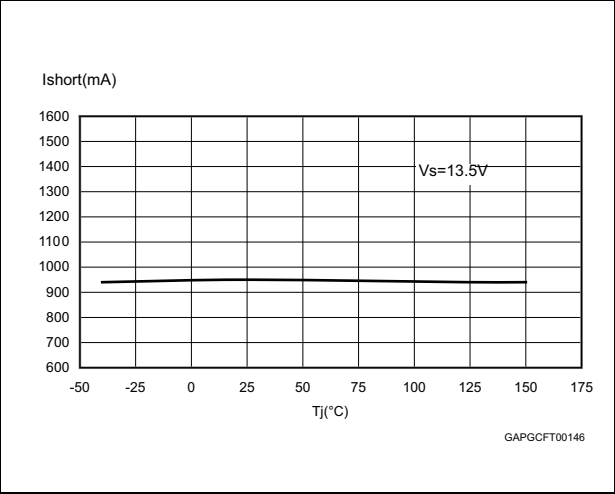


Figure 13. Short-circuit current vs. input voltage

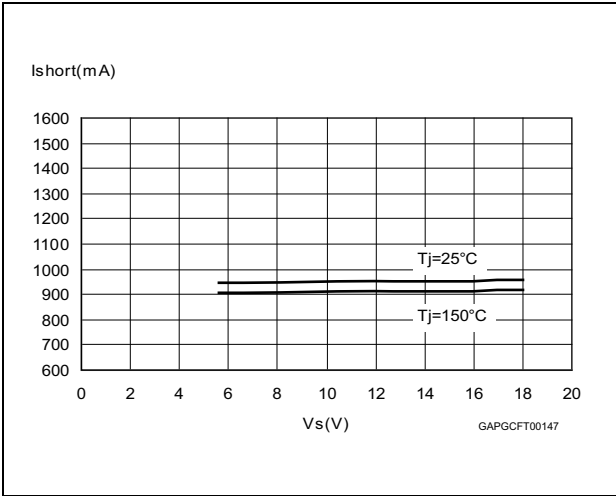


Figure 14. V_{Rhth} vs. T_j

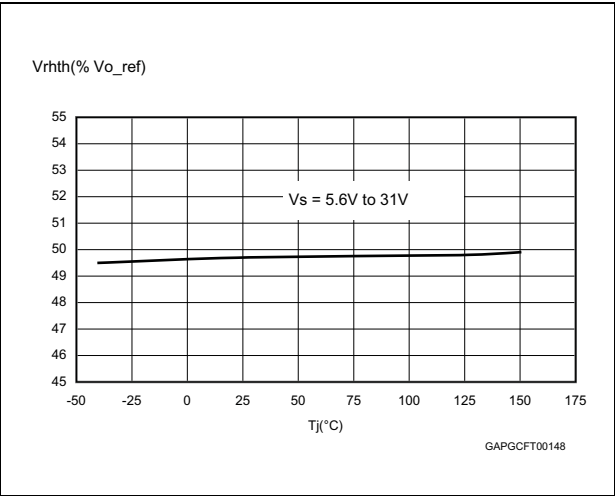


Figure 15. V_{Rth} vs. T_j

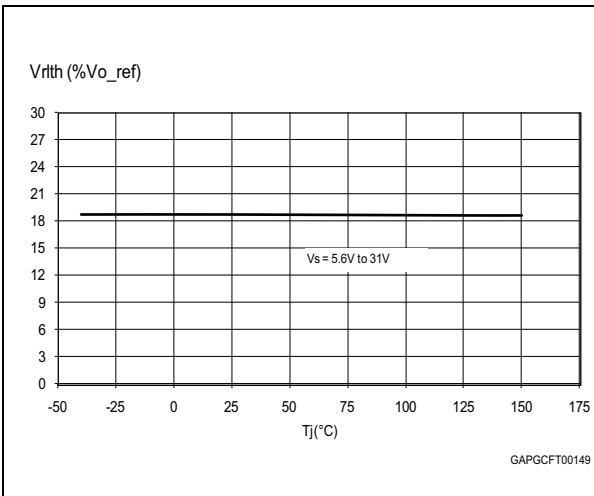


Figure 16. V_{EWi_thh} vs. T_j

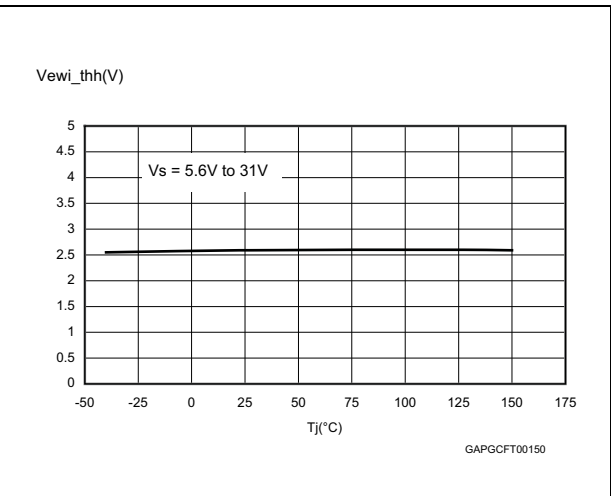


Figure 17. V_{EWi_thl} vs. T_j

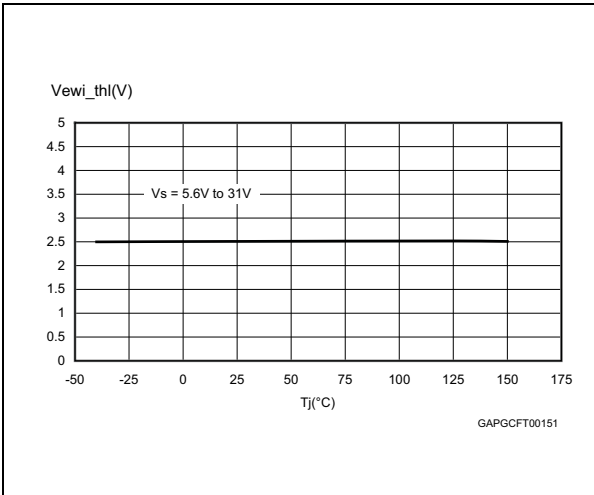


Figure 18. I_{cr} vs. T_j

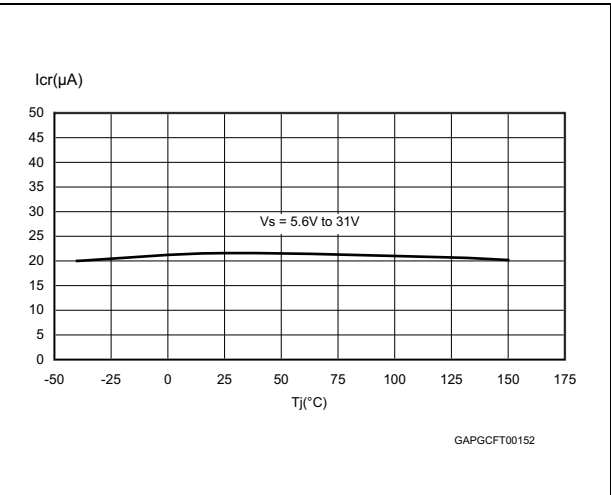


Figure 19. I_{dr} vs. T_j

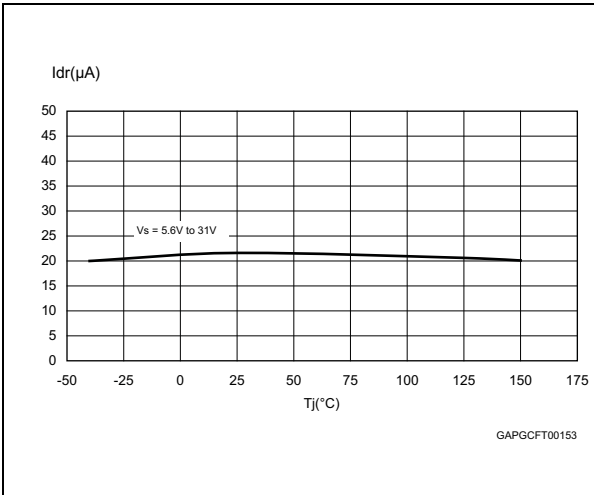
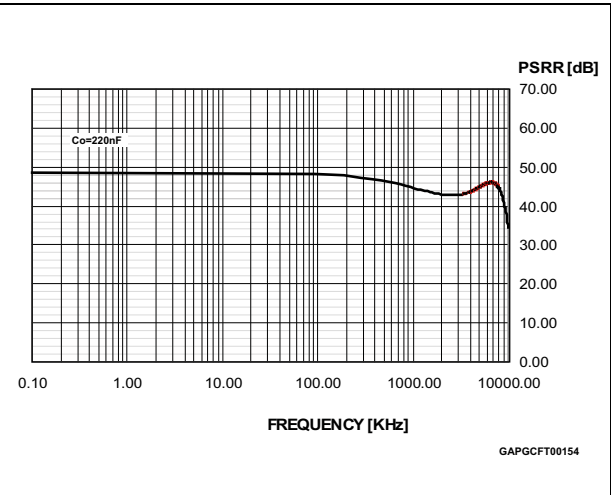


Figure 20. PSRR

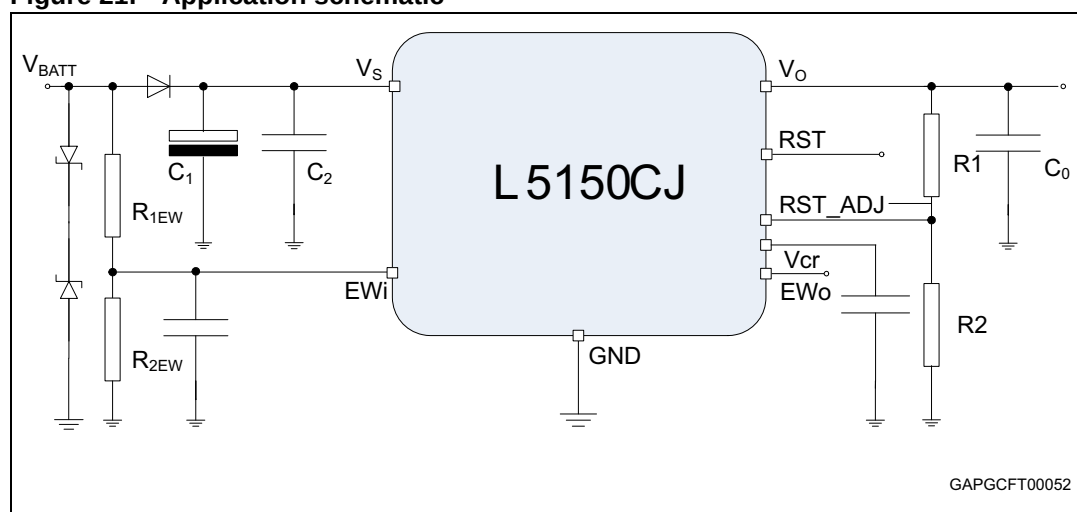


3 Application information

3.1 Voltage regulator

The voltage regulator uses a p-channel mos transistor as a regulating element. With this structure a very low dropout voltage at current up to 150 mA is obtained. The output voltage is regulated up to input supply voltage of 40 V. The high-precision of the output voltage (2%) is obtained with a pre-trimmed reference voltage. The voltage regulator automatically adapts its own quiescent current to the output current level. In light load conditions the quiescent current goes to 55 μ A only (low consumption mode). This procedure features a certain hysteresis on the output current (see [Figure 7](#)). Short-circuit protection to GND and a thermal shutdown are provided.

Figure 21. Application schematic



The input capacitor $C_1 \geq 100 \mu\text{F}$ is necessary as backup supply for negative pulses which may occur on the line. The second input capacitor $C_2 \geq 220 \text{ nF}$ is needed when the C_1 is too distant from the V_S pin and it compensates smooth line disturbances. The C_0 ceramic capacitor, connected to the output pin, is for bypassing to GND the high-frequency noise and it guarantees stability even during sudden line and load variations. Suggested value is $C_0 = 220 \text{ nF}$ with $\text{ESR} \geq 100 \text{ m}\Omega$.

Stability region is reported in [Figure 22](#).

Figure 22. Stability region

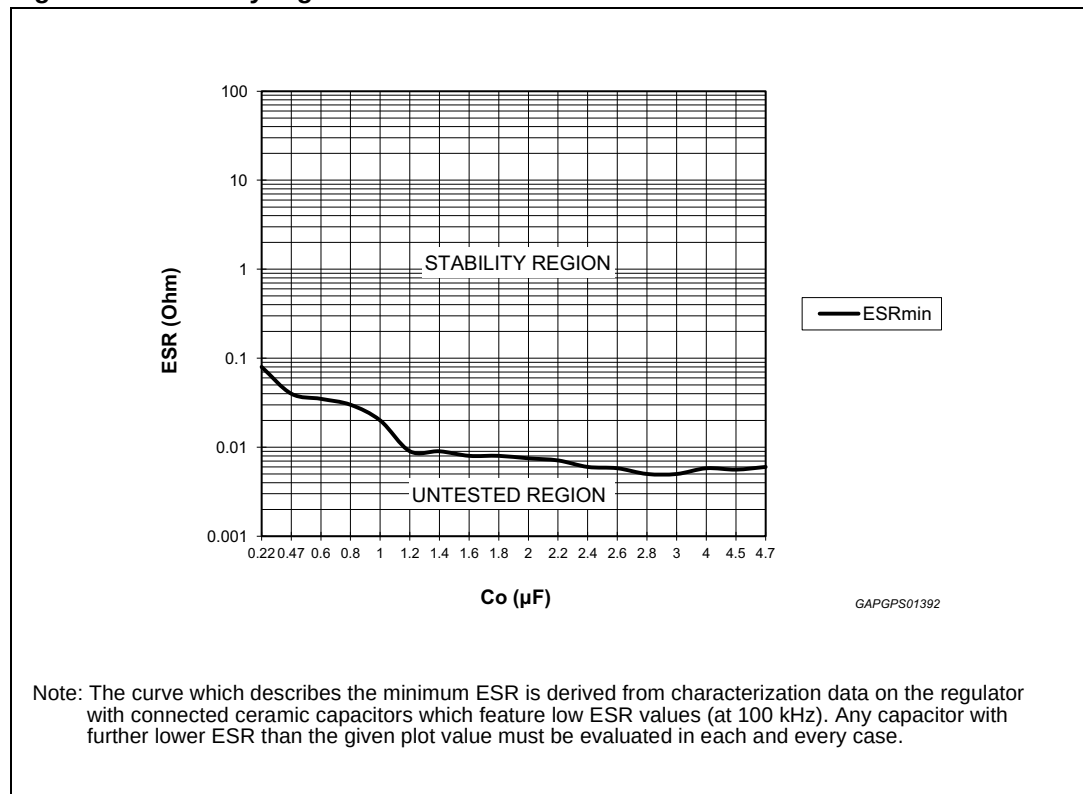
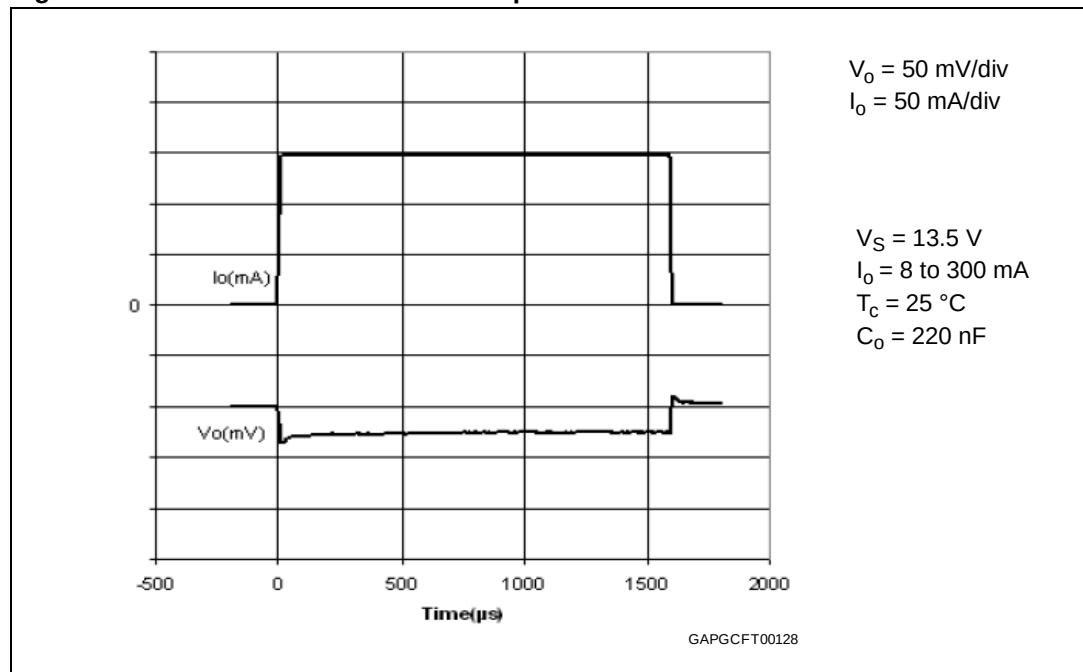


Figure 23. Maximum load variation response



3.2 Reset

The reset circuit monitors the output voltage V_o . If the output voltage becomes lower than V_{o_th} then R_{es} goes low with a delay time (t_{rr}). When the output voltage becomes higher than V_{o_th} then R_{es} goes high with a delay time t_{rd} . This delay is obtained by 32 periods of oscillator. The oscillator period is given by:

Equation 1

$$T_{osc} = [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{cr} + [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{dr}$$

where:

I_{cr} = 20 μ A is an internally generated charge current,

I_{dr} = 20 μ A is an internally generated discharge current,

V_{Rhth} = 2.5 V (typ) and V_{Rlth} = 0.9 V (typ) are two voltage thresholds,

C_{tr} is an external capacitor put between V_{cr} pin and GND.

Reset pulse delay T_{rd} is given by:

Equation 2

$$t_{rd} = 32 \times T_{osc}$$

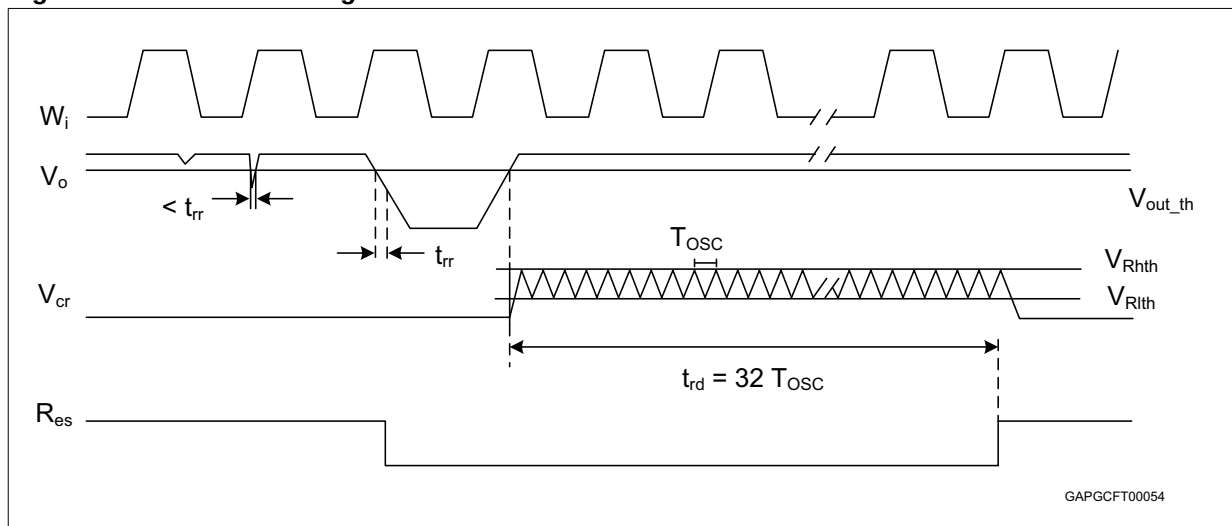
The Output Voltage Reset threshold can be adjusted via an external voltage divider $R_1 + R_2$ (R_1 connected between R_{es_Adj} and V_0 , R_2 connected between R_{es_Adj} and GND) according to the following formula:

Equation 3

$$V_{thre} = [(R_1 + R_2) / R_2] \times V_{Res_adj}$$

The Output Voltage Reset threshold can be decreased down to 3.5 V. If it is needed to maintain it to its default value (8% below V_{0_ref} typical), it is enough to connect the R_{es_Adj} pin directly to GND.

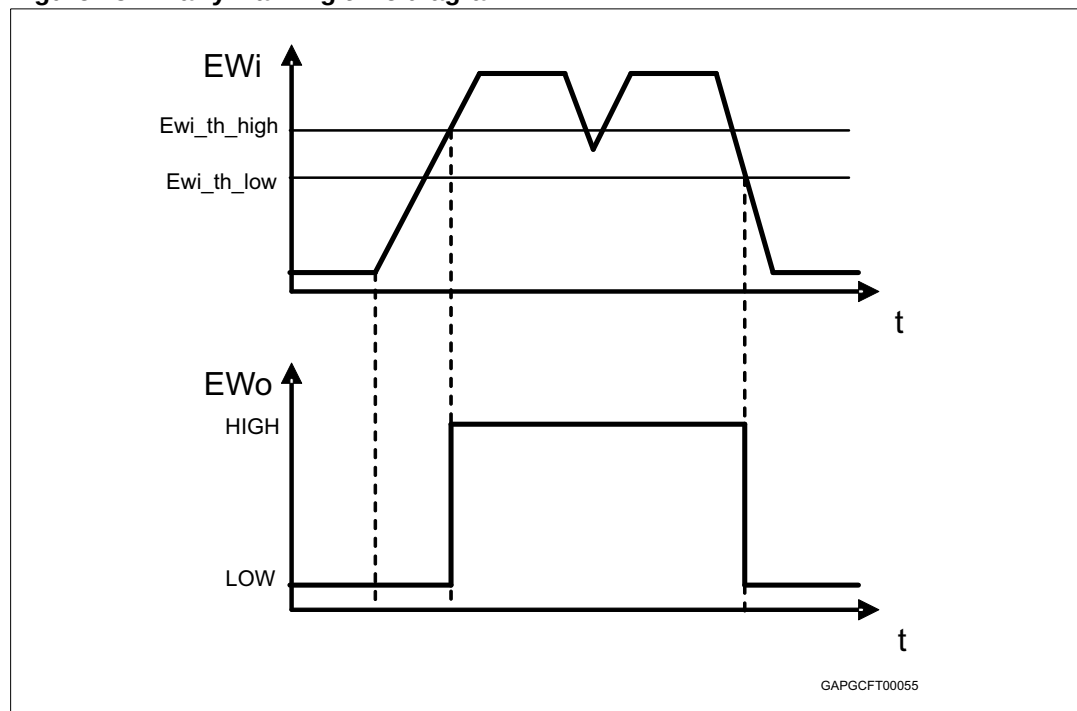
Figure 24. Reset time diagram



3.3 Early warning

This circuit compares the EW_i input signal with the internal voltage reference (typically 2.5 V). The use of an external voltage divider makes the comparator very flexible in the application. This function can be used to supervise the supply input voltage either before or after the protection diode and to give additional information to the microprocessor such as low voltage warnings.

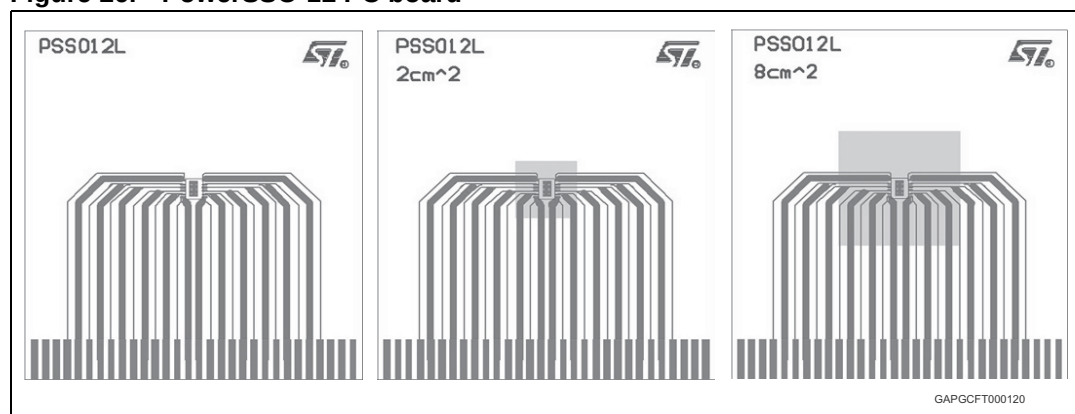
Figure 25. Early warning time diagram



4 Package and PCB thermal data

4.1 PowerSSO-12 thermal data

Figure 26. PowerSSO-12 PC board⁽¹⁾



1. Layout condition of R_{th} and Z_{th} measurements (PCB: double layer, thermal vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70 μ m (front and back side), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 25 μ m, footprint dimension 4.1 mm x 6.5 mm).

Figure 27. $R_{thi-amb}$ vs PCB copper area in open box free air condition

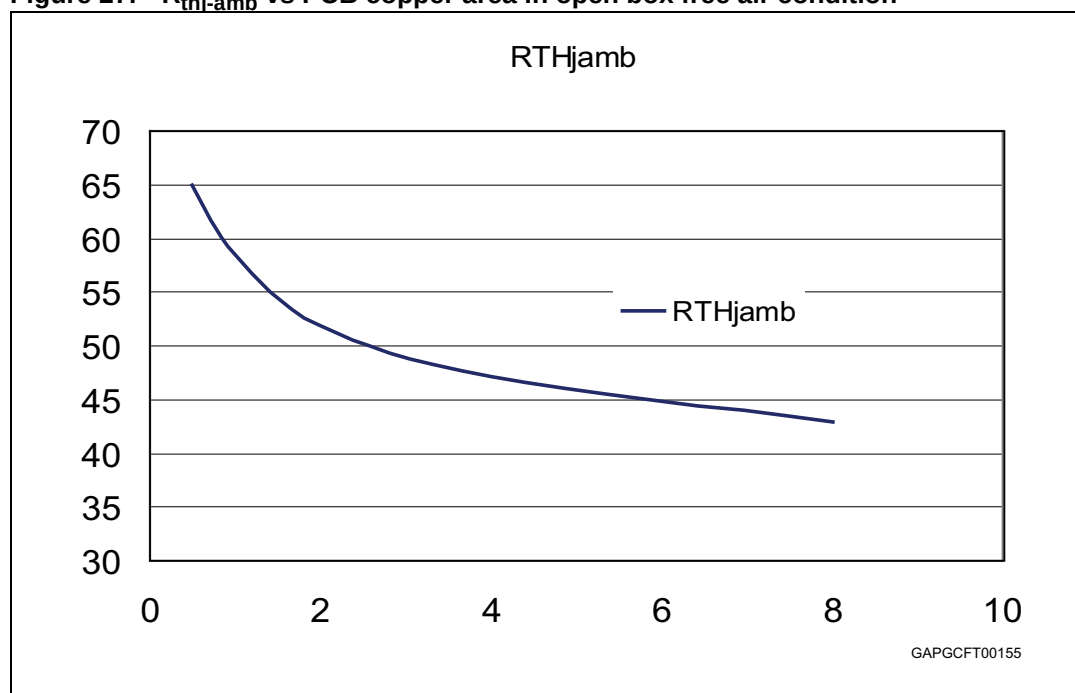
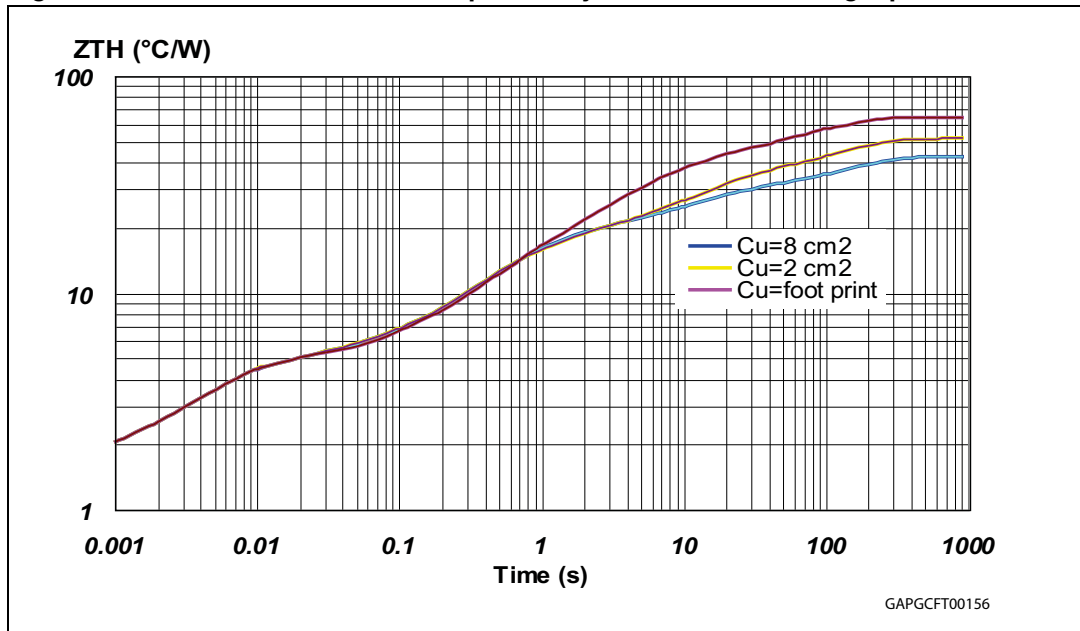


Figure 28. PowerSSO-12 thermal impedance junction ambient single pulse



Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 29. Thermal fitting model of Vreg in PowerSSO-12

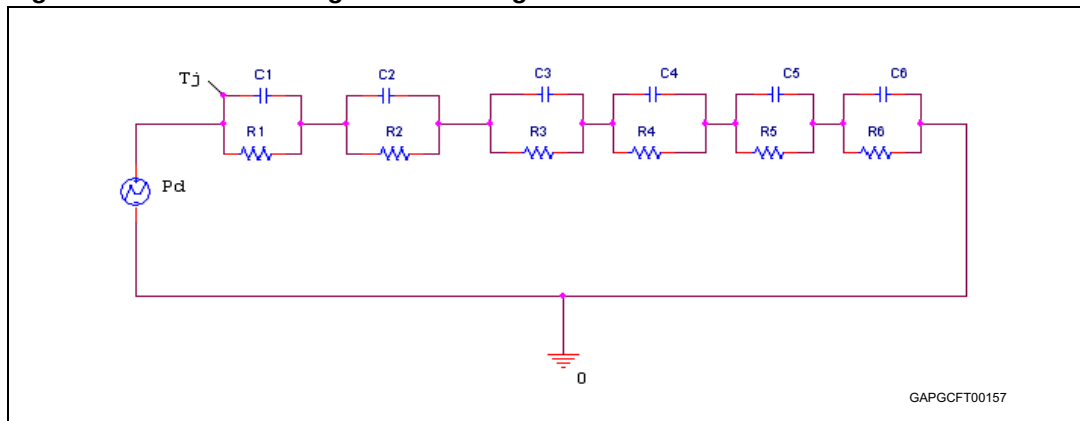
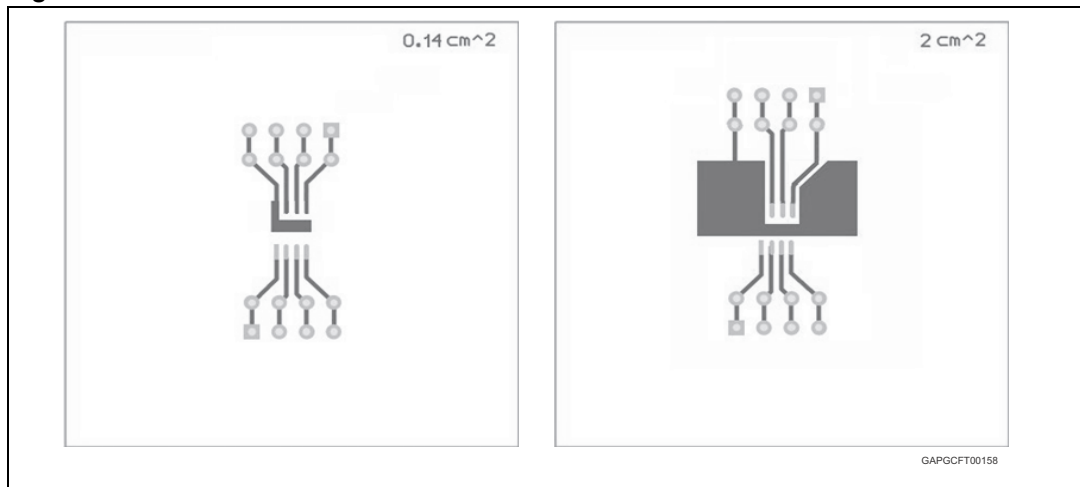


Table 8. PowerSSO-12 thermal parameter

Area (cm ²)	Footprint	2	8
R1 (°K/W)	1.53		
R2 (°K/W)	3.21		
R3 (°K/W)	5.2		
R4 (°K/W)	7	7	8
R5 (°K/W)	22	15	10
R6 (°K/W)	26	20	15
C1 (W.s/°K)	0.00004		
C2 (W.s/°K)	0.0016		
C3 (W.s/°K)	0.08		
C4 (W.s/°K)	0.2	0.1	0.1
C5 (W.s/°K)	0.27	0.8	1
C6 (W.s/°K)	3	6	9

4.2 SO-8 thermal data

Figure 30. SO-8 PC board⁽¹⁾



1. Layout condition of R_{th} and Z_{th} measurements (PCB: double layer, thermal vias, FR4 area = 48 mm x 48 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m (front and back side), Cu thickness on vias 25 μ m, Footprint dimension 4.1 mm x 6.5 mm).

Figure 31. $R_{thj-amb}$ vs. PCB copper area in open box free air condition

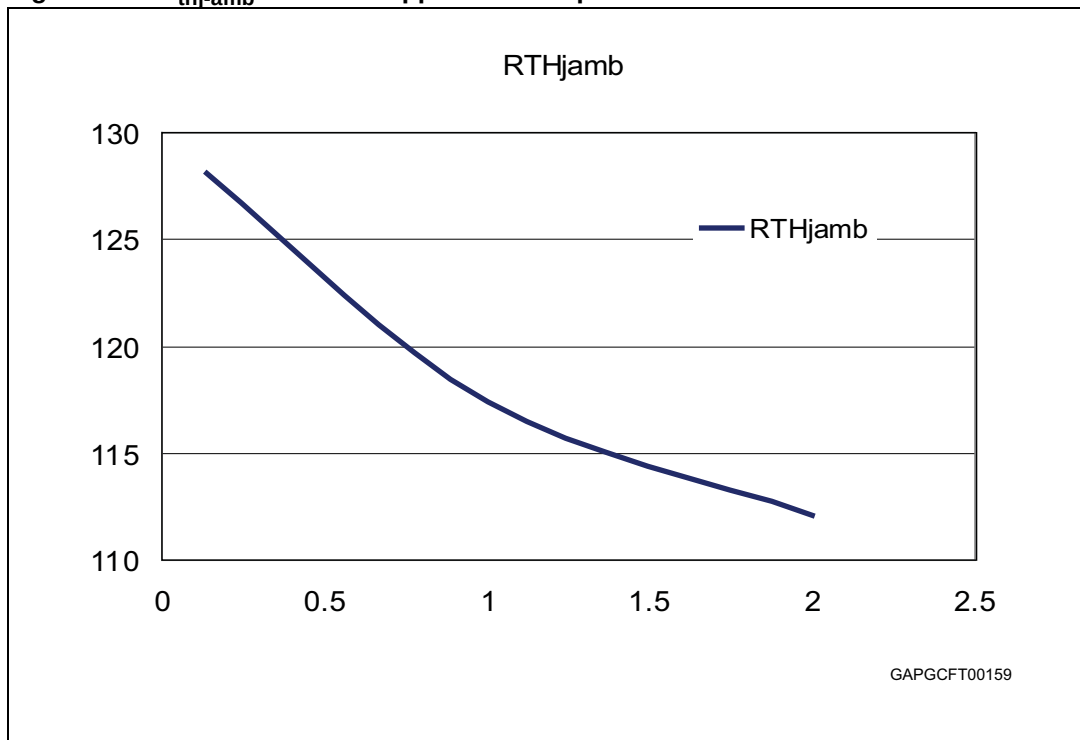
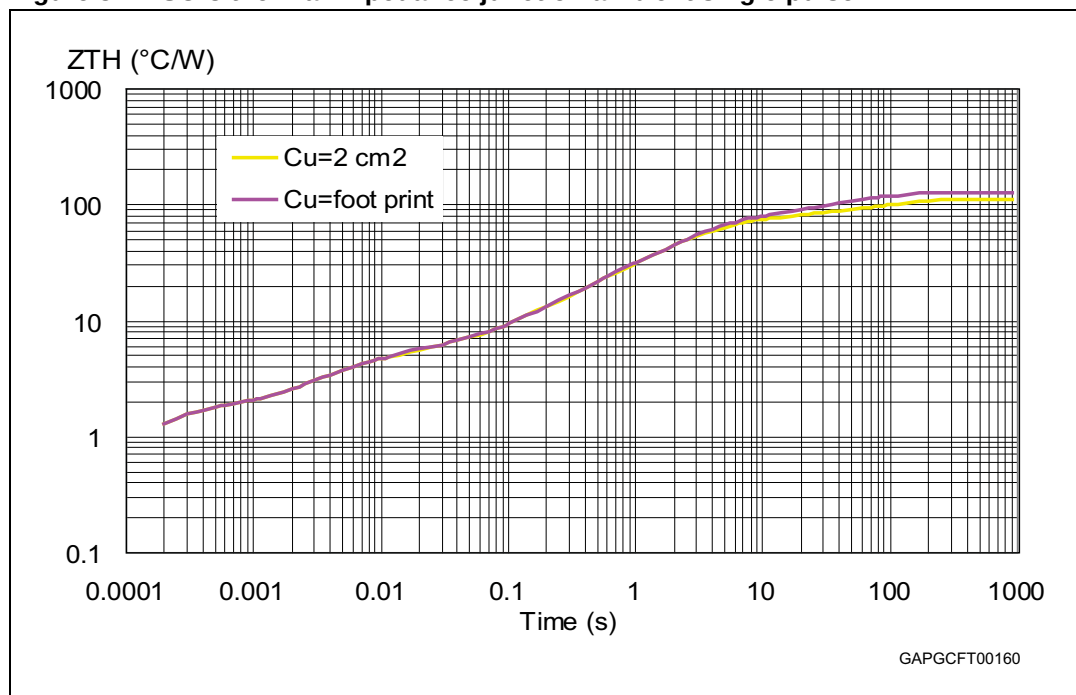


Figure 32. SO-8 thermal impedance junction ambient single pulse**Equation 5: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

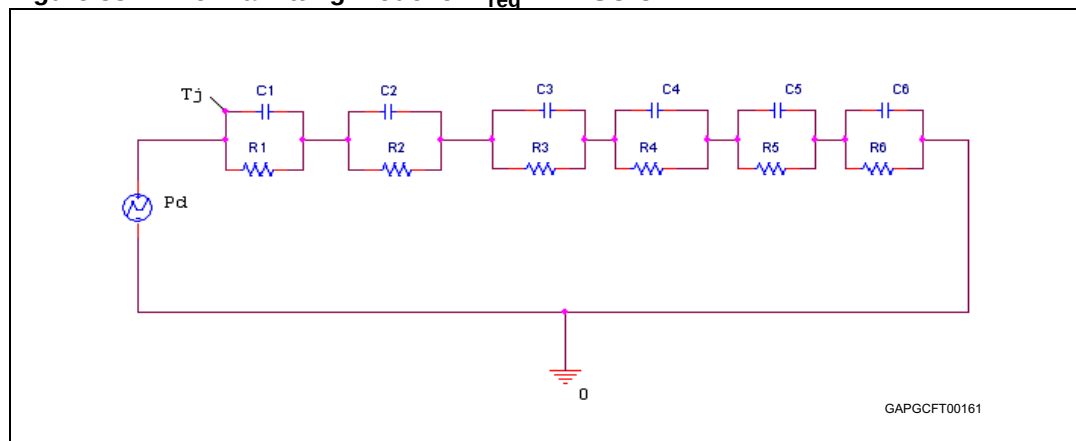
Figure 33. Thermal fitting model of V_{reg} in in SO-8

Table 9. SO-8 thermal parameter

Area (cm ²)	Footprint	2
R1 (°K/W)	1.53	
R2 (°K/W)	3.21	
R3 (°K/W)	5.4	
R4 (°K/W)	32	
R5 (°K/W)	34	
R6 (°K/W)	52	36
C1 (W.s/°K)	0.00004	
C2 (W.s/°K)	0.0016	
C3 (W.s/°K)	0.04	
C4 (W.s/°K)	0.05	
C5 (W.s/°K)	0.15	
C6 (W.s/°K)	1	2.5

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 PowerSSO-12 mechanical data

Figure 34. PowerSSO-12 package dimensions

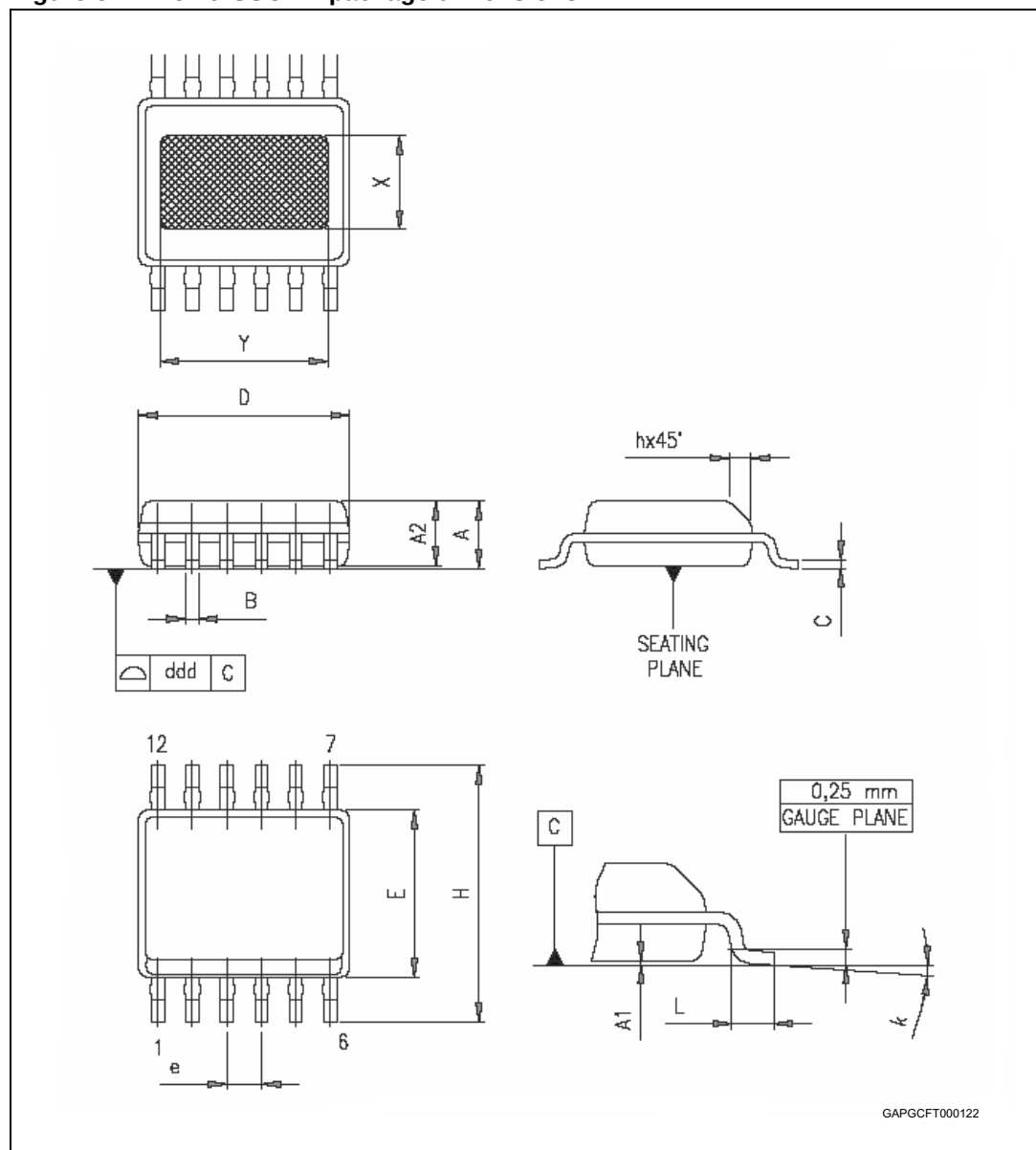


Table 10. PowerSSO-12 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	1.900		2.500
Y	3.600		4.200
ddd			0.100

5.3 SO-8 package information

Figure 35. SO-8 package dimensions

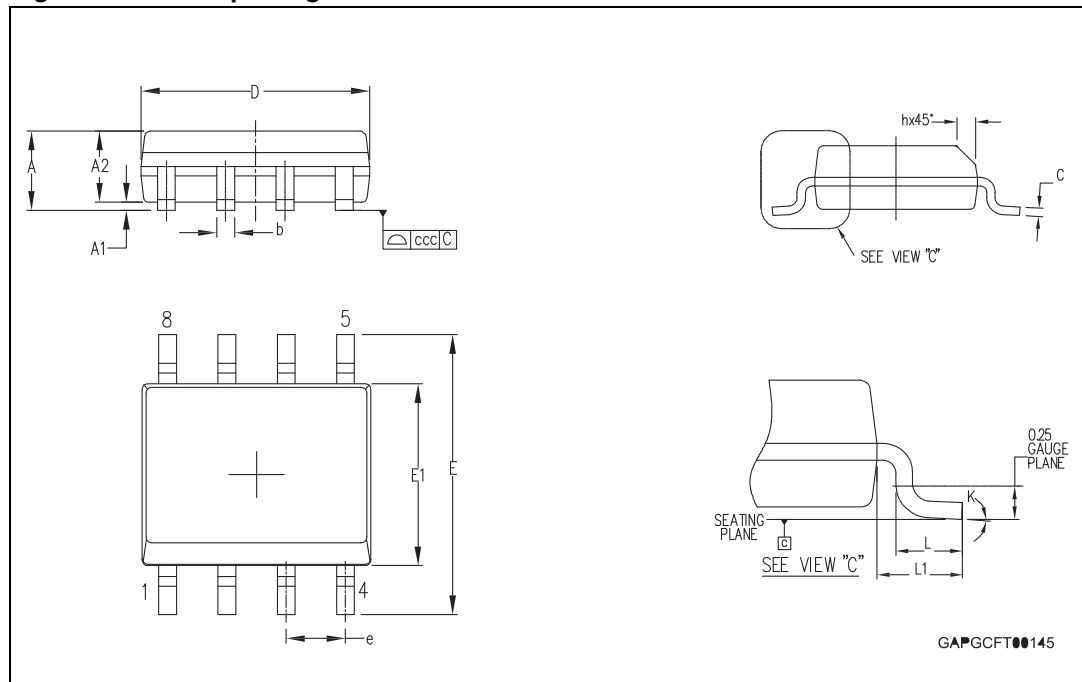


Table 11. SO-8 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D ⁽¹⁾	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 ⁽²⁾	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

5.4 PowerSSO-12 packing information

Figure 36. PowerSSO-12 tube shipment (no suffix)

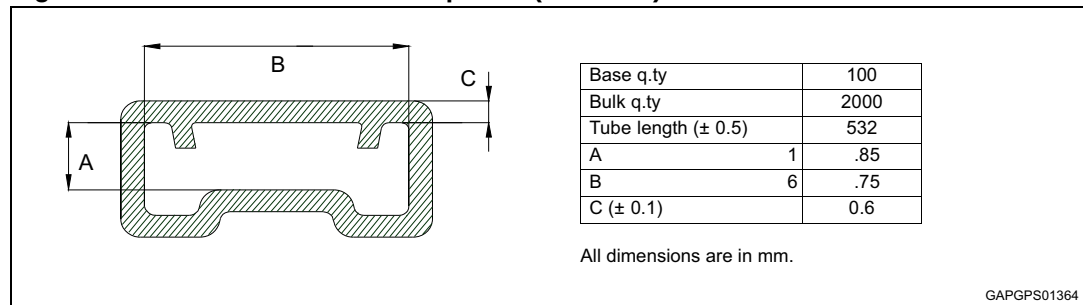
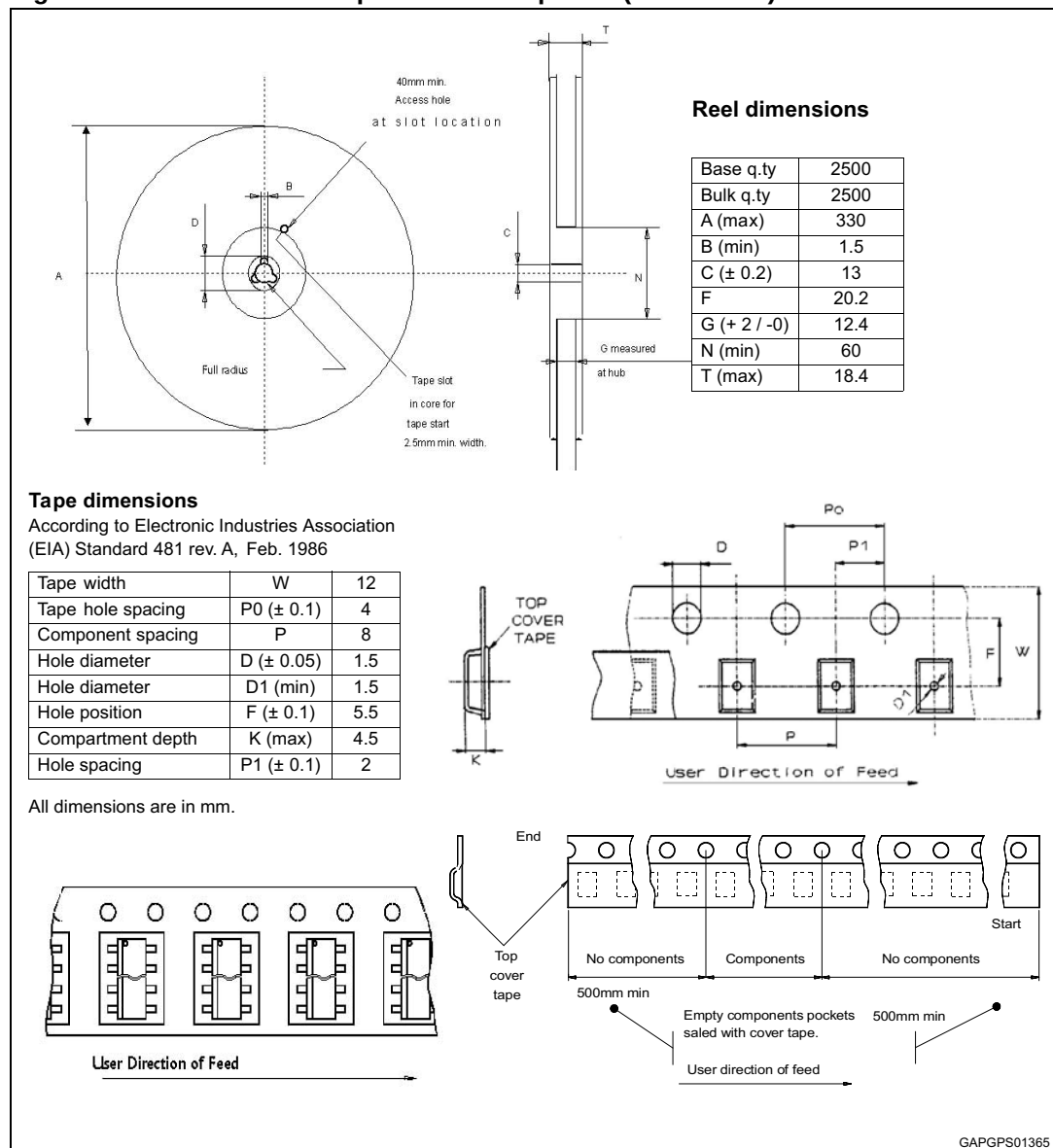


Figure 37. PowerSSO-12 tape and reel shipment (suffix "TR")



5.5 SO-8 packing information

Figure 38. SO-8 tube shipment (no suffix)

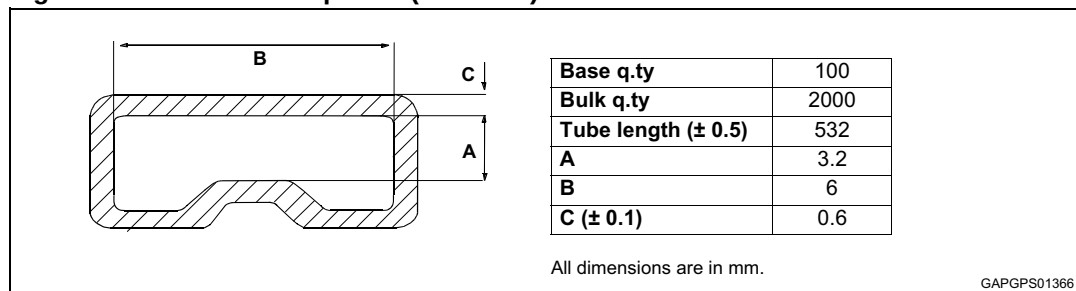
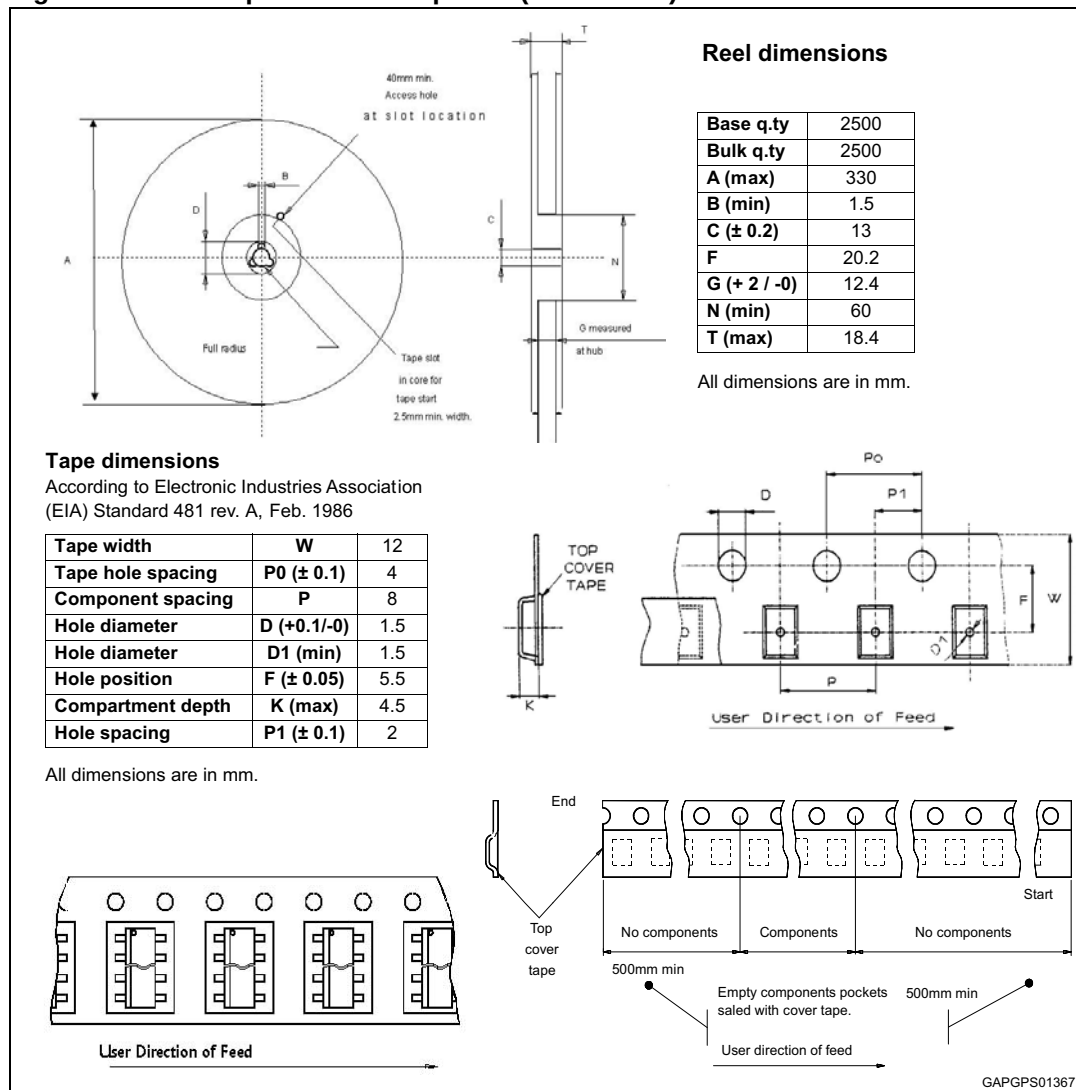


Figure 39. SO-8 tape and reel shipment (suffix "TR")



6 Revision history

Table 12. Document revision history

Date	Revision	Changes
09-Aug-2007	1	Initial release.
06-Mar-2008	2	Updated Table 5.: General: – changed V_{O_ref}, V_{line}, V_{load} test conditions – added notes to I_{lim} and V_{dp} parameters – added I_{oth_H}, I_{oth_L}, I_{oth} parameters. Updated Table 6.: Reset: – added V_{res_adj} parameter – changed V_{Rlth} values (min./ typ./ max.) from 17/20/23 to 20/23/26 ($\% V_{O_ref}$). Modified Section 3.2: Reset.
09-May-2008	3	Updated Table 5.: General : – changed I_{lim} values (Min./Typ./Max.) from 0.7/1/1.30 A to 280/470/660 mA – V_{O_ref} parameter : updated I_o test condition Old -> $I_o = 0.1$ mA to 10 mA New -> $I_o = 0.1$ mA to 8 mA.
13-Oct-2008	4	Updated Table 5.: General : – V_{load} parameter : updated I_o test condition Old -> $I_o = 5$ mA to 150 mA New -> $I_o = 8$ mA to 150 mA.
23-Oct-2008	5	Added S0-8 package option.

Table 12. Document revision history (continued)

Date	Revision	Changes
16-Apr-2009	6	Updated corporate template from V2 to V3 Updated Figure 2: Configuration diagram (top view) Table 2: Pins description – Added new row Table 3: Absolute maximum ratings – V_{EN}: deleted row Table 4: Thermal data – $R_{thj-amb}$: changed value – Added new row – Updated TableFootnote Table 5: General – V_{load}: changed max value for $V_S = 8\text{ V}$ to 18 V, added new row – I_{qn_1}: changed Test conditions (added $T_j = 25\text{ °C}$), added new row Table 6: Reset – V_{Rlth}: changed min/typ/max value – V_{Res_adjl}: replaced with V_{Rlth}, changed Parameter Table 7: Early warning – Updated symbols Added Figure 3: Output voltage vs. T_j Added Figure 4: Output voltage vs. V_S Added Figure 5: Drop voltage vs. output current Added Figure 6: Current consumption vs. output current Added Figure 7: Current consumption vs. output current (at light load condition) Added Figure 8: Current consumption vs. input voltage ($I_o = 0.1\text{ mA}$) Added Figure 9: Current consumption vs. input voltage ($I_o = 75\text{ mA}$) Added Figure 10: Current limitation vs. T_j Added Figure 11: Current limitation vs. input voltage Added Figure 12: Short-circuit current vs. T_j Added Figure 13: Short-circuit current vs. input voltage Added Figure 14: V_{Rhth} vs. T_j Added Figure 15: V_{Rlth} vs. T_j Added Figure 16: V_{EWi_thh} vs. T_j Added Figure 17: V_{EWi_thl} vs. T_j Added Figure 18: I_{cr} vs. T_j Added Figure 19: I_{dr} vs. T_j Added Figure 20: PSRR Section 3.1: Voltage regulator – Updated text – Added Figure 21: Application schematic – Added Figure 23: Maximum load variation response Section 3.2: Reset – V_{Rlth}: changed value from 1.15 V to 0.9 V in Equation 1 Added Section 4: Package and PCB thermal data Changed Section 5.1: ECOPACK®

Table 12. Document revision history (continued)

Date	Revision	Changes
09-Jun-2009	7	Changed document title Table 5: General – $I_{\text{oth_H}}$, $I_{\text{oth_L}}$: added test condition Updated Figure 4: Output voltage vs. V_S Section 3.3: Early warning – changed internal voltage reference typical value from 1.23 V to 2.5 V Updated Figure 28: PowerSSO-12 thermal impedance junction ambient single pulse Updated Figure 32: SO-8 thermal impedance junction ambient single pulse
04-Dec-2009	8	Updated features list. Updated Table 2: Pins description. Updated Section 3.1: Voltage regulator. Corrected Equation 3 on Section 3.2: Reset.
26-Mar-2010	9	Updated Table 5: General: – $I_{\text{qn_1}}$, $I_{\text{qn_150}}$: removed test condition $E_n = \text{high}$.
12-Apr-2010	10	Table 4: Thermal data: – $R_{\text{thj-amb}}$: updated PowerSSO-12 value
14-Mar-2011	11	Table 4: Thermal data: – $R_{\text{thj-amb}}$: updated PowerSSO-12 value – $R_{\text{thj-lead}}$: updated SO-8 value
30-Jan-2012	12	Updated Figure 22: Stability region on page 15 .
07-Feb-2012	13	Modified Figure 22: Stability region on page 15 .
17-Apr-2012	14	Table 6: Reset: – T_{rd}: updated maximum value
19-Sep-2013	15	Updated disclaimer.

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